**Technion**

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High Speed Digital System Lab

Display Controller

Documentation

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# Scope

This document aims to describe the TOP Display Controller, with its components.

# Abbreviations

1. WBS – Wishbone Slave
2. WBM – Wishbone Master
3. FIFO – First In First Out
4. DC – Dual Clock
5. VESA - Video Electronics Standards Association
6. TB – Test bench

# General Description

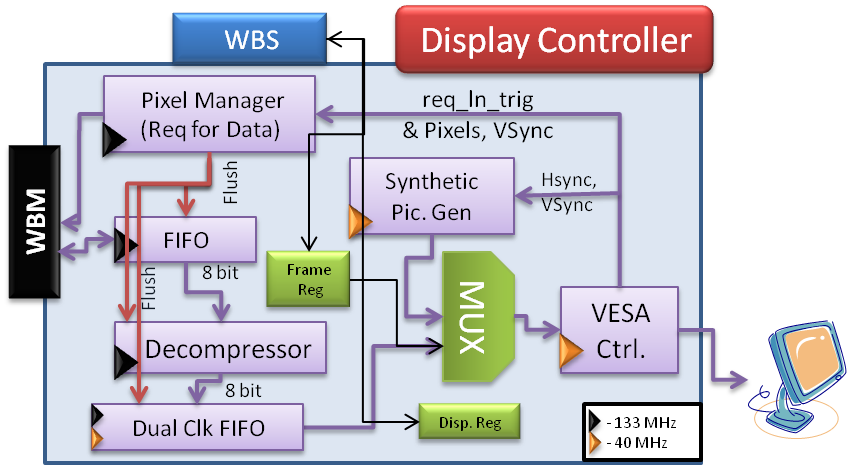


Figure 1 - Display Controller Schematics

The Display Controller is consumed of the following blocks:

1. **Pixel Manager** – Counts the number of received pixels so far. When VSync signal is received, flushes the Single Clock and Dual Clock FIFOs, and restarts the read from the beginning of the SDRAM relevant bank. The *Pixel Manager* initializes new transaction upon '*req\_ln\_trig*' assertion, in case the number of requested pixels has not been received yet.
2. **Decompressor** – Decompresses data, which comes from the FIFO (8 bits of color value, followed by 8 bits of repetitions).
3. **Synthetic Picture Generator** – Generator synthetic pattern to the VESA Controller.
4. **VESA Controller** – Generates VESA signals to the VGA, from the input RGB.
5. **FIFO** – Single Clock FIFO, which stores the incoming data from the WBM.
6. **Dual Clock FIFO** – stores the incoming RGB decompressed data, until it is being read by the VESA controller.
7. **WBM** – Wishbone Master – initializes, according to the *Pixel Manager* commands, read transaction from the SDRAM.
8. **WBS** – Wishbone Slave – stores register's data into the Frame Registers (holds the picture's position) and Display Register, which is actually the type register. It functions as the MUX's selector.

# Display Controller TOP Pinout

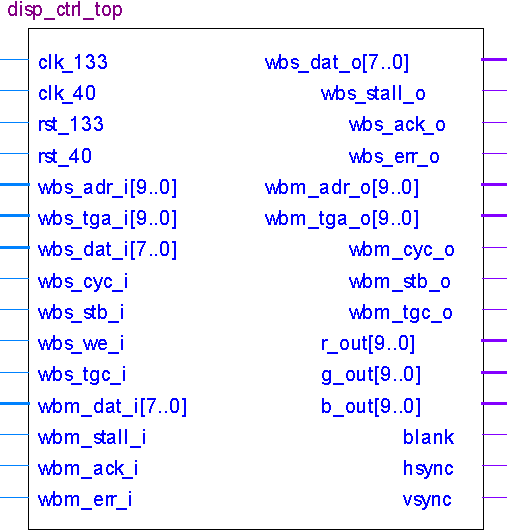


Figure 2 - SDRAM Controller Pinout

| Pin Name | Direction | Description |
| --- | --- | --- |
| Clk\_133 | In | Wishbone Clock (133MHz) |
| Clk\_40 | In | VESA Clock (40MHz) |
| Rst\_133 | In | Reset, where the reset de-assertion is synchronized to the 133MHz clock. Reset polarity will be set according to the generic parameter 'reset\_polarity\_g' |
| Rst\_40 | In | Reset, where the reset de-assertion is synchronized to the 40MHz clock. Reset polarity will be set according to the generic parameter 'reset\_polarity\_g' |
| Wbs\_adr\_i[9..0] | In | Wishbone Input Address |
| Wbs\_tga\_i[9..0] | In | Required burst length – 1. i.e: for burst length of 5 words, burst\_len should be 4. |
| Wbs\_dat\_i[7..0] | In | Register's data |
| Wbs\_cyc\_i | In | '1' – Wishbone cycle active, '0' - Inactive |
| Wbs\_stb\_i | In | Wishbone Strobe (Data valid / request for data) |
| Wbs\_we\_i | In | '1' to write data to SDRAM, '0' to read data from SDRAM |
| Wbs\_tgc\_i | In | Cycle Tag. Should be '1' to write to registers. |
| Wbm\_dat\_i[7..0] | In | Input data from SDRAM |
| Wbm\_stall\_i | In | Stall from Wishbone Master (SDRAM is not ready) |
| Wbm\_ack\_i | In | Input data is valid (Acknowledged) |
| Wbm\_err\_i | In | Error from master (Incorrect address / SDRAM error) |
| Wbs\_dat\_o[7..0] | Out | Register's data for reading |
| Wbs\_stall\_o | Out | Registers are not ready to be read |
| Wbs\_ack\_o | Out | Register's Data Acknowledged / Output data is valid |
| Wbs\_err\_o | Out | Error in communicating with registers |
| Wbm\_adr\_o[9..0] | Out | Read address from SDRAM |
| Wbm\_tga\_o[9..0] | Out | Burst size – 1 (16 bits) from SDRAM |
| Wbm\_cyc\_o | Out | Wishbone Cycle. '1' for Cycle Active, '0' for inactive |
| Wbm\_stb\_o | Out | Wishbone Strobe (Read data) |
| Wbm\_tgc\_o | Out | Wishbone Cycle tag. '1' for starting transaction from the beginning of the relevant SDRAM's bank |
| R\_out[9..0] | Out | Red value to VGA |
| G\_out[9..0] | Out | Green value to VGA |
| B\_out[9..0] | Out | Blue value to VGA |
| Blank | Out | Blanking signal to VGA |
| Hsync | Out | Horizontal Sync to VGA |
| Vsync | Out | Vertical sync to VGA |

Table 1 – Display Controller TOP Pinout

# Display Controller TOP Generic Parameters

| Generic Parameter | Default Value | Description |
| --- | --- | --- |
| Reset\_polartiy\_g | '0' | Reset active in this polarity |
| hsync\_polarity\_g | '1' | HSync polarity |
| vsync\_polarity\_g | '1' | VSync polarity |
| blank\_polarity\_g | '0' | Blank polarity |
| red\_default\_color\_g | 0 | Default Red pixel for Frame |
| green\_default\_color\_g | 0 | Default Green pixel for Frame |
| blue\_default\_color\_g | 0 | Default Blue pixel for Frame |
| red\_width\_g | 8 | Default std\_logic\_vector size of Red Pixels |
| green\_width\_g | 8 | Default std\_logic\_vector size of Green Pixels |
| blue\_width\_g | 8 | Default std\_logic\_vector size of Blue Pixels |
| req\_delay\_g | 1 | Number of clocks between the "req\_data" request to the "data\_valid" answer |
| req\_lines\_g | 3 | Number of lines to request from image transmitter, to hold in its FIFO |
| hor\_active\_pixels\_g | 800 | Active pixels per line |
| ver\_active\_lines\_g | 600 | Active lines per frame |
| hor\_left\_border\_g | 0 | Horizontal Left Border (Pixels) |
| hor\_right\_border\_g | 0 | Horizontal Right Border (Pixels) |
| hor\_back\_porch\_g | 88 | Horizontal Back Porch (Pixels) |
| hor\_front\_porch\_g | 40 | Horizontal Front Porch (Pixels) |
| hor\_sync\_time\_g | 128 | Horizontal Sync Time (Pixels) |
| ver\_top\_border\_g | 0 | Vertical Top Border (Lines) |
| ver\_buttom\_border\_g | 0 | Vertical Bottom Border (Lines) |
| ver\_back\_porch\_g | 23 | Vertical Back Porch (Lines) |
| ver\_front\_porch\_g | 1 | Vertical Front Porch (Lines) |
| ver\_sync\_time\_g | 4 | Vertical Sync Time (Lines) |
| Synth\_bit\_g | 2 | Relevant bit in type register, which indicates whether to display synthetic image pattern ('1') or image from SDRAM ('0') |
| Rep\_size\_g | 7 | 27=128 🡺Maximum of 128 repetitions per transmitted byte. Bit number 8 is saved for pixel repetition('0') or line repetition('1'). |
| Fifo\_depth\_g | 3840 | Number of bytes in Single Clock FIFO |
| Fifo\_log\_depth\_g | 10 | Logarithm of fifo\_depth\_g |
| Change\_frame\_clk\_g | 120000000 | Synthetic image : change frame's position every 3 seconds (120,000,000/40MHz = 3 sec) |
| Hor\_pres\_pixels\_g | 640 | 640 active pixels |
| Ver\_pres\_lines\_g | 480 | 480 active lines |

Table 2 - Display Controller TOP Generic Parameters

# Resources

Required resources, when synthesizing, using Synplify, for Altera's Cyclon II FPGA:

* 971 Combinational Cells
* 24 Embedded Cells
* 590 FF

**Maximum Working Frequency**: 150MHz

# Pixel Manager Pinout

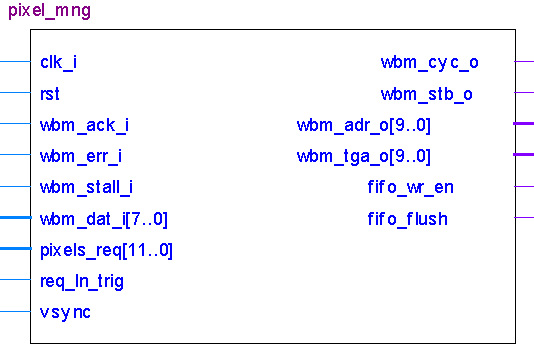


Figure 3 – Pixel Manager Pinout

| Pin Name | Direction | Description |
| --- | --- | --- |
| Clk\_i | In | Wishbone Clock (133MHz) |
| Rst | In | Reset. Reset is active according to 'reset\_polarity\_g' generic parameter |
| Wbm\_ack\_i | In | Data Acknowledged from WBS to WBM |
| Wbm\_err\_i | In | Error from WBS to WBM |
| Wbm\_stall\_i | In | WBS is not ready to transmit data to WBM |
| Wbm\_dat\_i[7..0] | In | Input data from WBS |
| Pixels\_req[11..0] | In | Number of requested pixels from VESA controller (Signal is synchronized to 40MHz VESA clock) |
| Req\_ln\_trig | In | '1' – VESA indicates that 'pixels\_req' pixels should be loaded to FIFO |
| Vsync | In | VSync from VESA controller, in order to flush FIFOs, and restart receiving data from SDRAM bank |
| Wbm\_cyc\_o | Out | WBM Cycle is active |
| Wbm\_stb\_o | Out | Read strobe |
| Wbm\_adr\_o[9..0] | Out | Read address to SDRAM |
| Wbm\_tga\_o[9..0] | Out | Burst length – 1 to SDRAM |
| Fifo\_wr\_en | Out | Write enable to Single Clock FIFO |
| Fifo\_flush | Out | Flushes both FIFOs |

Table 3 – Pixel Manager Pinout

# Pixel Manager Generic Parameters

| Generic Parameter | Default Value | Description |
| --- | --- | --- |
| Reset\_polartiy\_g | '0' | Reset active in this polarity |
| vsync\_polarity\_g | '1' | VSync polarity |
| Screen\_hor\_pix\_g | 800 | Actual screen resolution – Horizontal |
| Hor\_pixels\_g | 640 | Horizontal active pixels |
| Ver\_lines\_g | 480 | Vertical active lines |
| Req\_lines\_g | 3 | Number of lines, to request each 'req\_ln\_trig' from vesa (Number of pixels) |
| Rep\_size\_g | 7 | 27=128 🡺Maximum of 128 repetitions per transmitted byte. Bit number 8 is saved for pixel repetition('0') or line repetition('1'). |

Table 4 – Pixel Manager Generic Parameters

# Resources

Required resources, when synthesizing, using Synplify, for Altera's Cyclon II FPGA:

* 183 Combinational Cells
* 71 FF

**Maximum Working Frequency**: 161MHz

# Runlen Extractor Pinout

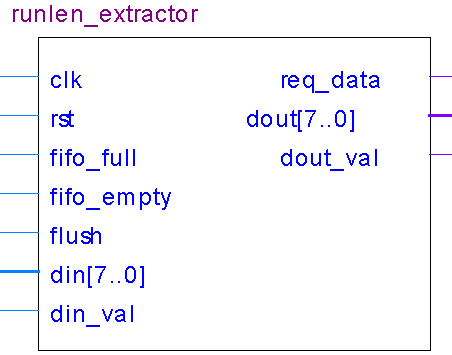


Figure 4 – Runlen Extractor Pinout

| Pin Name | Direction | Description |
| --- | --- | --- |
| Clk | In | Input Clock (133MHz) |
| Rst | In | Reset. Reset is active according to 'reset\_polarity\_g' generic parameter |
| Fifo\_full | In | Dual clock FIFO is full. Do not extract more pixels |
| Fifo\_empty | In | Single clock FIFO is empty. No data can be read |
| Flush | In | Stop decompressing, and purge current decompression action |
| Din[7..0] | In | Input data (pixel value / repetition) from FIFO |
| Req\_data | Out | Request data from FIFO (read enable to FIFO) |
| Dout[7..0] | Out | Output data (pixel value) to DC FIFO |
| Dout\_val | Out | Output data is valid (write enable to DC FIFO) |

Table 5 – Runlen Extractor Pinout

# Runlen Extractor Generic Parameters

| Generic Parameter | Default Value | Description |
| --- | --- | --- |
| Reset\_polartiy\_g | '0' | Reset active in this polarity |
| Pixels\_per\_line\_g | 640 | Active vertical lines |
| Rep\_size\_g | 7 | 27=128 🡺Maximum of 128 repetitions per transmitted byte. Bit number 8 is saved for pixel repetition ('0') or line repetition('1'). |
| Width\_g | 8 | Input / Output data width |

Table 6 – Runlen Extractor Generic Parameters

# Resources

Required resources, when synthesizing, using Synplify, for Altera's Cyclon II FPGA:

* 54 Combinational Cells
* 38 FF

**Maximum Working Frequency**: 191MHz

# Display Controller TOP Waves

## Start of reading

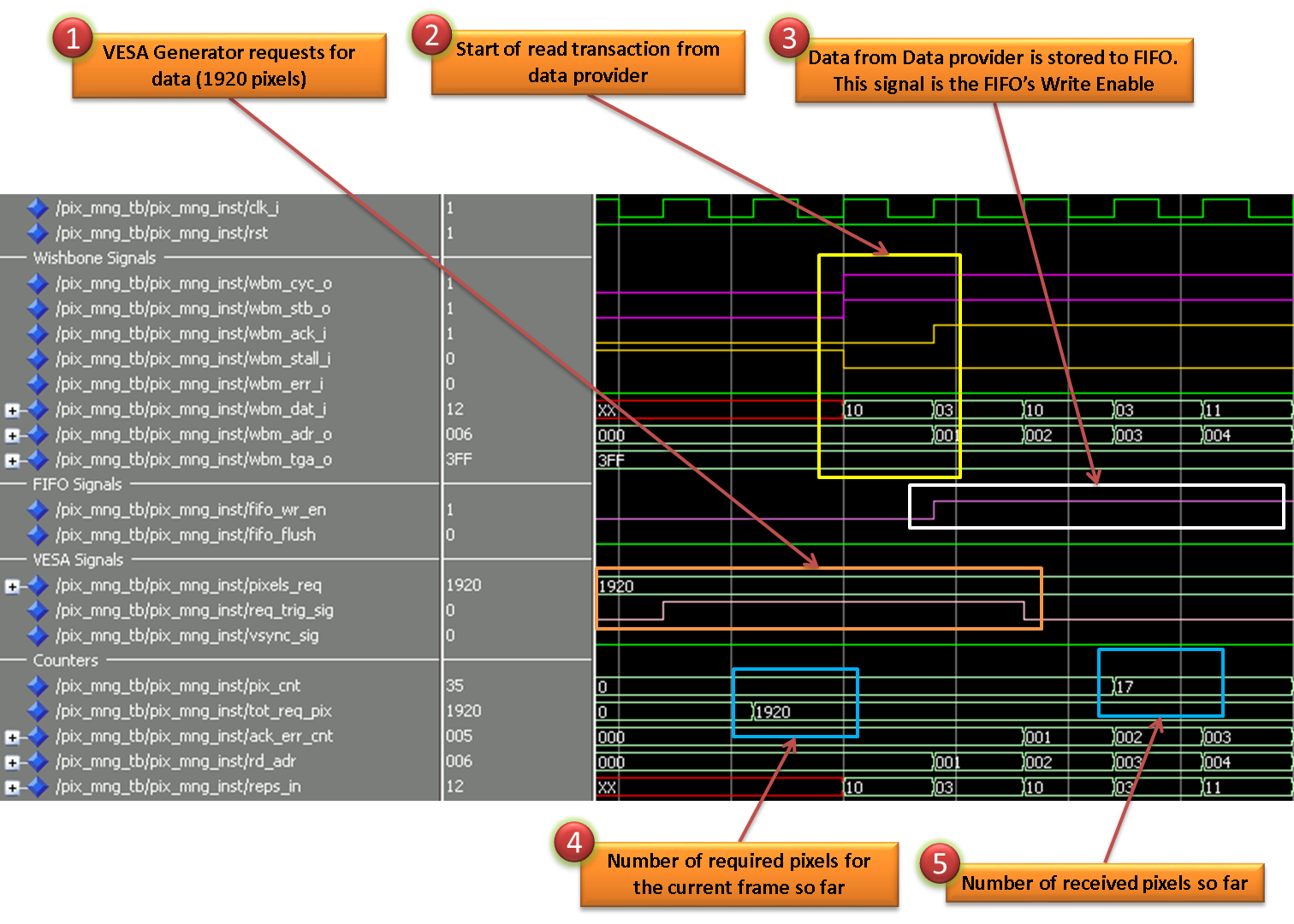


Figure 5 – Start of Reading

## End of Image

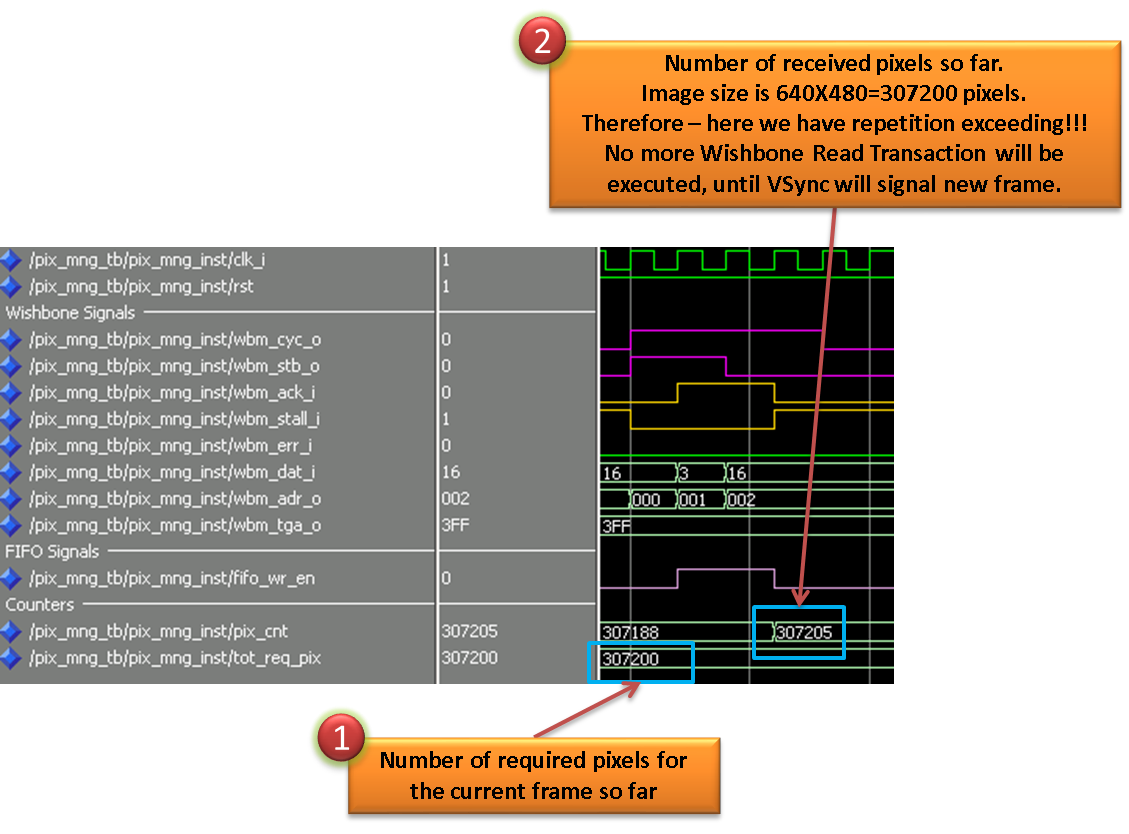


Figure 6 – End of Image

## Runlen Extractor Wave

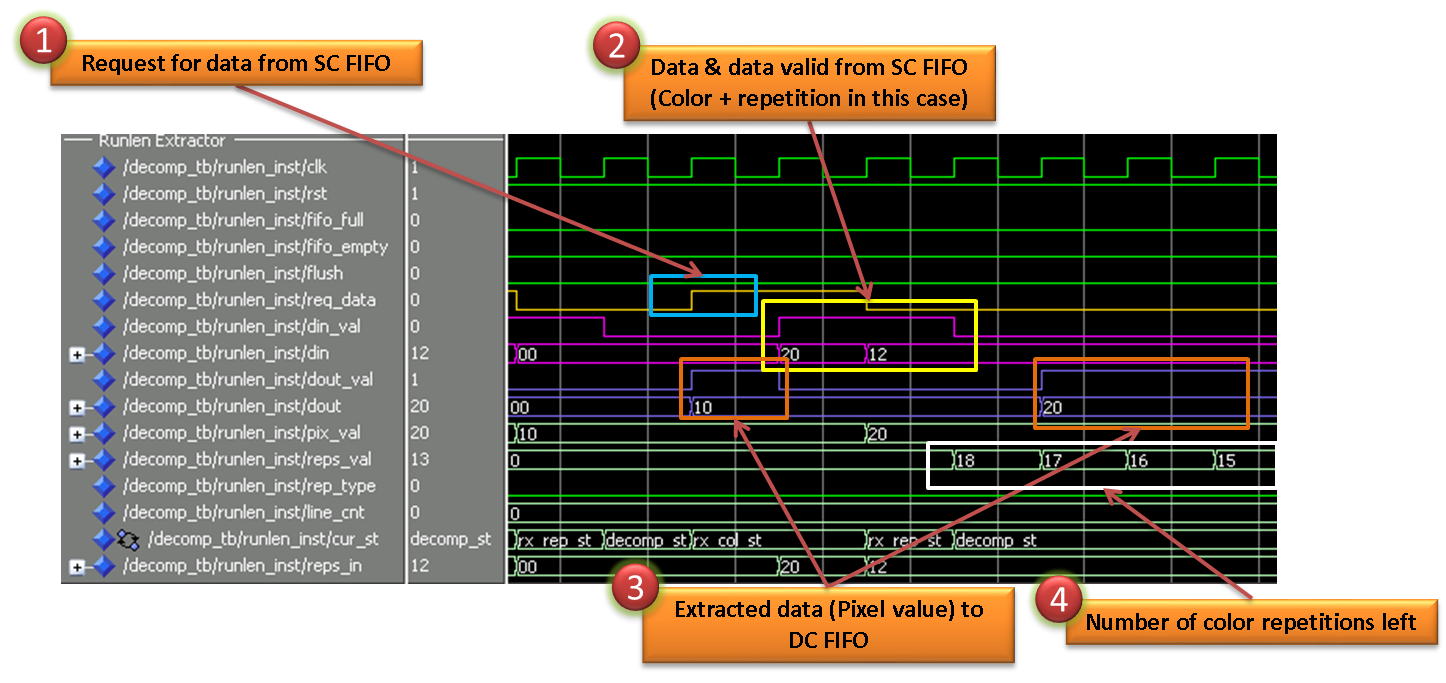


Figure 7 – Runlen Extractor Wave

# Performed Tests

## Runlen Extractor

1. Injected data, using both modes:
   1. 7 bits for repetition, 1 bit for pixels repetition / lines repetition
   2. 8 bits for pixels repetitions
2. Single Clock FIFO is empty
3. Dual Clock FIFO is full
4. Flush data in the middle of the transaction

## Pixel Manager

1. Injected data, using both modes:
   1. 7 bits for repetition, 1 bit for pixels repetition / lines repetition
   2. 8 bits for pixels repetitions
2. VSync signal, in the middle / end of the transaction
3. Repetitions exceeds maximum available pixels (more than 640X480 = 307,200 pixels)
4. Number of received pixels is exactly 640X480

## Display Controller TOP

1. Error in SDRAM, while reading
2. Changing Type Register's value (causes to synthetic image / normal image to be displayed)
3. Changing frame register's value:
   1. At exact 640X480 – works file
   2. At less / more than that size – image is deformed
4. Flushing image in the middle of the transmission