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IS42S16400 SDRAM Controller

Documentation

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# Scope

This document aims to describe the IS42S16400 SDRAM controller, together with an example environment of how to use it.

# Abbreviations

1. SDRAM – Synchronous Dynamic Random Access Memory
2. RAS – Row Address
3. CAS – Column Address
4. TB – Test bench

# General Description

## SDRAM

The IS42S16400 SDRAM is a high-speed 67,108,864 bit synchronous dynamic random-access memory, organized as 1,048,576 X 16 X 4 (word X bit X bank).

Required clock is 133MHz. All inputs and outputs are synchronized with the positive edge of the clock.

## SDRAM Controller

The SDRAM controller implements the IS42S16400 SDRAM Controller, with the following characteristics:

1. Row width: 12 bits
2. Column width: 8 bits
3. Bank width: 2 bits
4. Address structure:
   1. Bank (21 downto 20)
   2. Row (19 downto 8)
   3. Column (7 downto 0)
5. CAS Delay = 3 (required for 133MHz clock)
6. Burst Length = Full Page (256 words - cyclic)
7. 4096 refreshes cycles will be automatically execute per each 64 ms.
8. Maximum read/write burst length is 256. In case 256-(column address) is less than the burst length – only 256-(column address) words will be written / read.

The SDRAM Controller is *Wishbone Compatible* with one exception: Given address at start of burst is auto-incremented by SDRAM, independently in the following given addresses (WBS\_ADR\_I).

## Supported commands

Two ACT commands are supported by this controller:

1. Write burst command – up to 256 words (512Kbyte)
2. Read burst command – up to 256 words (512Kbyte)

# SDRAM Controller Pinout

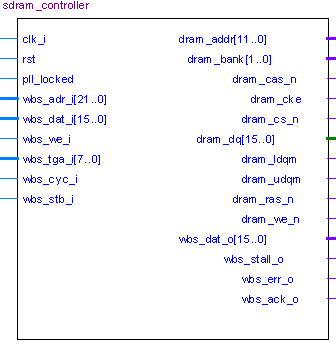


Figure 1 - SDRAM Controller Pinout

| Pin Name | Direction | Description |
| --- | --- | --- |
| Clk\_i | In | Wishbone Clock (133MHz) |
| Rst | In | Reset. Reset polarity will be set according to the generic parameter 'reset\_polarity\_g' |
| Pll\_locked | In | Indicates that the PLL is locked, for CKE (Clock Enable) indication |
| Wbs\_adr\_i[21..0] | In | Address (bank, row, column) |
| Wbs\_dat\_i[15..0] | In | Data from the user, to write to the SDRAM |
| Wbs\_we\_i | In | '1' to write data to SDRAM, '0' to read data from SDRAM |
| Wbs\_tga\_i[7..0] | In | Required burst length – 1. i.e: for burst length of 5 words, burst\_len should be 4. |
| Wbs\_stb\_i | In | Wishbone Strobe (Data valid / request for data) |
| Wbs\_cyc\_i | In | '1' – Wishbone cycle active, '0' - Inactive |
| Dram\_addr[11..0] | Out | Address to SDRAM |
| Dram\_bank[1..0] | Out | Bank to SDRAM |
| Dram\_cke | Out | Clock Enable to SDRAM |
| dram\_cas\_n | out | CAS signal to SDRAM |
| Dram\_cs\_n | Out | Chip Select to SDRAM. Set to '0' by the controller |
| Dram\_dq[15..] | Inout | Data to / from SDRAM |
| Dram\_ldqm | Out | Data Masking to SDRAM |
| Dram\_udqm | Out | Data Masking to SDRAM |
| Dram\_ras\_n | Out | RAS signal to SDRAM |
| Dram\_we\_n | Out | WE signal to SDRAM |
| Wbs\_dat\_o[15..0] | Out | Data to the user, from the SDRAM |
| Wbs\_stall\_o | Out | Repeat last command |
| Wbs\_err\_o | Out | Error – Burst exceeds page / Wishbone protocol error |
| Wbs\_ack\_o | Out | Data valid / Data acknowledge |

Table 1 - SDRAM Controller Pinout

# SDRAM Controller Generic Parameters

| Generic Parameter | Default Value | Description |
| --- | --- | --- |
| Reset\_polartiy\_g | '0' | Reset active in this polarity |

Table 2 - SDRAM Controller Generic Parameters

# Resources

Required resources, when synthesizing, using Synplify, for Altera's Cyclon II FPGA:

* 16 Buffers (Directional)
* 11 AND gates
* 17 OR gate
* 146 DFF
* 375 MUX
* 32 I/O Buffer (TRI)
* 2 State Machines
* 9 Addition operator
* 4 Equal Operator
* 8 Less than operator
* 33 Selector Operator

**Maximum Working Frequency**: 206MHz

# Initialization Process

Refer to Page 15 in the SDRAM documentation. Refer to Simplified State Diagram, page 9, for more information.

1. NOP input conditions, as well as available clock, CKE='1', DQM='1' for a minimum of 200us
2. Precharge command for all banks
3. After tRP (all banks become idle), issue 8 auto-refresh commands
4. Issue a mode register set commands

## Phase 1 – Idle for 200 us

Figure 2 - Init - 200 us

## Phase 2, 3, 4 – Precharge, Auto Refresh, Mode Register

Figure 3 - Init - Precharge, Auto Refresh, Mode Register

# Burst Read / Write

Writing / reading to/from the SDRAM, using this controller, is possible only by using full page burst. A full-page burst opens a row (RAS), and start writing /reading data from the column that is specified during the CAS strobe.

An opened row consumed of 256 word (each column is 16 bits = word). In case the required burst length is greater than (256 - column address), then only (256 - column address) words will be written / read, to prevent cyclic reading or overwriting data. *WBS\_ERR\_O* flag will rise at end of burst.

For example: suppose *WBS\_TGA\_I* (burst length) = FF (255) and the address *WBS\_ADR\_I*(7 downto 0) = FC (252). In this case only 4 words will be written / read, and the rest 252 words will be ignored.

## Burst Write

The controller expects the following data and signals to perform write burst:

1. WBS\_CYC\_I – Wishbone Cycle '1'
2. WBS\_STB\_I – Wishbone Strobe '1'
3. WBS\_ADR\_I – Wishbone Address[[1]](#footnote-1)
4. WBS\_DAT\_I – Wishbone Input data
5. WBS\_TGA\_I – Wishbone Tag Address. Here it is used a burst length (0🡪255, which means 1 words up to 256 words)
6. WBS\_WE\_I – Wishbone Write Enable '1'

When the controller enters its idle state (no reading/writing), it can acknowledge the command. The following signals will strobe by the controller:

1. '~RAS ' signal will be negated – Row will be opened, and then the signal will be asserted.
2. '~CAS' signal will be negated to select column, and then the signal will be asserted
3. '~WE' signal will be negated together with '~CAS' according to 'we\_i' command.
4. Controller will negate WBS\_STALL\_O to indicate that the SDRAM is ready.
5. Controller will assert WBS\_ACK\_O to indicate that the data has been acknowledged.
6. Data will be written to the SDRAM.

Figure 4 - Write Burst

## Burst Read

The controller expects the following data and signals to perform read burst:

1. WBS\_CYC\_I – Wishbone Cycle '1'
2. WBS\_STB\_I – Wishbone Strobe '1'
3. WBS\_ADR\_I – Wishbone Address[[2]](#footnote-2)
4. WBS\_TGA\_I – Wishbone Tag Address. Here it is used a burst length (0🡪255, which means 1 words up to 256 words)
5. WBS\_WE\_I – Wishbone Write Enable '1'
6. WBS\_DAT\_O – Wishbone Output data

When the controller enters its idle state (no reading/writing), it can acknowledge the command. The following signals will be strobe by the controller:

1. '~RAS ' signal will be negated – Row will be opened, and then the signal will be asserted.
2. '~CAS' signal will be negated to select column, and then the signal will be asserted
3. Controller will negate WBS\_STALL\_O to indicate that the SDRAM is ready.
4. Controller will assert WBS\_ACK\_O to indicate that the output data is valid.
5. Data will be read from the SDRAM.

Figure 5 - Read Burst

## End of Write Burst

An end of burst, both for reading and writing, is ended by executing the PRE (precharge) command. Data masking must be asserted during PRE command of end write burst.

Figure 6 - End Write Burst

## End of Read Burst

An end of burst, both for reading and writing, is ended by execute the PRE (precharge) command. Data will be available three clocks after the precharge, because of the CAS delay, which was set to 3, during the *Mode Register* command.

Figure 7 - End Read Burst

## Errors

Error (WBS\_ERR\_O) will occur in the following cases:

1. Burst length exceeds page. WBS\_ERR\_O will assert after the last WBS\_ACK\_O.
2. WBS\_STB\_I is asserted when it should be negated.

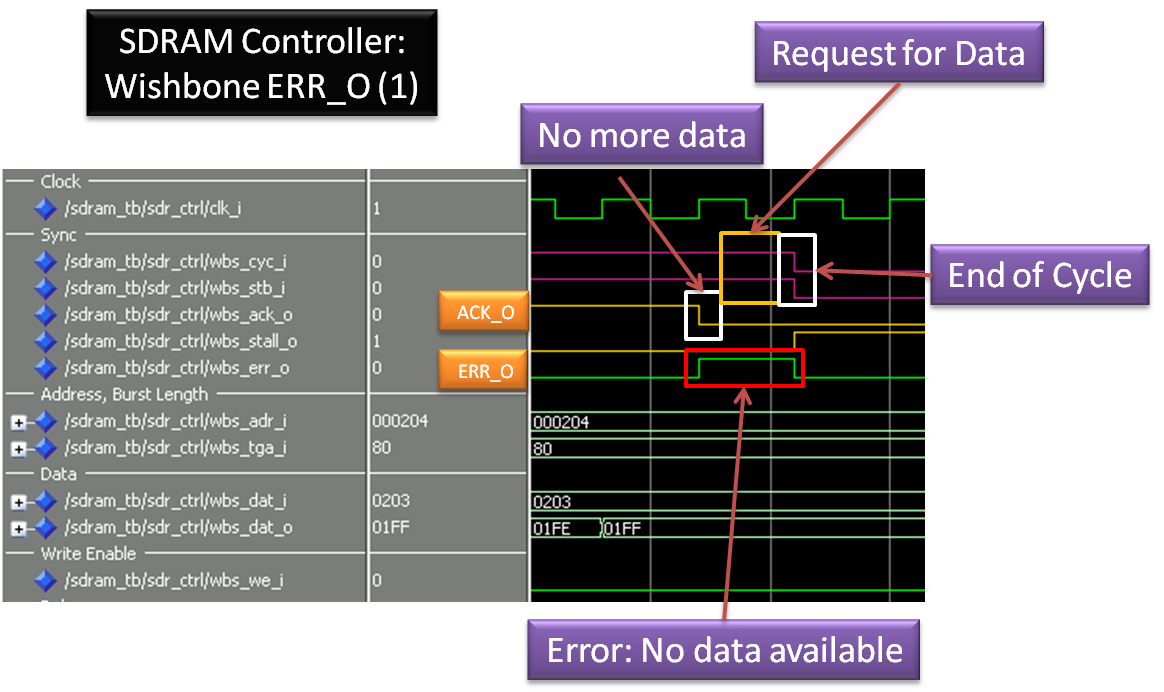


Figure 8 – WBS\_ERR\_O (1) – Read Cycle

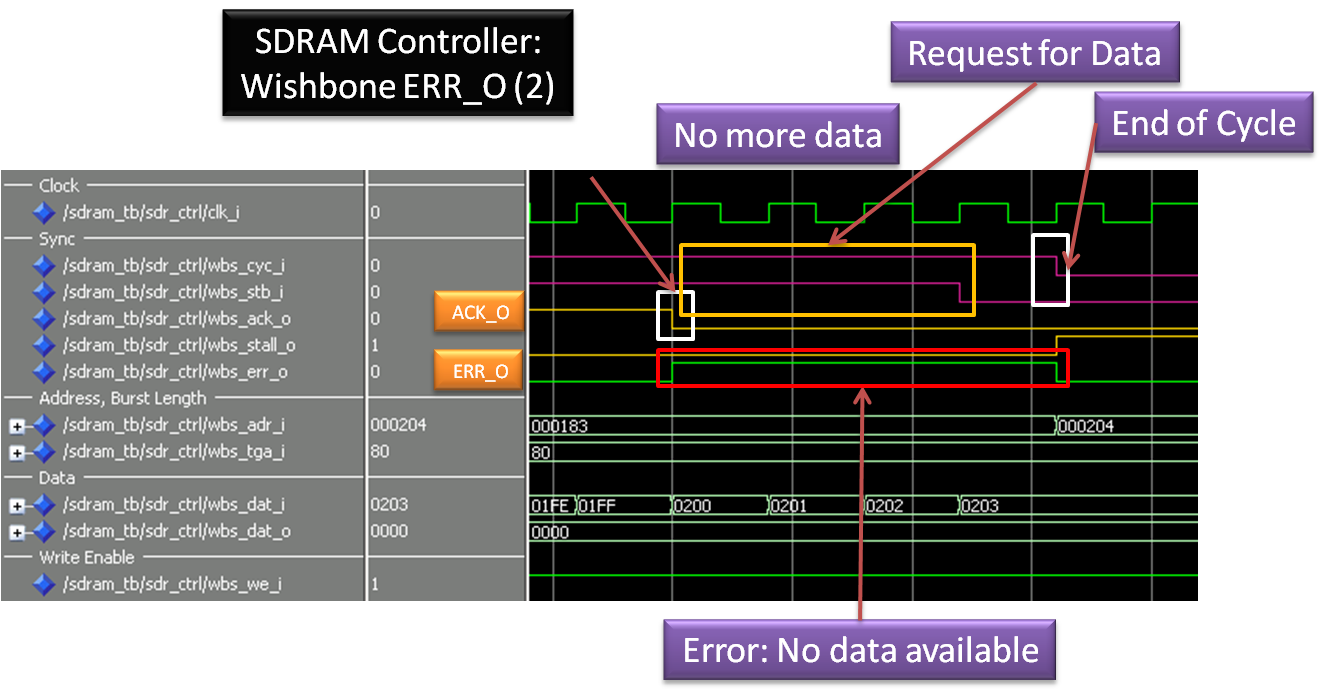


Figure 9 – ERR\_O (2) – Write Cycle

# Final State Machine

There are two FSMs in the design:

1. Init FSM – Executed ONLY after reset, to initialize SDRAM
2. Main FSM – Active during normal operation, after Init FSM becomes inactive.

## Init FSM

1. **INIT\_IDLE\_ST**: Ready to start init / Init done
2. **INIT\_WAIT\_200us\_ST**: Wait 200 us (NOP command)
3. **INIT\_PRECHARGE\_ST**: Precharge all banks
4. **INIT\_WAIT\_PRE\_ST**: Wait to tRP
5. **INIT\_AUTO\_REF\_ST**: Perform Auto Refresh (8 cycles)
6. **INIT\_AUTO\_REF\_WAIT\_ST**: Wait tRC
7. **INIT\_MODE\_REG\_ST**: Mode Register
8. **INIT\_WAIT\_MODE\_REG\_ST**: Wait tRSC (Mode Register set time)

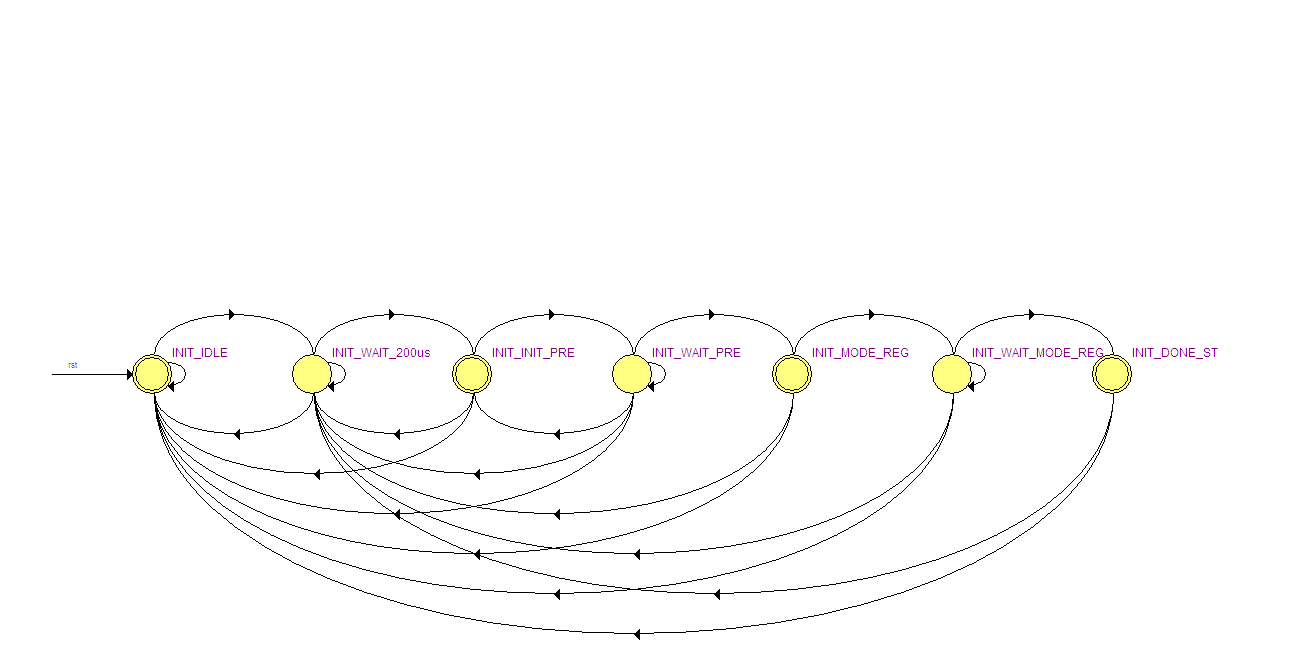


Figure 8- Init FSM

## Main FSM

1. **IDLE\_ST**: Idle
2. **REFRESH\_ST**: Refresh
3. **REFRESH\_WAIT\_ST**: Wait tRC (Time between two ACT commands)
4. **ACT\_ST**: ACT Command (Read / Write)
5. **WAIT\_ACT\_ST**: Wait tRCD (RAS to CAS Delay)
6. **WRITE0\_ST**: Write Burst : Chunk 1 to len-1 (16 bits)
7. **WRITE1\_ST**: Write Last chunk, before precharge: chunk len (16 bits)
8. **WRITE\_BST\_STOP\_ST**: Wait for tRC (in the precharge state)
9. **READ0\_ST**: Read command - Nothing happens (Time until command is being accepted by SDRAM)
10. **READ1\_ST**: Nothing happens (1 of 3)
11. **READ2\_ST**: Nothing happens (2 of 3)
12. **READ3\_ST**: Nothing happens (3 of 3)
13. **READ4\_ST**: Data delay, since 'dram\_dq' data comes right after clock's rising edge
14. **READ5\_ST**: Read Burst: Chunk 1 to len-1
15. **READ\_BST\_STOP\_ST**: Read last Chunk, chunk 'len', and wait for tRC (in the precharge state)
16. **WAIT\_PRE\_ST**: Wait tRC (Row Cycle Time) to seperate between two ACT commands

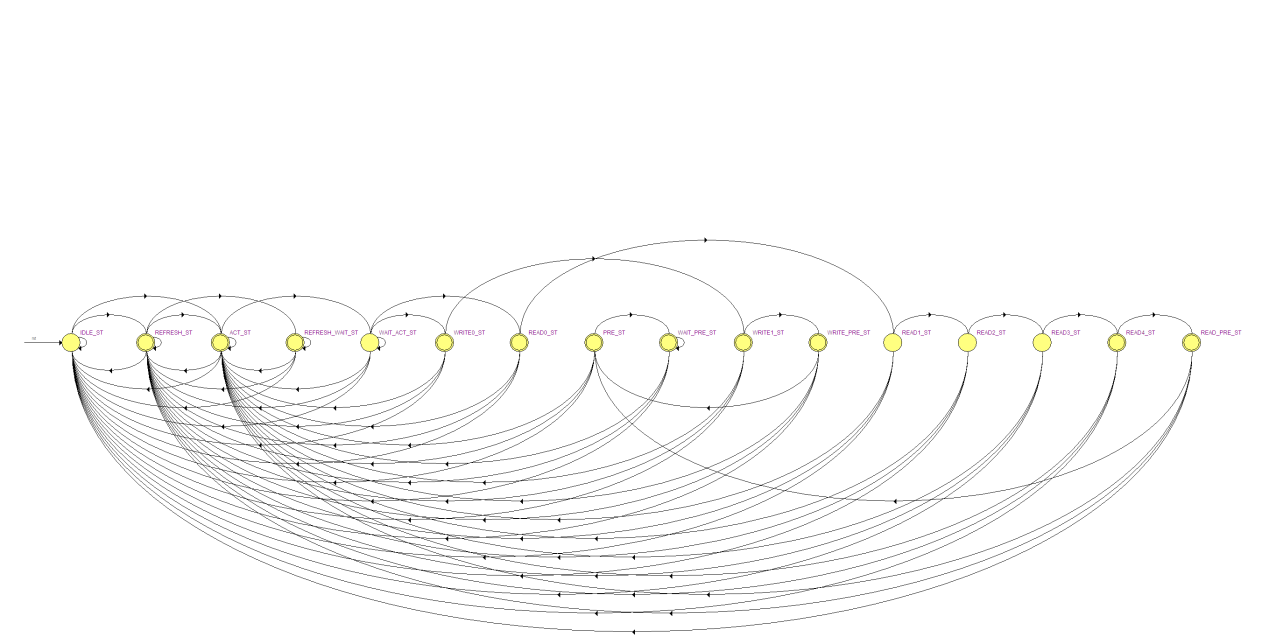


Figure 9 - Main FSM

# Performed test for SDRAM Controller

1. Burst length exceeds page. Causes WBS\_ERR\_O after last WBS\_ACK\_O.
2. WBS\_STB\_O is active when it shouldn't. Causes WBS\_ERR\_O.
3. Write / Read Burst length of 1, 2, 3, 4, 127, 128, 129, 256

1. According to Wishbone standard, the address should be incremented. The SDRAM auto increments the initial address. [↑](#footnote-ref-1)
2. According to Wishbone standard, the address should be incremented. The SDRAM auto increments the initial address. [↑](#footnote-ref-2)