POLITECNICO DI TORINO

Master Degree in Computer Engineering: Embedded Systems
MICROELECTRONICS SYSTEMS

Design and Development of a DLX Microprocessor

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Chapter 1

Introduction

This report aims at being a short documentation on the Microelectronic Systems course project at the first year of the master degree both in Computer and Electronics Engineering at Politecnico di Torino.
The target is the **design** and the **implementation** phase of a pipelined processor by VHDL, as is described in [1], followed by a simple **synthesis** and a **physical layout** definition. The main flow has passed through the following steps:

1. Design and implementation at RTL level
2. Simulation by assembly codes
3. Synthesis and gathering results about timing, area and power consuption
4. Realization of the physical layout

For 1 and 2, I used the *Xilinx ISE Design Suite 14.7*, although during the laboratory sessions the tool was *ModelSim*. I made this choice because I think it's better both from the management of files point of view and for the more intuitive interface of the simulation tool. The synthesis step has been performed by *Synopsys' DesignVision*, whose license has been granted to the Politecnico di Torino. In order to use it, I haved to use a virtual machine, running on *Linux*, provided by the Department of Electronics and Telecommunications servers. Same conditions for the last step, by *Cadence Innovus Implementation System*. Moreover, I liked exploiting *GitHub* functionalities to make easier the passage of data from my *Windows* laptop and the virtual machine; you can download it from `https://github.com/sandrosalvato94/MyDLX`

1.1 Basic vs Pro version

Specification are described in [2], you can find it among files in Documents directory. Summarizing, basics features for the Basic version are:

- **Pipeline**
- **Simple instruction set** (see below)
- **Simple datapath**
- **Basic synthesis**
- **Basic physical design**
- This **report**

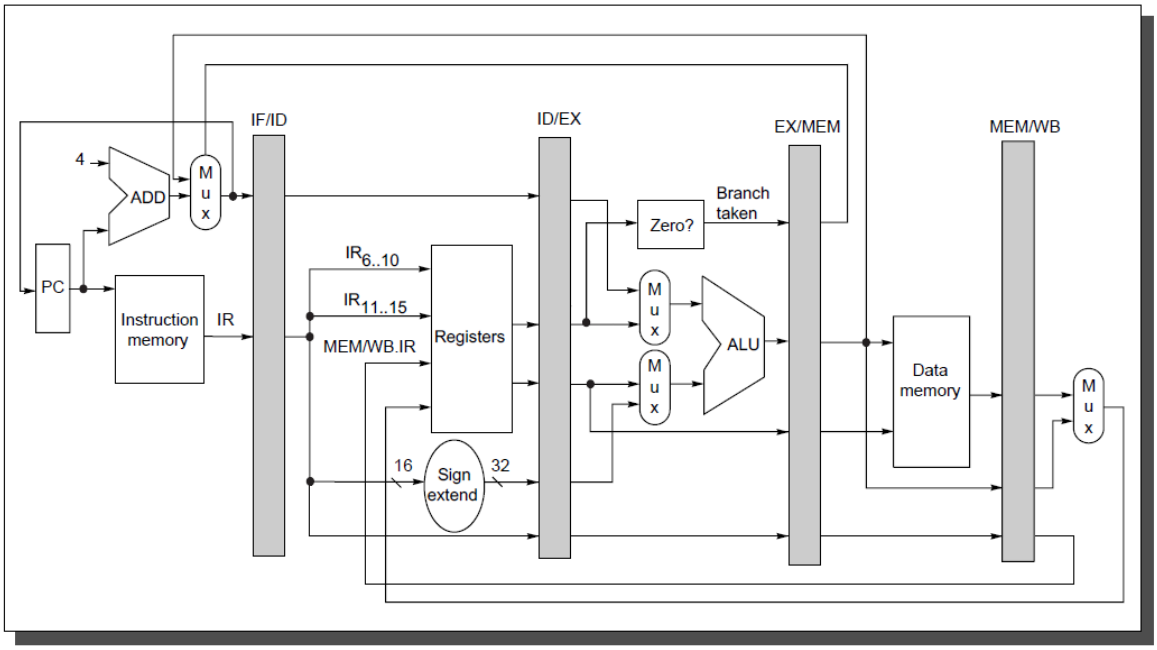

Figure 1.1: Basic DLX Datapath. Figure 3.4 from [1]

Among pro hints, these are reported:

- **Extended instruction set** (see below)
- **Extended datapath**
- **Windowing**
- **Control Hazard**
- **Optimization of the power consuption**
- **Caching**
- **Advanced synthesis**
- **Advanced physical design**
- **Whatever I wanted...**

I targeted the pro version, exploring and implementing the following features:

-

Bibliography

[1] *Computer Architecture: A Quantitative Approach.* Morgan Kaufmann, 2011.

[2] Giovanna Turvani Mariagrazia Graziano, Giulia Santoro. Design and development of dlx microprocessors. Microelectronic Systems Final Project Specification.