Ming-Shiuan Tsai

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Professional Summary

Master's level electrical engineering with multiple tape-out (including layout), circuit testing experiences and strong fundamental electrical and electronics design knowledge. Seeking to leverage my knowledge and skills to bring a prospective design and assistance to the position of Electrical Engineer.

Education

Purdue University, Indiana, USA *Dec. 2017*

Master of science in Electrical and Computer Engineering **Overall GPA: 3.57/4**

- Specialize in VLSI and Integrated Circuit Design
- Related Course: System-On-Chip Design, High-Speed Mixed-Signal IC, Embedded Systems, MOS VLSI Design, CMOS Analog IC Design, Solid State Devices.

National Tsing Hua University (NTHU), Hsinchu, Taiwan *Jun. 2015*

Bachelor of Science in Electrical Engineering **Overall GPA: 3.95/4.3**

- Specialize in VLSI and Integrated Circuit Design

Skills

- **Circuits & Systems**: Microelectronics, Design of analog circuits (Cadence spectrum ADE simulator, Cadence Virtuoso), Digital VLSI systems (Verilog, Design Compiler, SOC Encounter & IC Compiler)
- **Programming**: Python, C, Verilog, Matlab
- **Lab Equipment**: Wire Bond Machine, Spectrum Analyzer, Oscilloscope, Digital Multimeter, Function Generator

Working Experience

Application Engineer *Jan. 2018 – present*

- Everel America, Inc.
  - Create data sheets and provide technical explanations to customer
  - Collect and identify technical data from customer
  - Provide training to new employees or customers
  - Increase the successful rate of inquiries by 15%
  - Successfully solve problems of providing qualified products to customer

Research & Project Experience

Purdue University, West Lafayette, IN, USA

Research Project *Oct. 2015 – Oct. 2017*

- A Single-Chip Wireless Microelectrode Array for Neural Recording and Stimulation
  - Designed Ultra-compact and energy-efficient Low Noise Amplifier(LNA), Multiplexer(MUX).
  - Designed integrated neural amplifiers using DC clamping topology in 45 nm CMOS SOI
  - Solved input DC offset problem during neuron measurement

ECE568 Embedded System *Spring 2016*

- Implemented Raspberry Pi along with passive components to perform image capture and reorganization in the python language
- Implemented Freescale Freedom Development Platform (FRDM-KL46Z) with GPIO, I2C, hardware and software Interrupt to perform e-compass.

ECE559 MOS VLSI Design *Fall 2015*

- Designed a low power (<0.64 mW), high speed (520MHz) multiplier implemented with wallace tree algorithm
- Improved the performance by applying a latency predictor and worst path analysis
- Implemented cadence spectrum and cadence virtuoso

ECE595 CMOS Analog IC Design *Fall 2015*

- Designed a low power (<3 mW), high gain (> 80dB), high CMRR@1KHz(> 100dB) folded cascade operational amplifier
- Analyzed and verified the trade-off between essential functionalities

Languages

- Chinese, English, Taiwanese