FAST NATIONAL UNIVERSITY
School of Computing
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Course Title:	Computer Organization and Assembly Language
Task:	Quiz 5
Section:	BCS-3A
Date:	30th Nov, 2022

Q1 (2 Points): Find at least 3 data hazards in following pipelined instructions. Each stage takes only 1 cycle.

Assembly code in MIPS Architecture	
Pipeline Stages	FI, DI , EX, Mem , WB
Instruction 1:	add R2, R1, R3
Instruction 2:	xor R3, R2, R4
Instruction 3:	add R3, R1, R2

Use following method to write hazard between two instructions.
For Example: Instruction X & Instruction Y on register Z, Instruction X & Instruction Z on register A

RAW: I1 & I2 on R2
WAR: I1 & I2 on R3
WAW:I2 & I3 on R3

Q2 (2 Points): Add stall cycles in given table to remove the hazards from instructions given in **Q1**.

	Clock Cycle																			
Instruction no	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Q3 (2 Point): Find the corresponding address in RAM if Index, tag and offset number is given for differently mapped caches. Show calculations. Index and Tags are given in hex.

i. Direct Mapped Cache
Index= 15 Tag= 255
Address in RAM?

Tag 10 0101 0101
Index 1 0101
Physical Address 100 1010 1011 0101(Assuming index size is 5 bits)