(a) MOSFET-Level Netlist

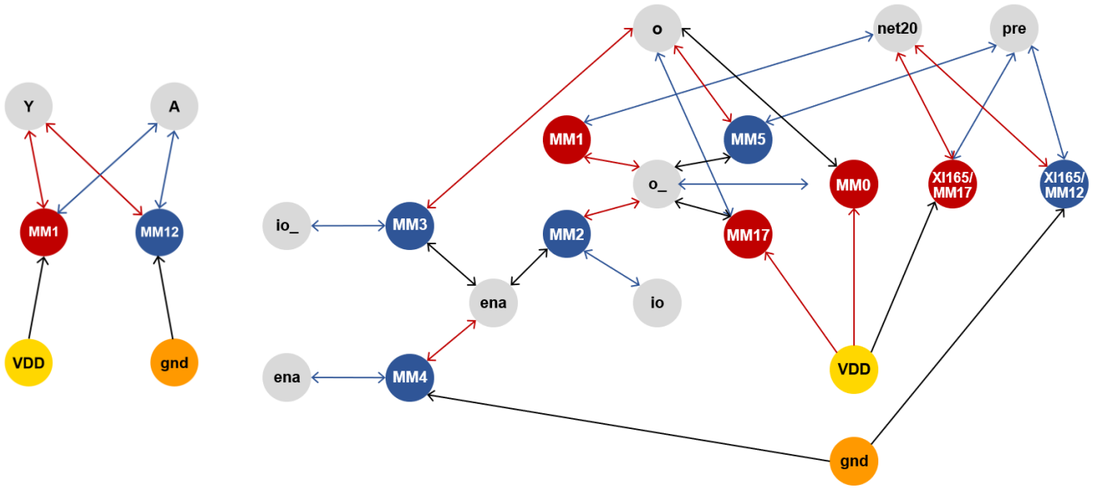
Target circuit

```
.SUBCKT inv A Y
MM1 Y A vdd! vdd! PMOS W=Wp L=Lp M=M
MM12 Y A gnd! vbb! NMOS W=Wn L=Ln M=M
.ENDS
```

Entire circuit

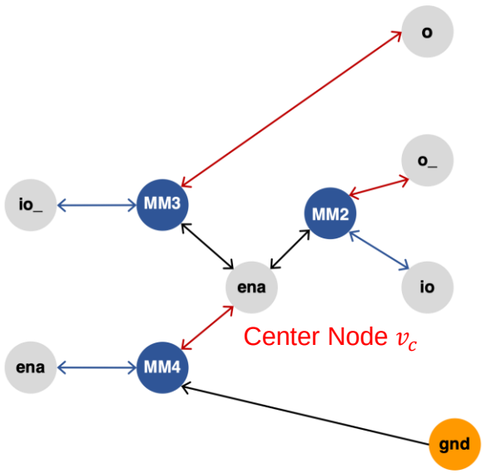
```
.SUBCKT main_sense ena io io_ o o_ pre
XI165 pre net20   inv Ln=0.35u Wn=4u M=1 Lp=0.35u Wp=8u
MM5 o pre o_ vbb! NMOS W=1.4u L=350.00n M=1
MM2 o_ io net21 vbb! NMOS W=7u L=350.00n M=1
MM3 o io_ net21 vbb! NMOS W=7u L=350.00n M=1
MM4 net21 ena gnd! vbb! NMOS W=7u L=350.00n M=1
MM0 vdd! o_ o vdd! PMOS W=14u L=350.00n M=1
MM1 o_ net20 o vdd! PMOS W=1.4u L=350.00n M=1
MM17 vdd! o o_ vdd! PMOS W=14u L=350.00n M=1
.ENDS
```

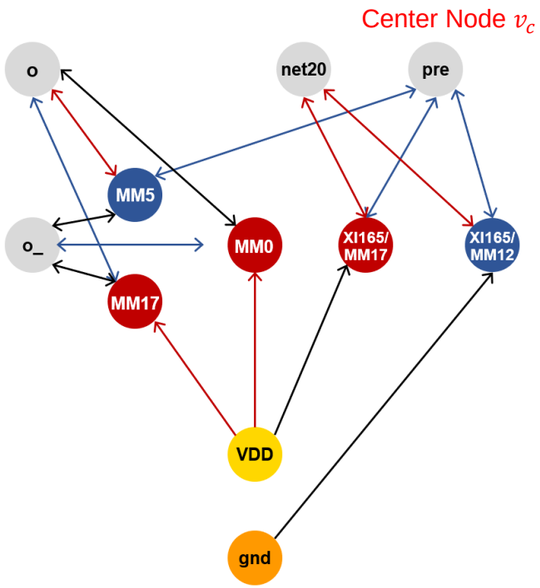
(b) 2.1 Transformation of Netlists into Graphs



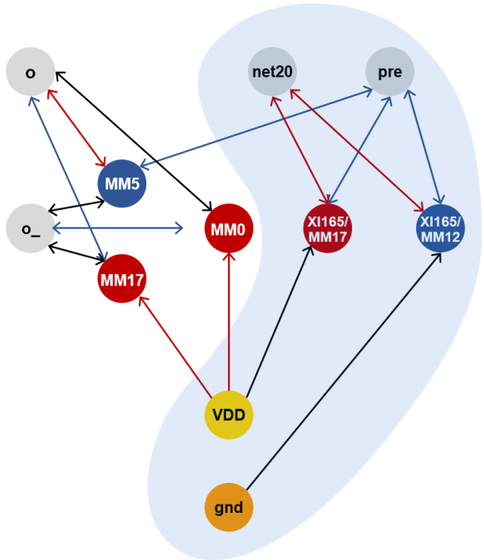
Target circuit $\mathcal{G}_T$ Entire circuit $\mathcal{G}_E$

(c) 2.2 K-hop Subgraph Formation

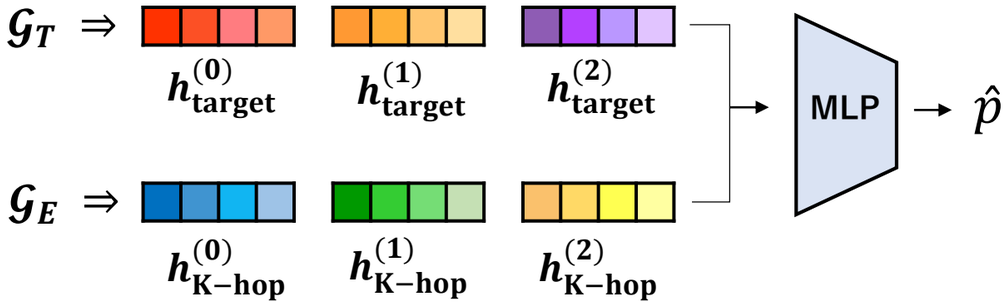




(e) 2.4 Target Graph Matching



(d) 2.3 Target Region Prediction



$$\mathcal{L}(y, \hat{p}) = -\frac{1}{N}\sum_{i=1}^{N}[y_i \log(\hat{p}_i) + (1 - y_i)\log(1 - \hat{p}_i)]$$