

Conformal Lec User Manual

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Practical ECOs using Conformal ECO tool - Cadence

Gates On the Fly Use Case: Conformal LEC failures debug www.nandigits.com Conformal LEC schematic Conformal LEC GUI debug tool gave some useful information, but not sufficient and efficient. The schematic from LEC debug tool printed out too many gates and connections. The culprit gates were hiding somewhere.

Conformal LEC failures debug by using Gates On the Fly

EE 577b Spring 2010 Conformal Logic Equivalence Checking (LEC) Tutorial. by Ko-Chung Tseng This tutorial provides a quick getting-strated guide to Cadence Conformal logic equivalence checking. The basic flow is to input both an RTL netlist and a synthesized netlist and then have Conformal check whether both netlists are equal.

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Cadence Conformal suite of tools contains a tool called Logic Equivalence Checker or LEC. Section 4 of this tutorial describes how to formally verify that the synthesized design is functionally equivalent to the RTL description using LEC. This section can be skipped if one chooses to use Formality for equivalence checking. During the ...

Digital Logic Synthesis and Equivalence Checking Tools ...

different Cadence Conformal LEC capabilities and what benefits they provide, describing information can provide a significant saving of time and increase in user productivity. .. on the implementation team is similar to manual ECOs.

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1 The Conformal LEC software does not support the read_comments_as_HDL synthesis directive, and the directive does not affect the Conformal LEC software. Table 17-1 lists supported pragmas and trigger keywords for formal verification. c Do not use Verilog 2001-style pragma declarations. The Quartus II software and the

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