

Cadence Conformal Lec User Manual

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Conformal Equivalence Checker - Cadence Design Systems

Equivalence Checking Using Cadence Conformal LEC Formal Hardware Verification ... CONFORMAL-LEC Preferences Window LEC> add compared points —all LEC> compare LEC> Compare done! Compared points Equi ent Non—equi u al ent T -VHDL —Rev i sed

Equivalence Checking Using Cadence Conformal LEC

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different Cadence Conformal LEC capabilities and what benefits they provide, describing information can provide a significant saving of time and increase in user productivity. .. on the implementation team is similar to manual ECOs.

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EE 577b Spring 2010 Conformal Logic Equivalence Checking (LEC) Tutorial. by Ko-Chung Tseng This tutorial provides a quick getting-started guide to Cadence Conformal logic equivalence checking. The basic flow is to input both an RTL netlist and a synthesized netlist and then have Conformal check whether both netlists are equal.

Cadence Conformal Tutorial | Electronic Design | Design

Conformal ECO Steps R1 vs R2 • Compare LEC golden RTL and Modified RTL. • Review the non-equivalence points. R1 vs LAY1 • Compare Golden PNR netlist with original RTL. This should be clean. R2 vs G2 • New RTL with ECO fix compared with synthesized netlist of R2 for equivalence. This should be clean. LAY1 vs G2 • Non-equivalence expected.

Practical ECOs using Conformal ECO tool - Cadence

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Cadence Encounter Conformal Support This chapter describes equivalence checking with the Cadence Encounter Conformal ... Conformal LEC software to verify the functional equivalence of the register transfer level (RTL) source code and post-fit.vo with the Quartus II software when using

17. Cadence Encounter Conformal Support - intel.com

Again the ref/user manuals should help you with that. What do you not understand about the synchronization rules? I found the whole two flows things a bit confusing at first and only after talking to Cadence people did I understand it. I assume if you have read the documentation (or part of it :) then you know that Lec has 2 CDC flows.

can LEC provide cdc check? - Logic Design - Cadence ...

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LEC - Conformal RTL to netlist mismatch. hnfq over 6 years ago. ... The Cadence Design Communities support Cadence users and technologists interacting to exchange ideas, news, technical information, and best practices to solve problems and get the most from Cadence technology. The community is open to everyone, and to provide the most value, we ...

LEC - Conformal RTL to netlist mismatch - Logic Design ...

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Page 1 ENCOU N TE R C O N F O R M A L E Q U I V A L E N C E C H E C K E R Cadence Encounter Conformal Equivalence Checker (EC), ® ® ® makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the only complete equivalence checking solution available for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.

CADENCE ENCOUNTER CONFORMAL EQUIVALENCE CHECKER DATASHEET ...

sedEquivalence Checking Using Cadence Conformal LEC Conformal Lec User Manual Cadence ® Conformal ® Equivalence Checker (EC) makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the industry's only complete equivalence checking

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Gates On the Fly Use Case: Conformal LEC failures debug www.nandigits.com Conformal LEC schematic Conformal LEC GUI debug tool gave some useful information, but not sufficient and efficient. The schematic from LEC debug tool printed out too many gates and connections. The culprit gates were hiding somewhere.

Conformal LEC failures debug by using Gates On the Fly

Best known methods for using Cadence Conformal LEC at Intel 3 The design that we use as our test case is a high-performance, dual-port gigabit Ethernet controller for servers and embedded system design [7].

Best known methods for using Cadence Conformal LEC at Intel

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