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This reference flow is a complete RISC-based SoC design plus a set of UVM verification components (UVCs), allowing users to learn about the UVM and execute their UVM testbenches. The UVM Reference Flow is a subset of the Incisive Verification Kit, which provides powerful hands-on workshops, labs, and videos for comprehensive user understanding.

Universal Verification Methodology - Cadence

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Vermont SAMS Reference Manual - asd.vermont.gov

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