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VHDL Lab Manual | Avijit Bose - Academia.edu

2. Write HDL code to control speed, direction of DC and Stepper motor. 3. Write HDL code to accept 8 channel Analog signal, Temperature sensors and display the data on LCD panel or Seven segment display. 4. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude. 5.

HDL Lab - Institute of Technology

EXPERIEMENT NO. 1 Simulation using all the modeling styles and Synthesis of all the logic gates using Verilog HDL AIM: Perform Zero Delay Simulation of logic all the gates written in behavioral, dataflow and structural modeling style in Verilog using a Test bench. then, Synthesize each one of them on two different EDA tools.

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HDL Cholesterol Laboratory Procedure Manual

Lab Manual 5. LAB 1 The MIPS datapath in Verilog: The IF stage Objective: To implement and test the Instruction Fetch (IF) pipeline stage of the MIPS five stage ... units, which can be quite tedious, time consuming, and beyond the scope of this lab series. The slightly revised MIPS datapath to be

implemented is in figure 1.1 on page Lab 1-2.

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