Current Starved Ring Oscillator Based ADC Using 18nm FinFET Technology

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Abstract -- The goal of achieving high performance, low power consumption, and small area footprint is still central to the field of analog-to-digital converters (ADCs). This work describes a new methodology that enables the design of Current Starved Ring Oscillator (CSRO) architecture using 18nm FinFET technology. The CSRO based ADC meets the growing needs of contemporary electronic systems with promised improvements in speed, power efficiency, and portability. The intrinsic qualities of FinFET transistors are utilized by the CSRO architecture to produce high performance metrics. Such as improved sub threshold behavior, lower leakage currents, and superior gate control, all of which are essential for low power consumption and high speed operation. In addition, compared to conventional ADC designs, the 18 nm production node enables tighter component integration, resulting in a compact ADC design. The precise analog-to-digital conversion is made possible by controlling the oscillation frequency through the use of current starving techniques. In order to reduce power consumption and mitigate electromagnetic interference, starving ring oscillators are important components of contemporary electronics. They also ensure regulatory compliance and extend battery life. The ability of the GDI (Gate Diffusion Input) technique to lower space overhead and power consumption makes it essential for digital circuit design. It provides an effective solution for low-power and high-density applications in contemporary integrated circuits. The proposed CSRO-to need ADC with GDI technique experiences a delay of 1.208 ns and power of 356.8 mW. This shows that the proposed ADC is 0.2 times faster than the ADC without GDI technique.

Keywords- Current starved ring oscillator, ADC, GDI technique, FinFET technology

I.INTRODUCTION

A.CURRET STARVED RING OSCILLATOR

Current starved ring oscillators (CSROs) are fundamental building blocks in digital and mixed-signal electronic circuits and provide stable clock signals during generation. It has a series of inverter stages connected in a ring configuration as shown in Figure 1.1, with each stage driven by a finite current source. When the signal propagates through the inverter, it causes periodic oscillations and provides a precise and controllable output frequency. CSROs are widely used in many applications such as clock generation, frequency synthesis, and phase-locked loops (PLLs) where reliable and accurate signal timing is important. In an oscillator devoid of ring current, "current starvation" is a limiting factor for the bias current introduced. This parameter is important to control the oscillation frequency of the oscillator. The necessity of current starvation arises from two objectives, namely, ensuring frequency control and low performance of the oscillator. By limiting the bias current, engineers can adjust the switching speed of the transistors in the oscillator inverter, thus fine-tuning the circuit oscillation frequency. Fig. 1 represents the circuit diagram of current starved ring oscillator. This level control is necessary to adjust the oscillator's output to meet the specific frequency pattern determined by the application. Additionally, limiting the bias current can reduce power consumption in the oscillator, which is especially important for high-power applications such as portable electronic devices or IoT.

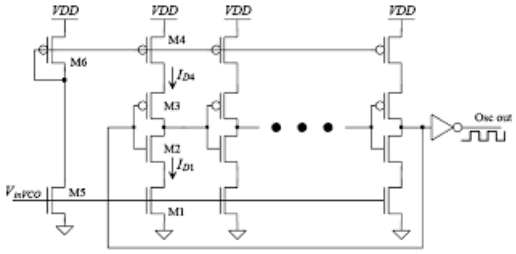

Fig.1Current starved ring oscillator

B.ANALOG TO DIGITAL CONVERTER

Current starved ring oscillators and counters in ADC architecture represent a new approach to digital to digital conversion that combines simplicity with performance to meet the demands of the product. Use electricity today. Unlike traditional power controlled oscillators, which often suffer from high power consumption, current-hungry oscillators work by controlling biased current flow through the ring inverter. This unique mechanism enables precise frequency modulation, forming the basis of analog signal quantization. By connecting the oscillator to the electronic counter, the oscillation frequency is converted into a digital output, helping to capture the

signal in the specified time. This combination has unique benefits such as better energy efficiency, making it particularly suitable for battery and paper applications.

C.FinFET TECHNOLOGY

A FinFET is a form of Field-Effect Transistor that is not completely planar but instead has a thin vertical fin. The pathway created between the source and drain is entirely wrapped by the gate on three sides. In comparison to planar FETs, the larger surface area generated between the gate and channel offers better control of the electric state and lower leakage. Compared to planar FETs, FinFETs yields significantly higher electrostatic control of the channel and improved electrical properties. The fin, which serves as the semiconductor channel, has the gate electrode wrapped around each of its three sides. The gate electrode receives a voltage that creates an electric field that regulates the channel's current flow. FinFETs can function at lower voltages than planar FETs, which lowers their power requirements. FinFET technology has a variety of advantages over bulk CMOS, including scalability of the transistor beyond 28nm, greater speed, reduced leakage, lower power consumption and higher driving current. The two distinct types of FinFET gate structures are shorted gate (SG FinFET) and independent gate (IG FinFET).Fig.2 represents the two types of FinFET gate structures.

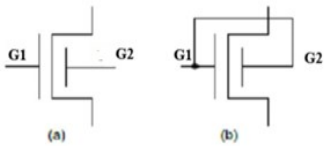

Fig.1 (a) Independent gate FET (b) Shorted gate FET

D.GDI TECHNIQUE

The gate diffusion input technique employs a single basic cell to accomplish a variety of logic operations. The four terminals of the GDI cell are D (common diffusion node), P (input to drain/source of PMOS), N (input to drain/source of NMOS), and G (common gate input) in fig.2. The basic logic gates like AND, OR, NOT, NAND, and NOR as well as higher-level operations like adders, subtractions, and multipliers can all be implemented using the GDI cell. Table 1 illustrates the different function of GDI cell GDI circuits often use less power and are faster and smaller than conventional CMOS circuits. It is an effective technique for designing low-power digital circuits and it is particularly well-suited for applications such as portable devices and battery powered systems.

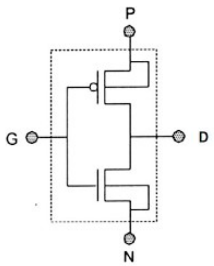

Fig.2 Basic GDI cell

Table 1 Different logic function realization using GDI cell

N	P	G	OUTPUT	FUNCTION
0	B	A	A'B	F1
B	1	B	A'+B	F2
1	B	A	A+B	OR
B	0	A	A.B	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B'	B	A	A'B+AB'	XOR
B	B'	A	AB+A'B'	XNOR

II. LITERATURE REVIEW

The current starved ring oscillator based ADC has been designed with different modules such as NAND gates, D Flip flops and Counter. In the conventional method using CMOS the VCO based ADC has high power consumption and propagation delay when compared to FinFET technology.

Prakash Sharma et al (2022) proposed the ring oscillators and current starved voltage-controlled oscillators (CS-VCOs) especially for frequency generation and timing applications. In comparison to CS-VCOs, CMOS ring oscillators usually consume less power. In regards to phase noise performance, NMOS ring oscillators outperform CS-VCOs and CMOS ring oscillators. Sanjay Kumar et al (2020) proposed that the ring oscillators have minimum transistor count and a fairly simple design. Because of this, they are more susceptible to aging-related changes in the circuit and variances in the process. The high sensitivity of oscillation frequency of this oscillator to degradation causes and process variations is a major advantage for reliability characterization.

Renjie et al (2020) proposed the Voltage Controlled ring oscillators with VCO gain. The VCOs are essential components of many electronic systems, whereas challenges like supply voltage fluctuations, process variances, and temperature changes can all impact the functions.. Satyendra et al (2020) has proposed the Current Starved ring Oscillator with 16nm technology. The CSROs are essential parts of many mixed-signal and digital integrated circuits, providing benefits including accurate frequency control, small size, and low power consumption.
Ravi et al (2020) proposed the current starved ring oscillator for high frequency. The CSVCOs are vital parts of wireless transceivers, frequency synthesizers, and a variety of communication systems because they can produce consistent oscillations over a large tuning range with minimal power consumption. Prithivi raj et al (2021) proposed the high frequency current starved sleep voltage controlled oscillator. It has the crucial parts of PLLs. CSVCOs provide 8 accurate clock generation and frequency synthesis in a range of integrated circuits and communication systems.

John et al (2020) proposed the gain voltage controlled with spin hall nano oscillator (SHNO) damping. Due to their tunable features and prospective uses in data processing and storage, SHNOs have become attractive options for spintronic gadgets. Energy savings and usefulness are two major benefits of being able to control the

damping of SHNOs using voltage control. Changsik et al (2022) has proposed the digital low dropout regulator (DLDO) with voltage controlled oscillator. The DLDOs are essential components of contemporary integrated circuits as they deliver little dropout voltage and consistent, controlled output voltages.

Dina (2023) proposed the voltage controlled based analog to digital converter in CMOS. The creation and implementation of analog-to-digital converters (ADCs) based on voltage-controlled oscillators (VCOs) on 130-nm CMOS technology is for use in biological applications. Analog-to-digital converters (ADCs) are essential parts of biomedical signal processing systems that enable analog signals to be converted into digital data for analysis and interpretation. Xinpeng Xing et al (2023) proposed the calibration algorithm for VCO. The fully digital calibration techniques for analog-to-digital converters (ADCs) based on voltage-controlled oscillators (VCOs), are advantageous for a variety of applications, such as wireless communication, sensor networks, and biomedical devices. Jiang et al (2021) has designed the Analog-to-Digital Converter (ADC) design for compute-in-memory (CIM) arrays are examined in the study "Analogto-Digital Converter Design Exploration for Compute-in-Memory Accelerators". For deep neural networks, multiply-and-accumulate (MAC) operations must be executed efficiently.

Das et al (2021) proposed the accurate conversion of analog biological signals (such as ECG and EEG) to digital data is crucial for processing and analysis in biomedical applications. ADCs and DACs are essential to this method. The amount of bits required to represent an analog signal is determined by its resolution. Mahmood et al (2020) proposed the low-power circuit design research has been driven by the growing desire for electronics that use less power. JK flip- 11 flops, Master-Slave arrangements, and even specialized designs aimed at particular low-power techniques could come under this classification. Vallabhuni et al (2020) proposed the advantages of FinFETs (Fin Field Effect Transistors) over conventional MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) have made them a potential technology for low-power digital circuit.

Mukherjee (2023) proposed the inherent speed of light, QD-SOAs may be able to function at significantly quicker speeds than electronic NAND gates. Electronic signals are used in conventional NAND gates. In the existing method the current-starved ring oscillator and counter modules in the analog to digital converter design are made 12 possible by the NAND gate and D flip flop. The present method uses CMOS technology to create the starving ring oscillator. In comparison to FinFET technology, it uses a higher amount of power. The proposed strategy is made with FinFET technology and uses the GDI methodology for D flip flops and NAND gates. In comparison, the GDI technique uses fewer transistors than the traditional methods. It also reduces the total amount of power consumption and delay together with the reduction in number of transistors.

III EXISTING METHODOLOGY

A.CSRO USING CMOS TECHNOLOGY

The current-starved ring oscillator, a cornerstone in CMOS (Complementary Metal-Oxide-Semiconductor) technology, serves as a fundamental component for generating clock signals and synthesizing frequencies within digital systems.Fig.3 illustrates the current starved ring oscillator, its architecture consists of an odd number of interconnected inverter stages forming a loop. Each stage incorporates PMOS (P-type Metal-Oxide-Semiconductor) and NMOS (N-type Metal-Oxide Semiconductor) transistors, arranged in series between the power supply voltage (VDD) and ground (GND), with interconnected gates. One of these stages operates at a higher bias current, designated as the current-starved stage, while the remaining stages operate at lower currents. When a clock signal is applied, the inverter stages cyclically charge and discharge the capacitive load at each stage output.

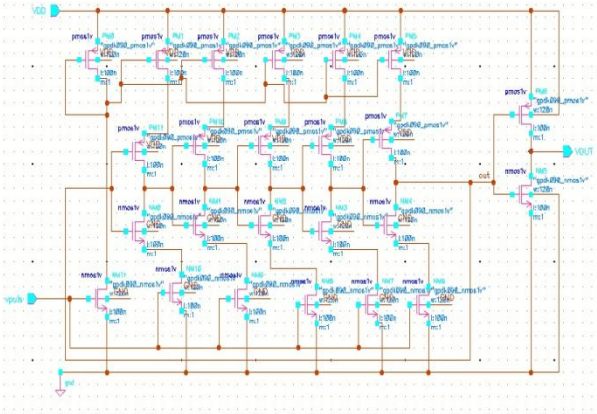

Fig.3 Current starved ring oscillator using CMOS technology

B.CSRO BASED ADC USING CMOS TECHNOLOGY

The CSRO-VCO based ADC compresses of oscillator, D Flip Flop and counters. A D flip flop is a synchronous sequential logic device that stores one bit of binary information. It has two inputs: CLK (clock) and D (data). Fig.4 represents the CSRO based ADC circuit diagram. The value of the D input on the rising edge of the clock signal equals the Q output of the D flipflop. The D flip-flop maintains the current state (Q) when the clock signal is weak. The D flip-flop stores the value of The D input when the clock signal is high.Flip-flops are simple memory components with the ability to store binary data, and they are commonly used in the construction of counters. The binary counter, which counts in binary from 0 to 2^n - 1, where n is the number of bits used, is the most popular kind of counter. An encompassing method for transforming analog signals into digital representations is to incorporate a counter and a current-starved ring oscillator (CSRO) into an analog-to-digital converter (ADC). The ADC receives its clock signal from the CSRO, which offers a precise and reliable timing signal that is essential for proper sampling.

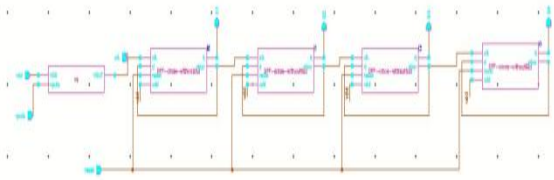

Fig.4 CSRO based ADC using CMOS Technology

IV .PROPOSED METHODOLOGY

A.CSRO USING FinFET TECHNOLOGY

Circuit used in integrated circuits to produce clock signals or other periodic waveforms is called Oscillator. Current starved Ring Oscillator describes how the oscillator functions by regulating the current that is delivered to the ring of inverters. The structure of five stages CSRO based VCO is displayed in Fig.5 represents the current starved ring oscillator using FinFET technology.

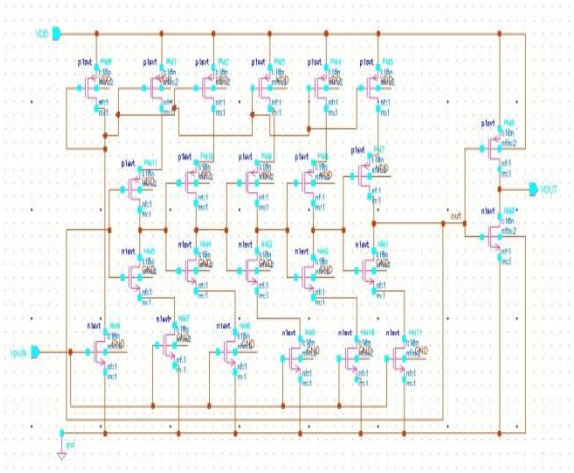

Fig.5 CSRO using FinFET technology

B.NAND GATE WITH GDI USING FinFET TECHNOLOGY

The GDI technique makes use of configuration of NAND or NOR gates as shown in Figure 4.2, which are each made up of a mix of parallel and series transistors. The basic design starts with the creation of a timed inverter, which is an inverter with an additional input for the clock signal, created by utilizing GDI based NAND gate. The integration of GDI based gates subsequently enables the creation of a feedback path and data input.Fig.6 and 7 represents the 2-input NAND gate and 3-input NAND gate.

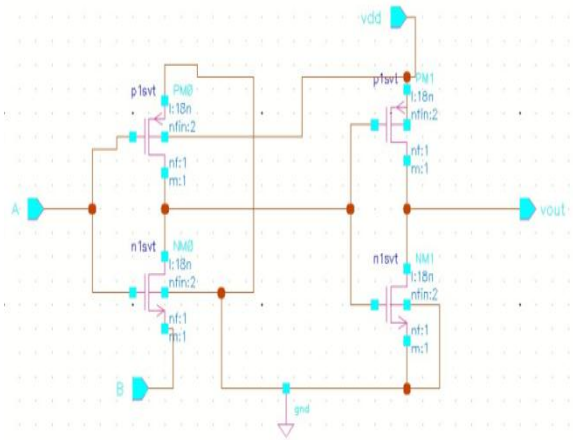

Fig.6 2-input NAND gate with GDI technique

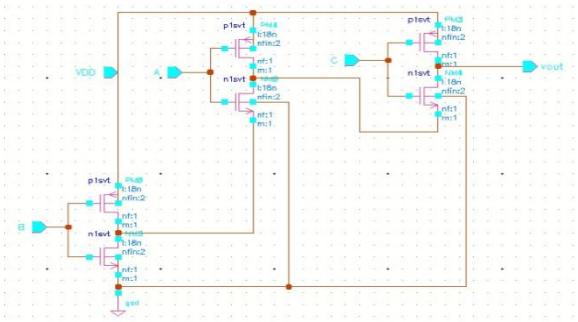

Fig.7 3-input NAND gate with GDI technique

C. D FLIP FLOP WITH GDI TECHNIQUE USING FinFET TECHNOLOGY

D Flip-Flops (DFFs) can be used to build a binary counter that makes the counting of binary values in response to clock pulses easier. Every DFF functions as a storage unit for a single counter value bit. The feedback loop can be created so that the counter can cycle through binary values by connecting the Q output of each DFF to the D input of the next DFF. Fig. 8 illustrates the architecture of D flip flop using GDI Technique.

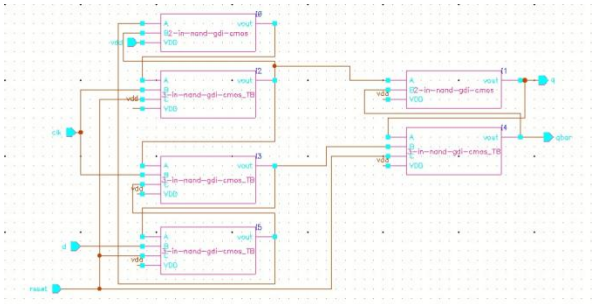

Fig.8 D flip flop employs GDI technique using FinFET technology

D. *CSRO BASED ADC WITH GDI TECHNIQUE USING FinFET TECHNOLOGY*

Integration of D flip-flops and counters into ADCs using FinFET Transistors represents a major advance in the conversion of analog to digital circuits. The utilization of D flip- flops, and counters in ADCs can increase speed, reduce power consumption, and increase reliability. Fig.9 represents the CSRO based ADC employing GDI using FinFET technology.

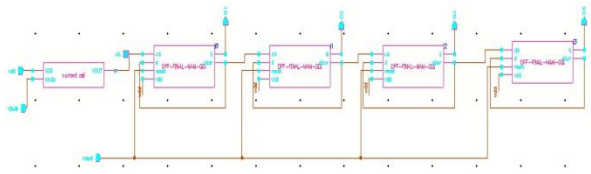

Fig.9 CSRO based ADC in FinFET Technology

V.RESULTS AND DISCUSSIONS

A.EXISTING METHOD

1) Current Starved Ring Oscillator: The schematic of 5-Stage CSRO-VCO circuit is shown in Fig.10. It uses a supply voltage of 1.2V. Fig.11 displays the simulation outcome of 5-Stage CSRO employing 90nm CMOS technology which generates frequency of 10 GHz.

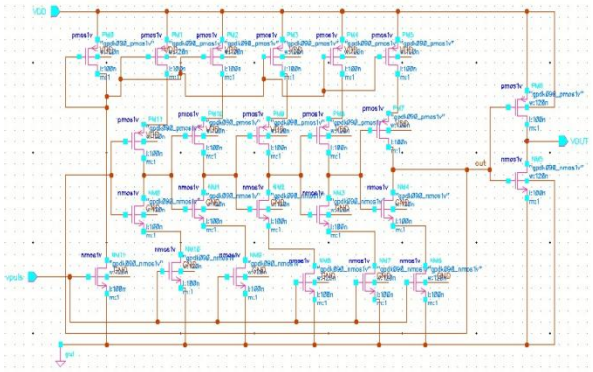

Fig.10 5-Stage CSRO using 90nm CMOS Transistor

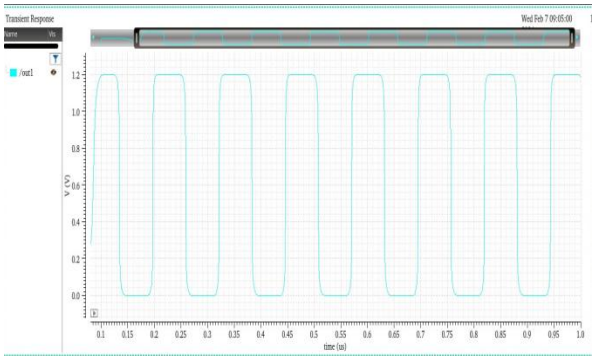

Fig.11 Output of CSRO using 90nm CMOS Transistor

The Table 1 illustrates the Average power and delay for existing Current Starved Ring Oscillator with 90nm CMOS technology circuit various input combinations from 0.6V to 1.4V. The current starved ring oscillator conserves average 428.39mW of power and a delay of 3.86ns.Fig.13 illustrates the graphical representation of power and delay analysis of CSRO using FinFET Technology

Table 1 Average power and delay of CSRO for various input conditions

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	636.71	9.32
1.2	5.80.75	6.08
1	482.26	2.13
0.8	372.75	1.51
0.6	302.46	0.45
AVERAGE	428.39	3.86

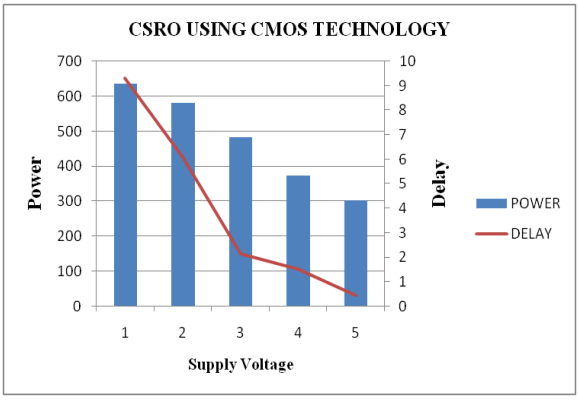

Fig.13 Power and delay of CSRO using CMOS Technology

2) 2-Input and 3-Input NAND Gate: The schematic of 2 input NAND 3 input NAND gate circuits are designed with CMOS Transistor are shown in Fig.14 (a) and Fig.14 (b). It uses a supply voltage of 1.2V. Fig.15 and Fig.16 displays the simulation outcome of 2 Input NAND gate and 3-Input NAND gate designed using 90nm CMOS transistors.

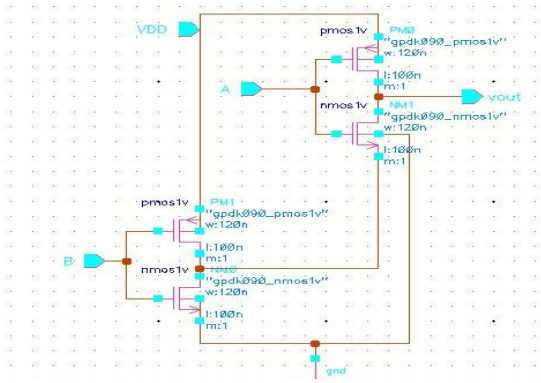

Fig.14 (a) 2 -Input NAND gate with GDI technique

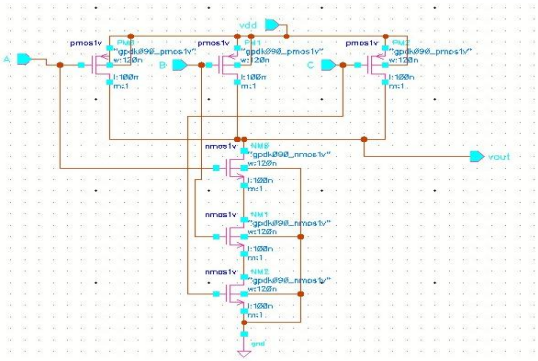

Fig.14 (b) 3 -Input NAND gate with GDI technique

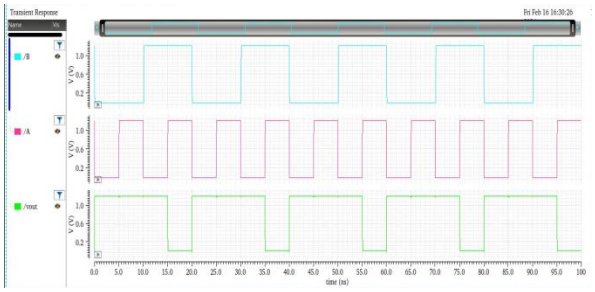

Fig.15 Output of 2 –Input NAND Gate

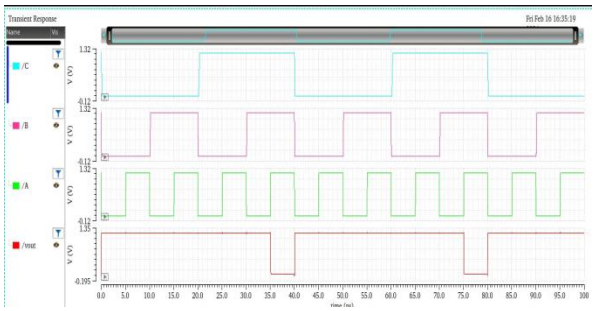

Fig.16 Output of 3 –Input NAND Gate

3)D Flip Flop Using FinFET Technology: The schematic of D Flip Flop circuit shown in Fig.17 designed with 2 Input and 3 Input NAND gate without using GDI Technology. It uses a supply voltage of 1.2V. Fig.18 displays the simulation outcome employing 90nm CMOS technology.

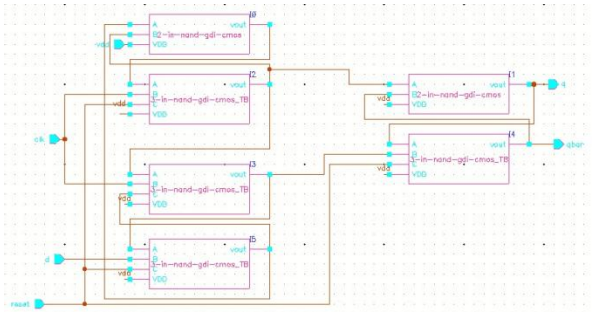

Fig.17 D flip flop using CMOS Technology

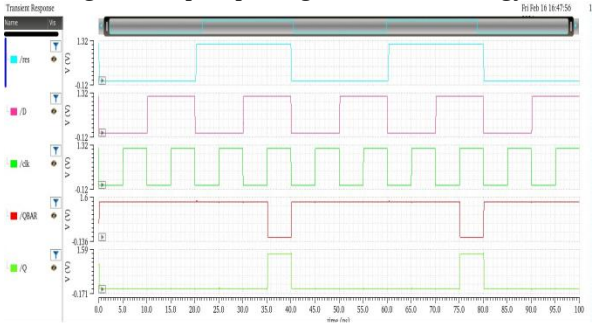

Fig.18 Output of D flip flop using CMOS Technology

The Table 2 illustrates the Average power and delay for existing D Flip Flop with 90nm CMOS transistor and without GDI Technology circuit various input combinations form 0.6V to 1.4V. The D Flip Flop conserves 97.325mW of power and a delay of 31.09ns.Fig 19 illustrates the graphical representation of the power and delay analysis of D flip flop using CMOS Technology

Table 2 Average Power and Delay of D Flip Flop for Various supply voltage

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	41.94	32.54
1.2	61.21	25.13
1	82.26	32.57
0.8	110.19	32.59
0.6	122.91	32.64
AVERAGE	97.325	31.09

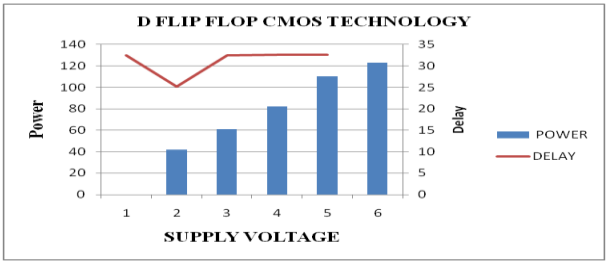

Fig.19 Power and delay of D flip flop using CMOS Technology

4)*VCO Based ADC*: The schematic of ADC circuit designed with Current Starved Ring Oscillator with different counters using D Flip Flop without GDI Technology in fig.20. It uses a supply voltage of 1.2V. Fig.21 displays the simulation outcome employing 90nm CMOS Transistor.

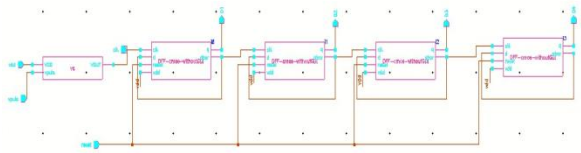

Fig.20 VCO Based ADC using CMOS Technology

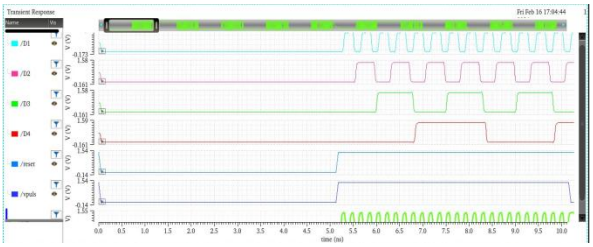

Fig.21 Output of VCO Based ADC using CMOS Technology

The Table 3 illustrates the Average power and delay for existing CSRO-VCO based ADC with 90nm CMOS technology and without GDI Technology circuit various input combinations from 0.6V to 1.4V. The CSRO-VCO based ADC conserves 442.5mW of power and a delay of 2.8ns.Fig.22 illustrates the graphical representation of power and delay analysis of VCO based ADC.

Table 3 Average Power and Delay of CSRO-VCO Based ADC Using 90nm CMOS Transistor

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	781.3	4.2
1.2	714.3	2.15
1	497.6	2.16
0.8	401.6	2.2
0.6	108.0	3.65
AVERAGE	442.5	2.8

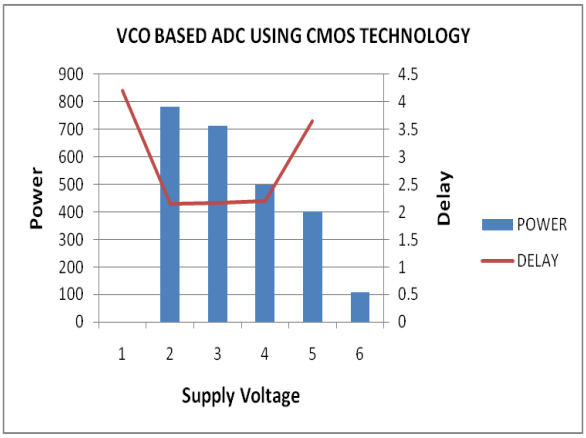

Fig.22 Power and delay of VCO Based ADC using CMOS Technology

B.PROPOSED METHOD

1) Current Starved Ring Oscillator: The schematic of 5-satge CSRO-VCO circuit is shown in Figure 23. It uses a supply voltage of 1.2V. Figure 24 displays the simulation outcome of 5-stage CSRO employing 18nm FinFET Transistors which generates frequency of 10 GHz.

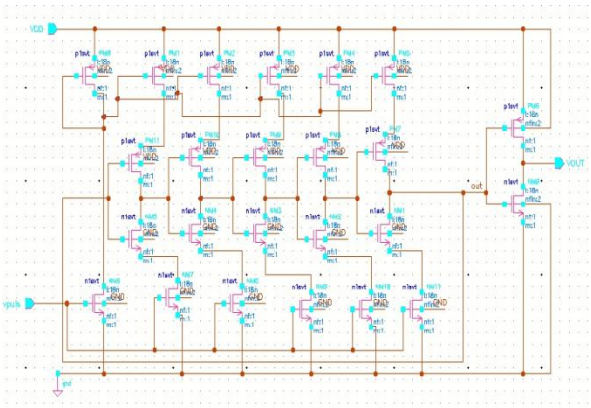

Fig.23 5-Stage CSRO using 90nm CMOS Transistor

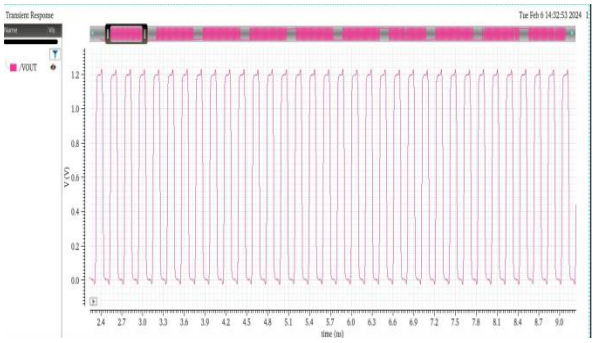

Fig.24 Output of CSRO using 90nm CMOS Transistor

The Table 4 illustrates the Average power and delay table for Proposed Current Starved Ring Oscillator with 18nm FinFET technology circuit various input combinations from 0.6V to 1.4V. The current starved ring oscillator conserves 335.51mW of power and a delay of 1.13ns.Fig.25 illustrates the graphical representation of power and delay analysis of CSRO using FinFET technology.

Table 4 Average Power and Delay of CSRO-VCO Using 18nm FinFET Transistor

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	533.11	6.25
1.2	336.53	0.24
1	372.35	0.17
0.8	446.30	0.12
0.6	218.06	0.06
AVERAGE	335.51	1.13

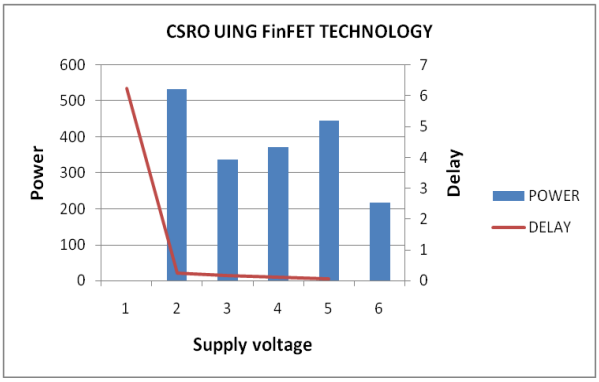

Fig.25 Power and delay of CSRO using CMOS Technology

2) *2 Input and 3 Input NAND Gate:* The schematic of 2 input and 3 input NAND gate circuits are designed with FinFET Transistor and with GDI Technology are shown in Figure 26 (a) and Figure 26 (b). It uses a supply voltage of 1.2V. Figure 27 and 28 displays the simulation outcome of 2 Input and 3 Input NAND gate designed using 18nm FinFET technology.

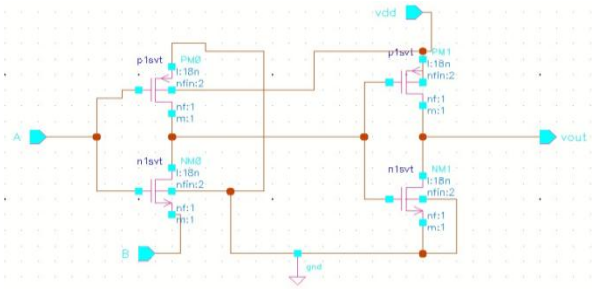

Fig.26 (a) 2 -Input NAND gate with GDI technique

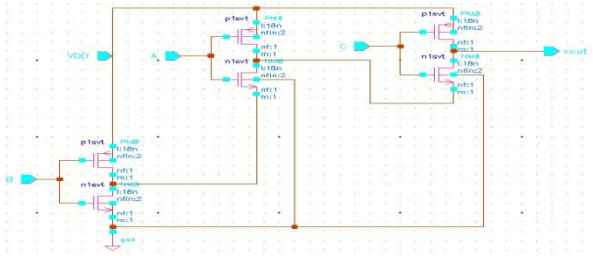

Fig.26 (b) 3 -Input NAND gate with GDI technique

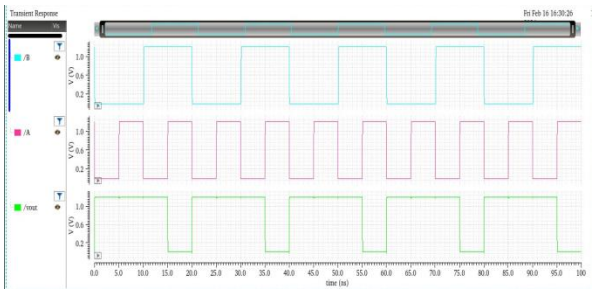

Fig.27 Output of 2 –Input NAND Gate

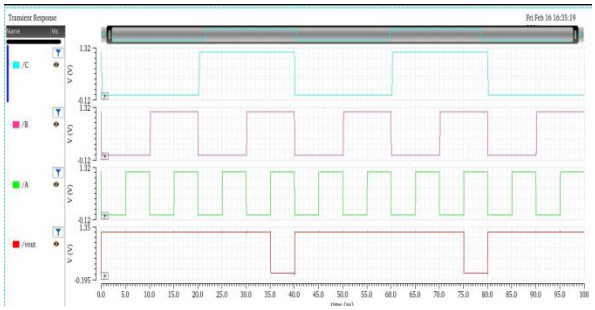

Fig.28 Output of 3 –Input NAND Gate

3) D Flip Flop With GDI : The schematic of D Flip Flop circuit shown in Figure 29 designed with 2 Input and 3 Input NAND gate using FinFET Transistor and GDI. It uses a supply voltage of 1.2V. Figure 30 displays the simulation outcome employing 18nm FinFET technology.

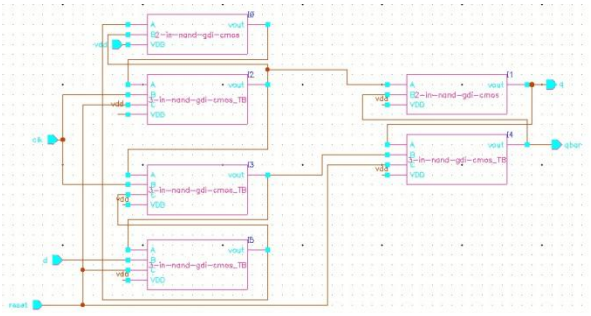

Fig.29 D flip flop using CMOS Technology

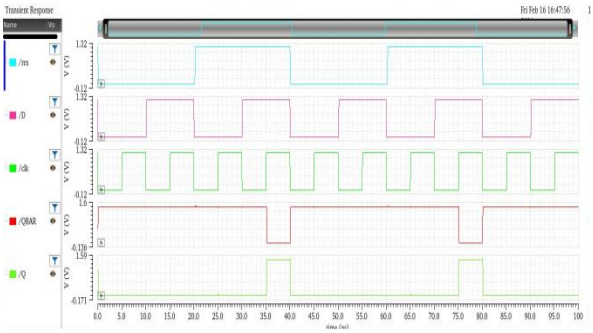

Fig.30 Output of D flip flop using CMOS Technology

The Table 5 illustrates the Average power and delay for existing D Flip Flop with 18nm FinFET transistor and with GDI Technology circuit various input combinations from 0.6V to 1.4V. The D Flip Flop conserves 91.15mW of power and a delay of 16.57ns.Fig.31 illustrates the graphical representation of power and delay analysis of D flip flop.

Table 5 Power and Delay analysis of D Flip Flop

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	143.97	12.52
1.2	121.131	32.57
1	101.64	12.56
0.8	81.17	12.57
0.6	59.95	12.62
AVERAGE	91.15	16.57

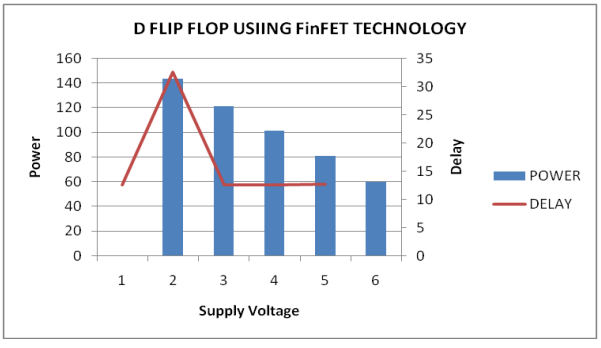

Fig.31 Power and delay of D flip flop using CMOS Technology

4) ADC USING FinFET TECHNOLOGY: The schematic of CSRO-VCO based ADC circuit designed with D Flip Flop and Counters using 18nm FinFET Transistor with GDI Technology. In Figure 32, it uses a supply voltage of 1.2V. Figure 33 displays the simulation outcome employing 18nm FinFET Transistor.

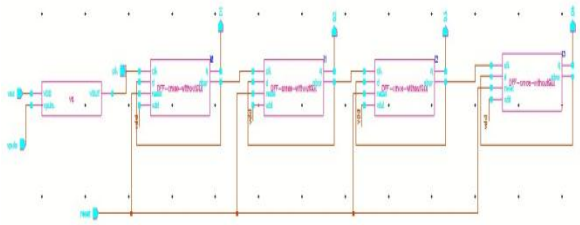

Fig.32 VCO Based ADC using CMOS Technology

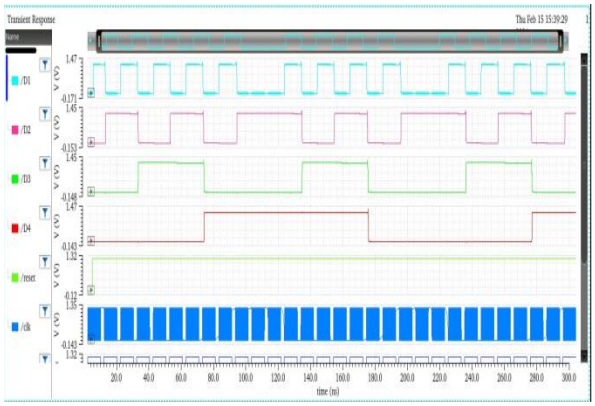

Fig.33 Output of VCO Based ADC using CMOS Technology

The Table 6 illustrates the Average power and delay for proposed CSRO- VCO based ADC with 18nm FinFET Transistor and GDI Technology circuit various input combinations from 0.6V to 1.4V. The CSRO-VCO based ADC conserves 2.3mW of power and a delay of 1.2ns. Fig.34 illustrates the graphical representation of power and delay analysis of VCO based ADC.

Table 6 Average Power and Delay of CSRO-VCO Based ADC Using 18nm FinFET Transistor

SUPPLY VOLTAGE (V)	POWER (mW)	DELAY (ns)
1.4	2.21	1.6
1.2	2.25	1.65
1	2.4	1.94
0.8	2.3	0.65
0.6	2.34	0.2
AVERAGE	2.3	1.20

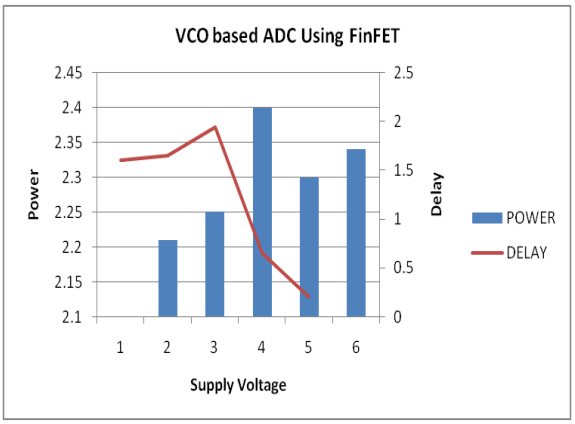

Fig.34 Power and delay of VCO Based ADC using CMOS Technology

C) Discussion: It is observed that CSRO-VCO based ADC designed with 18nm FinFET Transistors using GDI Technique has low power consumption of 2.3mW and less delay of 1.2ns. Comparison of ADC with 90nm CMOS Transistor (with and without GDI) and 18nm FinFET Transistor (with and without GDI) is shown in Table 7.Fig 35 and 36 illustrates the graphical representation of without and with GDI in CMOS and FinFET Technology.

Table 7 Performance Analysis Table of ADC

PERFORMANCE PARAMETERS	90nm CMOS TECHNOLOGY		18nm FinFET TECHNOLOGY	
	WITHOUT GDI	WITH GDI	WITHOUT GDI	WITH GDI
POWER(mW)	442.5	401.0	391.0	356.8
DELAY(ns)	2.8	2.3	1.44	1.208

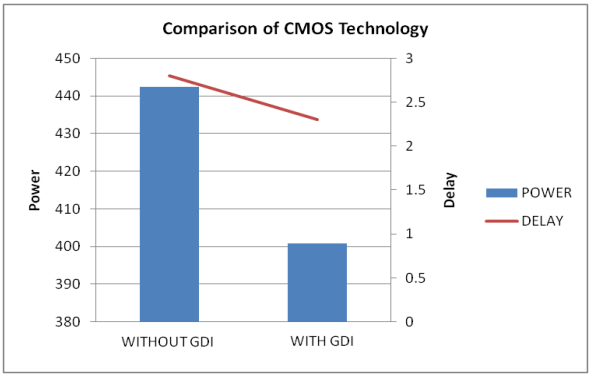

Fig.35 Power and delay of without and with GDI using CMOS Technology

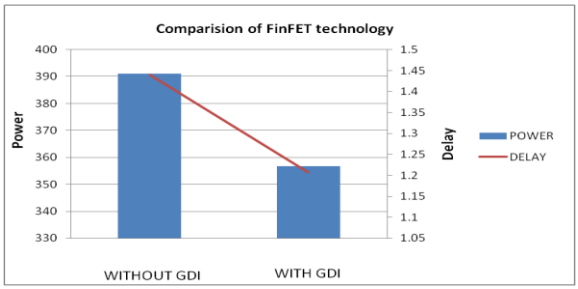

Fig.36 Power and delay of without and with GDI using FinFET Technology

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