Design of Proficient 4 – Tap FIR Filter with Hybrid Full adder and Dadda multiplier using 18nm FinFET Technology

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***Abstract* — The output of a digital filter with Finite Impulse Response (FIR) depends solely on the number of input samples that passed before it. FIR filter is used to equalize audio signals, eliminate noise and carry out other audio processing operations. They are used to sharpen and remove noise in an image. FIR filters are also used in communication to equalize channels and eliminate interference. Reduced power, size and propagation delay makes FinFET more advantageous than CMOS technology. The Gate Diffusion Input (GDI) technique is used to reduce the number of transistors and area thereby increasing the performance of the circuit. The Dadda multiplier reduces the stages of partial products which is equal to the number of bits used to calculate the output. The design of FIR filter using hybrid adders and multiplier in FinFET technology is used in applications where speed and power efficiency is demanded. The proposed method uses a hybrid full adder to generate sum and carry utilizing XOR-XNOR gates and 2X1 MUX. The GDI methodology was used to build the hybrid full adder employing FinFET transistors and it is used in the design of Dadda multiplier. The hybrid full adder, Dadda multiplier and D flip flop is also designed using GDI technique. The delay of the proposed FIR filter is 20.587ns which is 4.3% less than the existing FIR filter at the expense of power consumption. This shows that the 4 – tap proposed FIR filter is ____ faster than the conventional FIR filter.**

Keywords — FIR filter, XOR-XNOR MUX based hybrid full adder, Dadda multiplier, GDI technique, FinFET technology

I.INTRODUCTION

A.HYBRID FULL ADDER

A hybrid full adder is a circuit that produces sum and carry functions using various logic implementation techniques. This can be done to improve the circuit's area, performance or power consumption. In high-performance and low-power applications like microprocessors, digital signal processors and battery-powered devices, hybrid full adders are frequently utilized. Full adders with hybrid technology may use less energy than full adders with conventional technology. Full adders that are hybrids can be made to take up less space than full adders that are conventional. In order to create a common type of hybrid adder ripple-carry and carry-look-ahead adders must be combined. For high-precision calculations, a ripple-carry adder may be slower even though its adder architecture is straightforward and effective. Carry-look-ahead adders have faster adder architecture, but they also require more space and complexity. A hybrid adder, which combines the two designs, may operate at the speed of a carry-look-ahead adder and the effectiveness of a ripple-carry adder. Digital signal processors are another example of high-performance applications that use hybrid adders.

B.DADDA MULTIPLIER

A Dadda multiplier is a sort of digital multiplier that performs multiplication using a tree-structured hierarchy of adders. Dadda multipliers are often faster than other types of multipliers, such as array multipliers and Booth multipliers due to its ability to perform out the multiplication operation in parallel. It is little faster and uses fewer gates than the Wallace multiplier due to a distinctive reduction tree. In the initial stage of the multiplier, the partial products are produced. The tree of adders is then used to reduce the partial products into a group. The final phase of the multiplier produces the actual product. It is frequently employed in high-performance applications like digital signal processors and microprocessors where it consumes small amount of power and is comparatively area-efficient.

C.FinFET TECHNOLOGY

A FinFET is a form of Field-Effect Transistor that is not completely planar but instead has a thin vertical fin. The pathway created between the source and drain is entirely wrapped by the gate on three sides. In comparison to planar FETs, the larger surface area generated between the gate and channel offers better control of the electric state and lower leakage. Compared to planar FETs, FinFETs yields significantly higher electrostatic control of the channel and improved electrical properties. The fin, which serves as the semiconductor channel, has the gate electrode wrapped around each of its three sides. The gate

electrode receives a voltage that creates an electric field that regulates the channel's current flow. FinFETs can function at lower voltages than planar FETs, which lowers their power requirements. FinFET technology has a variety of advantages over bulk CMOS, including scalability of the transistor beyond 28nm, greater speed, reduced leakage, lower power consumption and higher driving current. The two distinct types of FinFET gate structures are shorted gate (SG FinFET) and independent gate (IG FinFET).Fig.1 represents the types of FinFET gate structures.

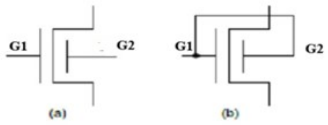


Fig.1 (a) Independent gate FET (b) Shorted gate FET

D.GDI TECHNIQUE

The gate diffusion input technique employs a single basic cell to accomplish a variety of logic operations. The four terminals of the GDI cell are D (common diffusion node), P (input to drain/source of PMOS), N (input to drain/source of NMOS), and G (common gate input) in fig.2. The basic logic gates like AND, OR, NOT, NAND, and NOR as well as higher-level operations like adders, subtractions, and multipliers can all be implemented using the GDI cell. Table 1 illustrates the different function of GDI cell GDI circuits often use less power and are faster and smaller than conventional CMOS circuits. It is an effective technique for designing low-power digital circuits and it is particularly well-suited for applications such as portable devices and battery powered systems.

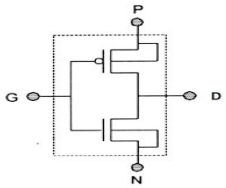


Fig.2 Basic GDI cell

Table 1 Different logic function realization using GDI cell

N	P	G	OUTPUT	FUNCTION
0	B	A	A'B	F1
B	1	B	A'+B	F2
1	B	A	A+B	OR
B	0	A	A.B	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B'	B	A	A'B+AB'	XOR
B	B'	A	AB+A'B'	XNOR

E.FIR FILTER

The FIR filters are employed in digital signal processing, communications systems, image processing, audio processing and many more. It works by combining the incoming signal and multiplying input samples by a corresponding filter coefficient, adding these results and creating a single output sample. The coefficients of the filter define its frequency response. The desired frequency response of the filter is multiplied by a window function in the windowing technique to create the FIR filter. To produce the FIR filter, the frequency sampling method samples the desired frequency response of the filter. Fig.3 shows the 4-tap FIR filter in direct form.

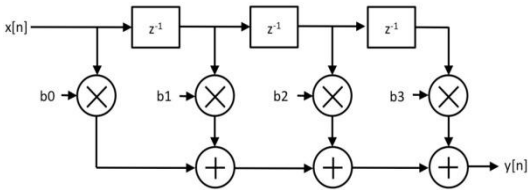


Fig.3 Direct form of 4-tap FIR filter

II. LITERATURE REVIEW

The existing FIR filter has been designed using different types of adders and multipliers. In the conventional methods, the propagation delay and power consumed by the FIR filter circuit are higher compared to those designed with hybrid adders. The below authors have proposed the hybrid adders designed using CMOS technology.

The conventional full adders are designed with 28 transistors. . The proposed adder consists of an XOR-module with two 2:1 multiplexer. The XOR gate is designed with pass transistor logic using the GDI technique [8]. According to experimental findings, power reduction is more effective than traditional adders by 12.99%. The FIR filter was designed utilizing the GDI approach and a Nikhilam multiplier in addition to the standard full adder [10]. The Vedic multiplier, which is used to reduce area and power, is the source of the Nikhilam multiplier. According to the simulation results, the proposed filter offers a 3.2mW reduction in power consumption at 1.2GHz operating frequency.The proposed XOR- XNOR cell uses hybrid logic, which combines CMOS and pass-transistor logic, to achieve high speed and low power consumption. The experimental results showed that the proposed circuit reduced the power delay product by 2% to 28.3% compared to existing full adder designs [4]. The design has five distinct modules, including an XOR-XNOR cell, two multiplexers, a swing-restored transmission gate, and a swing-restored pass transistor with 45nm CMOS logic with multilevel threshold voltages [18]. The suggested approach results in a 92% decrease in power delay product and a 57% reduction in power usage.

The hybrid full adder is constructed using two different modules that each create sum and carry separately. For sum generation in the first module, an XOR cell with transmission gate logic is used. The second module

employs transmission gate logic for carry generation and a 2:1 multiplexer and AND-OR cell. Four AND gates and two half-adders are used in the construction of the 2x2 Vedic multiplier. A hybrid full adder and Vedic multiplier were used in the design of FIR filter [19]. The Dadda algorithm which is a parallel multiplication algorithm reducing the partial products in a minimum number of stages [7]. Implementation of the Dadda multiplier GDI logic reduces the number of transistors which improves the speed and reduces power consumption. The three different types such as 22T, 26T, 26T with buffer are designed hybrid full adder with an XOR-XNOR cell developed using FinFET technology [16]. The proposed hybrid adder is constructed employing an XOR-XNOR Cell. The implementation of hybrid adder has three different modules [5]. The output of the hybrid full adder is created by connecting these three modules together. When compared to the prior way, this causes the propagation latency to be lowered to 36.1 ns and the power usage to 25.8mW. The proposed architecture is scalable to higher frequencies [14]. The proposed full adder cell assumes that a clock signal controls circuit activity since it is based on dynamic rational cognition. The simulation results show that the proposed full adder cell has a propagation delay of 151.75 to 248.25 ps with a supply voltage of 0.3V and a load capacitance of 1.4 to 9.4fF.

The hybrid full adder design that is based on a Gate Diffusion Input (GDI) and conventional complementary metal-oxide semiconductor (CCMOS) logic [15]. A 15T adder uses to combine the Gate Diffusion Input (GDI) logic with FinFET technology. Compared to conventional MOSFET transistors, FinFET technology has a number of benefits, including faster switching and less power consumption [1]. The GDI logic enables the implementation of complex logic operations with a small number of transistors. Wallace multipliers combine the partial products in a sequence, whereas Dadda multipliers combine the partial products in a series form [2]. Using a novel hybrid 3-2 counter, Wallace and Dadda multipliers are produced. FHAS (Hybrid full adder and subtractor) circuit and it employs a hybrid logic design framework to combine the advantages of CMOS and pass-transistor logic [17]. The circuits using transmission gate architectures implement the multiplexer designs that determine whether the circuit has to do addition or subtraction operations. The addition and subtraction operations are implemented using dynamic XOR gates and dynamic XNOR gates [3]. The proposed circuit has been tested and evaluated using the HSPICE tool at the 32 nm CNFET technology.

The existing hybrid adders were developed using CMOS technology and a variety of nanoscale sizes. The CMOS technology consumes more area when compared to the GDI technique and FinFET transistors are used. Mainly conventional full adders and multipliers were used in the designing of the FIR filter. The filter is developed employing CMOS logic and hybrid adders with Vedic multipliers. Dadda multipliers and conventional adders have been used to construct filters. When comparing conventional full adders to hybrid full adders, conventional full adders have more transistors. FinFET technology offers low power consumption and great speed.

III. PROPOSED METHODOLOGY

A.HYBRID FULL ADDER USING FinFET TRANSISTORS

A digital adder that uses XOR-XNOR gates and a multiplexer to accomplish the full adder function is known as a hybrid full adder. This kind of adder is frequently employed in high-performance applications like digital signal processors and microprocessors due to its speed and efficiency. The sum and carry generation in this adder uses sequential steps of XOR-XNOR gates and 2:1 MUX. Fig.4 represents the proposed hybrid full adder using FinFET transistors. The sum and carry expression of the hybrid full adder are given below

$$\text{SUM} = A \oplus B \oplus C_{\text{IN}} \quad (1)$$

$$\text{CARRY} = AB + BC_{\text{IN}} + C_{\text{IN}}\text{A} \quad (2)$$

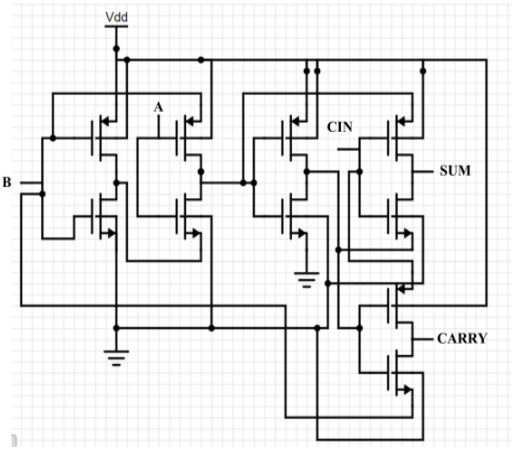


Fig.4 XOR-XNOR MUX based hybrid full adder

B.DADDA MULTIPLIER

The Dadda multiplier is a multiplication algorithm which is used to perform binary multiplication of two numbers, often in digital signal processing (DSP) and other computer applications. It takes two binary numbers X and Y as input for multiplication. These numbers are often represented as bit arrays, with X having n bits and Y having m bits. The partial products must be produced initially. The partial product is generated for each bit in X by multiplying it by each bit in Y. Consequently, the array n x m contains an array of partial products. In Dadda multiplier, a reduction tree is utilized to quickly add the partial products. The reduction tree combines complete adders and compressors to decrease the propagation time and adder stages. The architecture of 4X4 Dadda multiplier is shown in fig.5.

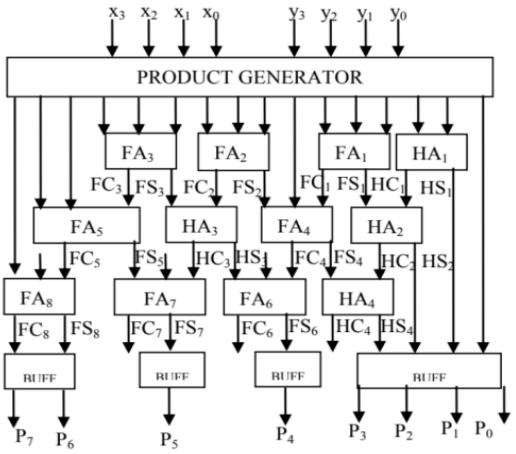


Fig.5 Architecture of 4X4 Dadda multiplier

C.FIR FILTER

A 4-tap FIR filter using hybrid full adder and Dadda multiplier is proposed. A hybrid full adder combines 2x1 MUX with XOR-XNOR module. The hybrid full adder is designed to achieve the balance between speed and area efficiency. A Dadda multiplier is a parallel multiplier that employs tree topology to reduce the number of partial products that must be added. The Dadda multipliers are well-known for their quick speed and simple spatial structures. Fig. 6 represents the block diagram of 4-tap FIR filter. The output of the FIR filter is obtained by adding the products of the Dadda multiplier using hybrid full adder is represented in eq.3.

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k) \qquad (3)$$

Where y (n) = output of the filter

h (k) = filter coefficients

x (n - k) = input samples

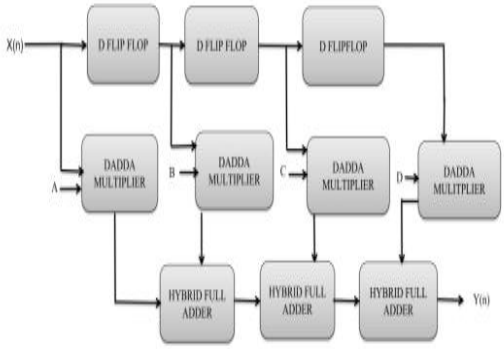


Fig.6 Block diagram of 4-tap FIR filter

IV. RESULTS AND DISCUSSION

A. EXISTING METHOD

1) Hybrid Full Adder using 90nm CMOS Technology: The schematic of hybrid full adder circuit employing GDI technique is shown in fig.7. It uses a supply voltage of 1.8V. Fig.8 displays the simulation outcome of hybrid full adder employing 90nm CMOS with GDI technique.

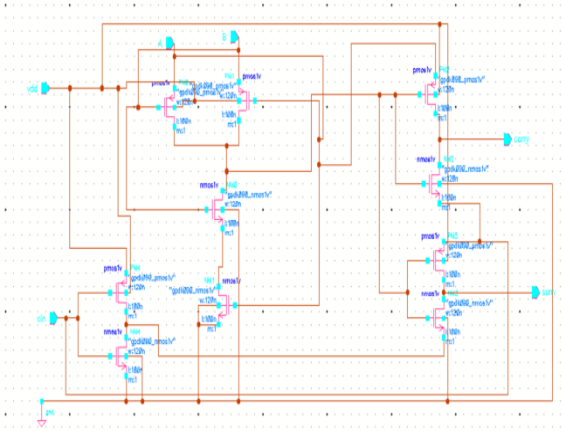


Fig.7 Hybrid full – adder using 90nm CMOS Transistor

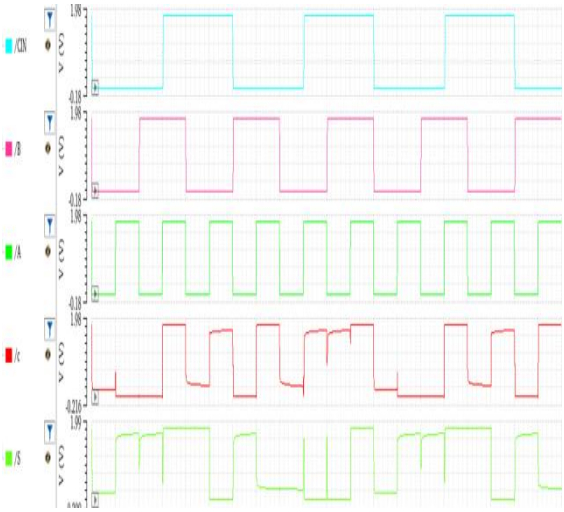


Fig.8 Output waveforms of hybrid full adder

B. PROPOSED METHOD

1) XOR-XNOR MUX based Hybrid Full adder: The schematic of XOR-XNOR MUX based hybrid full adder circuit with GDI technique is shown in fig.9. It uses a supply voltage of 1.8V. Fig.10 displays the simulation outcome of the proposed hybrid full adder with GDI technique employing 18nm FinFET transistors.

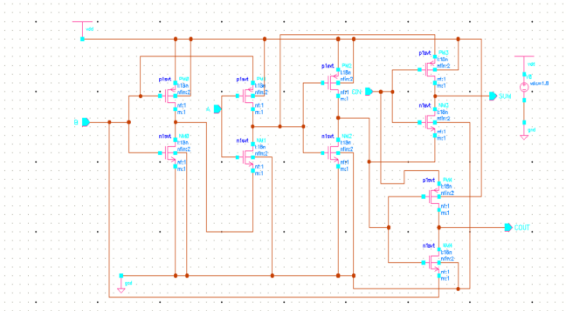


Fig. 9 XOR-XNOR MUX based hybrid full adder

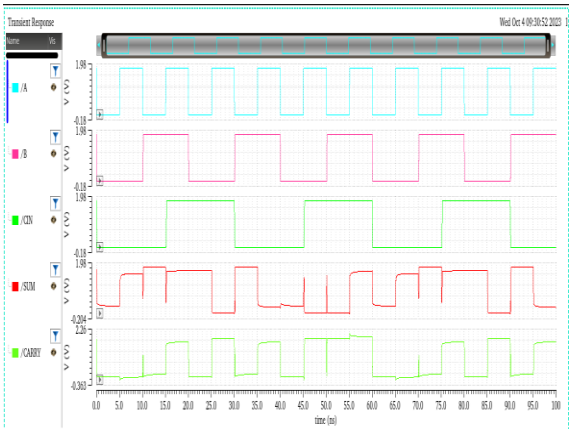


Fig. 10 Output waveforms of proposed hybrid full adder

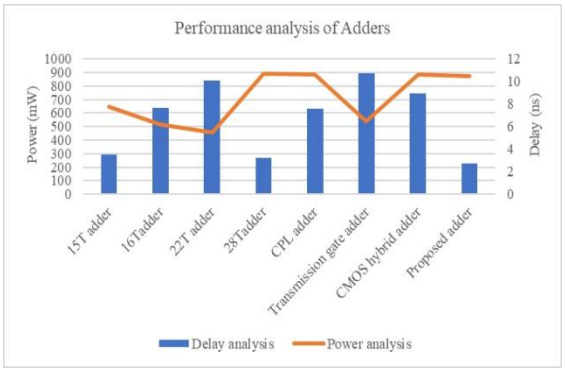
The proposed hybrid adder has a delay of 2.576 ns and it consumes 870.09 mW of power.

Hybrid full adder using 90nm CMOS transistors			Hybrid full adder using 18nm FinFET transistors		
Power	Delay	PDP	Power	Delay	PDP
887.16 mW	8.915 ns	7.909 nJ	870.09 mW	2.576 ns	6.606 nJ

The delay, power consumption, power delay product (PDP) and energy delay product (EDP) of various existing full adders are depicted in table 2.

Table 2 Performance analysis of various adders

Adders	No.of transistors	Power (mW)	Delay (ns)	PDP (nJ)	EDP
15T	15	647.14	3.498	2.264	7.919
16T	16	514.143	7.641	3.928	30.01
22T	22	458.264	10.102	4.629	46.762
28T	28	891.295	3.254	2.900	9.436
CPL	32	884.480	7.603	6.724	51.122
Transmission	20	538.43	10.717	5.766	9.90
adder					
CMOS hybrid full adder	10	887.16	8.915	7.909	70.50
Proposed full adder	10	870.09	2.756	2.397	6.606



2) Dadda Multiplier: The schematic of Dadda multiplier using GDI technique is shown in fig. 11. It uses a supply voltage of 1.8V. Fig.12 displays the simulation outcome of Dadda multiplier using GDI technique employing 18nm FinFET transistors.

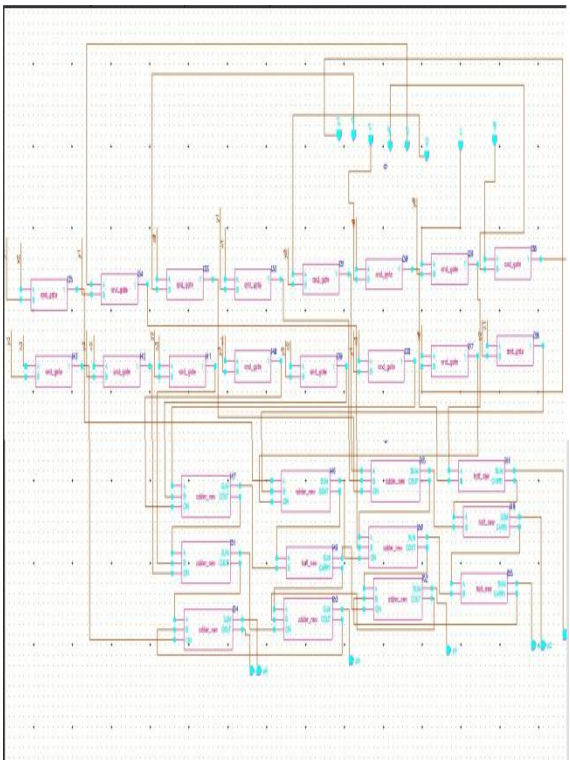


Fig.11 Dadda Multiplier with proposed hybrid full adder

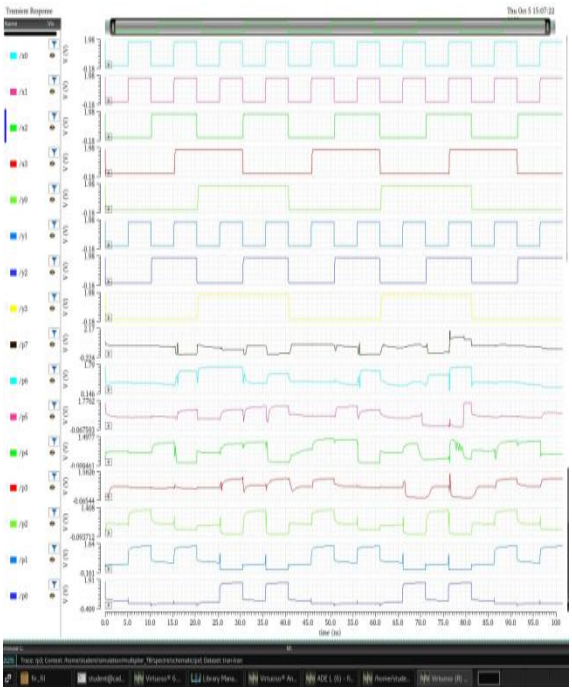
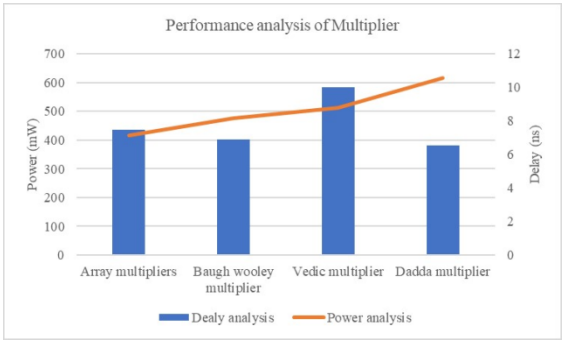


Fig. 12 Output waveforms of Dadda Multiplier using proposed hybrid full adder

The delay, power consumption, power delay product (PDP) and energy delay product (EDP) of various existing full multipliers are depicted in table 3.

Table 3 Performance analysis of various multipliers

Multipliers	No.of transistors	Power (mW)	Delay (ns)	PDP (nJ)	EDP
Array multiplier	280	415.866	7.451	3.098	23.083
Baugh-wooley multiplier	410	474.92	6.907	3.280	22.654
Vedic multiplier	280	512.18	10.006	5.124	51.24
Dadda multiplier	136	615.18	6.532	4.018	26.19



3) FIR Filter: The schematic of 4-tap FIR filter using GDI technique is shown in fig.13. It uses a supply voltage of 1.8V. Fig. 14 displays the simulation outcome of FIR filter employing hybrid full adder and Dadda multiplier using in 18nm FinFET transistors.

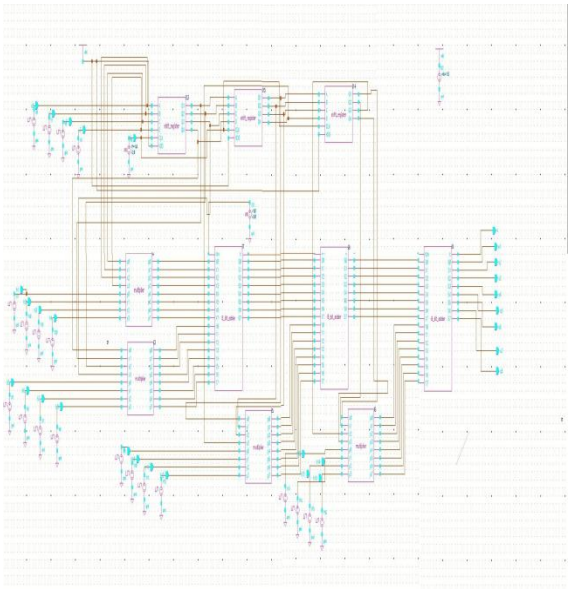


Fig. 13 4-tap FIR Filter using FinFET transistor

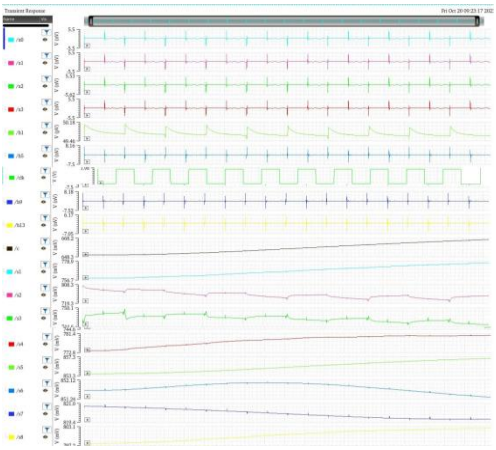
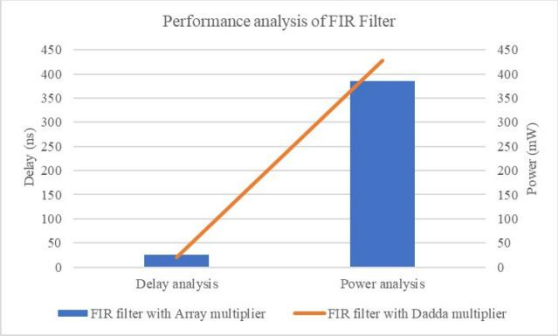


Fig. 14 Output waveforms of proposed 4-tap FIR filter

The delay, power consumption, power delay product (PDP) and energy delay product (EDP) of various existing full filters are depicted in table 4.

Table 4 Performance analysis of various filters

Fliters	No.of Transistors	Power (mW)	Delay (ns)	PDP (nJ)	EDP
Filter with array multiplier	1488	385.034	24.898	9.586	238.67
Filter with dadda multiplier	768	427.142	20.587	8.793	181.02



V CONCLUSION

The FinFET technology has a variety of benefits including improved scalability, less power consumption and higher performance compared to conventional CMOS technology. The GDI approach is a type of architecture that implements several logic operations using only two transistors. It has been demonstrated that the hybrid adders that use Gate Diffusion Input (GDI) approach are particularly successful in lowering propagation delay while maintaining high operating speed. This makes them perfect for usage in a variety of applications including high-performance computing systems, battery-powered gadgets and portable electronics. The proposed GDI hybrid full adder using FinFET technology has low latency and it is power and area efficient than conventional CMOS adders. The proposed Dadda multiplier is also area and power efficient than conventional CMOS multipliers. The propagation delay of proposed hybrid full adder using FinFET technology is 7.57ns which is less compared to CMOS hybrid full adder having a propagation delay of 10.05ns. In a similar line, the propagation delay of proposed dadda multiplier is 12.80ns. It is obvious that the proposed FIR filter achieves high speed than conventional CMOS FIR filters and consumes 427.41mW of power.

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