About Department of Electronics Engineering

Department of Electronics Engineering, established in year 1999, is accredited by National Board of Accreditation (NBA), New Delhi for the period of 3 years from July 2016 and reaccredited on June 2019 for next 3 years. The department has also received permanent affiliation form University from 2017-18. The overall UG intake of the department is 120 students for first year and 60 students for Direct Second Year.

The department has a clear vision to become a center of excellence in the varied domains of Electronics Engineering. It is rich in human resources with expertise in various domains. Well- equipped laboratories to cater domain specific experimentation and research. Electronics Engineering department at VIT has always rendered cumulative efforts to enhance learning by conducting various workshops, Value Added Courses, talks by experts, seminars and short term training programs.

Objectives of STTP:

1. To provide an exposure to current trends and research in the fields of VLSI.
2. To provide hands-on training on advanced industry and research tools

About VIT

Vidyalankar Institute of Technology (VIT) is an 'A+' grade NAAC Accredited Engineering degree college approved by the AICTE, the DTE (Maharashtra), and affiliated to the University of Mumbai. Incepted in the year 1999, the Institute has steadily gained recognition and attracts top talent from across the country.

VIT conducts graduate courses in Electronics Engineering, Electronics and Telecommunication Engineering, Computer Engineering, Information Technology Engineering and Biomedical Engineering with an average annual intake of about 900 students. The Institute also conducts Masters in Engineering programs in Electronics and Telecommunication Engineering, Computer Engineering, and Information Technology Engineering in addition to Masters in Management Studies. Institute also offers doctoral program (Ph.D.) in Computer Engineering.

Our vision is to provide an educational environment based on ethics, discipline and knowledge. Three programs namely Electronics Engineering, Electronics and Telecommunication Engineering and Biomedical Engineering have received NBA accreditation and reaccreditation status. The infrastructure at institute won the Design Share 2007 Award and it proposes an appealing sight which is learning environment friendly. We, at Vidyalankar Institute of Technology, aim to create industry-ready professionals, research scholars and proficient entrepreneurs by infusing the right blend of technological expertise, professional acumen, and social sensitivity in academics and sensitize them towards society.

We encourage innovative thinking and intellectually stimulate them towards technology and research by generating indigenous and appropriate laboratories and activities.

VIT | Vidyalankar Institute of Technology

Accredited A+ by NAAC

Department of Electronics Engineering

in association with

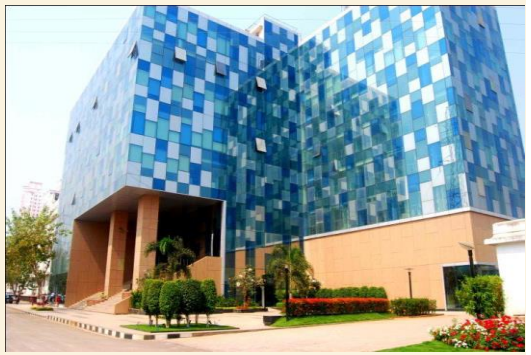
Entuple Technologies

Announces a Two Days Faculty Development Program on

"Cadence Advanced Tools"

November 13 to November 14, 2019

Venue-M201, VIT, Wadala, Mumbai



Workshop Contents:

Day-1:

- Review of the generic amplifier performance Parameters-Gain, Power Dissipation, Frequency Response.
- Synthesis of Basic Amplifier Circuit Topologies
- Basic Amplifier Circuit Topologies: CS, CD and CG
- Large and Small Signal DC performance analysis and design of basic amplifiers
- Lab 1: PDK device characterization for analog model parameters
- Lab 2: Hands-on tutorial on Design and simulation of a CS amplifier for large and small signal DC performance
- Lab 3: Design and simulation of the bias circuit for CS amplifier: Hands-on tutorial
- Lab 4: DC performance characterization of basic CMOS differential amplifier,
- OP-AMP

Day-2:

SEMI CUSTOM DESIGN

- Functional Verification flow using Incisive
- RTL synthesis and basic DFT flow using Genus
- PD flow with innovus that includes
    - Floor planning
    - Power planning
    - Placement
    - CTS
    - Routing
    - Generation of GDS II
- STA with Tempus
- Static and Dynamic power analysis with Voltus
- Logical Equivalence check with conformal
- DFT flow using Modus
- Block implementation flow
- Detail floor planning flow

Schedule:

Duration: November 13 to November 14, 2019
Timings: 10:00 a.m. to 5.00 p.m.

Patrons:
Ms. Rashmi Deshpande (Chair Person, Vidyalankar Dnyanapeeth Trust)
Mr. Vishwas Deshpande (Trustee, Vidyalankar Dnyanapeeth Trust)
Mr. Avinash Chatorikar (Trustee, Vidyalankar Dnyanapeeth Trust)
Mr. Milind Tadwalkar (Director, Vidyalankar Dnyanapeeth Trust)
Dr. S. A. Patekar (Principal, Vidyalankar Institute of Technology)
Prof. Varsha Bhosale (Vice Principal, Vidyalankar Institute of Technology)

Convener:
Dr. Sangeeta Joshi

Co-Convener:
Mr. Sunil Kavatkar

Organized by:

Vidyalankar Institute of Technology
Vidyalankar College Marg,
Wadala (E), Mumbai- 400 037
Telefax: +91 22 24161126
Web: www.vit.edu.in

For Registration and Queries:

Contact-
Mr. Sunil Kavatkar-
9960182054 – sunil.kavatkar@vit.edu.in

Registration Form

Name_____

Designation: _____

Department :_____

Qualification:_____

Contact Number:_____

E-Mail:_____

Date: _____

Place: _____

_____
Signature of Applicant

Note: There is no registration fee for the participants