a complete overview of all **20 AHB protocol test cases** spanning functional, negative, and stress scenarios—organized into categories for clarity:

**🧪 AHB Protocol Verification Test Matrix**

| **Category** | **Test ID** | **Scenario** | **Status** | **Test Class Name** |
| --- | --- | --- | --- | --- |
| **Transfer Type Errors** | T1 | Use undefined/reserved HTRANS (e.g., BUSY) | ✅ | ahb\_test\_illegal\_trans |
|  | T2 | Burst with HTRANS = IDLE throughout (invalid sequence) | ✅ | ahb\_test\_idle\_burst |
| **Size & Alignment Violations** | T3 | Misaligned address for given transfer size | ✅ | ahb\_test\_misaligned\_addr |
|  | T4 | HSIZE larger than data bus width | ✅ | ahb\_test\_oversize\_transfer |
| **Address Errors** | T5 | Wrap burst with incorrect boundary alignment | ✅ | ahb\_test\_wrap\_misalign |
|  | T6 | INCR burst crossing 1KB boundary without proper wrap | ✅ | ahb\_test\_incr\_cross\_1kb |
| **Master Protocol Violations** | T7 | HREADY = 0 permanently (bus stall) | ✅ | ahb\_test\_hready\_stall |
|  | T8 | Change HBURST mid-burst without abort | ✅ | ahb\_test\_burst\_switch |
| **Slave Protocol Violations** | T9 | Invalid HRESP value | ✅ | ahb\_test\_bad\_hresp |
|  | T10 | Slave asserts HREADY = 0 but completes transfer | ✅ | ahb\_test\_hready\_misuse |
| **Invalid Signal Usage** | T11 | HWRITE = X during active transaction | ✅ | ahb\_test\_x\_write |
|  | T12 | Toggle HSEL while HTRANS != IDLE | ✅ | ahb\_test\_hsel\_toggle |
| **Split/Retry Behavior** | T13 | Slave issues SPLIT but never re-arbitrates | ✅ | ahb\_test\_split\_stall |
|  | T14 | RETRY issued continuously, no successful transfer | ✅ | ahb\_test\_retry\_loop |
| **Arbitration & Contention** | T15 | Multiple masters drive bus simultaneously | ✅ | ahb\_test\_contention |
|  | T16 | Master locks bus indefinitely | ✅ | ahb\_test\_lock\_hold |
| **Clock/Reset Issues** | T17 | Perform transfer during reset assertion | ✅ | ahb\_test\_active\_during\_reset |
|  | T18 | Glitch in HCLK during active transaction | ✅ | ahb\_test\_clock\_glitch |
| **Illegal Configurations** | T19 | Reserved HBURST = 3'b101 used | ✅ | ahb\_test\_reserved\_hburst |
|  | T20 | All control signals undefined/‘X’ during transfer | ✅ | ahb\_test\_undefined\_ctrl |

Each test is isolated, reproducible, and driven via a corresponding UVM sequence.