**Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity shiftregister is

Port ( clk : in STD\_LOGIC;

reset : in STD\_LOGIC;

datain : in STD\_LOGIC\_VECTOR (3 downto 0);

sel : in STD\_LOGIC\_VECTOR (1 downto 0);

sl\_in : in STD\_LOGIC;

sr\_in : in STD\_LOGIC;

dataout : out STD\_LOGIC\_VECTOR (3 downto 0));

end shiftregister;

architecture Behavioral of shiftregister is

begin

process(reset, clk, sel, sl\_in, sr\_in, datain)

variable TEMP : STD\_LOGIC\_VECTOR (3 downto 0);

begin

if reset = '1' then

TEMP := "0000";

elsif clk'event and clk = '1' then

case Sel is

when "11" => TEMP := datain;

when "01" => TEMP := TEMP(2 downto 0) & sl\_in;

when "10" => TEMP := sr\_in & TEMP(3 downto 1);

when others => NULL;

end case;

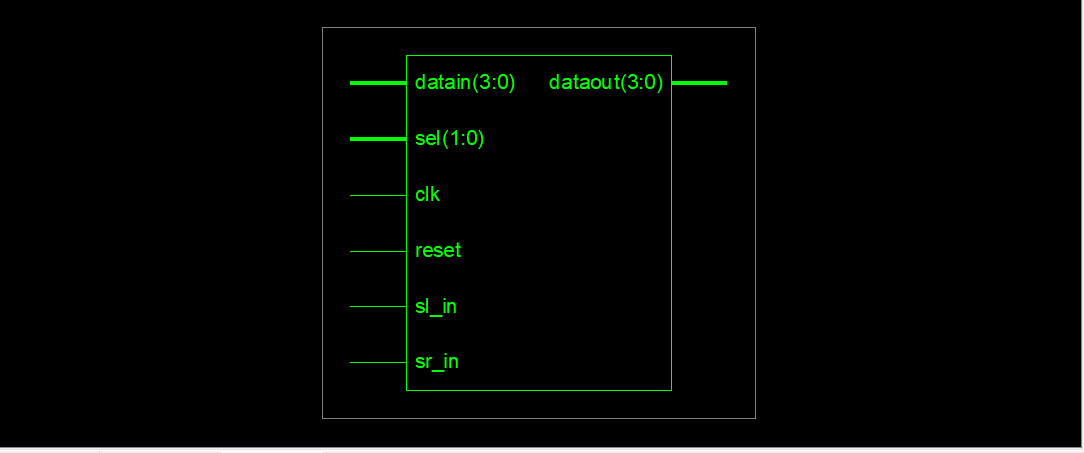
end if;

dataout <= TEMP;

end process;

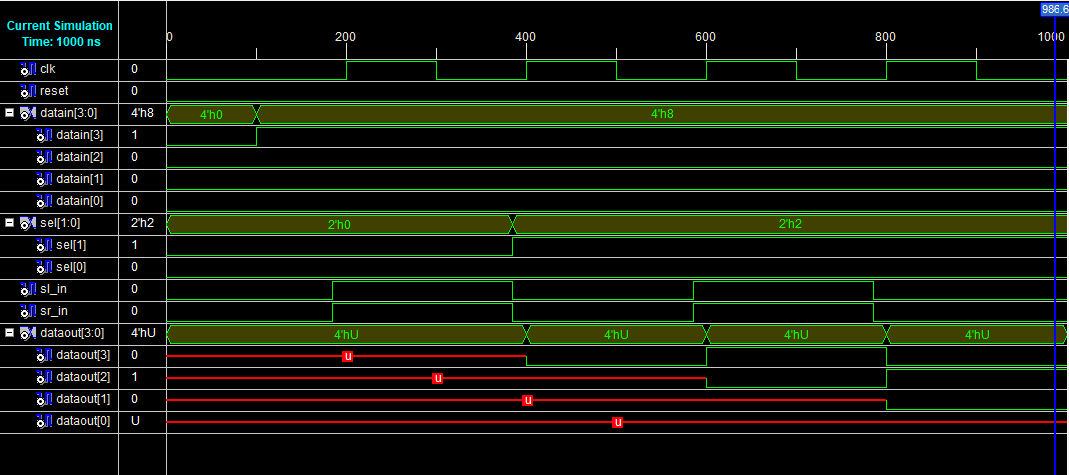
end Behavioral;

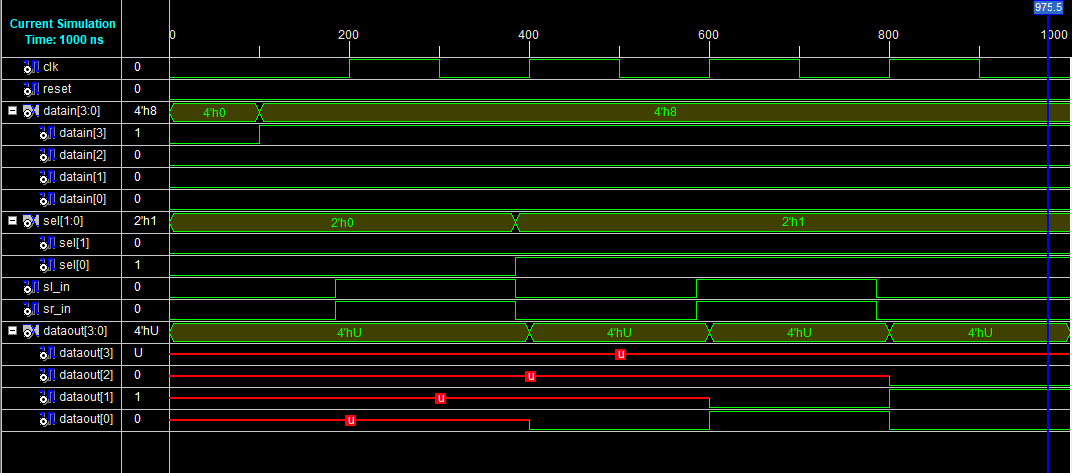
**RTL Diagram :**

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**Output :**

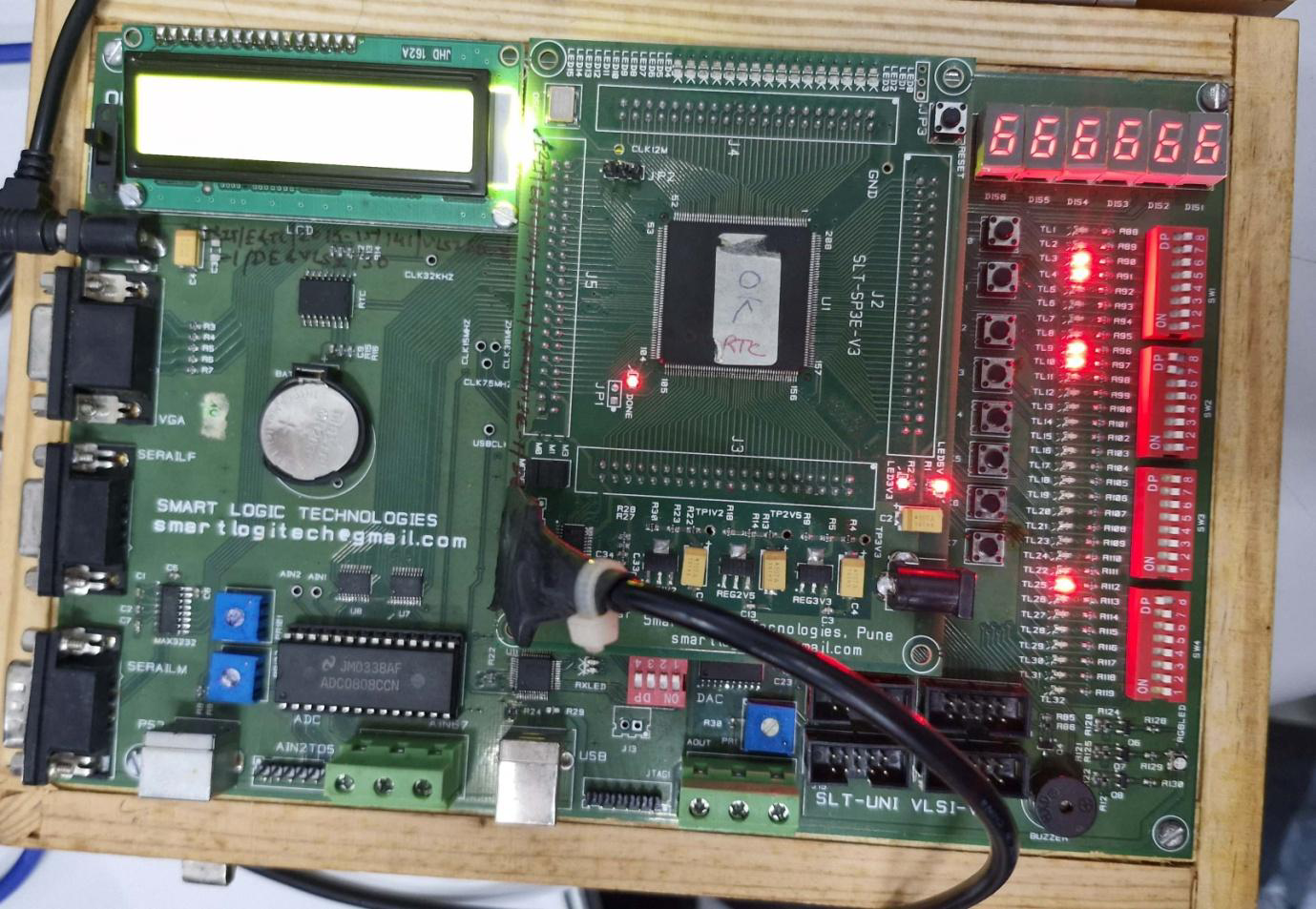
Left Shift :

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Right Shift :



**Hardware Output :**



**Pin Assignment :**

| **Sr. No.** | **Signal Name** | **Pin Designation** | **Direction** | **FPGA Pin No.** |
| --- | --- | --- | --- | --- |
| 1 | clk | Clock 555: 1Hz | Input | P132 |
| 2 | reset | Key0 | Input | P204 |
| 3 | dataout[0] | TL1 | Output | P205 |
| 4 | dataout[0] | TL2 | Output | P206 |
| 5 | dataout[0] | TL3 | Output | P203 |
| 6 | dataout[0] | TL4 | Output | P200 |
| 7 | datain[0] | TL9 | Input | P192 |
| 8 | datain[1] | TL10 | Input | P193 |
| 9 | datain[2] | TL11 | Input | P189 |
| 10 | datain[3] | TL12 | Input | P190 |
| 11 | SL\_in | TL17 | Input | P179 |
| 12 | SR\_in | TL18 | Input | P180 |
| 13 | sel[0] | TL25 | Input | P165 |
| 14 | sel[1] | TL26 | Input | P167 |