

Sangjae Park

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Seoul, Korea

SUMMARY

RTL Engineer at Anapass Inc, Seoul Korea, specialize in OLED TCON ASIC chip. Skilled in RTL design and backed by a academic record in DRAM micro-architecture. Dedicated to robust and efficient hardware through innovative solutions.

Research Interest: Computer Architecture, Memory Architecture, HW/SW Co-design, ASIC Chip Design


EDUCATION

- **Sungkyunkwan University** Jan 2021 - Jan 2023
M.S. in Electrical and Computer Engineering Suwon, Korea
 - Thesis: On-Die Dynamic Remapping Cache: Strong and Independent Protection Against Intermittent Faults (Advisor: Prof. Jungrae Kim)
 - GPA: 4.44/4.5(\approx 4.0/4.0)
- **Sungkyunkwan University** March 2017 - Jan 2021
B.S in Electrical and Electronic Engineering Suwon, Korea
 - GPA: 3.75/4.5(\approx 3.53/4.0), Major: 4.03/4.5(\approx 3.73/4.0)

EXPERIENCE

- **Anapass Inc** Jan 2023 - Current
SoC RTL Enginner @R&D Center Seoul, Korea
 - Served in this position as an alternative to the **mandatory military duty** required of all Korean males.
 - Products: OLED TCON/TED (sold to Samsung Display)
 - My primary responsibilities centered on DFT, DSC codec, and Gate Pulse I/O, while also requiring deep understanding of high-speed interfaces like eDP and IP integration due to their close inter-dependencies.
 - Played a key role resolving yield loss issues via post-silicon debugging, working closely with manufacturing teams.

PROJECTS

- **Anapass: Design Custom ASIC for Display Driver Controller** Jan 2023 - Current
Tools: Tessent-MemBIST, verdi, xcelium
 - Develop display controller IC regarding Notebook, Tablet, and automotive.
 - As RTL Engineer, integrate multiple IPs and design RTL blocks.
- **SKKU: Development of intelligent in-memory error correction devices for high reliability memory** Apr 2021 - Jan 2023
Skill: C++11 [\[github\]](#) 
 - Developed smart error correction algorithms tailored for eDRAM-based in-memory computing.
 - Actively collaborated with the FPGA-team to explore commercial DRAM vulnerabilities, as well as supporting the RTL team for rigorous verification
 - Funded by Institute for ICT Planning & evaluation (IITP, 2021-0-00863)

PATENTS AND PUBLICATIONS

- [Journal] Yuseok Song, Sangjae Park, Michael B. Sullivan and Jungrae Kim. SEC-BADAE: An Efficient ECC With No Vacancy for Strong Memory Protection. In *IEEE Access*, Vol.10, 2022. [\[Paper\]](#) [\[NVIDIA Research\]](#)
- [Journal] Sangjae Park and Jungrae Kim. On-Die Dynamic Remapping Cache: Strong and Independent Protection Against Intermittent Faults. In *IEEE Access*, Vol.10, 2022. [\[Paper\]](#)
- [Patent] Jungrae Kim and Sangjae Park. Apparatus and method for remppaing of memory. Patent No.KR1020210096297A. [\[Patent\]](#)

OPEN-SOURCE CONTRIBUTION

- **gem5-Ramulator2**

language: C++, Python

Dec 2023

[[github](#) 

- Provides an environment for integrating gem5 with Ramulator2.
- While integrating the two simulators, I discovered and addressed several bugs and improvements, contributing to both the gem5 and Ramulator2 official repositories.

- **Parallel-Task-Harbor**

language: Python

Feb 2025

[[github](#) 

- Python-based parallel task automation script designed to simplify the simulation of hundreds or thousands of different tasks simultaneously.

SKILLS

- **Programming Languages:** C++11, python
- **Hardware Language/Tool:** System-Verilog, Tessent-MemBIST, xcelium
- **Framework/Simulator:** gem5, pytorch

HONORS AND AWARDS

- **Graduate Merit Scholarship (A half-tuition for 2-year)**

2021 - 2022

Sungkyunkwan University

- **Dean's LIST**

Nov 2020

Sungkyunkwan University

- **Student Success Scholarship (Full-tuition for 1-year)**

March 2020

Sungkyunkwan University