fstaH N7A update on 2024.06.18

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Update Items

- N7A DRC Signoff Checking Flow
- Usage of Aging Timing Analysis
- Option of Keeping Unconnected Cells
- N7A Hold Uncertainty Update

N7A DRC Signoff Checking Flow

- **fstaH support TSMC N7A DRC signoff rule. There will be three additional checking flow on the clock tree:**

1. **N7A Only allow LVT and ULVT type cells on the clock tree**
   fstaH will report an error if finding any SVT/HVT cells on it.

```
** Error(fstaDRC-16): According to the DRC criteria of N7A, there are Vt type violations in the clock tree, please check the "drc_clkTreeCellLowVt.rpt" for detailed information.
```

Check it in drc_clkTreeCellLowVT.rpt

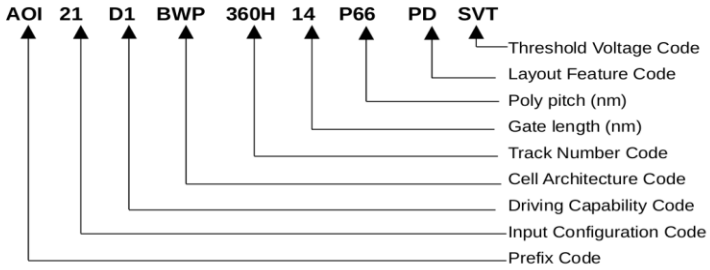
```
*** Clock_Tree: pclk, Clock_Name: clk_cfg_bus_out_vpu
        Library: tcbn07_bwph240l11p57pd_baseat_svtssgnp_0p675v_m40c_cworst_CCworst_T_ccs, Vt type: SVT, Instance List: (Count: 1)
                (MUX2D1BWP240H11P57PDSVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/tessent_persistent_cell_SH
IFT_REG_CLK_mux
================================================================================================================================================

*** Clock_Tree: aclk, Clock_Name: clk_vcd_aclk_out_vpu
        Library: tcbn07_bwph240l11p57pd_baseat_svtssgnp_0p675v_m40c_cworst_CCworst_T_ccs, Vt type: SVT, Instance List: (Count: 1)
                (MUX2D1BWP240H11P57PDSVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_aclk_750m_inst/occ_control/tessent_persistent_cell_SH
IFT_REG_CLK_mux
================================================================================================================================================

*** Clock_Tree: coreclk, Clock_Name: clk_vcd_coreclk_out_vpu
        Library: tcbn07_bwph240l11p57pd_baseat_svtssgnp_0p675v_m40c_cworst_CCworst_T_ccs, Vt type: SVT, Instance List: (Count: 56)
                (MUX2D1BWP240H11P57PDSVT) u_vc9000d_subsys/u_part2/u_part2_sram_wrapper/u_rams/u_p2_g2_prefetch_cache_ram/u_ram/rf_sp_960x128_u_me
```

N7A DRC Signoff Checking Flow

- **fstaH support TSMC N7A DRC signoff rule. There will be three additional checking flow on the clock tree:**

2. Restriction of cell's driving capability.

- In TSMC libraries, the keyword D0~DXX represents Driving Capability
- Only allow the cells >= D2 size on the clock tree.



** Error(fstaDRC-17): According to the DRC criteria of N7A, there are driving capability violations in the clock tree, please check the "drc_clkTreeCellDC.rpt" for detailed information.

Check it in drc_clkTreeCellDC.rpt

```
*** Clock_Tree: pclk, Clock_Name: clk_cfg_bus_out_vpu
   DrivingCapability                    Reference                    Instance
=============================================================================================================================================

                  D1        MUX2D1BWP240H11P57PDSVT u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/tessent_persiste
nt_cell_SHIFT_REG_CLK_mux


*** Clock_Tree: aclk, Clock_Name: clk_vcd_aclk_out_vpu
   DrivingCapability                    Reference                    Instance
=============================================================================================================================================

                  D1        MUX2D1BWP240H11P57PDSVT u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_aclk_750m_inst/occ_control/tessent_persiste
nt_cell_SHIFT_REG_CLK_mux
```

N7A DRC Signoff Checking Flow

- **fstaH support TSMC N7A DRC signoff rule. There will be three additional checking flow on the clock tree:**

3. **N7A Only allow Single Gate Length on the clock tree**
   fstaH will report an error if finding any gate length mismatched on the same path.

```
** Error(fstaDRC-15): There are multiple Gate Length cells specified in the clock tree, please check the
"drc_clkTreeCellGl.rpt" for detailed information.
```

Check it in drc_clkTreeCellGl.rpt

```
*** Clock_Tree: pclk, Clock_Name: clk_cfg_bus_out_vpu
      Library: tcbn07_bwph240l11p57pd_baseat_svtssgnp_0p675v_125c_cworst_CCworst_T_ccs, Gate Length: 11, Instance List: (Count: 1)
            (MUX2D1BWP240H11P57PDSVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/tessent_persistent_cell_SHIFT_REG_CLK_mux
      Library: tcbn07_bwph240l11p57pd_baseat_ulvtssgnp_0p675v_125c_cworst_CCworst_T_ccs, Gate Length: 11, Instance List: (Count: 8)
            (CKLNQD8BWP240H11P57PDULVT) u_vc9000d_subsys/u_part0/u_part0_subip/u_cmd/u_slave_apb/clk_gate_slave_wdata_reg_1_latch
            (CKLNQD10BWP240H11P57PDULVT) u_vc9000d_subsys/u_part0/u_part0_subip/u_cmd/u_slave_async/clk_gate_slave_rdata_reg_0_latch
            (CKLNQD8BWP240H11P57PDULVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/tessent_persistent_cell_cgc_fast_clock
            (CKBD8BWP240H11P57PDULVT) u_vcd_wrap_occ_wrapper/u_mmt_dft_OCC_pclk_FREQ_250M_post/u_mmt_clk_buf/d0nt_clk_buf
            (CKLNQD8BWP240H11P57PDULVT) u_vc9000d_subsys/u_part0/u_part0_subip/u_cmd/u_slave_apb/clk_gate_PRDATA_reg_0_latch_clone
            (CKLNQD8BWP240H11P57PDULVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/tessent_persistent_cell_cgc_SHIFT_REG_CLK
            (CKLNQD8BWP240H11P57PDULVT) u_vc9000d_subsys/u_part0/u_part0_subip/u_cmd/u_slave_apb/clk_gate_PRDATA_reg_0_latch_clone_1
            (CKLNQD8BWP240H11P57PDULVT) u_vc9000d_subsys/u_part0/u_part0_subip/u_cmd/u_slave_apb/clk_gate_slave_wdata_reg_0_latch
      Library: tcbn07_bwph240l8p57pd_baseat_lvtssgnp_0p675v_125c_cworst_CCworst_T_ccs, Gate Length: 8, Instance List: (Count: 2)
            (BUFFD8BWP240H8P57PDLVT) pclk_11716364528_N7BUF
            (MUX2D4BWP240H8P57PDLVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/tessent_persistent_cell_clock_out_mux
      Library: tcbn07_bwph240l8p57pd_baseat_ulvtssgnp_0p675v_125c_cworst_CCworst_T_ccs, Gate Length: 8, Instance List: (Count: 11)
            (DCCKND4BWP240H8P57PDULVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/CTS_ccl_inv_03435
            (DCCKBD4BWP240H8P57PDULVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/tessent_persistent_cell_fast_clock_buf
            (DCCKND4BWP240H8P57PDULVT) u_vcd_wrap_occ_wrapper/vcd_wrap_psw_lb_tessent_occ_pclk_250m_inst/occ_control/CTS_ccd_inv_03684
```

N7A DRC Signoff Checking Flow

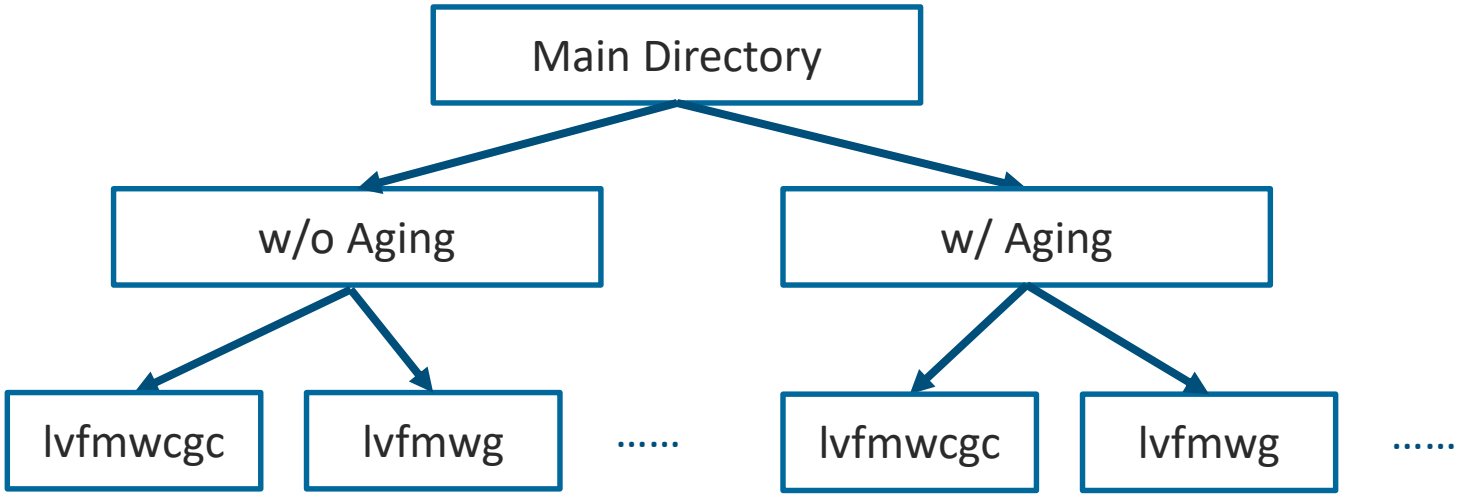
- In Faraday's non-CK type flow, we won't report a non-CK cell in the drc_nonClkCell.rpt if we can't find the CK version of the cell.
- fstaH will report the all non-CK type cells **even the cell has no any CK version**.

```
Clock Root: clk_csr_i, Clock_Name: clk_cfgbus_out_hsif
================================================================================================================================================
MUX2D4BWP240H8P57PDLVT u_blk_xgmac_wrap_occ_wrapper/blk_xgmac_wrap_lb_tessent_occ_clk_csr_i_250m_inst/tessent_persistent_cell_clock_out_mux
MUX2D1BWP240H11P57PDSVT u_blk_xgmac_wrap_occ_wrapper/blk_xgmac_wrap_lb_tessent_occ_clk_csr_i_250m_inst/occ_control/tessent_persistent_cell_SHIFT_REG_CLK_mux
BUFFD8BWP240H8P57PDLVT clk_csr_i_I1716288403_N7BUF
```

There's no "ckbuffd1" footprint in the library

Usage of Aging Timing Analysis

- **Hangtu project requires aging effect as timing signoff criteria.**
- **To avoid confusion, please divide the folder into non-aging libs and aging libs to run fstaH.**



- **For Setup timing check, just change the libraries to aging libs.**
  - For example:

tcbn07_bwph240l8p57pd_baseat_lvtssgnp_0p675v_m40c_cworst_CCworst_T_hm_lvf_p_ccs.db

↓

tcbn07_bwph240l8p57pd_baseat_lvtssgnp_0p675v_m40c_cworst_CCworst_T_hm_lvf_p_ccs.agedb

Usage of Aging Timing Analysis

- **For Hold timing check:**
  - Change to aging libs.
  - Put the all *_aging.pt to your directory specified in STA_MARGIN_POCV_DIR (aging file reference : **/auto/t_ASICQA2024/ada/proj/FXW1AA001A/FE/0_Initial/bakAC/POCVM_AGING/***)
  - Add two options in setup.ftc.fsta:
    STA_USERSPECIFIED_SPECIAL_DERATE_FROM_PROJ_BASED_SETUP = Signoff_derate_7_setup_aging.tcl
    STA_USERSPECIFIED_SPECIAL_DERATE_FROM_PROJ_BASED_HOLD = Signoff_derate_7_hold_aging.tcl
  - Please be aware of any Error meesage **fstaAging-005** in the log.

```
** Error(fstaAging-005): /home/t_FXW1AA001A_FE/kc_test/sta/flow/aging/out_pt/tcbn07_
bwph240l8p57pd_mbat_svtssgnp_0p675v_m40c_cworst_CCworst_T_aging.pt doesn't exist.
```

Option of Keeping Unconnected Cells

- Add an option of keeping unconnected cells in Primetime.
  STA_KEEP_UNCONNECTED_CELLS = ON
- There is a variable be added in the script:

```
set link_keep_unconnected_cells true
```

N7A Hold Uncertainty Update

- The hold uncertainty of N7A is changed from 0ps to 5ps.

```
set_propagated_clock [all_clocks]
set_clock_uncertainty -hold 0.005 [all_clocks]
set_noise_parameters -enable_propagation -analys
```

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