

fstaH usage

Ming/DMD.LDF

2019

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Outline

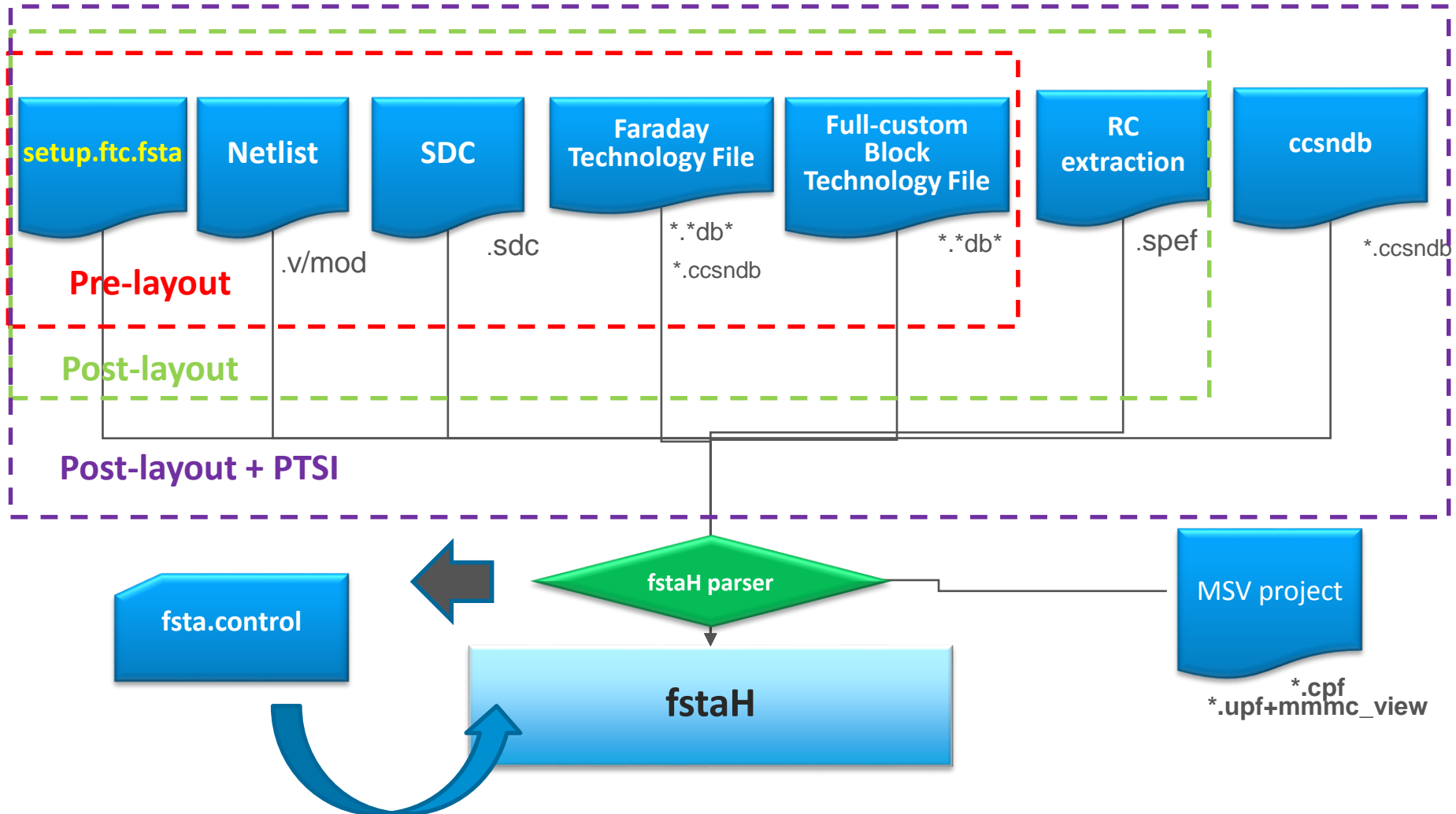
- fstaH introduction
- fstaH option
- fstaH scenario
- setup.ftc.fsta



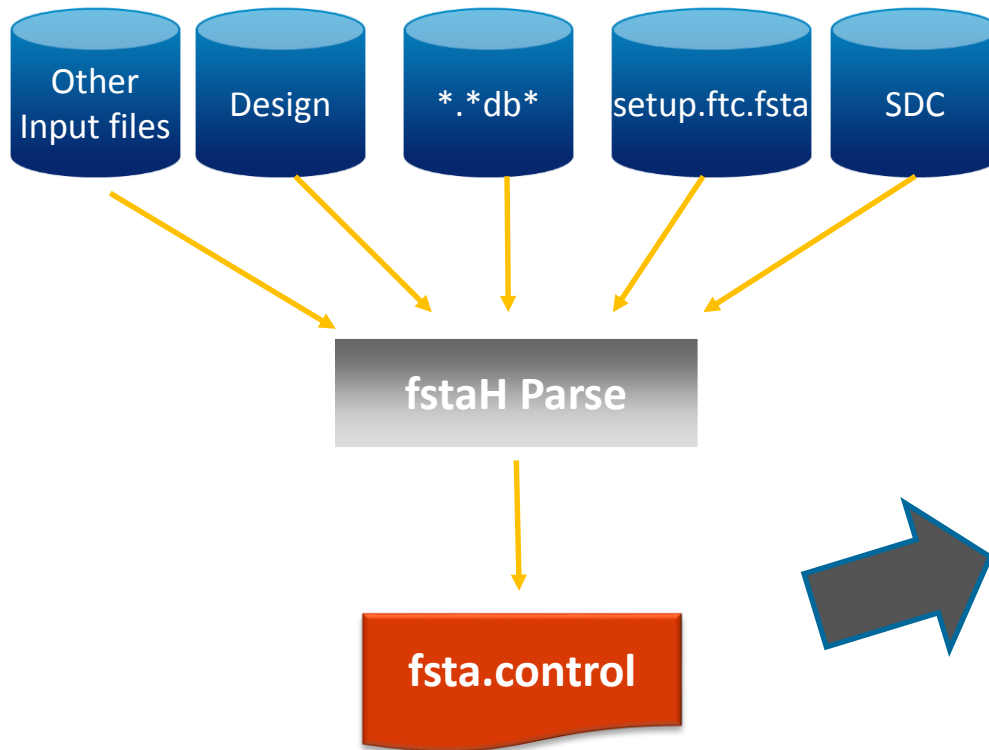
fstaH introduction



Basic Setting - Input Files



Basic Setting - “fsta.control”



Check your input files setting
for each scenario

NETLIST = FZOTG266HF0F.v
TOP = FZOTG266HF0F

[CORNER_BEGIN]

STA_TIMING_LIB = tt1p2v125c_typ

SDC = FZOTG266HF0F.sdc

CORE_LIB = fsf0f_ehs_core_tt1p2v125c.ccdB

MACRO_LIB = FZOTG266HF0F_A_TT1P2V125C.db

ETM_LIB =

SPEF_TOP = FZOTG266HF0F_typ125c.spef.gz

SPEF_BLOCKS =

INCR_SDF_TOP =

SDF =

[CORNER_END]



Basic Setting - Output Files

fstaH



fsta_script



fsta.log

out.log

cksum.log

ErrorMessage.log

setuptime_derating log

holdtime_derating.log

Log file

Design.rpt

CheckTiming.rpt

Constraint.rpt

SetupChk.rpt
CkGatingSetup.rpt

Removal.rpt

HoldChk.rpt
CkGatingHold.rpt

PulseWidth.rpt

Annotated.rpt

Coverage.rpt

Recovery.rpt

Margin.rpt

skew.rpt

dutycycle.rpt

General timing reports

glitch.rpt

big_incr_delay.rpt

ptsi_debug.log

ptsi

sdf

setup/
hold_to_tweaker

Setup/hold.twf

tweaker

settrans

setload

CKC

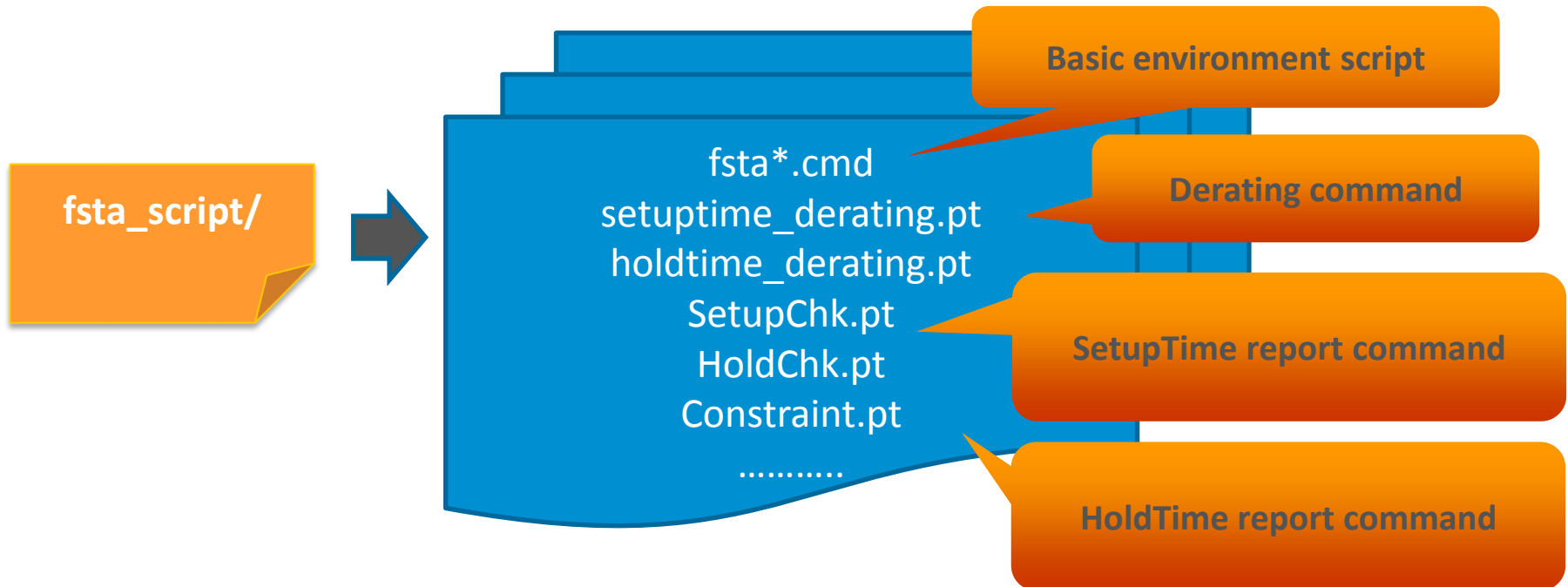
Case

fdrc

sdc-driven
fdrc

Basic Setting - fsta_script

- fstaH will output execution scripts in *rpts/fsta_script folder





fstaH option



timing check option

- **fstaH -help : Show help message**
- **Syntax:**
 - General Syntax : `fstaH -group <sdh_id> <mode 1> <mode 2> <mode ...> [-ip/-nonip] [-ptsi] [-glitch] [-gen_aocv_index] [-chk_aocv_index]`
 - CPF-In Flow Syntax: `fstaH -msv <cpf_file_name> <mode 1> <mode ...> [-ip/-nonip] [-ptsi] [-glitch] [-gen_aocv_index] [-chk_aocv_index]`
- **Option:**
 - `[-ip/-nonip]` : Specify design will be used for other design (-ip) or not (-nonip)
 - `[-ptsi]` : Enable Primetime-SI analysis and generate glitch report ("Notice [-ptsi] should using with [-ip/-nonip]")
 - `[-glitch]` : Only glitch report ("Notice [-glitch] can mix with [-ptsi]")
 - `[-gen_aocv_index]` : fstaH only generates aocv table index and aocv table for each scenario in folder `\${DESIGN}_AOCV`
 - `[-chk_aocv_index]` : fstaH only verify aocv table index and aocv table for each scenario in folder `\${DESIGN}_AOCV`

AOCV flow

- AOCV mode needs to generate aocv table index at first
 - %> fstaH -group \$SDC aocvwg -gen_aocv_index
 - %> fstaH -msv \$project aocv -gen_aocv_index

```
=====
** Information(fstaMsg-2): Generating AOCV Table Index: "RDN1_rdn_domain_wrapper.aocv_index"
=====
Finish fsta_ux.tcl main_flow : Fri Jul 01 03:41:06 PM CST 2016
```

- %> fstaH -group \$SDC aocvwg -ptsi [-nonip|-ip]
- %> fstaH -msv \$project aocv -ptsi [-nonip|-ip]

```
=====
** Information(fstaMsg-1): Summary for FSJ0FS060A AOCVWG_RCMAX125C_PTSI_setup_rpts
** Information(fstaMsg-1): Report Design.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report Annotated.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report Constraint.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report SetupChk.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report SetupChk_reg2reg.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report SetupChk_in2reg.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report SetupChk_reg2out.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report CkGatingSetup.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report Coverage.rpt has 0 warnings and 0 violations.
** Information(fstaMsg-1): Report CheckTiming.rpt has 5 warnings and 0 violations.
** Information(fstaMsg-1): Report sta2xml.rpt has 0 warnings and 0 violations.
Finish fsta_ux.tcl main_flow : Fri Jul 01 04:23:56 PM CST 2016
Program ends normally.
```

ac_scan false path generation

- **Please follow STA sign-off criteria**
- **For process $\geq 40\text{nm}$:**
 - (non-CPF-in)
 - `fstaH -gen_ac_scan_constraint <proj>_TDF <mode1> <mode2> ... [-ptsi] [-ip/-nonip]`
 - `<mode>` : n / b / w / wcc / ocvw / ocvwcc
 - (CPF-in)
 - `fstaH -gen_ac_scan_cpf_constraint <cpf_file_name> <mode 1> <mode 2> ...[-ptsi] [-ip/-nonip]`
 - `<mode>` : Only "BW" and "OCV" are allowed.
- **For process = 28nm, the recommended generation corners are below :**
 - (non-CPF-in)
 - `fstaH -gen_ac_scan_constraint <proj>_TDF aocvwg aocvwgc aocvbg aocvbcgh -ptsi [-ip/-nonip]`
 - (CPF-in)
 - `fstaH -gen_ac_scan_cpf_constraint <cpf_file_name> AOCV -ptsi [-ip/-nonip]`

fdrc database generation

- **Generate SetTrans and SetLoad**

- [-trans] : Input Transition (digital number)
- [-load] : Output Loading (digital number)
- [-drive_cell_sdc] : User Specify Boundary Constraint, only allow one corner. (SDC file)
- (non-CPF-in)
 - fstaH -gen_trans_load <mode 1> <mode ...> [-trans 0.15] [-load 0.03] [-drive_cell_sdc]
 - <mode> : Only "B", "N", "W", "WCC", "BCH", "WG", "WCGC", "WCG0", "BG", "BCGH" are allowed.
- (CPF-in)
 - fstaH -msv <cpf_file> <mode> -gen_trans_load [-trans 0.15] [-load 0.03] [-drive_cell_sdc]
 - <mode> : Only "BW" is allowed.

- **Generate CKC & Case analysis file for sdc-driven fdrc**

- (non-CPF-in)
 - fstaH -group <sdc_id_1> <mode> -group <sdc_id_2> <mode> -gen_files_for_fdrc
 - <mode> : Only "B", "N", "W", "WCC", "BCH", "WG", "WCGC" are allowed.
- (CPF-in)
 - fstaH -msv <cpf_file> <mode> -gen_files_for_fdrc
 - <mode> : Only "BW" is allowed.

User Specified Script

- **fstaH XXX -script_setup <script> -script_hold <script>**

Clock_latency.pt :
report_clock_timing -type summary -nosplit > clock_latency.rpt

Clock_latency.pt

fstaH XXX -script_setup Clock_latency.pt

*rpts/clock_latency.rpt

Collect timing result into xml file

- STA2XML Syntax: `fstaH -sta2xml`
- Example:
 - `${working_directory}/Constraint.xml`

View Group	Time	sdc/cpf view	RCorner	PVT	OCV	PTSI	total(lost)	in2reg		reg2reg		reg2out		recovery/removal		clock gating	
								WNS	#vio	WNS	#vio	WNS	#vio	WNS	#vio	WNS	#vio
shift	Setup	FSJ0FS172A_shift	CMAX	ssg0p81v1	AOCV	PTSI	17(-0)	0	0	0	0	0	0	-0.07	17	0	0
			CMIN	fg0p99v12	AOCV	PTSI	64(-0)	0	0	-0.048	53	0	0	-0.013	11	0	0
			RCMAX	fg0p99v12	AOCV	PTSI	80(-0)	0	0	-0.037	65	0	0	-0.018	15	0	0
	Hold	FSJ0FS172A_shift	CMAX	ssg0p81v1	AOCV	PTSI	89(-0)	0	0	-0.141	89	0	0	0	0	0	0



fstaH scenario



fstaH scenario

fstaH Scenario	Process
MSV	
CPF	All Process
UPF	All Process
PreLayout	
ZWLM	All Process
AWLM	All Process
PostLayout	
SPEF-in Flow	All Process

fstaH -check

- Check general setting in setup.ftc.fsta
 - %> fstaH –check

fstaH is in SPEF-in with RC-corner and w/o ETM db Flow now, this flow is used for 65nm process and below w/o ETM db

Please check the following variable in setup.ftc.fsta

STA_PERFORMANCE_EVALUATE_ENABLE = OFF

SDF_PER_CORNER_OR_CPF_FLOW = ON

- Check input files setting
 - %> fstaH –gen_fsta_control

fstaH scenario

- ZWLM Flow
- AWLM Flow
- MSV Flow
 - cpf
 - upf
- SPEF-in w/o RC-Corner Flow
- SPEF-in with RC-Corner Flow
 - w/o ETM
 - with ETM

fstaH scenario

- **ZWLM Flow**
- AWLM Flow
- MSV Flow
 - cpf
 - upf
- SPEF-in w/o RC-Corner Flow
- SPEF-in with RC-Corner Flow
 - w/o ETM
 - with ETM

ZWLM Flow

- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = **ON**
 - STA_PERIOD_DISCOUNT = 0.60
- **Output file**
 - Report Directories:
 - \${DirName}_ZWLM_rpts

fstaH scenario

- ZWLM Flow
- **AWLM Flow**
- MSV Flow
 - cpf
 - upf
- SPEF-in w/o RC-Corner Flow
- SPEF-in with RC-Corner Flow
 - w/o ETM
 - with ETM

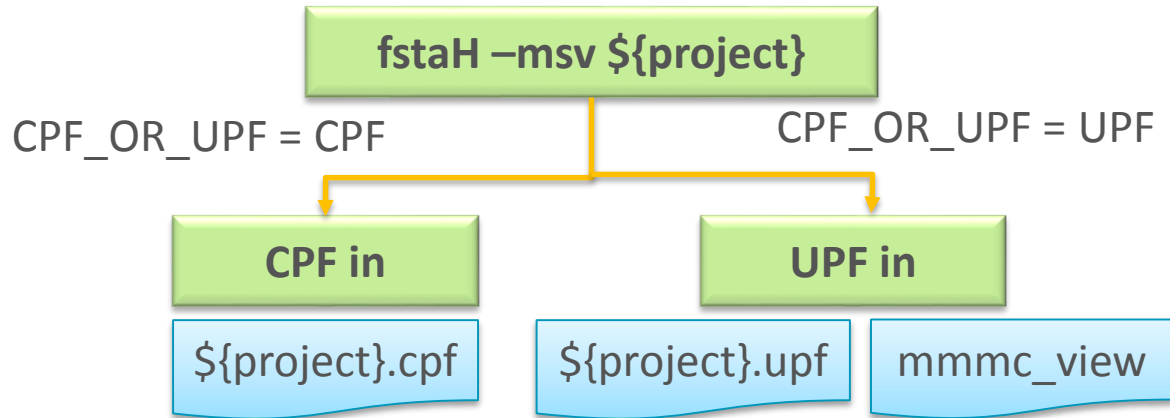
AWLM Flow

- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = **AUTO**
 - STA_PERIOD_DISCOUNT = 0.85(40nm↑) | 0.79(28nm)
- **Output file**
 - Report Directories:
 - \${DirName}_**AUTO**_rpts

fstaH scenario

- ZWLM Flow
- AWLM Flow
- **MSV Flow**
 - cpf
 - upf
- SPEF-in w/o RC-Corner Flow
- SPEF-in with RC-Corner Flow
 - w/o ETM
 - with ETM

MSV flow



- **Usage**

- `fstaH -msv ${project} ${op_mode}`
 - `${op_mode}` can be BW, OCV or AOCV
 - “**BW**”, “**OCV**”, and “**AOCV**” used to distinguish into “**NO Derating**”, “**Derating by OCV**”, “**Derating by AOCV and OCV**”

MSV flow - cpf

- **Input file**
 - .db
 - .v
 - .sdc
 - **\${project}.cpf**
 - \${project}_\${rccorner}.spef
- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = OFF
 - SDF_PER_CORNER_OR_CPF_FLOW = ON
 - CPF_OR_UPF = **CPF**
 - CPF_DEFAULT_ANALYSIS_VIEW = view1
 - CPF_SETUP_ANALYSIS_VIEW = view1
 - CPF_HOLD_ANALYSIS_VIEW = view2 view3
 - CPF_VIEW_TO_RC_CORNER = “view1 \$rccorner1 \$rccorner2”
“view2 \$rccorner3 \$rccorner4” “view3 \$rccorner3 \$rccorner4”

MSV flow - upf

- **Input file**
 - .db
 - .v
 - .sdc
 - **\${project}.upf**
 - **mmmc_view**
 - \${project}_\${rccorner}.spef
- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = OFF
 - SDF_PER_CORNER_OR_CPF_FLOW = ON
 - CPF_OR_UPF = **UPF**
 - CPF_DEFAULT_ANALYSIS_VIEW = view1
 - CPF_SETUP_ANALYSIS_VIEW = view1
 - CPF_HOLD_ANALYSIS_VIEW = view2 view3
 - CPF_VIEW_TO_RC_CORNER = “view1 \$rccorner1 \$rccorner2”
“view2 \$rccorner3 \$rccorner4” “view3 \$rccorner3 \$rccorner4”

fstaH scenario

- ZWLM Flow
- AWLM Flow
- MSV Flow
 - cpf
 - upf
- **SPEF-in**
 - w/o RC-Corner Flow (90nm~350nm)
 - w/ RC-Corner Flow (28nm~65nm)

SPEF-in w/o RC-Corner Flow (90nm~350nm)

- **Input file**
 - .db
 - .v
 - .sdc
 - `${project}.spef (110nm~350nm) | ${project}_typical.spef (90nm)`
- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = OFF
 - SDF_PER_CORNER_OR_CPF_FLOW = ON
 - STA_PVT_W = SS0P81V125C
 - STA_PVT_B = FF0P99VM40C
- **Usage**
 - `fstaH -group ${sdcname} w b ocvb`
 - `fstaH -group ${sdcname} w -ptsi`

SPEF-in w/ RC-Corner Flow (28nm~65nm)

- **Input file**
 - .db
 - .v
 - .sdc
 - \${project}_\${rccorner}.spef
- **setup.ftc.fsta**
 - STA_PERFORMANCE_EVALUATE_ENABLE = OFF
 - SDF_PER_CORNER_OR_CPF_FLOW = ON
 - STA_PVT_W = SS0P81V125C
 - STA_RCCORNER_WC = CMAX125C RCMAX125C
- **Usage**
 - fstaH -group \${sdcname} ocvw w



setup.ftc.fsta



PVT and rccorner

- If I want to run `wcc_cmax` and `wcc_rcmax` ...

```
%fstaH -group $sdcname wcc  
STA_PVT_WCC = SS0P81VM40C  
STA_RCCORNER_WCC = CMAXM40C RCMAXM40C  
STA_TIMING_LIB_SS0P81VM40C_CMAX = ...  
STA_TIMING_LIB_SS0P81VM40C_RCMAX = ...
```

- If I want to run `ocvwcc_cmax` and `ocvwcc_rcmax` w/o ETM model

```
%fstaH -group $sdcname ocwcc  
STA_PVT_WCC = SS0P81VM40C  
STA_RCCORNER_WCC = CMAXM40C RCMAXM40C  
STA_TIMING_LIB_SS0P81VM40C_CMAX = ...  
STA_TIMING_LIB_SS0P81VM40C_RCMAX = ...
```

- If I want to run `ocvwcc_cmax` and `ocvwcc_rcmax` w/ ETM model

```
%fstaH -group $sdcname ocwcc  
STA_PVT_WCC = SS0P81VM40C  
STA_RCCORNER_WCC = CMAXM40C RCMAXM40C  
STA_TIMING_LIB_SETUP_SS0P81VM40C_CMAX = ...  
STA_TIMING_LIB_SETUP_SS0P81VM40C_RCMAX = ...
```

fstaH will auto transfer SS0P81VM40C to SSG0P81VM40C when running wgcg
User don't need to specify STA_PVT_WCGC = SSG0P81VM40C

Library Setting

- When STA_AUTO_GET_LINK_LIBRARY = OFF

- PVT and rccorner definition:
STA_PVT_WCC = SS0P81VM40C
STA_RCCORNER_WCC = CMAXM40C

- library with **normal corner** :
STA_TIMING_LIB_SS0P81VM40C_CMAX = \$ss_core \$ss_IP

- library with **normal corner** :
STA_TIMING_LIB_SS0P81VM40C_CMAX = \$ss_core \$ss_IP

- library & **non_derate-ETM** with **normal corner** :
STA_TIMING_LIB_SS0P81VM40C_CMAX = \$ss_core \$ss_IP \$ss_ETM_cmax

- library & **setup-ETM** with **global corner** :
STA_TIMING_LIB_SETUP_SSG0P81VM40C_CMAX = \$ssg_core \$ssg_IP \$setup_ssg_ETM_cmax

- library & **hold-ETM** with **global corner** :
STA_TIMING_LIB_HOLD_SSG0P81VM40C_CMAX = \$ssg_core \$ssg_IP \$hold_ssg_ETM_cmax

If I want to
run
wcc_cmax/
wgcg_cmax
corner.....



Timing report parameter

- The following parameters setting will append to `report_timing -path_type ... -sig ...`
 - STA_MAX_PATH
 - STA_MAX_PBA_PATH
 - STA_PBA_METHOD
 - STA_RPT_PATHTYPE
 - STA_NWORST
 - STA_SLACK_LESS_THAN
 - STA_SLACK_GREATER_THAN
 - STA_SIGNIFICANT_DIGITS
 - STA_DELAY_CALC_DEBUG : add “-transition_time -capacitance -net” when `report_timing`.
- **STA_SPLITRPT_INT03PART** : Enable/Disable the function to split the setup/hold timing report into three different files according to the path type.
 - [Setup|Hold]Chk_in2reg.rpt
 - [Setup|Hold]Chk_reg2reg.rpt
 - [Setup|Hold]Chk_reg2out.rpt
- **STA_CRPR_THRESHOLD** : Specify the amount of pessimism that crpr is allowed to leave in the timing report.
 - Default: 1 (minimum value)

User specified parameter - Uncertainty/OCV

- **STA_USERSPECIFIED_MARGIN**
 - If this option is set to “OFF”, fstaH will automatically apply the hold time uncertainty for each process sign-off criteria. If users want to specify hold time uncertainty, users can set this option to “ON”.
 - Example:
 - STA_USERSPECIFIED_MARGIN = ON
 - [SDC] set_clock_uncertainty -hold 0.055 [all_clocks]
- **STA_USERSPECIFIED_DERATING_FILE**
 - If this option is set to “OFF”, fstaH will automatically apply derate value for each process sign-off criteria. If users want to specify derate value, users can set this option to “derating.pt”
 - Example:
 - STA_USERSPECIFIED_DERATING_FILE = derating.pt

User specified parameter – Propagated clock

- **Propagated clock but w/o spef**
 - [setup.ftc.fsta]
 - STA_PERFORMANCE_EVALUATE_ENABLE = AUTO
 - STA_USERSPECIFIED_CLOCK_PROPAGATED = ON
 - [sdc]
 - set_propagated_clock [all_clocks]
- **Not propagated clock but w/ spef**
 - [setup.ftc.fsta]
 - STA_PERFORMANCE_EVALUATE_ENABLE = OFF
 - STA_USERSPECIFIED_CLOCK_PROPAGATED = ON
 - [sdc]
 - remove_propagated_clock [all_clocks]

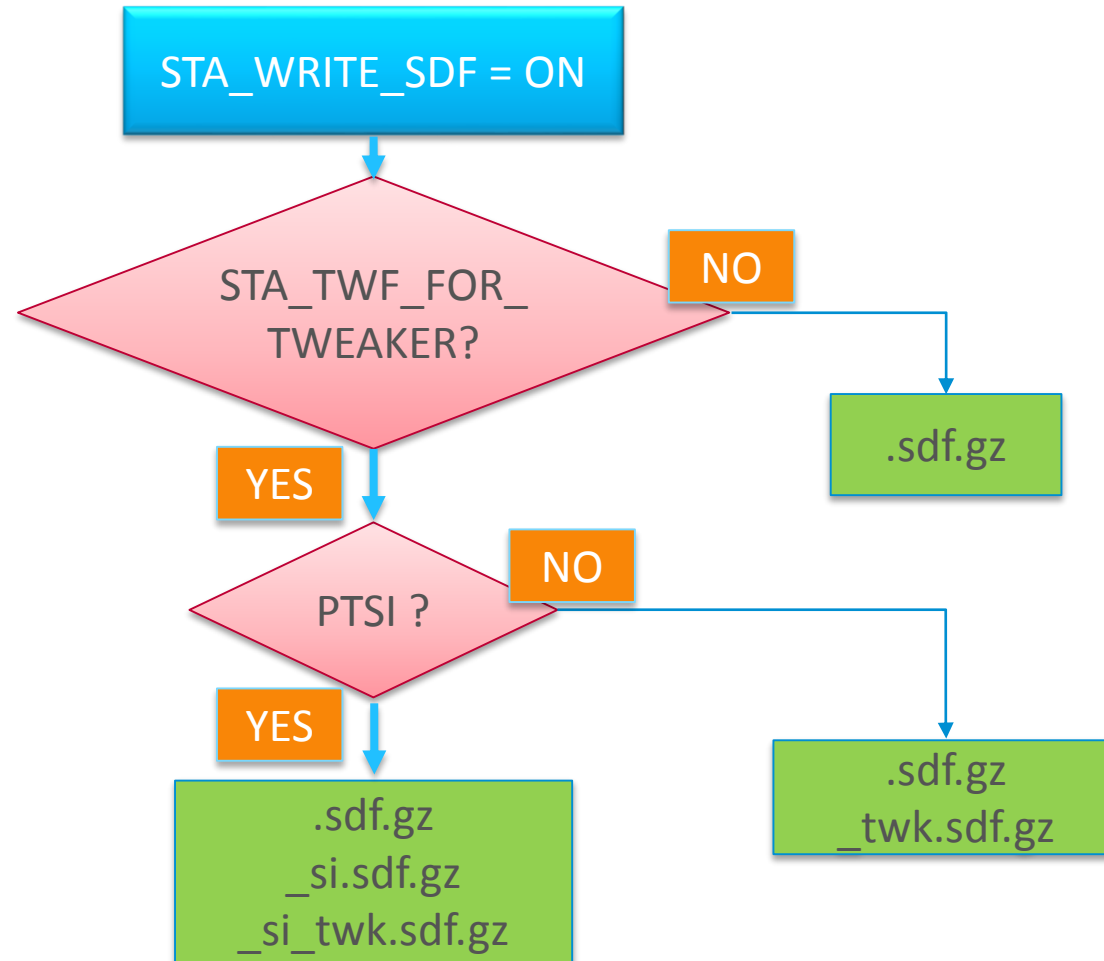
Boundary constraint

- **DEFAULT_INPUT_SLEW**
 - Specify the input slew for the input port which does not set in sdc.
- **DEFAULTPAD**
 - Specify the output load for output port which does not set in sdc.

DMSA related

- **STA_DMSA**
 - Enable/Disable to run the distributed STA.
- **STA_MULTICORE_NUM**
 - Specify the maximum number of CPU cores that can be used for each subsequently launched remote process.
- **STA_MULTIPROC_NUM**
 - Specify the number of processes to launch per host for future PrimeTime jobs.
- **STA_LICENSE_NUMBER**
 - Specify the number of scenarios to run simultaneously.
- **HOSTS**
 - Specify the available machine to run the distributed STA.
 - You have the permission to login these remote machines.
 - You have add the name of these remote machines into ~/.rhosts.

SDF related



1. .sdf.gz
 - Generate for simulation
 - Not include the timing arc for internal pin
 - Effected by "STA_SDF_WITHOUT_INSTANCE"
2. _si.sdf.gz
 - (1.) + ptsi
3. _twk.sdf.gz
 - Generate for tweaker
 - include the timing arc for internal pin
 - Not effected by "STA_SDF_WITHOUT_INSTANCE"
4. _si_twk.sdf.gz
 - (3.) + ptsi

Auto apply ETM and pure analog to STA_SDF_WITHOUT_INSTANCE

- When using etm.db and pure analog to generate top.sdf, sdf may include ETM timing arc at sdf, this will cause simulation warning

```

- sdf (CELL
      (CELLTYPE "FZOTG300HHOL")
      (INSTANCE u_core/u_SBS_USB3_TOP/FZOTG300HHOL_inst_0)
      (DELAY
        (ABSOLUTE
          (IDPATH APB_CLK APB_READY (0.6182::0.6446) (0.5975::0.6194)))

```

- VCS simulation : *Warning-[SDFCOM_TANE] TIMINGCHECK Annotation Not Enabled*

- At setup.ftc.fsta , add instance at STA_SDF_WITHOUT_INSTANCE , fstaH will not generate this instance timing arc at .sdf.gz and _si.sdf.gz

- STA_SDF_WITHOUT_INSTANCE = (empty) or doesn't exists this variable, fstaH auto apply ETM and pure analog to filter

- timing_model_type == extracted
- Pure analog : FXPORK* , FXADC* , FXLVDS* , FXAFE*
- Check the result at *rpts/fsta script/WriteSDF.pt

```

write_sdf -context verilog -significant_digits 4 -input_port_nets -output_port_nets -v
ersion 3.0 -exclude checkpins -include "setphold recem" -no_edge -no_internal_pins
-exclude_cells "u_core/u_FXADC882HHOL_FTCM8A_1 u_core/u_FXADC882HHOL_FTCM8A u_core/u_DW
CAXI_PCIE_OXSERDES201HHOL/OXSERDES201HHOL_inst_0 u_core/u_ax_e_core/u_por_bf u_core/u_S
BS_USB3_TOP/FZOTG300HHOL_inst_0 u_core/u_SYSC/u_FTSCU100/u_PWRCTRL_UNIT/u_PCUPOR/u_CORE
POR" -compress gzip FSH0AS038A_FSH0AS038A_post_tc_VIEW_TCCOM_PM_ALL_ON_typical_si.sdf.
gz

```

- STA_SDF_WITHOUT_INSTANCE = OFF
 - write_sdf w/o "-exclude_cells"
- STA_SDF_WITHOUT_INSTANCE = u_core/u_SBS_USB3_TOP/FZOTG300HHOL_inst_0
u_core/u_DWCAXI_PCIE_OXSERDES201HHOL/OXSERDES201HHOL_inst_0
 - fstaH will not auto apply ETM and pure analog, but apply user defined instances

Tweaker related

- **STA_TWF_FOR_TWEAKER**
 - When this option is “ON”, fstaH will generate file for tweaker.
- **STA_SDF_OF_EACHSDC**
 - When this option is “ON”, fstaH will generate the sdf file according to different sdc settings. This means that each sdc will generate a unique corresponding *sdf* file. When this value is off, fstaH will remove the case_analysis settings to generate a general sdf.

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