|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name |  | No. |  | Div/Dept | DSD/ACD/ACT | Job  Date：2024/08/05  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 🗹W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2024, below are a brief description of the tasks and what I learned:   * Continue Test Chip flow: * Modify SDC * Check Post DFT data |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * How is FSN0FS142A\_MBIST.sdc file generated when running run\_fsta.csh ? |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Complete Test Chip flow * Prepare knowledge for Final report |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Nguyen Thanh Sang  (2024/08/05) | (Signature/Date) | (Signature/Date) |

1. **MODIFY SDC**







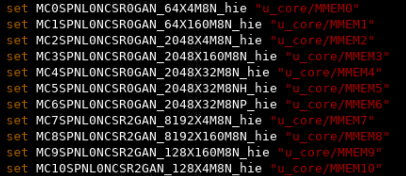


**Step 1: Make mbist\_tail.sdc**

>> *touch mbist\_tail.sdc*

**Step 2: Open Function SDC and find the “Memory macro hierachy setting”**

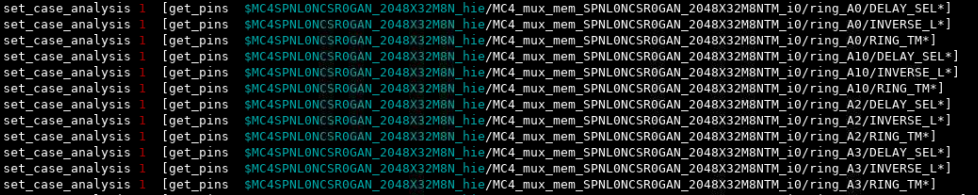
Purpose: set hierachy name for memory



**Step 3: Open Function SDC and find the “Set case analysis”**

**<set\_case\_analysis>** : *specifies the port or pin that is set to the constant value*

**Syntax:** set\_case\_analysis *value port\_or\_pin\_list*



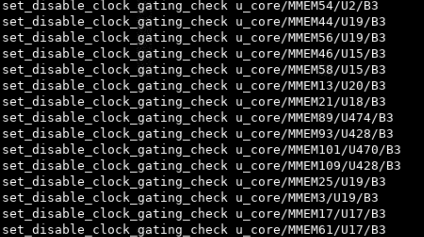
: change 0 to 1 to enter test mode in mbist

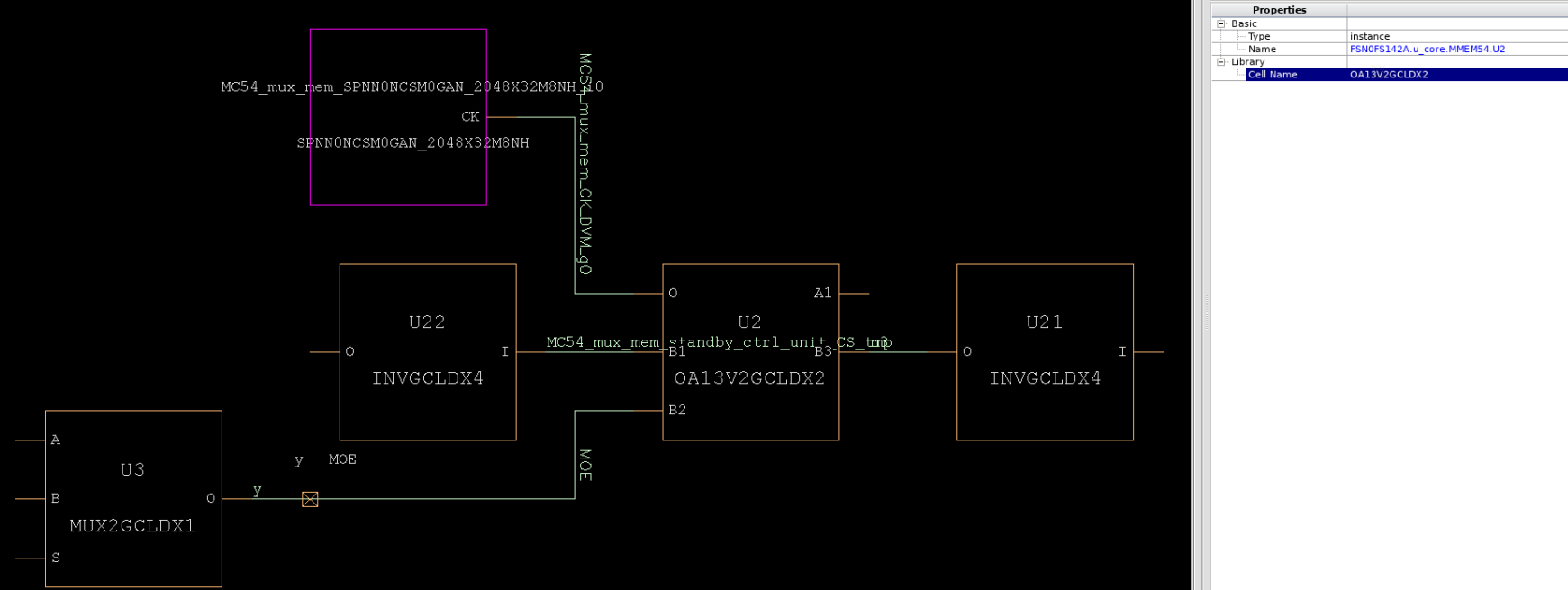
**Step 4: Open Function SDC and find the “set\_disable\_clock\_gating\_check”**

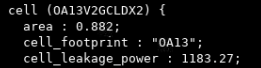
**<set\_disable\_clock\_gating\_check>** : *the disable check turns off the clock gating check on the specific pin, as we are not concerned with this pin*

**Syntax:** set\_disable\_clock\_gating\_check *port\_or\_pin\_list*

**Purpose:** to disable clock gating of pin some combination cells don’t affect the output clock defined in Function SDC





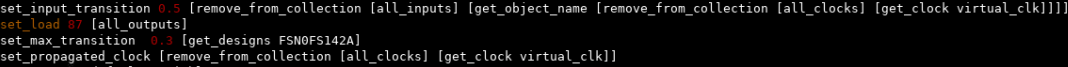
**Step 5: Open Function SDC and copy below setting to mbist\_sdc\_tail.sdc**

set\_input\_transition *transition port\_list* : specifies the transition time on an input pin

set\_load *value objects* : set the value of capacitive load on pin or net in design

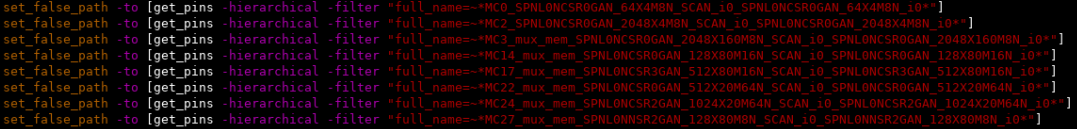
set\_max\_transition *value object\_list* : specifies the max transition time on a port or on a design

set\_propagated\_clock *object\_list* : specifies that clock latency needs to be computed, that is, it is not ideal

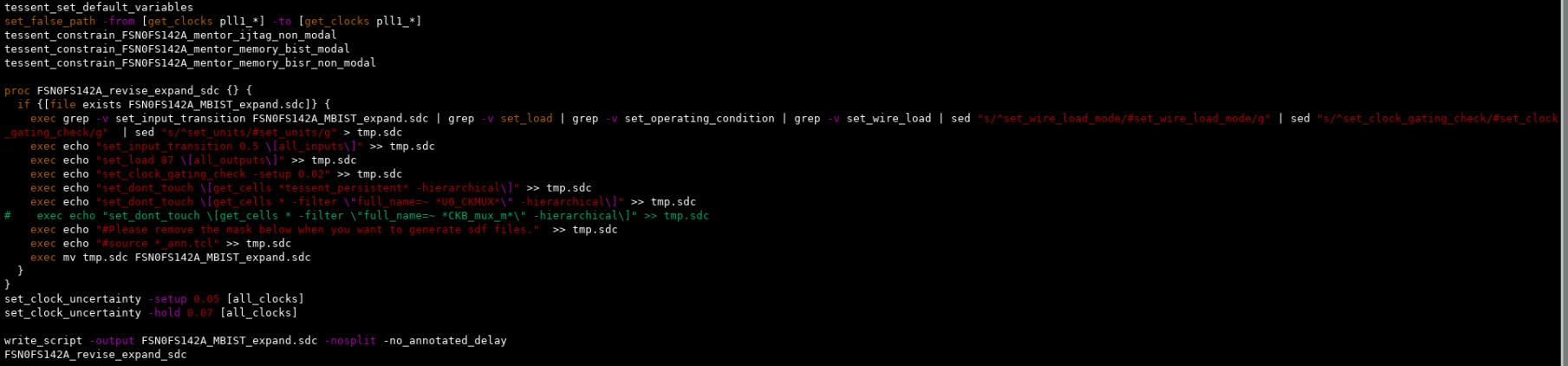


**Step 6: Set false path**

**Purpose:** Set false path for memory instance that is not MBIST target. If not we have violation related to paths through non-mbist mem



**Step 7: Add below setting to mbist\_sdc\_tail.sdc**



to prevent objects such as: cells, net, design change

Set a uncertainty value to match sign-off table

to avoid clock crossing



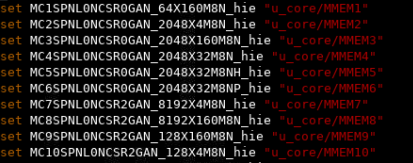


**Step 1: Make user\_clk.sdc**

>> *touch user\_clk.sdc*

**Step 2: Open Function SDC and find the “Memory macro hierachy setting”**

**Purpose:** set hierachy name for memory

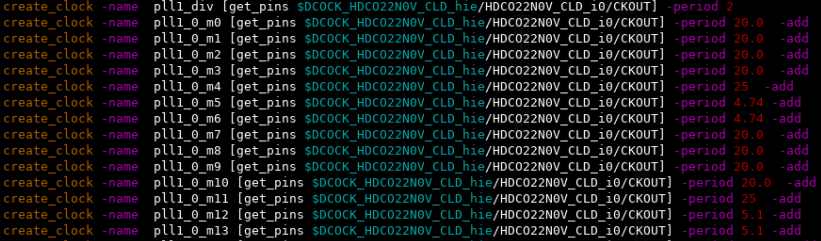


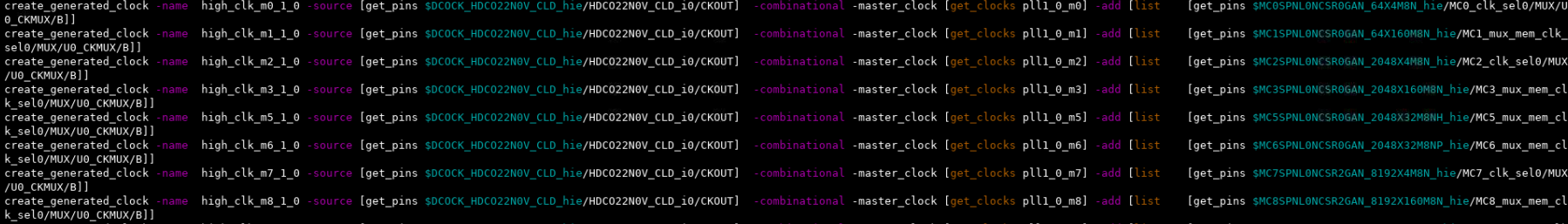
**Step 3: Open Function SDC and copy clock constrains to user\_clk.sdc**

**Syntax:** create\_clock *[-name clock\_name] [source\_objects] [-period period\_value]*

*[-add]* : define master clock

create\_generated\_clock *[-name clock\_name] -source master\_pin* : define an internally generated clock





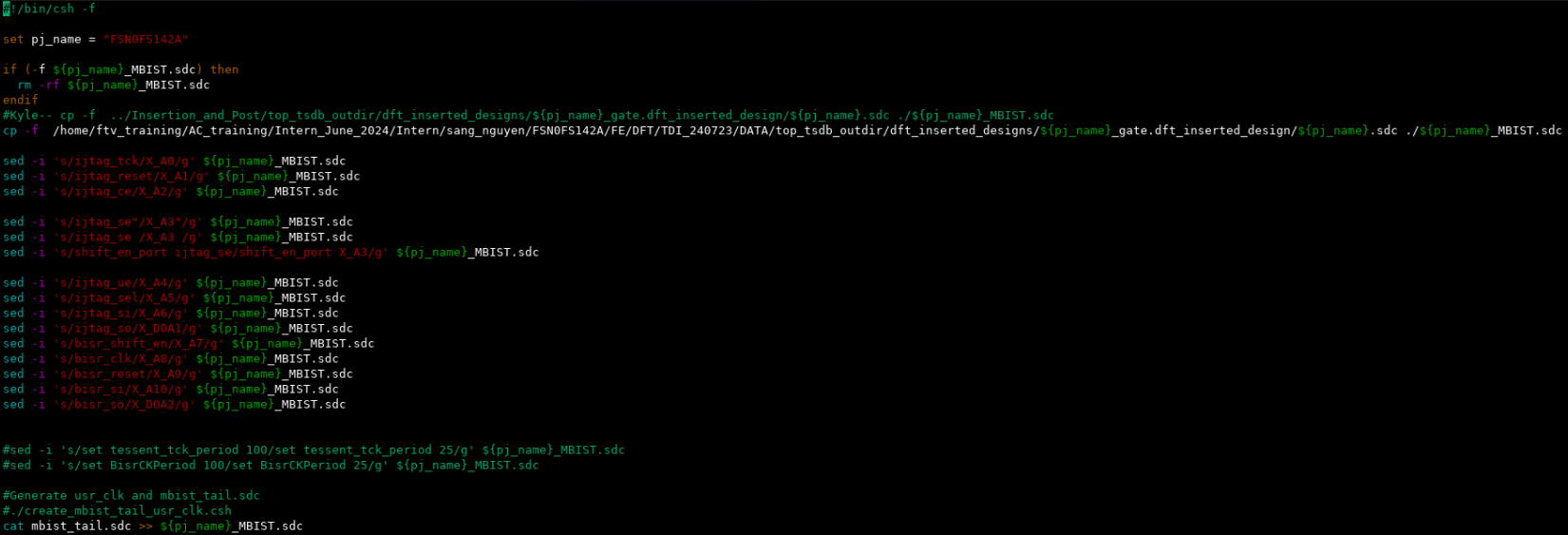
**FSN0FS142A\_MBIST.sdc**



**Step 1:** **Run “modify\_sdc.csh” to generate “FSN0FS142A\_MBIST.sdc”**

>> *./modify\_sdc.csh*

**Purpose:** sed “s/pattern1/pattern2/g” to replace all pattern appeat in function sdc to change port name of IJTAG and BISR to respect with post DFT netlist.







**Step 1:** **Executive FSTA to generate “FSN0FS142A\_MBIST\_expand.sdc”**

>> *./run\_fsta.csh*

**Step 2: Copy “FSN0FS142A\_MBIST\_expand.sdc” to ../SDC\_ECO**



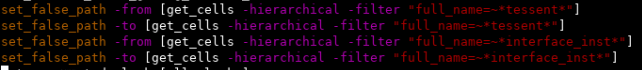
**Step 3: Add below constraints**

**Purpose:** In reality, there’s no connection in timing between *u\_core\_MMEM\*\_MOE\_latch* and *PLL clock*, cause at the PLL clock active, u\_core\_MMEM\*\_MOE\_latch signal and all\_test\_latch signal keep stable at high until the end of test

**FSN0FS142A.sdc**



**set\_false\_path** for paths related to MBIST

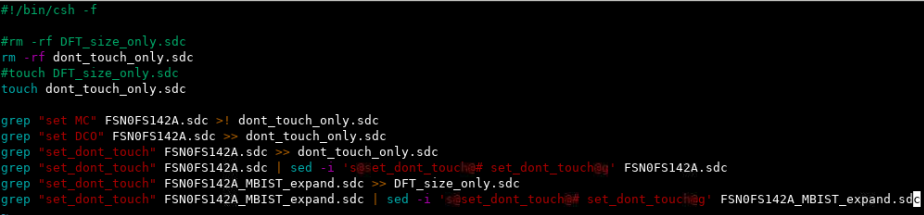




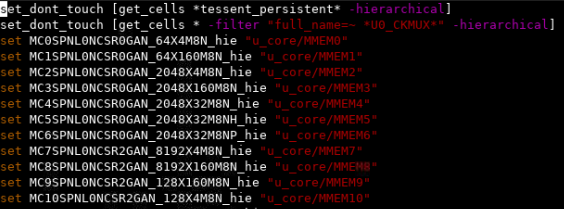


**Step 1: Run “make\_size\_only.csh” script**

>> *./make\_size\_only.csh*



**Step 2: Open Function SDC and find the “Memory macro hierachy setting”**

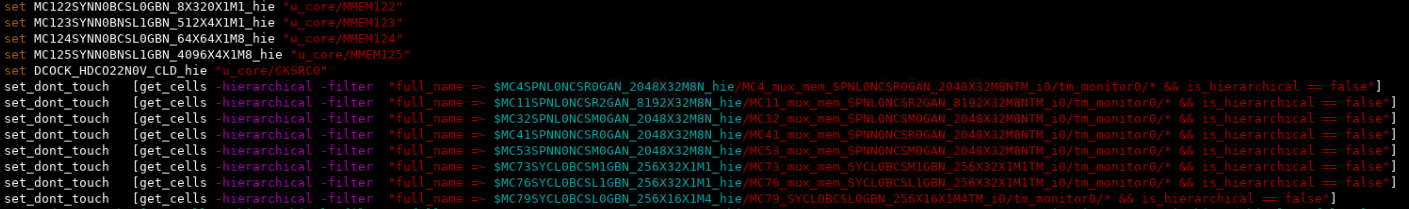
****

* **DFT\_size\_only.sdc:** contains command set\_dont\_touch target to DFT cell that’s able to size for timing optimization (cells are set dont\_touch from DFT sdc)





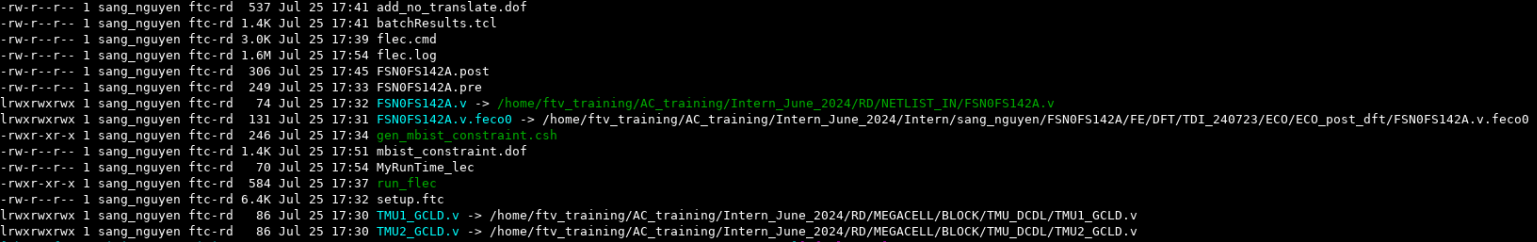
* **dont\_touch\_only.sdc:** contains TM cells (cells and net are set\_dont\_touch in function sdc)



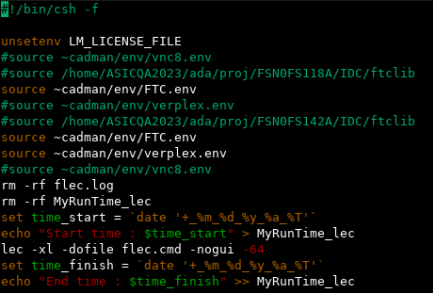
1. **POST\_DFT DATA CHECK:**

* **flec:**

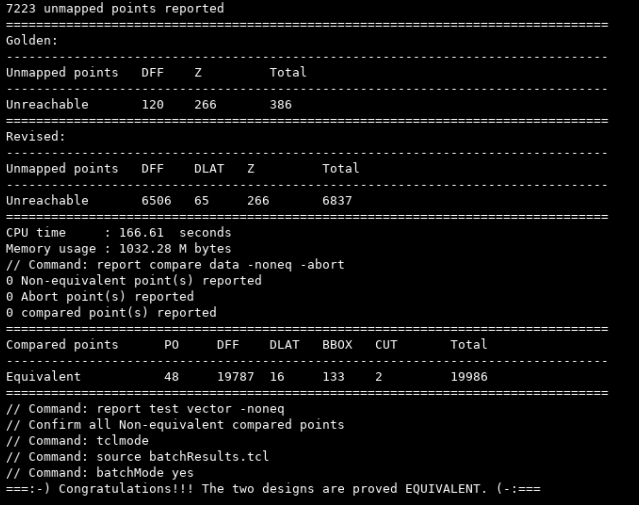
/home/ftv\_training/AC\_training/Intern\_June\_2024/Intern/sang\_nguyen/FSN0FS142A/FE/DFT/TDI\_240723/ECO/FLEC



**run\_flec:**

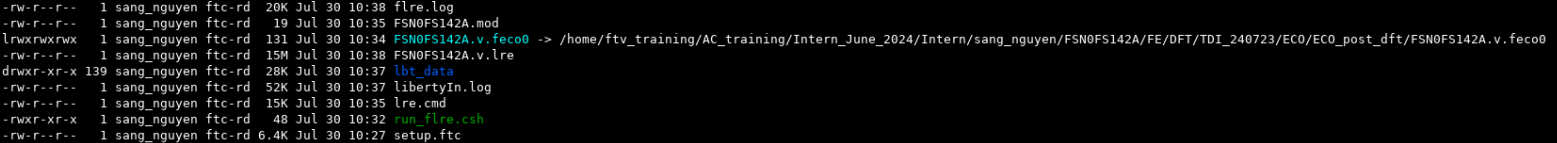


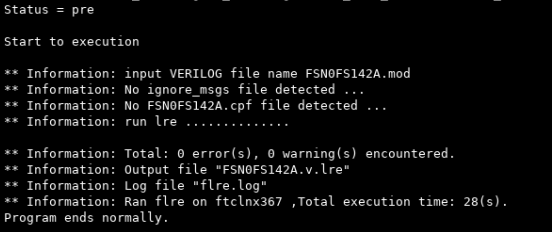
**flec.log:**



* **flre:**

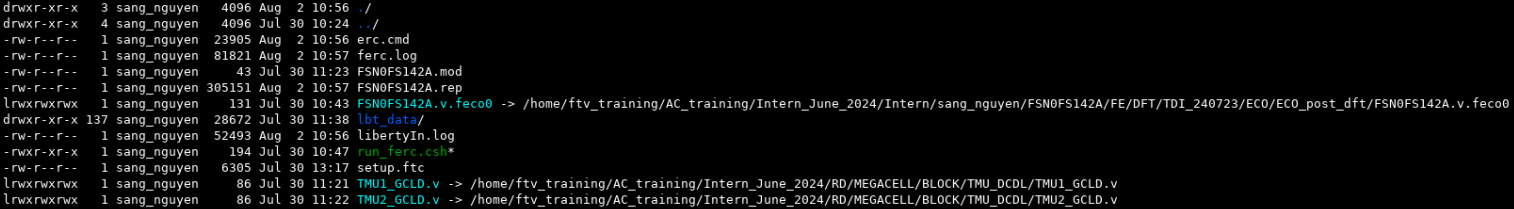
/home/ftv\_training/AC\_training/Intern\_June\_2024/Intern/sang\_nguyen/FSN0FS142A/FE/Pre\_Sim/TDI\_Jul\_30\_post\_DFT/flre



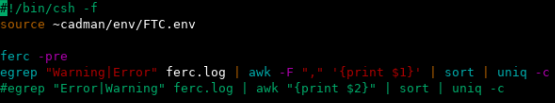


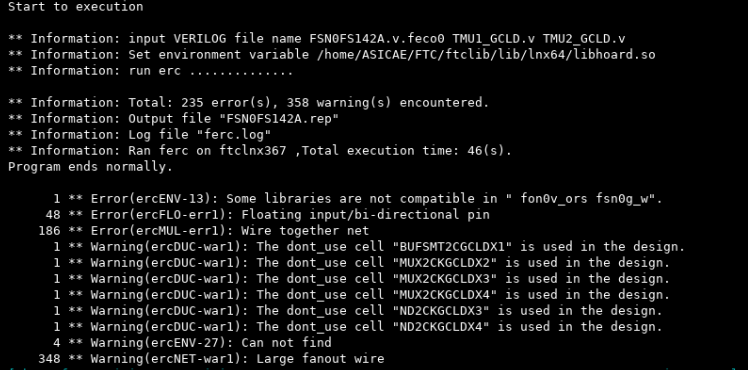
* **ferc:**

/home/ftv\_training/AC\_training/Intern\_June\_2024/Intern/sang\_nguyen/FSN0FS142A/FE/Pre\_Sim/TDI\_Jul\_30\_post\_DFT/ferc



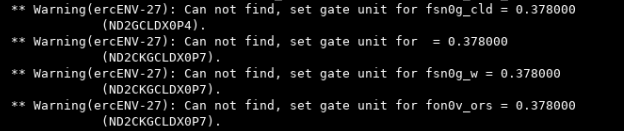
**run\_ferc:**





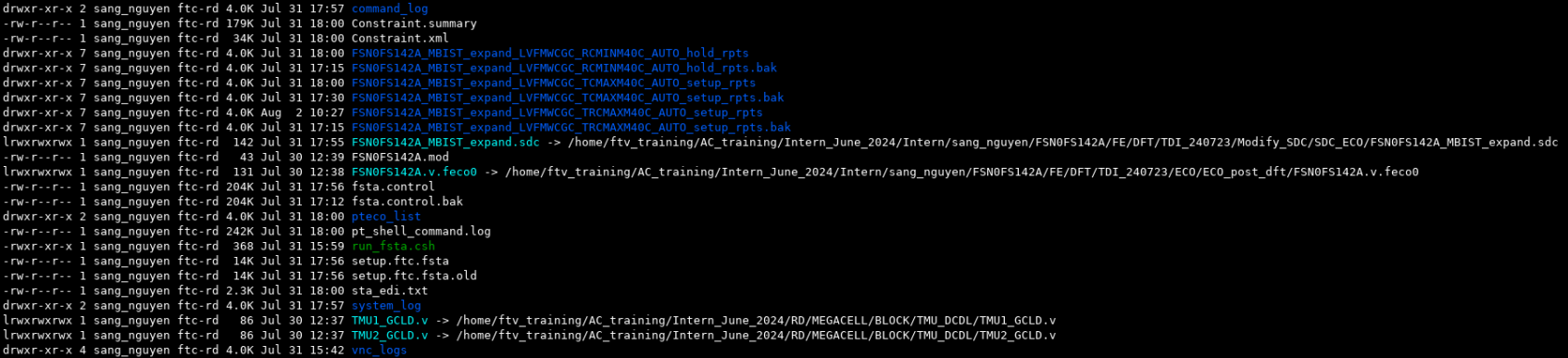
***Problem:***



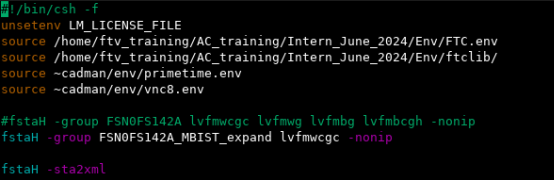


* **fsta:**

/home/ftv\_training/AC\_training/Intern\_June\_2024/Intern/sang\_nguyen/FSN0FS142A/FE/Fsta/Pre\_STA/TDI\_July\_30\_post\_DFT

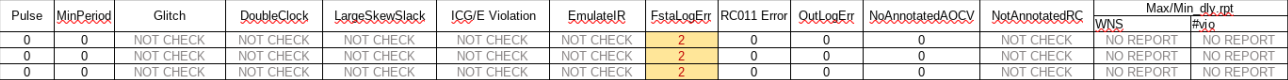


**run\_fsta.csh:**



**Constraint.xml:**





**2 errors in FstaLog Error Column:**



* The error indicates that we have set “STA\_PERIOD\_DISCOUNT” differently from the default value of PrimeTime, it does not affect the tool running process. So, we can waive this error.

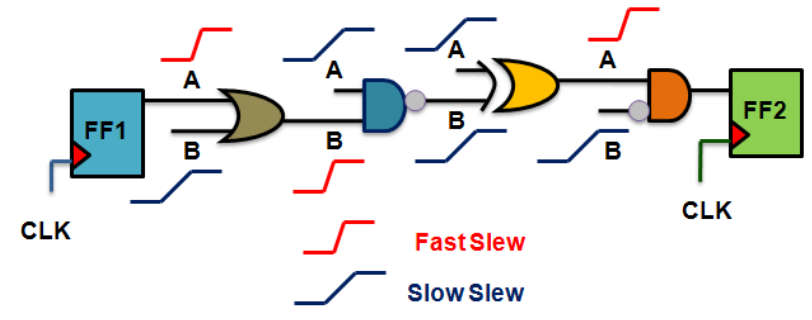


* The error indicates that we have set “slew\_derate\_from\_library” in library differently from the default value of PrimeTime. The slew value to actual characterized transition time is library\_transition\_time\_value \* slew\_derate

***PBA – GBA***

In GBA mode, pessimistic transition time is propagated at each cell of the timing graph. GBA is able to calculate all the path delays in circuits and report the critical paths in a fast way. However, it always introduces pessimism due to the worst-case slew propagation.

As for PBA, timing analysis pessimism is reduced at the cost of significantly greater runtime than GBA. In PBA, the slew of the output pin is computed based on the real slew of inputs. Then the actual path-specific slew is propagated on the path and used in delay calculation for cells, which helps to improve the accuracy of time analysis. However, as the number of timing paths increases, there is an exponential increment in the possibilities of transition propagation and delay calculation at each cell. It causes PBA runtime-intensive.

Consider the following example. Assume that we are doing setup check (max delay) for the timing path from FF1 to FF2.

In GPA, slews propagated to the outpin of each gates will be the worst, meaning it will be computed based on the gates’ output load and worst input slews, namely:

* Slew at pin B to Z for ◼
* Slew at pin A to Z for ◼
* …

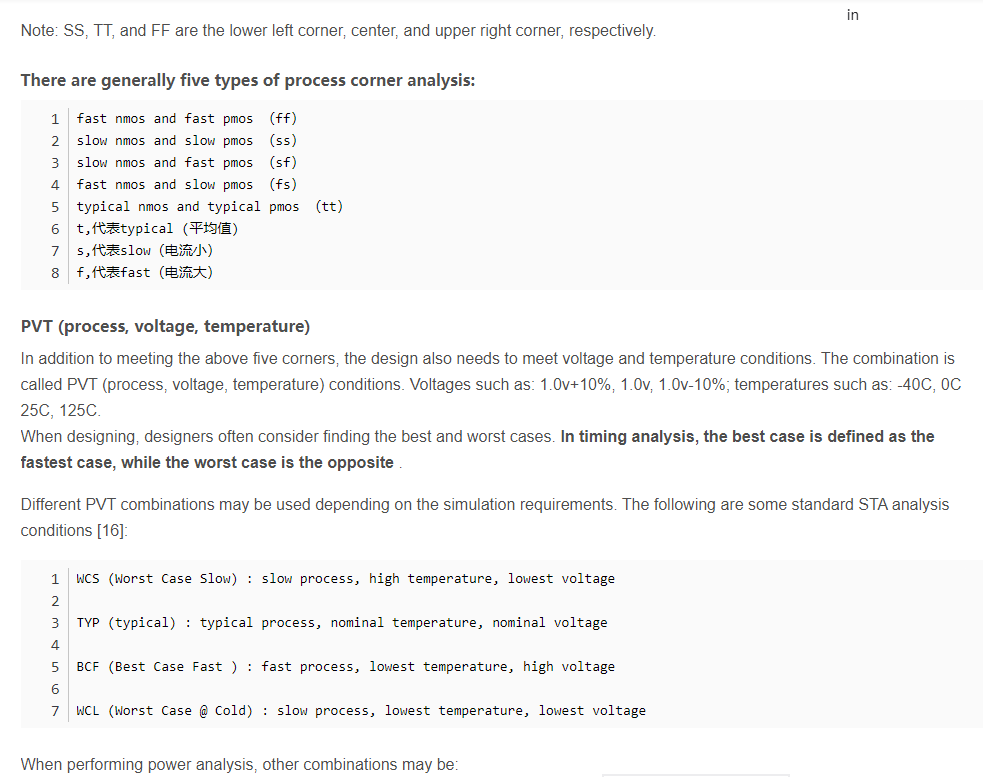
In PBA, the tool will consider the actual slew for the arcs encountered while traversing any particular timing path.

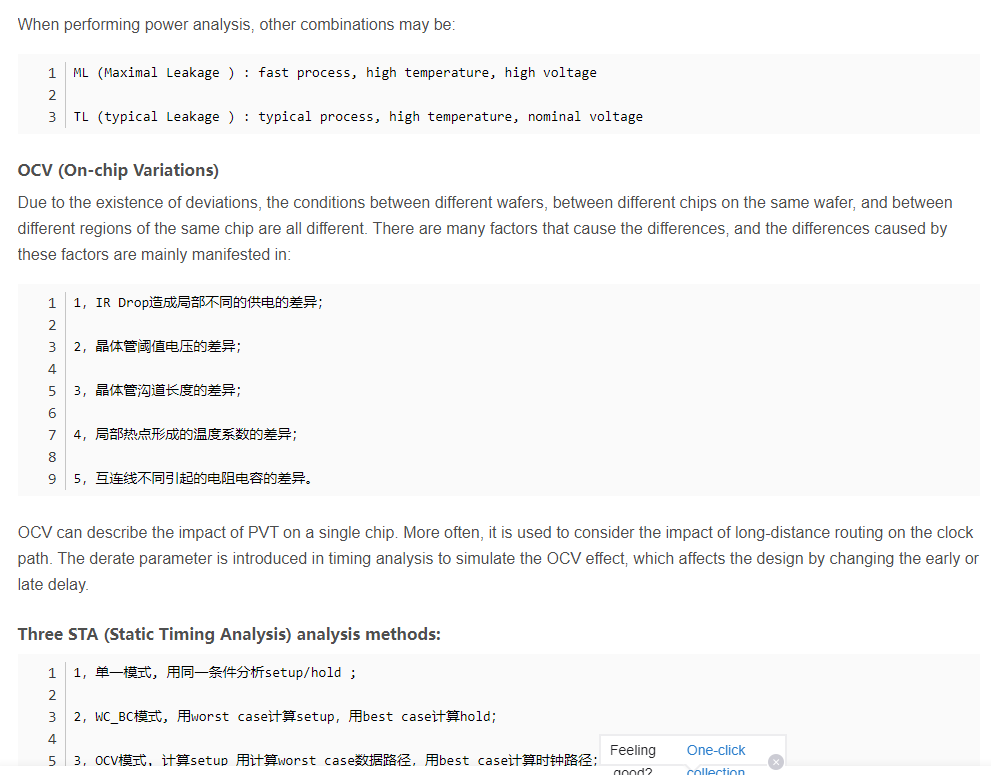
* Slew at pin A to Z for ◼
* Slew at pin B to Z for ◼
* …

***LVT | RVT | ULVT | SVF | HVT***

* ULVT = Ultra Low Voltage Threshold
* LVT = Lower Voltage Threshold - causes more power consumption and switching timing is optimized; used in time critical functions.
* SVT = Standard Voltage Threshold || RVT = Regular Voltage Threshold - offers trade-off between HVT and LVT i.e. moderate delay and moderate power consumption.
* HVT = Higher Voltage Threshold - causes less power consumption but timing is not optimized; used in power critical functions.

Threshold voltage is the voltage over which, depending on the technology, a certain phenomenon happens. For example, threshold voltage of a MOSFET is the value of the gate voltage when a conductive band forms between the transistor's source and drain.



<https://physicaldesignconcepts.blogspot.com/2019/03/rc-variation.html>

wcgc:

/home/ftv\_training/AC\_training/Intern\_June\_2024/Intern/sang\_nguyen/FSN0FS142A/FE/Fsta/Post\_STA/FDI\_240807/FDI\_240807\_postLayout\_STA/0P8V/FSN0FS142A\_MBIST\_expand/wcgc/FSN0FS142A\_MBIST\_expand\_LVFMWCGC\_TRCMAXM40C\_PTSI\_setup\_rpts

