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| Name | Nguyen Le Thao Vy | No. | 3341 | Div/Dept | DSD/ACD/ACT3 | Job  Date：Dec 15th 2023  Title | Engineer |
| Please tick  the period | First Month | □W1 □W2 🗹W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed:   All of the tasks I learned during this first week are based on the training plan of 2023, below are a brief description of topics and tasks I was working on:   * Topics of interest:   + On chip variation;   + Design kit - fpad;   + Testchip workflow. * Tasks that I was working on:   + Read materials – self-learn;   + Work on testchip FSFGFS016A. * Outcomes:   + Completed all e-courses;   + Got familiar with running design kit and working in project. |
| 1. What are the problems encountered this week? Any actions taken? Any help needed?  * Problem encountered:   + Being unfamiliar with the testchip workflow. * Actions taken:   + Went through the flow in [FTV\_ACD\_TestChip\_Flow\_202303](file:///T:\FTV\DSD\DSD_ACD\ACT4\02_Internal_Tech_Shared\03_Testchip\FTV_ACD_TestChip_Flow_202303) under mentor’s guidance. |
| 1. What are the tasks for next week? Any preparation needed in advance?  * Work on assigned project; * Make time for completing items listed in training plan. |
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| Name  (Date) | Mentor | Direct Supervisor |
| Nguyen Le Thao Vy  (2023/12/22) | (Signature/Date) | (Signature/Date) |

***Questions from previous review session***

1. What is tie cell?

Tie cells are special-purpose cells whose output is either constant high (tie high cell) or constant low (tie low cell). These cells are used to hold (tie) inputs of cells that require constant high / low input signal, i.e. floating / unused inputs.

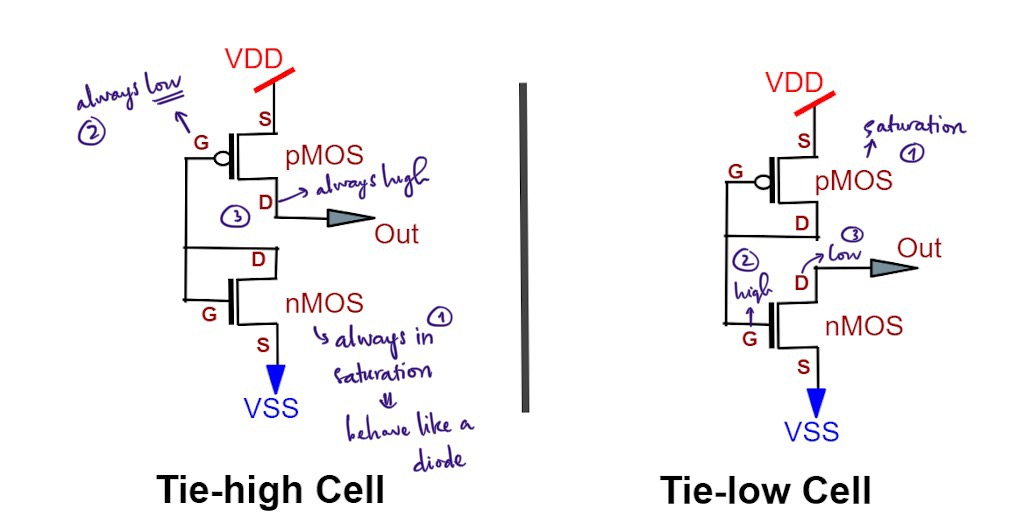


Figure 1: Tie-high and Tie-low cells

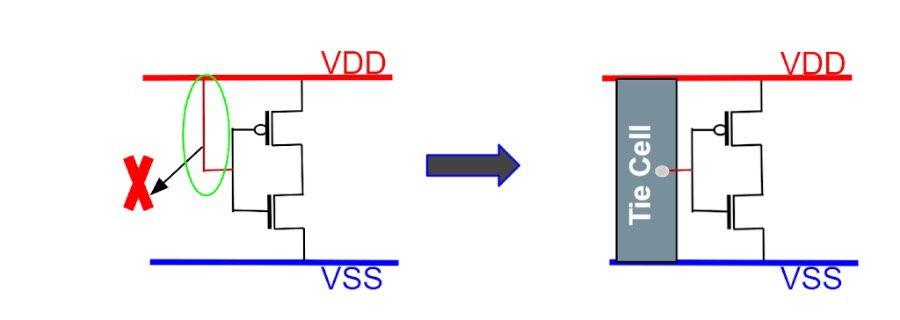
Why do we need tie cells? It is because directly connecting cells to the power / ground nets may cause the delicate gate oxide of transistors to be damaged due to voltage fluactions.

Figure 2: Cell(s) should not be connected directly to power / ground

1. How does high fanout worsen delay in circuits?

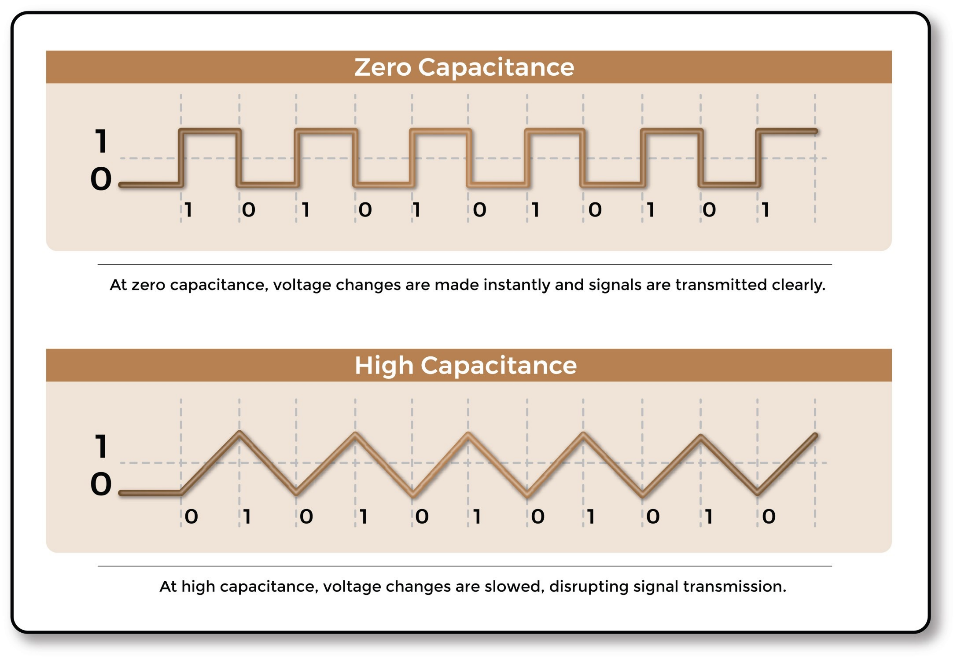
High fanout leads to increased capacitive load on the driving gate, and thus result in longer delay, since the higher the capacitance, the slower the voltage change.

Figure 3: Impact of capacitance on voltage

1. Explain delay fault.

Delays along every path from PI to PO or between internal latches must be less than the operational system clock interval. If the delay on at least one path of a circuit exceeds the clock period, it may fail to operate correctly at its specified speed (but can operate correctly at slower speed), and is said to experienced the delay fault.

Delay faults can be categorized as follows:

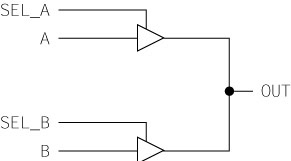
* + Transition faults: refer to timing failure that is large enough such that the delays of all paths through some gates to observable outputs exceed clock interval. Transition faults include delay in a rising (slow-to-rise) or falling (slow-to-fall) transition at inputs and outputs of logic gates.
  + Gate delay faults: refer to timing failure at a gate that in turn causes the delay of at least one path in the circuit through the fault site to exceed the specified cycle time.
  + Path delay faults: any path with a total delay exceeding the system clock interval is said to have a path delay fault.
  + …

1. Explain the importance of SDC file.

SDC file contains the timing constraints, logical relationship between signals, and physical design rules for a digital circuit. Its purposes are to specify the design intent and provide instructions to other tools (i.e. synthesis, STA, place-and-route tools..) on how to implement the design while meeting specific performance requirements. Quality of constraints dictates the quality and speed of implementation. Without these constraints, or with inappropriate / insufficient ones, chances are that circuits will not meet their intended clock frequencies, leading to unpredictable behavior or even failure.

Given the importance of the SDC file and its content, validation of the file is crucial in ensuring the correctness and consistency of the constraints inside. In this validation, errors related syntax (i.e. missing semicolon / misspelled keywords..) and semantic (i.e. conflicting / redundant / inconsistent / inapplicable constraints..) shall be uncovered.

1. How can an output be floating?

A pin is said to be floating if it is not driven to any defined logic level, thus it has an unknown voltage. Below is an example of a potential floating output:

If SEL\_A and SEL\_B are both not asserted, OUT will float to an unknown level.

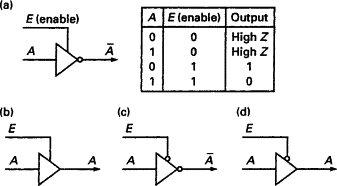
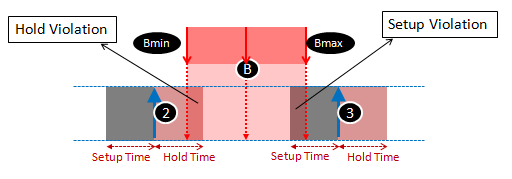
Another example is found in the tri-state buffer, in which if the enable signal is false, its output will be disconnected from the circuit and can be considered as being floating, high impedance, or high Z.

Figure 4: Tri-state buffer

1. Can a design violate setup and hold timing checks at once? How?

Simultaneous violation can occur when the timing checks is run in different scenarios / corners. In case the checks are performed at the same time on the same path, the answer should be no, since if there is enough delay to cause a setup violation, there that delay should also be enough to pass the hold check.



***FPAD – Faraday Pad File Generator***

FPAD is run mainly to generate the pad file information for the test and simulation flow. Apart from that, its functions include checking the control net connections of pad cells, as well as generating an **FTL** header file (.ftl) and a monitor file.

* 1. Required inputs: Netlist (.v / .v.gz / .mod) and design kit setting (setup.ftc)
  2. Outputs: Pad cell information file (.pad), FTL header file (.th), monitor file (.fv – if “TPRE = ON” in setup), and log file (fpad.log)
  3. Syntax: *fpad*

***OCV – On Chip Variation 🡪 AOCV – Advanced OCV 🡪 POCV – Parametric OCV***

**OCV** refers to the impact of variation of process parameters and environmental conditions (mainly voltage and temperature) in the fabrication process on the chip. This variation accounts for the fact that even though all chips are manufactured based on the same input data (.gds file), their electrical characteristics will not be truly identical.

If OCV is not handled well, it may lead to post-silicon failure, for instance, causing timing violations in a proper timing closure chip, due to an increase in delay of data path / launch clock path, or a decrease in delay of capture clock path.

To compensate for OCV, people have been using certain methods as below:

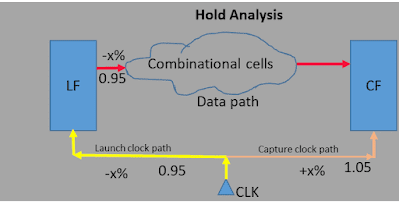
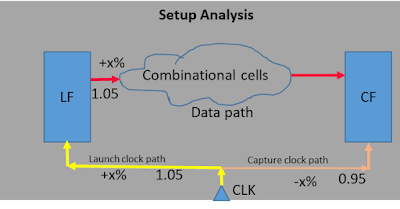
* **Fixed derate factor / OCV derate**: apply ±x% of additional delay to all the cells; it is ± because (in setup check, vice versa for hold check) the launching clock path needs to be derated by a positive value (adding delay to it) and the capture path by a negative value, as if it is faster than the nominal delay.

Figure 5: OCV derate in setup check

Figure 6: OCV derate in hold check

However, using a fixed timing derate for all the cells in the OCV is overly pessimistic, as chances are that it is very rare that all the cells will all be either late or early. In reality, most likely some cells will be late and some will be early, thus there will be a cancellation of effect.

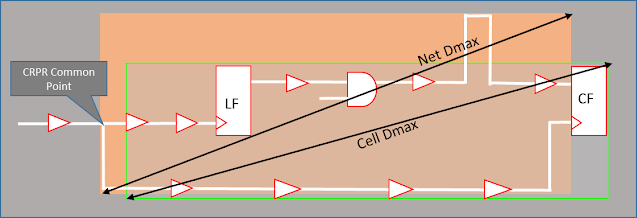
* **Distance and Depth –based derate factor - AOCV derate**: In AOCV, derate factor applying on each cell will be determined mainly based on distance and path depth of it, apart from that, its cell type and drive strength are also considered.
  + Distance: When distance increases, systematic variation would increase; and to mitigate the variation, a higher derate value is needed, thus along with the distance, derate value increases.

Figure 7: Cell and net distance

* + Path depth: In case of distance is kept constant and path depth increases, systematic variation would also be constant, and the random variations tend to cancel each other. Therefore, as path depth increases the derate factor would decrease.

In even lower technology nodes (below 40nm), AOCV too becomes inaccurate, as it cannot reduce pessimism any further, so people came up with another concept of POCV.

* **POCV**: In POCV, cell delay is calculated based on delay variation of the cell. This method uses a nominal delay value µ (instead of the min or max value of delay) to model the random variations and calculate arrival / required time. This nominal delay value is assumed to follow a normal distribution curve. Consider the case of using min / max delay, there is a greater chance that the delay would fall anywhere between the two extremes, whereas in POCV, it is likely that the delay will be at near the nominal value.