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| Name | Nguyen Le Thao Vy | No. | 3341 | Div/Dept | DSD/ACD/ACT3 | Job  Date：Jan 09th 2024  Title | Engineer |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | 🗹W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed:   All of the tasks I learned during this first week are based on the training plan of 2023, below are a brief description of topics and tasks I was working on:   * Topics of interest:   + Min period / pulsewidth;   + Timescale;   + Simulation - SPICE;   + Testchip workflow. * Tasks that I was working on:   + Read materials – self-learn;   + Work on testchip FSFGFS016A. * Outcomes:   + Learnt basic concepts that aid in working process;   + Got familiar with running design kit and working in project. |
| 1. What are the problems encountered this week? Any actions taken? Any help needed?  * Problem encountered:   + Being unfamiliar with the testchip workflow. * Actions taken:   + Went through the flow in [FTV\_ACD\_TestChip\_Flow\_202303](file:///T:\FTV\DSD\DSD_ACD\ACT4\02_Internal_Tech_Shared\03_Testchip\FTV_ACD_TestChip_Flow_202303) under mentor’s guidance. |
| 1. What are the tasks for next week? Any preparation needed in advance?  * Work on assigned project; * Make time for completing items listed in training plan. |
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| Name  (Date) | Mentor | Direct Supervisor |
| Nguyen Le Thao Vy  (2024/01/09) | (Signature/Date) | (Signature/Date) |

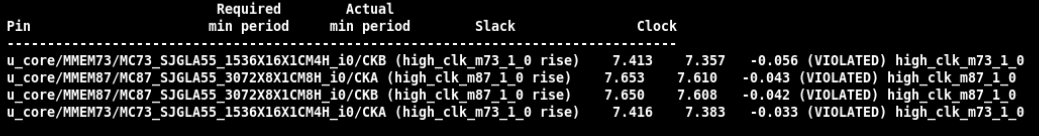
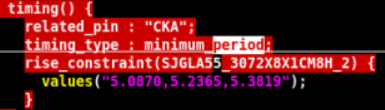
***Questions from previous session***

1. set\_dont\_touch

set\_dont\_touch sets the dont\_touch attribute on cells, nets, designs, and library cells so that they will be ignored when tools try to optimize the design.

**When is the dont\_touch attribute needed?** An instance needs to be set as dont\_touch in case they must not be replaced / modified (i.e. renamed, combined) during optimization. Some scenarios to be considered are listed as follows:

* + Using dont\_touch to maintain hierarchy when doing bottom-up optimization;
  + Using dont\_touch to exclude the pads from being used to optimize the design core logic;
  + …

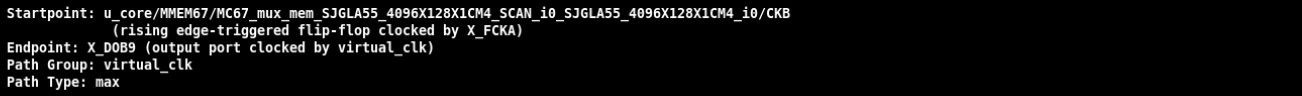
1. Explain the difference between min\_period value in .lib file and actual value obtained in STA.

Timing library / liberty file (.lib) contains timing / power parameters associated with cells inside the standard cell library of a particular technology node. .lib files are provided by standard cell library vendor or foundry, which means that the actual design was not taken into account when generating these values, hence the mismatch between values in .lib and the actual ones.

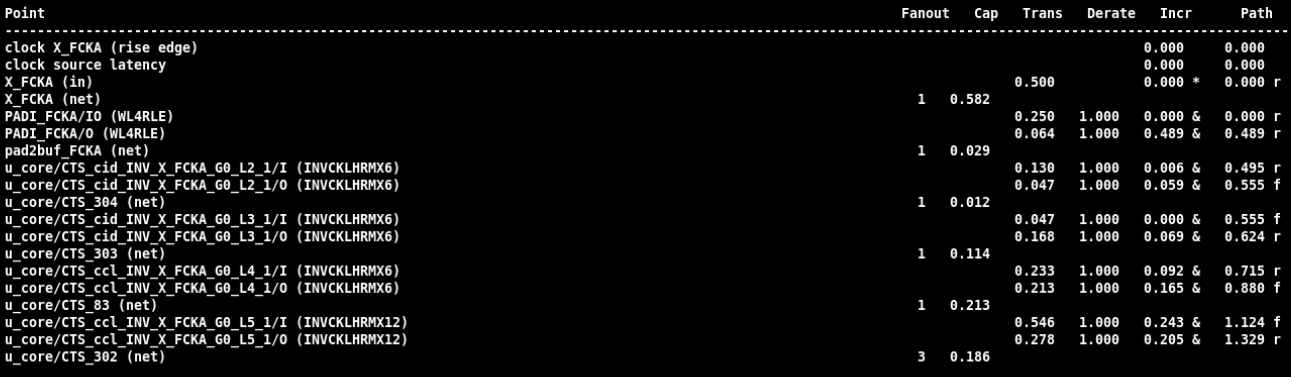
***STA – Timing report***

The report starts by showing:

* Path startpoint: can be clock pin / input port.
* Path endpoint: can be data input pin / output port.
* Path group name: timing analysis, reporting, and optimization are done separately for each path group.
* Path timing check type: “max” = maximum-delay setup check, or “min” = minimum-delay hold check.



Following is a large table showing point-by-point accounting of the delays along the timing path from startpoint to endpoint.



The table has columns labeled as:

* Point(s) = cell pins along the path.
* Fanout = number of inputs that are fed by the output pin.
* Cap = net capacitance value.
* Trans = transition time.
* Derate = derate value apply on the path.
* Incr = incremental contribution to the delay at each point.
* Path = cumulative delay up to that point; “r” and “f” refer to the sense of signal transition, either rising or falling , at that point of the path.

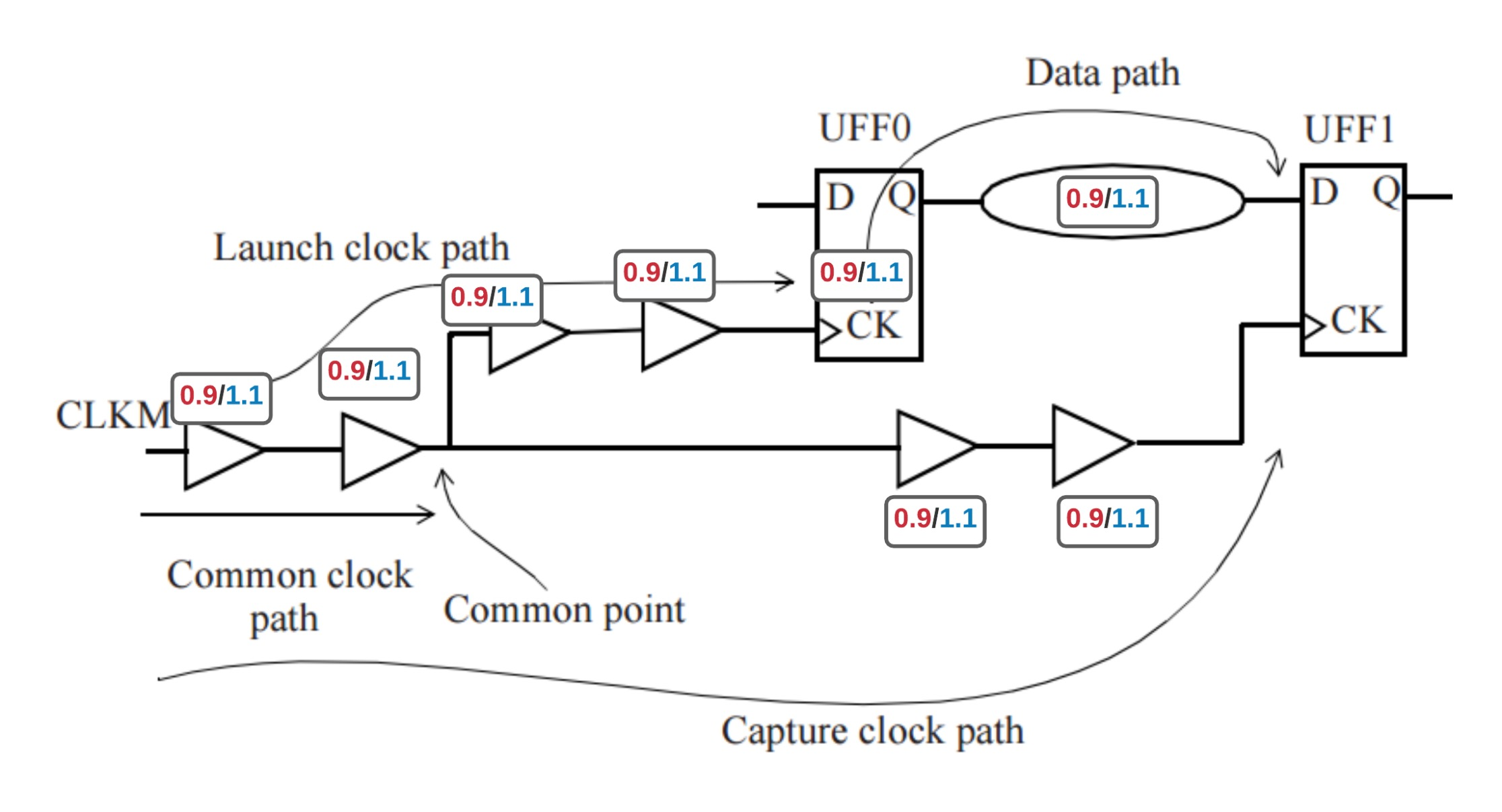
The path starts with the launch clock edge and ends at the data input of capture device. The “data arrival time” shown in the table is the (biggest possible) amount of elapsed time from source of the launch clock edge to the arrival of data at the endpoint.

After this is the accounting for the required arrival time. The “data required time” shown in the table is the latest allowable arrival time for the data at the path endpoint, considering the nominal capture clock edge time, the clock network delay, the clock reconvergence pessimism, and output external delay of the capture device.

At the end, the slack value shown at the end of the report is simply the data required time minus the data arrival time (for setup check, hold check vice versa).

***Example of applying OCV and CPPR***

Given a reg2reg path, in which all cells have a 1ns delay, the clock period is 3.5ns, setup and hold requirement of capture FF are 0.6ns and 0.4ns.

The derating factor applied is 10% 🡪 fastest / best delay value = 0.9ns and slowest / worst delay value = 1.1ns.

**OCV calculation:**

For setup analysis, the time available for data to travel (from launch FF to capture FF) must be larger or equal to the time needed for data to travel. In this case, the worst scenario is slow launch path and fast capture path.

🡪 Setup slack = min capture clock path – max launch clock path

= (3.5 + 0.9 + 0.9 + 0.9 + 0.9 – 0.6) – (1.1 + 1.1 + 1.1 + 1.1 + 1.1 + 1.1) = 6.5 – 6.6 = -0.1

For hold analysis, data must arrive at the capture FF after the hold time window. i.e. the minimum launch path delay must be large enough. The worst scenario is fast launch path and slow capture path.

🡪 Hold slack = min launch clock path – max capture clock path

= (0.9 + 0.9 + 0.9 + 0.9 + 0.9 + 0.9) – (1.1 + 1.1 + 1.1 + 1.1 + 0.4) = 0.6

**CPPR:** Using both min and max delays for same cells (the first two) adds extra / unnecessary pessimisim to the design – which needs to be adjusted / optimized using Common Point Pessimism Removal / Clock Reconvergence Pessimism.

Let the value to be used for common cells is 1.1ns, then the setup slack should become:

Setup slack (revised) = (1.1 + 1.1 + 0.9 + 0.9 + 3.5 – 0.6) – (1.1 \* 6) = 6.9 – 6.6 = 0.3