|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Nguyen Le Thao Vy | No. | 3341 | Div/Dept | DSD/ACD/ACT3 | Job  Date：Jan 09th 2024  Title | Engineer |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | 🗹W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

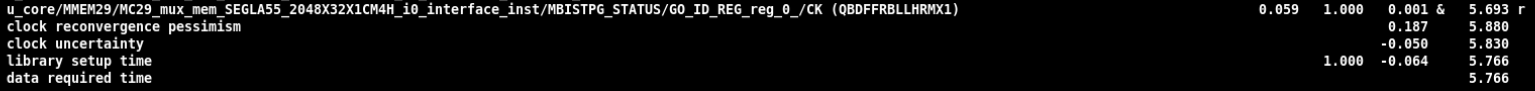
1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed:   All of the tasks I learned during this first week are based on the training plan of 2023, below are a brief description of topics and tasks I was working on:   * Topics of interest:   + Min period / pulsewidth;   + Timescale;   + Simulation - SPICE;   + Testchip workflow. * Tasks that I was working on:   + Read materials – self-learn;   + Work on testchip FSFGFS016A. * Outcomes:   + Learnt basic concepts that aid in working process;   + Got familiar with running design kit and working in project. |
| 1. What are the problems encountered this week? Any actions taken? Any help needed?  * Problem encountered:   + Being unfamiliar with the testchip workflow. * Actions taken:   + Went through the flow in [FTV\_ACD\_TestChip\_Flow\_202303](file:///T:\FTV\DSD\DSD_ACD\ACT4\02_Internal_Tech_Shared\03_Testchip\FTV_ACD_TestChip_Flow_202303) under mentor’s guidance. |
| 1. What are the tasks for next week? Any preparation needed in advance?  * Work on assigned project; * Make time for completing items listed in training plan. |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Nguyen Le Thao Vy  (2024/01/14) | (Signature/Date) | (Signature/Date) |

***Questions from previous session***

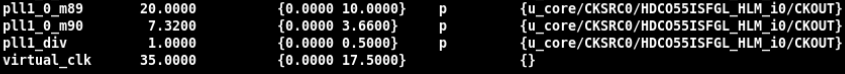
1. CPPR – How to choose max / min delay value to be applied for common cells?

In CPPR, extra pessimism is reduced by adding the CPPR value to min delay path, or subtracting CPPR value from max delay path.

Normally, for setup analysis, tool will add CPPR in required timing path (min path).

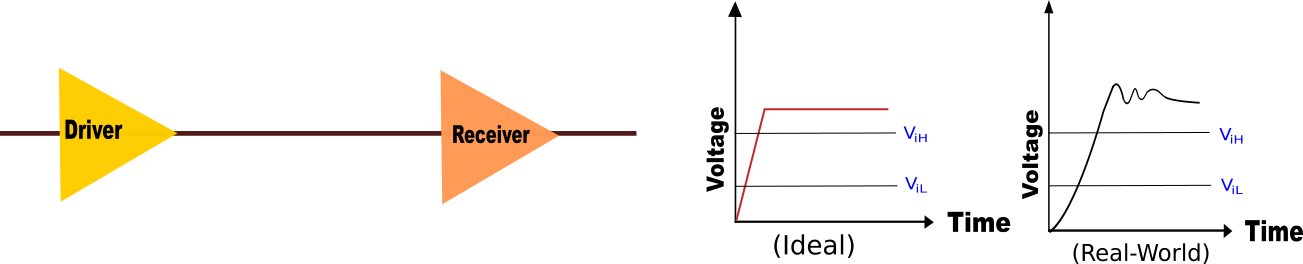
For hold analysis, CPPR is subtracted CPPR from required timing path (max path).

1. Clock network delay / clock source latency

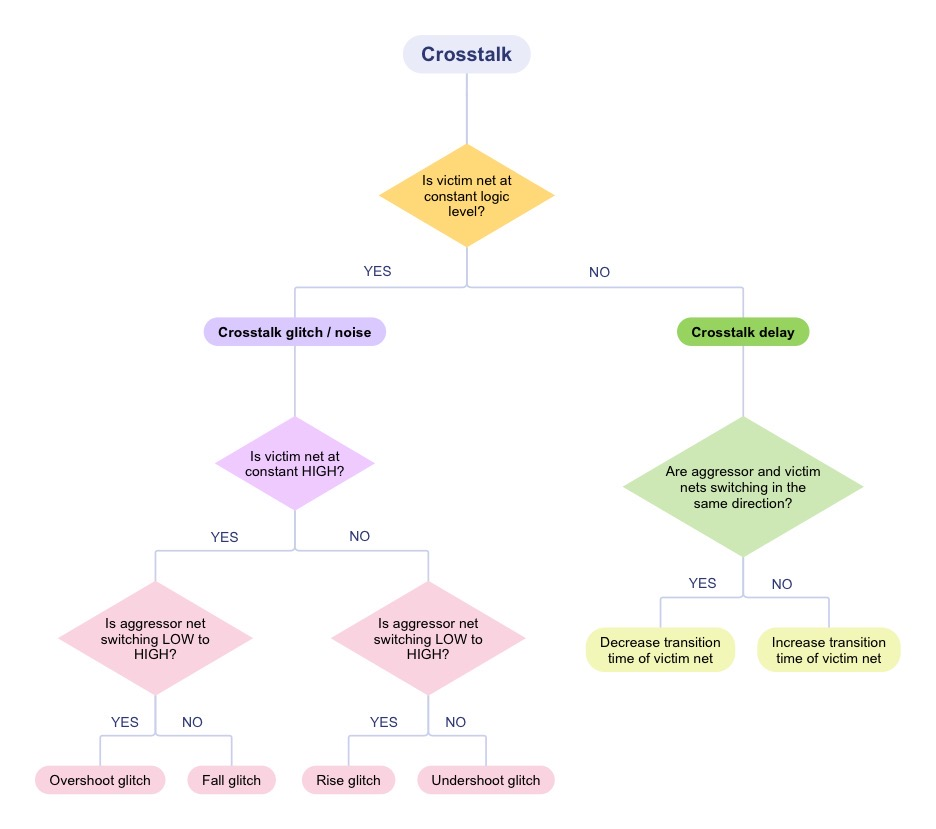
Clock network delay & source latency is equal to 0 because virtual clock is used.

To make virtual clock propagated, the command set\_propagated\_clock [remove\_from\_collection [all\_clocks] [get\_clock virtual\_clk]] can be used.

***Signal integrity***

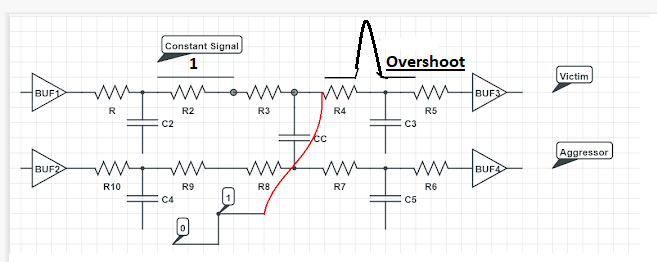
Signal integrity is the ability of an electrical signal to transmit data from one point to another without being corrupted / losing its quality.

In other words, it can be defined as the ability of the signal to carry information reliably and resist the effects of high-frequency electromagnetic interference from nearby signals. Some notable signal integrity –related issues are crosstalk, IR drop,…

**Crosstalk** = undesirable electrical interaction between two or more physically adjacent nets due to capacitive coupling, i.e. signal in one net (“aggressor”) can interfere with the operation of neighboring net(s) (“victim”).

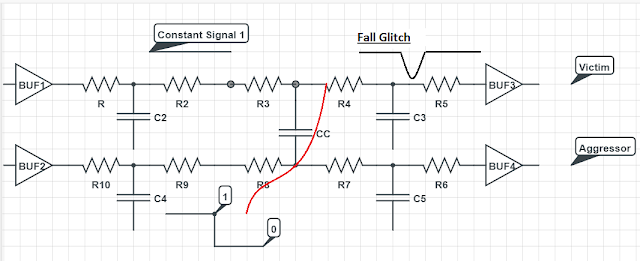
**Crosstalk glitch / noise**

Case 1: Victim net at constant HIGH – Aggressor net is switching LOW to HIGH

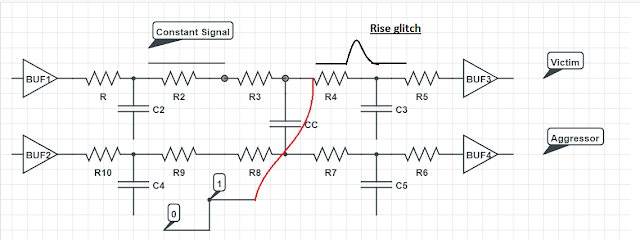


Overshoot glitch refers to victim net voltage being affected to raise above its steady HIGH value.

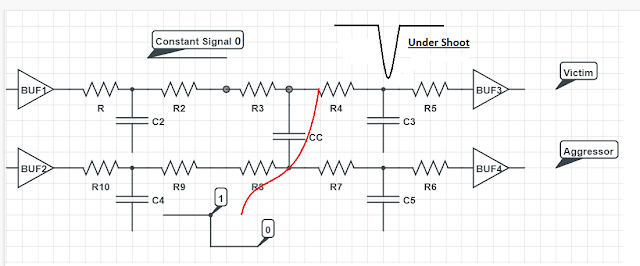
Case 2: Victim net at constant HIGH – Aggressor net is switching HIGH to LOW



Case 3: Victim net at constant LOW – Aggressor net is switching LOW to HIGH



Case 4: Victim net at constant LOW – Aggressor net is switching HIGH to LOW

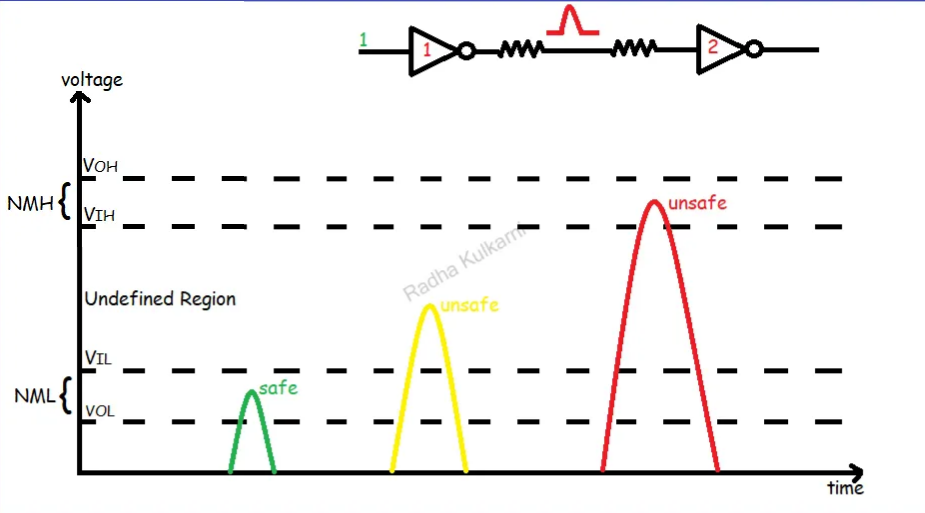


Undershoot glitch refers to victim net voltage being affected to dive below its steady LOW value.

**Effects of crosstalk glitch / noise** depend on 2 factors:

1. Glitch height: Consider two CMOS inverters are connected in series, and let a logic 1 (HIGH) is applied as Vin.

* If, due to crosstalk or other factors, the value of Vin after the first inverting operation falls between VOL and VIL, i.e., in the noise margin low region, the output is considered as safe, and a logic 0 is passed to inverter 2.
* Similarly, if the value of Vin falls between VIH and VOH, i.e., in the noise margin high region, the output is considered as unsafe, and a logic 1 is fed to inverter 2.
* If the value of Vin falls between NMH and NML, i.e., in the undefined region, it is considered as unsafe because Vin can take any value, i.e., logic 1 or 0.



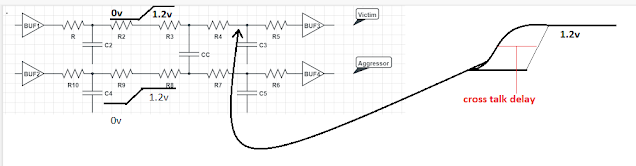
1. The logical connection of victim net

Unsafe case: Reset pins of memory is often at a constant logic value; if such pin’s net experiences an unsafe glitch, the memory might get reset 🡪 loss of data.

Safe case: Consider a two-input AND gate, in which one input is tied to constant LOW; if crosstalk happens at the other input’s net, it will have no impact on the gate’s output.

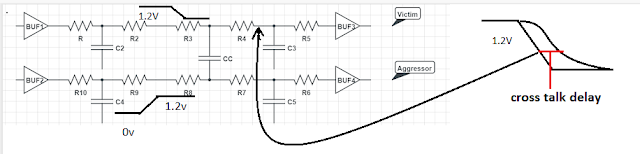
**Crosstalk delay**

Case 5: Victim net is switching in the same direction as Aggressor net



If the aggressor and victim nets are switching in the same direction, it results in a smaller delay for the victim net. The reduction in delay is known as a negative crosstalk delay.

Case 6: Victim net is switching in opposite direction with that of Aggressor net



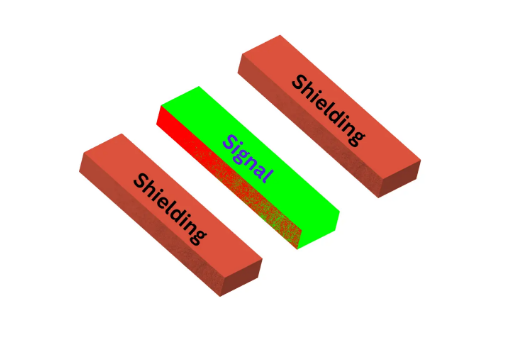
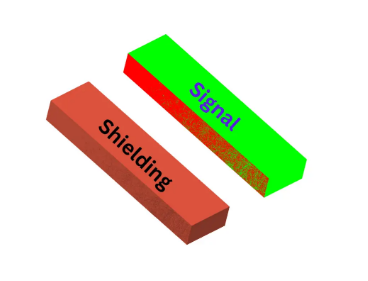
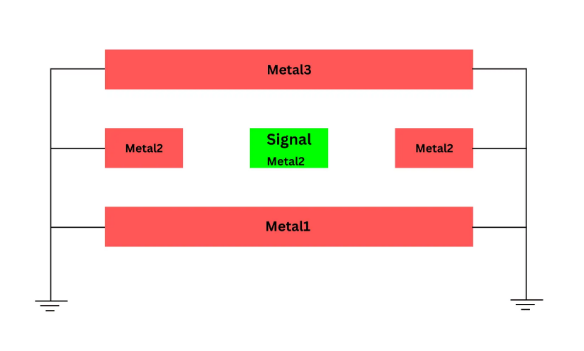
If the aggressor net is switching in the opposite direction of the victim net, it results in a larger delay for the victim net. The increase in delay is known as a positive crosstalk delay.

**Effects of crosstalk delay**

1. Imbalanced clock tree: Crosstalk delay may increase or decrease the delay of clock buffers in the clock path and a balanced clock tree could become imbalanced.
2. Timing violations:
   1. Setup: Crosstalk that leads to an (1) increased delay in data path and/or launch clock path or (2) decreased delay in capture clock path may cause setup violation;
   2. Hold: Crosstalk that leads to a (1) decreased delay in data path and/or launch clock path or (2) increased delay in capture clock path may cause hold violation.

**Reduce crosstalk**

1. Wire spacing: Increase the distance between wires, i.e. more spacing 🡪 less capacitance 🡪 less cross talk.
2. Shielding: In shielding, the victim nets are covered with wider nets called shielding nets – which are directly connected to a strong VDD or GND.

1. Upsize (increase drive strength) the driver of victim net or downsize (decrease drive strength) the driver of the aggressor net.

**IR drop**

IR drop refers to the electrical potential difference / voltage drop between two ends of a conducting wire during current flow, caused by wire resistance and current drawn off from power (Vdd) and ground (GND) grids. If wire resistance is too high or the current passing through the metal layer is larger than predicted, an unacceptable voltage drop may occur, which leads to a decrease in power supply voltage. That means the required power across the design is not reaching to the cells.

When the voltage supplied to a logic cell decreases, that changes its delay. This can result in violations of setup and hold timing and introduce noise in the power supply nets from the on-chip power/ground grid. Timing violations can result in costly down-binning during chip test, degrade performance in the field, or even cause a chip to stop operating properly.

**Types of IR drop**

1. Static: Static IR drop happens when the circuit is not functioning and depends on the resistor-capacitor (RC) network of the power delivery networks (PDN). Gate channel leakage current is mainly responsible for static IR drop.
2. Dynamic: When transistors are switching i.e. the circuit is in functional state, voltage drop in the PDN is known as dynamic IR drop. When the inputs are switching continuously, more current would flow in the instances and also in PDN. Thus, there will be more IR drop in the PDN 🡪 Dynamic IR drop is often higher than static IR drop.