
STM32
CubeMX

1. Description

1.1. Project

Project Name	Robot_Controller_v230514_HMS
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	03/04/2025

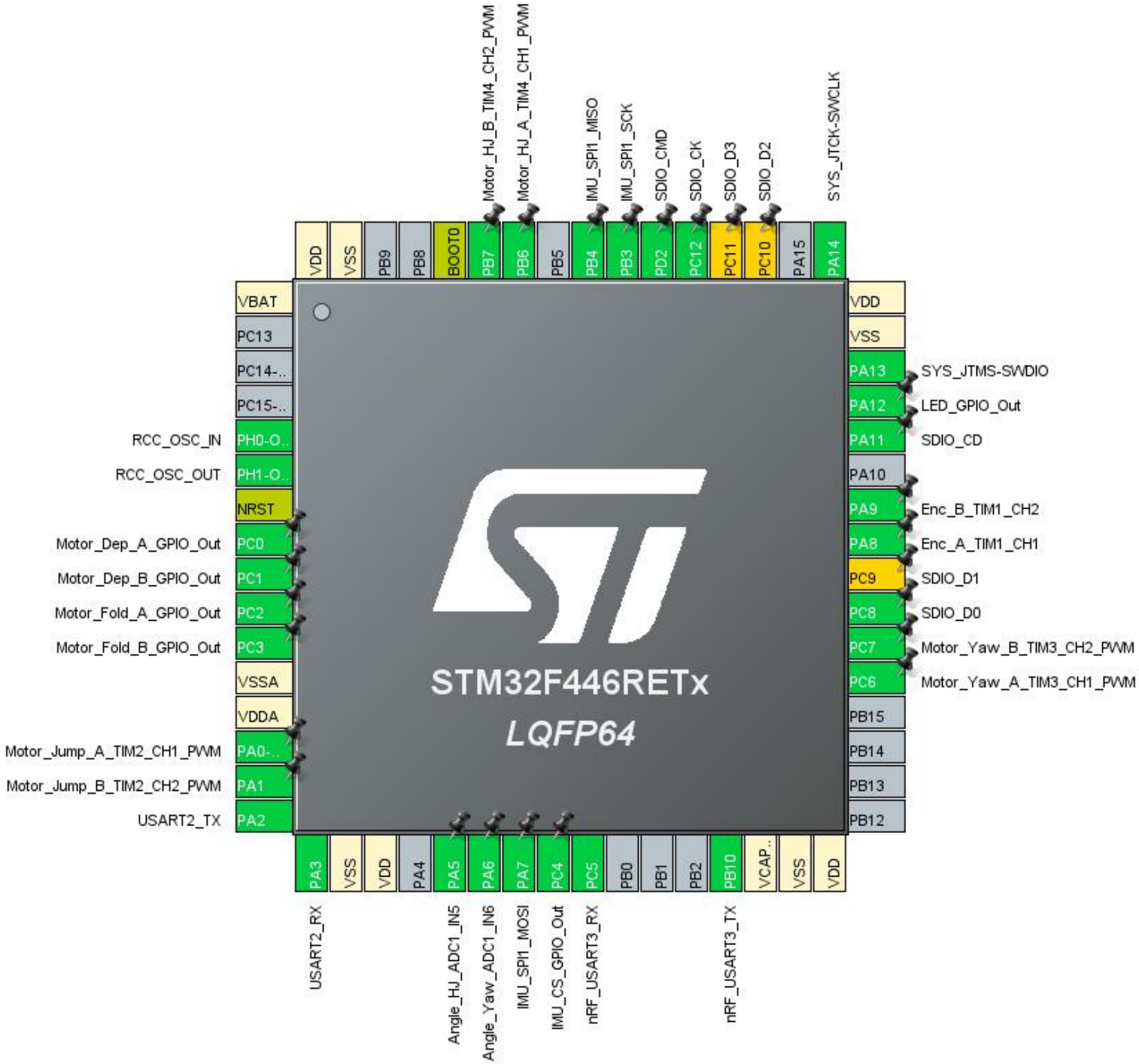
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

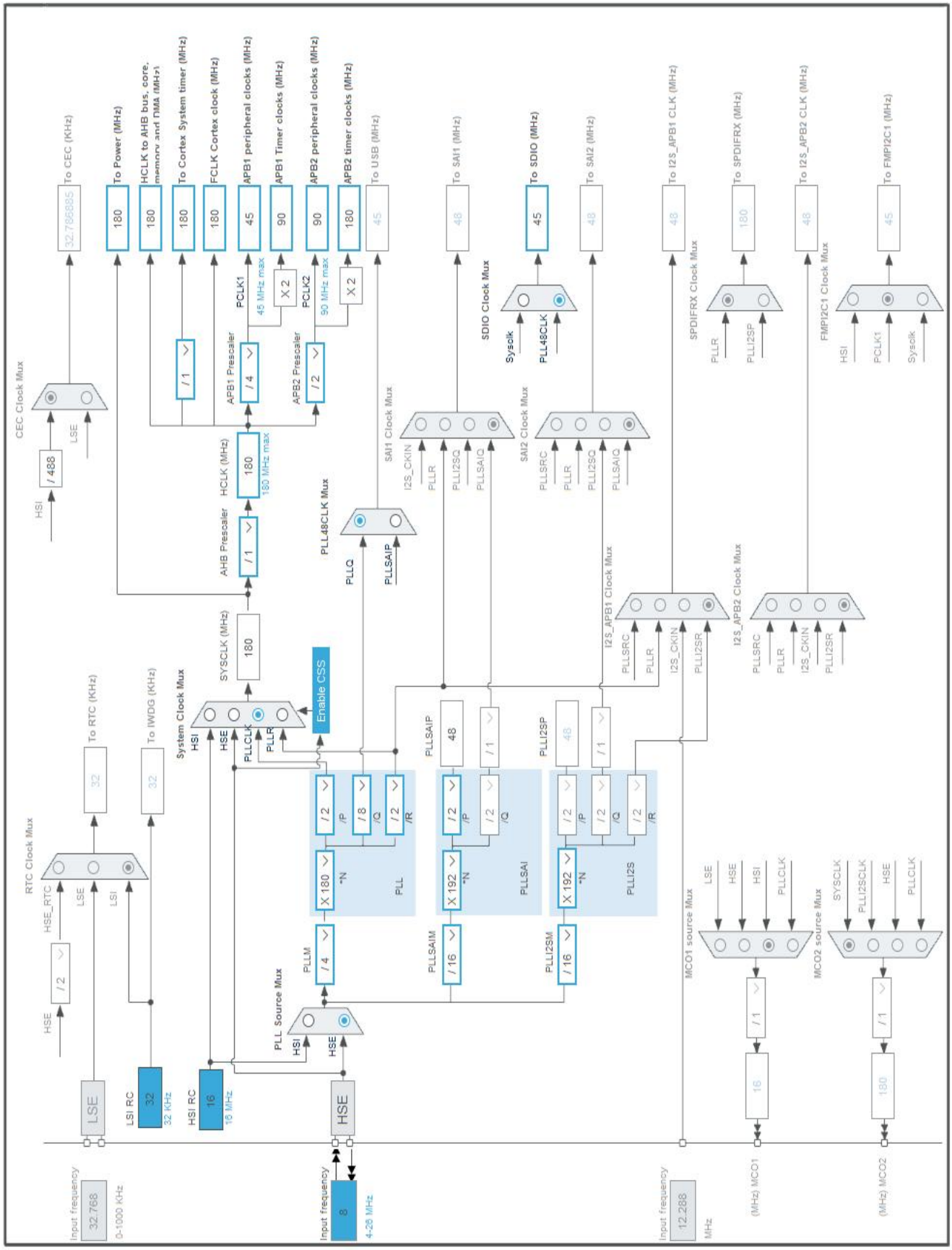
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	Motor_Dep_A_GPIO_Out
9	PC1 *	I/O	GPIO_Output	Motor_Dep_B_GPIO_Out
10	PC2 *	I/O	GPIO_Output	Motor_Fold_A_GPIO_Out
11	PC3 *	I/O	GPIO_Output	Motor_Fold_B_GPIO_Out
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM2_CH1	Motor_Jump_A_TIM2_CH1_PWM
15	PA1	I/O	TIM2_CH2	Motor_Jump_B_TIM2_CH2_PWM
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	ADC1_IN5	Angle_HJ_ADC1_IN5
22	PA6	I/O	ADC1_IN6	Angle_Yaw_ADC1_IN6
23	PA7	I/O	SPI1_MOSI	IMU_SPI1_MOSI
24	PC4 *	I/O	GPIO_Output	IMU_CS_GPIO_Out
25	PC5	I/O	USART3_RX	nRF_USART3_RX
29	PB10	I/O	USART3_TX	nRF_USART3_TX
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
37	PC6	I/O	TIM3_CH1	Motor_Yaw_A_TIM3_CH1_PWM
38	PC7	I/O	TIM3_CH2	Motor_Yaw_B_TIM3_CH2_PWM
39	PC8	I/O	SDIO_D0	
40	PC9 **	I/O	SDIO_D1	
41	PA8	I/O	TIM1_CH1	Enc_A_TIM1_CH1
42	PA9	I/O	TIM1_CH2	Enc_B_TIM1_CH2
44	PA11 *	I/O	GPIO_Input	SDIO_CD

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PA12 *	I/O	GPIO_Output	LED_GPIO_Out
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
51	PC10 **	I/O	SDIO_D2	
52	PC11 **	I/O	SDIO_D3	
53	PC12	I/O	SDIO_CK	
54	PD2	I/O	SDIO_CMD	
55	PB3	I/O	SPI1_SCK	IMU_SPI1_SCK
56	PB4	I/O	SPI1_MISO	IMU_SPI1_MISO
58	PB6	I/O	TIM4_CH1	Motor_HJ_A_TIM4_CH1_PWM
59	PB7	I/O	TIM4_CH2	Motor_HJ_B_TIM4_CH2_PWM
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

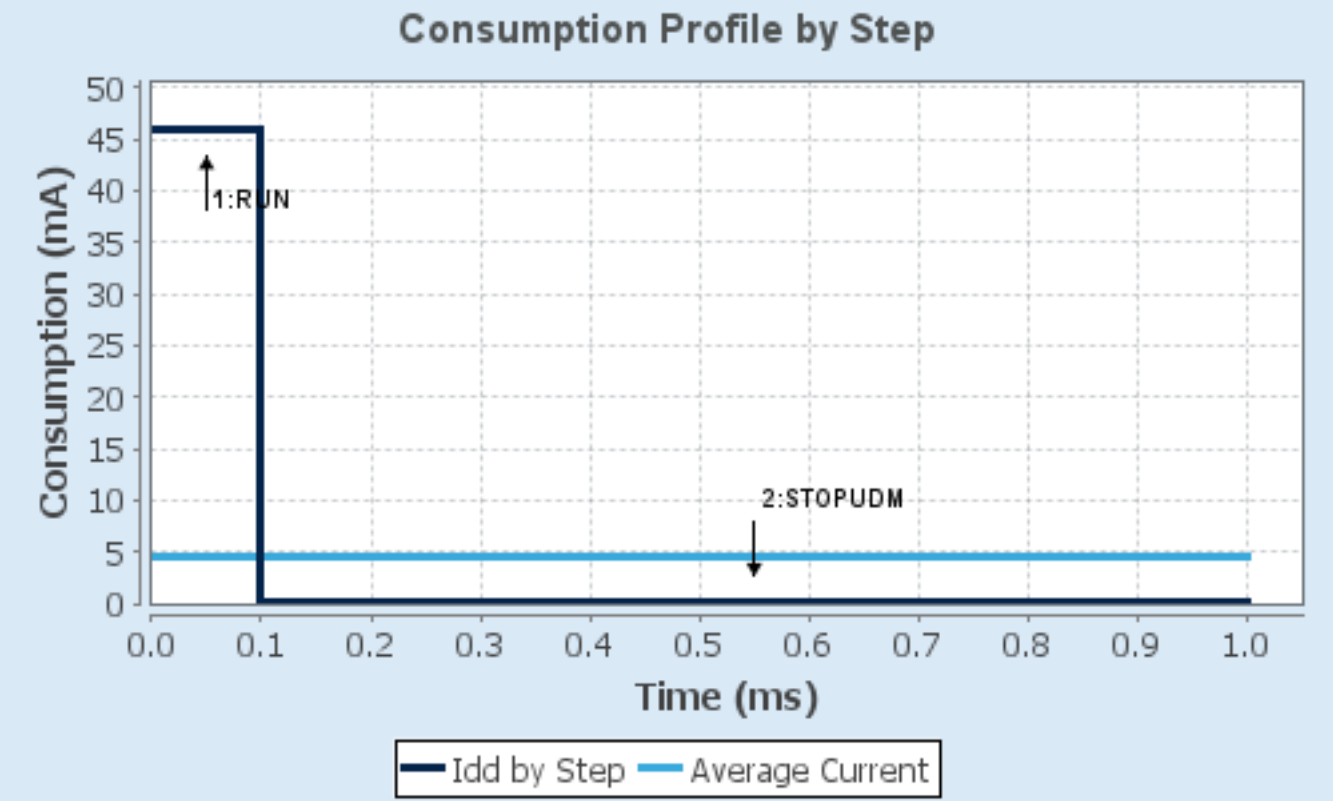
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/PREFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	Robot_Controller_v230514_HMS
Project Folder	H:\OneDrive\bsm\Github\Jump-Glider\2. Software\1. Robot
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x2000
Minimum Stack Size	0x4000

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_USART2_UART_Init	USART2
6	MX_USART3_UART_Init	USART3
7	MX_SDIO_SD_Init	SDIO
8	MX_SPI1_Init	SPI1
9	MX_TIM1_Init	TIM1
10	MX_TIM2_Init	TIM2
11	MX_TIM3_Init	TIM3

Rank	Function Name	Peripheral Instance Name
12	MX_TIM4_Init	TIM4
13	MX_TIM7_Init	TIM7
14	MX_FATFS_Init	FATFS

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN5

mode: IN6

3.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion
ADC_Regular_ConversionMode:	
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	**28 Cycles ***
Rank	**2 ***
Channel	**Channel 6 ***
Sampling Time	**28 Cycles ***
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

3.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

3.3. SDIO

Mode: SD 1 bit

3.3.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

3.4. SPI1

Mode: Full-Duplex Master

3.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***

Baud Rate	**1.40625 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.5. SYS

Debug: Serial Wire

3.6. TIM1

Combined Channels: Encoder Mode

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**34943 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.7. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.8. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2 ***

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.9. TIM4
mode: Clock Source
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2

3.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.10. TIM7

mode: Activated

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**44 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.11. USART2

Mode: Asynchronous

3.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

3.12. USART3

Mode: Asynchronous

3.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

3.13. FATFS

mode: SD Card

3.13.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	**Enabled with static working buffer on the BSS ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	**4096 ***
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

3.13.2. Advanced Settings:

SDIO/SDMMC:

SDIO instance	SDIO
Use dma template	**Enabled ***
BSP code for SD	Generic

3.13.3. Platform Settings:

Detect_SDIO	PA11

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	Angle_HJ_ADC1_IN5
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	Angle_Yaw_ADC1_IN6
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SPI1_MOSI
	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SPI1_SCK
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SPI1_MISO
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Enc_A_TIM1_CH1
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Enc_B_TIM1_CH2
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_Jump_A_TIM2_CH1_PWM
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_Jump_B_TIM2_CH2_PWM
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_Yaw_A_TIM3_CH1_PWM
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_Yaw_B_TIM3_CH2_PWM
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_HJ_A_TIM4_CH1_PWM
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_HJ_B_TIM4_CH2_PWM
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART3	PC5	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	nRF_USART3_RX
	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	nRF_USART3_TX
Single Mapped Signals	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_Dep_A_GPIO_Out
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_Dep_B_GPIO_Out
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_Fold_A_GPIO_Out
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_Fold_B_GPIO_Out
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	IMU_CS_GPIO_Out
	PA11	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	SDIO_CD
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GPIO_Out

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
SDIO_RX	DMA2_Stream6	Peripheral To Memory	Low
SDIO_TX	DMA2_Stream3	Memory To Peripheral	Low
SPI1_RX	DMA2_Stream2	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SDIO_RX: DMA2_Stream6 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SDIO_TX: DMA2_Stream3 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SPI1_RX: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
SDIO global interrupt	true	0	0
TIM7 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 stream1 global interrupt	unused		
DMA1 stream3 global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
DMA2 stream0 global interrupt	unused		
DMA2 stream2 global interrupt	unused		
FPU global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler

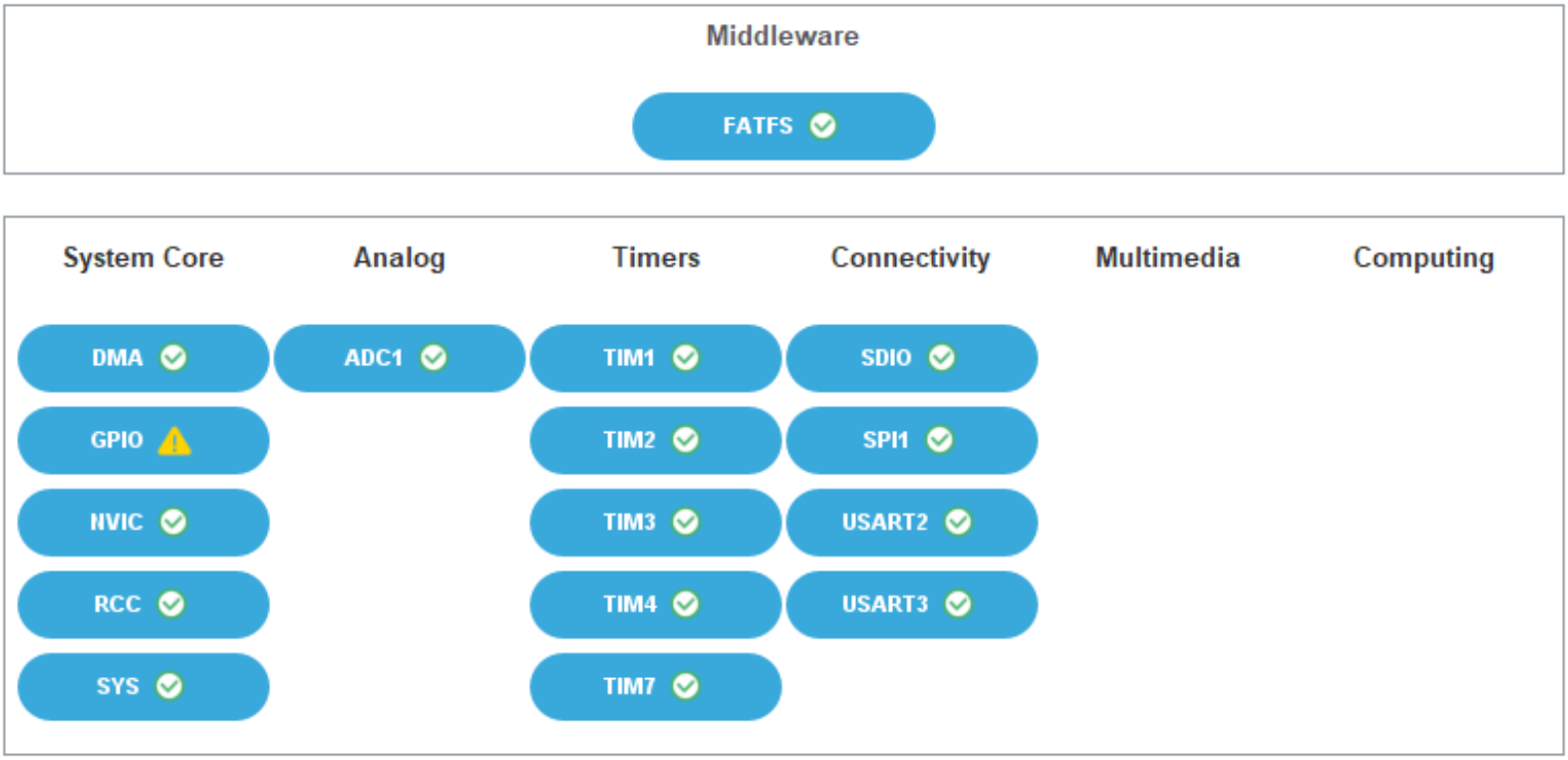
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
SDIO global interrupt	false	true	true
TIM7 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f4-svd.zip
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