

1. Description

1.1. Project

Project Name	Biarticular_Jumper_Main_Controller
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	03/04/2025

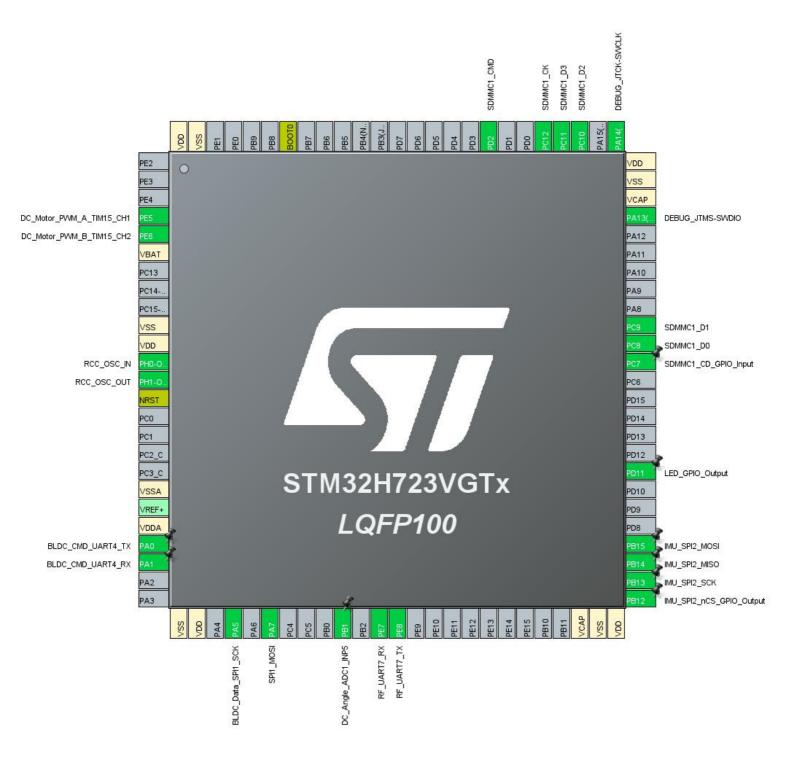
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



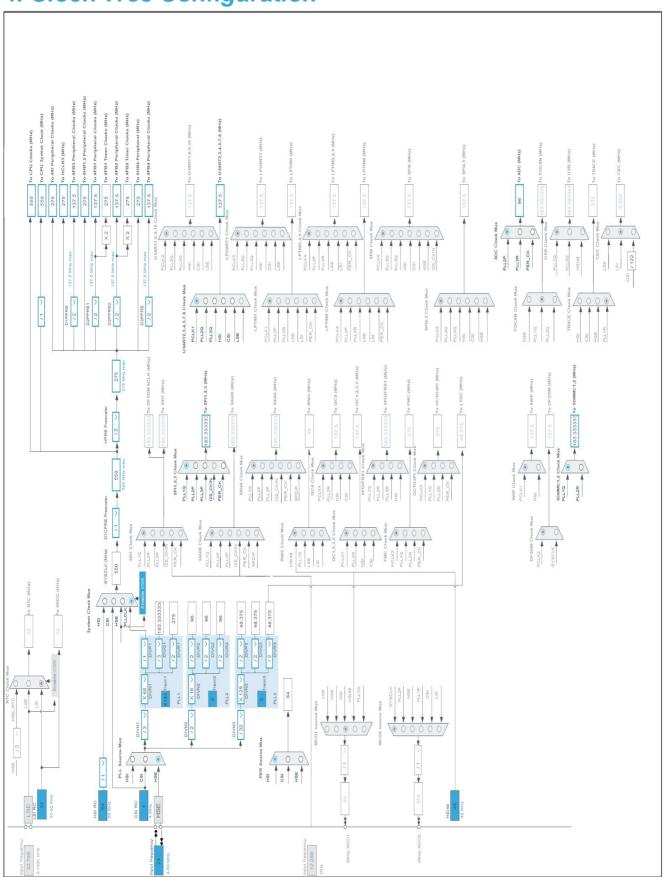
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after	Pin Type	Alternate Function(s)	Label
LQFF100	reset)		Function(s)	
4	PE5	I/O	TIM15_CH1	DC_Motor_PWM_A_TIM15_ CH1
5	PE6	I/O	TIM15_CH2	DC_Motor_PWM_B_TIM15_ CH2
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	UART4_TX	BLDC_CMD_UART4_TX
23	PA1	I/O	UART4_RX	BLDC_CMD_UART4_RX
26	VSS	Power		
27	VDD	Power		
29	PA5	I/O	SPI1_SCK	BLDC_Data_SPI1_SCK
31	PA7	I/O	SPI1_MOSI	
35	PB1	I/O	ADC1_INP5	DC_Angle_ADC1_INP5
37	PE7	I/O	UART7_RX	RF_UART7_RX
38	PE8	I/O	UART7_TX	RF_UART7_TX
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	IMU_SPI2_nCS_GPIO_Out put
52	PB13	I/O	SPI2_SCK	IMU_SPI2_SCK
53	PB14	I/O	SPI2_MISO	IMU_SPI2_MISO
54	PB15	I/O	SPI2_MOSI	IMU_SPI2_MOSI
58	PD11 *	I/O	GPIO_Output	LED_GPIO_Output
64	PC7 *	I/O	GPIO_Input	SDMMC1_CD_GPIO_Input
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	SDMMC1_D1	
72	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
	·			

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
75	VDD	Power		
76	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
78	PC10	I/O	SDMMC1_D2	
79	PC11	I/O	SDMMC1_D3	
80	PC12	I/O	SDMMC1_CK	
83	PD2	I/O	SDMMC1_CMD	
94	воото	Boot		
99	VSS	Power		
100	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
мси	STM32H723VGTx
Datasheet	DS13313_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

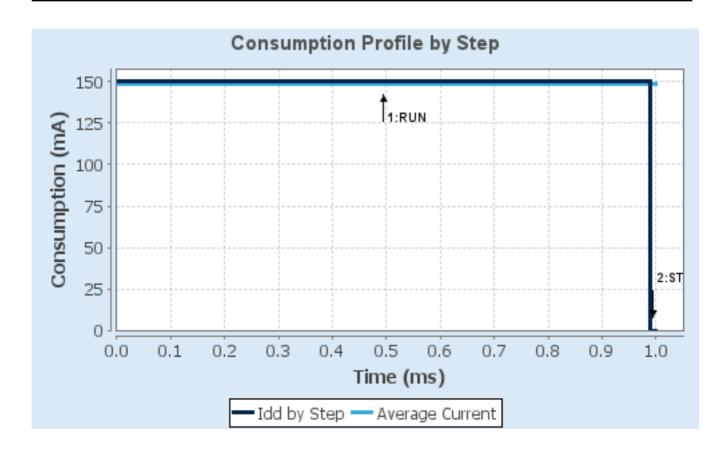
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-	NA
	ON/Cache	
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	96 µA
Duration	0.99 ms	0.01 ms
DMIPS	1177.0	0.0
Ta Max	102.72	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	148.5 mA
Battery Life	4 hours	Average DMIPS	1177.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Biarticular_Jumper_Main_Controller_H7
Project Folder	H:\OneDrive\bsm\Github\Biarticular-jumper\2. Software\1. Robot Controller\0.
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x300
Minimum Stack Size	0x500

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM7_Init	TIM7
5	MX_TIM5_Init	TIM5
6	MX_UART4_Init	UART4
7	MX_SPI2_Init	SPI2
8	MX_UART7_Init	UART7
9	MX_SDMMC1_SD_Init	SDMMC1
10	MX_FATFS_Init	FATFS
11	MX_TIM15_Init	TIM15

Rank	Function Name	Peripheral Instance Name
12	MX_SPI1_Init	SPI1
13	MX ADC1 Init	ADC1

3. Peripherals and Middlewares Configuration

3.1. ADC1

IN5: IN5 Single-ended

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 16-bit resolution

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular ConversionsEnableEnable Regular OversamplingDisableOversampling Ratio1Number Of Conversion1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

ChannelChannel 5Sampling Time1.5 CyclesOffset NumberNo offsetOffset Signed SaturationDisable

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

3.2. CORTEX_M7

3.2.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode Enabled *

Cortex Interface Settings:

CPU ICache Disabled **CPU DCache** Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault,

level 0

NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled MPU Region Base Address 0x0 * MPU Region Size 4GB MPU SubRegion Disable 0x87 * MPU TEX field level

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE **ENABLE** MPU Shareability Permission MPU Cacheable Permission **DISABLE** MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 1 Settings: MPU Region

Cortex Memory Protection Unit Region 2 Settings:

Disabled MPU Region

Cortex Memory Protection Unit Region 3 Settings: MPU Region

Cortex Memory Protection Unit Region 4 Settings:

Disabled MPU Region

Cortex Memory Protection Unit Region 5 Settings: MPU Region

Cortex Memory Protection Unit Region 6 Settings:

Disabled MPU Region

Cortex Memory Protection Unit Region 7 Settings:

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled **Cortex Memory Protection Unit Region 9 Settings:**

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

3.3. DEBUG

Debug: Serial Wire

3.4. MEMORYMAP

mode: Activated

3.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.5.1. Parameter Settings:

Power Parameters:

SupplySource PWR_LDO_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 16
HSI Calibration Value 64

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 3 WS (4 CPU cycle)

PLL range Parameters:

PLL1 input frequency range

Between 8 and 16 MHz

PLL2 input frequency range

Between 8 and 16 MHz

PLL1 clock Output range

Wide VCO range

PLL2 clock Output range Wide VCO range

3.6. SDMMC1

Mode: SD 4 bits Wide bus

3.6.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made Rising transition

SDMMC Clock output enable when the bus is idle

Disable the power save for the clock

SDMMC hardware flow control

The hardware control flow is disabled

SDMMC clock divide factor 5 *
Is external transceiver present ? no

3.7. SPI1

Mode: Receive Only Slave

3.7.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

Fifo Threshold 01 Data

Tx Crc Initialization PatternAll Zero PatternRx Crc Initialization PatternAll Zero PatternNss PolarityNss Polarity Low

Master Ss Idleness 00 Cycle
Master Inter Data Idleness 00 Cycle

Master Receiver Auto Susp Disable

Master Keep Io State Disable

IO Swap Disabled

3.8. SPI2

Mode: Full-Duplex Master

3.8.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 32 *

Baud Rate 5.729166 MBits/s *

Clock Polarity (CPOL) High *
Clock Phase (CPHA) 2 Edge *

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

Fifo Threshold Fifo Threshold 01 Data

Tx Crc Initialization Pattern All Zero Pattern

Rx Crc Initialization Pattern All Zero Pattern

Nss Polarity Nss Polarity Low

Master Ss Idleness00 CycleMaster Inter Data Idleness00 CycleMaster Receiver Auto SuspDisable

Master Keep Io State Disable

IO Swap Disabled

3.9. SYS

Timebase Source: SysTick

3.10. TIM5

Clock Source: Internal Clock

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 274 *
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 999999999 *

Internal Clock Division (CKD) No Division

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

3.11. TIM7

mode: Activated

3.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 54 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 9999 *

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx_EGR)

3.12. TIM15

mode: Clock Source

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

10 *

Up

499 *

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

3.13. UART4

Mode: Asynchronous

3.13.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable **Data Inversion** TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

3.14. UART7

Mode: Asynchronous

3.14.1. Parameter Settings:

Basic Parameters:

Baud Rate 9600 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.15. FATFS

mode: SD Card

3.15.1. Set Defines:

Version:

FATFS version R0.12c

Function Parameters:

FS_READONLY (Read-only mode) Disabled
FS_MINIMIZE (Minimization level) Disabled

USE_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE_FIND (Find functions)

USE_MKFS (Make filesystem function)

USE_FASTSEEK (Fast seek function)

USE_EXPAND (Use f_expand function)

USE_CHMOD (Change attributes function)

Disabled

USE_LABEL (Volume label functions)

Disabled

USE_FORWARD (Forward function)

Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)

USE_LFN (Use Long Filename)

MAX_LFN (Max Long Filename)

255

LFN_UNICODE (Enable Unicode)

STRF_ENCODE (Character encoding)

UTF-8

FS_RPATH (Relative Path)

Disabled

Physical Drive Parameters:

VOLUMES (Logical drives) 1

MAX_SS (Maximum Sector Size) 512

MIN_SS (Minimum Sector Size) 512

MULTI_PARTITION (Volume partitions feature) Disabled

USE_TRIM (Erase feature) Disabled

FS_NOFSINFO (Force full FAT scan) 0

System Parameters:

FS_TINY (Tiny mode) Disabled
FS_EXFAT (Support of exFAT file system) Disabled

FS_NORTC (Timestamp feature) Dynamic timestamp

FS_REENTRANT (Re-Entrancy) Disabled
FS_TIMEOUT (Timeout ticks) 1000
FS_LOCK (Number of files opened simultaneously) 2

3.15.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance SDMMC1
Use dma template Disabled
BSP code for SD Generic

3.15.3. Platform Settings:

Detect_SDIO PC7

^{*} User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
ADC1	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	DC_Angle_ADC1_INP5
DEBUG	PA13(JTMS/ SWDIO)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14(JTCK/ SWCLK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Data_SPI1_SCK
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	IMU_SPI2_SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	IMU_SPI2_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	IMU_SPI2_MOSI
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DC_Motor_PWM_A_TIM1 5_CH1
	PE6	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DC_Motor_PWM_B_TIM1 5_CH2
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_CMD_UART4_TX
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_CMD_UART4_RX
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	RF_UART7_RX
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	RF_UART7_TX
GPIO	PB12	GPIO_Output	Output Push Pull	Pull-up *	Low	IMU_SPI2_nCS_GPIO_Ou tput
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GPIO_Output
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SDMMC1_CD_GPIO_Inpu t

	Configuration Report
Daga 22	

Biarticular_Jumper_Main_Controller_H7 Project

4.2. DMA configuration

DMA request	Stream	Direction	Priority
UART7_RX	DMA2_Stream0	Peripheral To Memory	Low
UART7_TX	DMA2_Stream1	Memory To Peripheral	Low
UART4_TX	DMA1_Stream4	Memory To Peripheral	Low
SPI1_RX	DMA1_Stream2	Peripheral To Memory	Low

UART7_RX: DMA2_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

UART7_TX: DMA2_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

UART4_TX: DMA1_Stream4 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

SPI1_RX: DMA1_Stream2 DMA request Settings:

Mode: Circular *
Use fifo: Disable

Peripheral Increment: Disable

Memory Increment: Enable *

Peripheral Data Width: Byte

Memory Data Width: Byte

4.3. BDMA configuration

nothing configured in DMA service

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
SPI1 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
TIM7 global interrupt	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 stream2 global interrupt	unused		
DMA1 stream4 global interrupt	unused		
ADC1 and ADC2 global interrupts		unused	
SPI2 global interrupt		unused	
SDMMC1 global interrupt		unused	
UART4 global interrupt		unused	
DMA2 stream0 global interrupt		unused	
DMA2 stream1 global interrupt		unused	
FPU global interrupt		unused	
UART7 global interrupt		unused	
TIM15 global interrupt		unused	
HSEM1 global interrupt		unused	

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

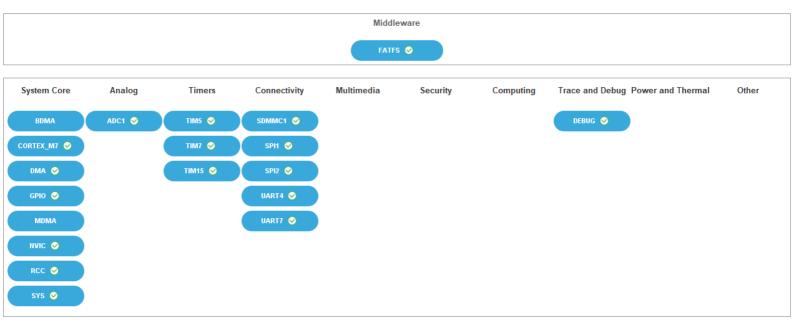
Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
SPI1 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
TIM7 global interrupt	false	true	true

^{*} User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers_st

m32h7_series_product_overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_stm8_functi

onal-safety-packages.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_software_development_tools.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers_st

m32h72x-3x_line_product-overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32-family-overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32h7rs-lines-overview.pdf

Brochures https://www.st.com/resource/en/brochure/brstm32h7.pdf

Brochures https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-

and-smart-i-os.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers https://www.st.com/resource/en/flyer/flstm32h7rs.pdf

Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2606-stm32-

- microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
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