
STM32
CubeMX

1. Description

1.1. Project

Project Name	Biarticular_Jumper_BLDC_Driver_H7
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	03/04/2025

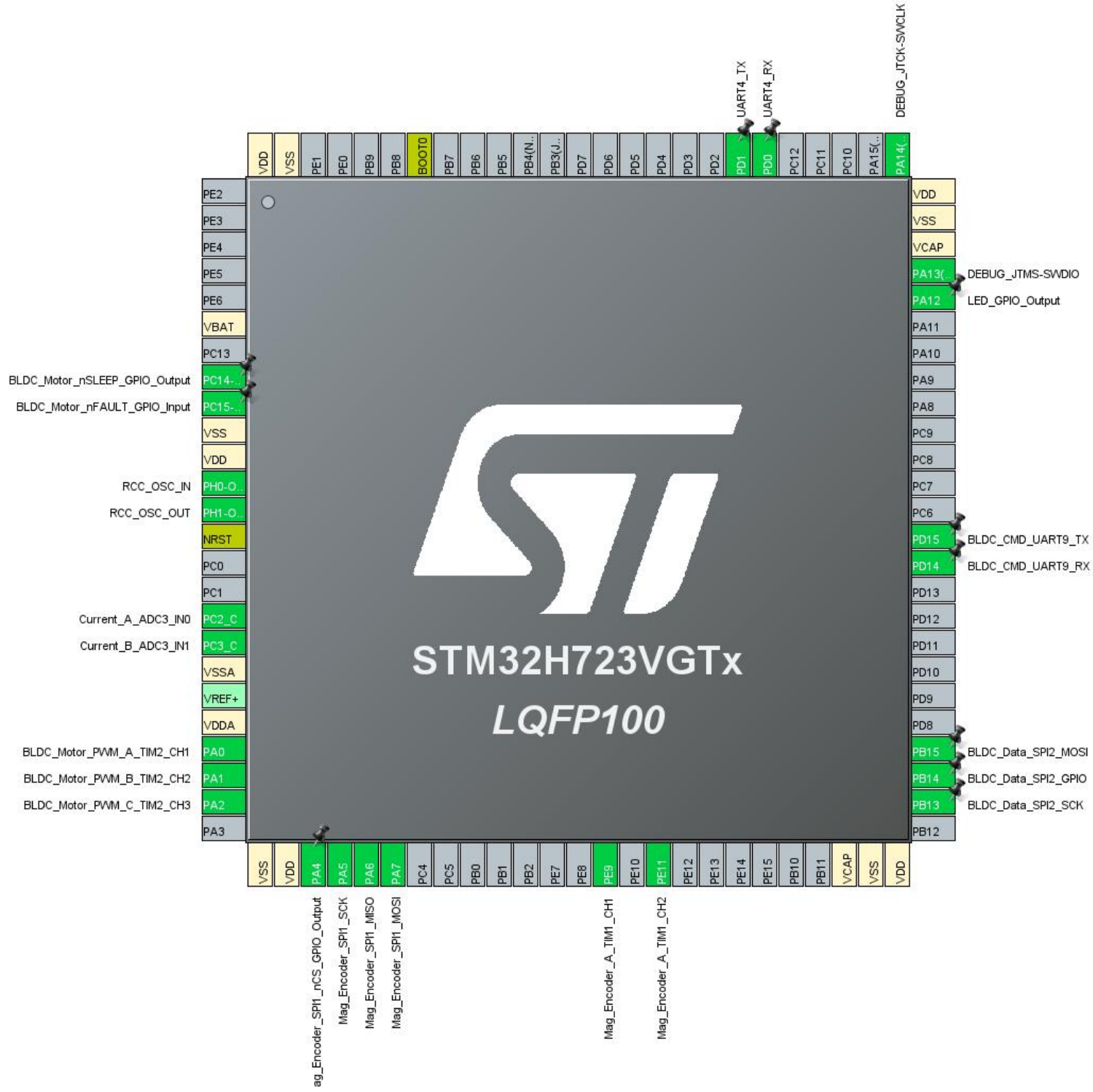
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



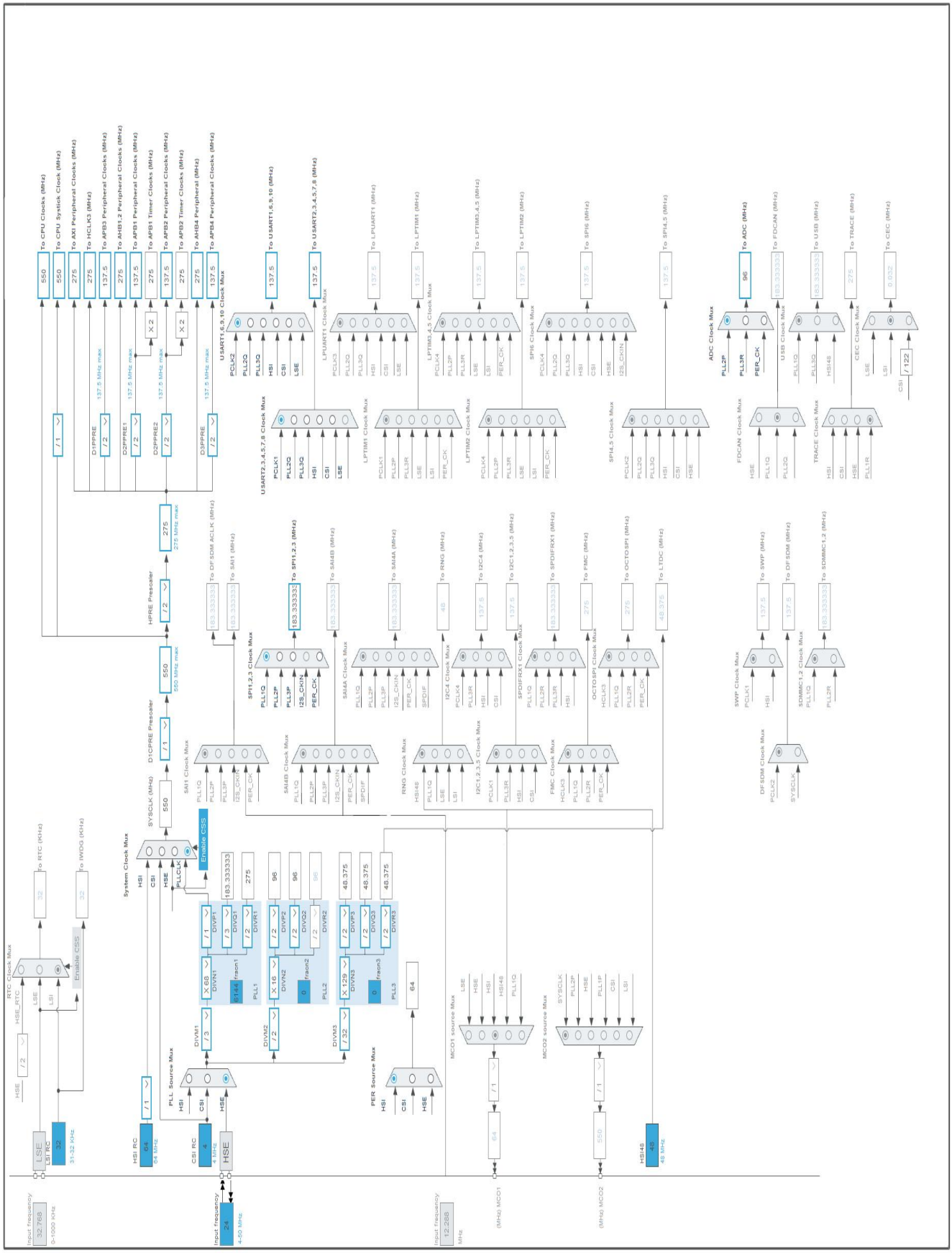
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN *	I/O	GPIO_Output	BLDC_Motor_nSLEEP_GPIO_Output
9	PC15-OSC32_OUT *	I/O	GPIO_Input	BLDC_Motor_nFAULT_GPIO_Input
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
17	PC2_C	I/O	ADC3_INP0	Current_A_ADC3_IN0
18	PC3_C	I/O	ADC3_INP1	Current_B_ADC3_IN1
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	TIM2_CH1	BLDC_Motor_PWM_A_TIM2_CH1
23	PA1	I/O	TIM2_CH2	BLDC_Motor_PWM_B_TIM2_CH2
24	PA2	I/O	TIM2_CH3	BLDC_Motor_PWM_C_TIM2_CH3
26	VSS	Power		
27	VDD	Power		
28	PA4 *	I/O	GPIO_Output	Mag_Encoder_SPI1_nCS_GPIO_Output
29	PA5	I/O	SPI1_SCK	Mag_Encoder_SPI1_SCK
30	PA6	I/O	SPI1_MISO	Mag_Encoder_SPI1_MISO
31	PA7	I/O	SPI1_MOSI	Mag_Encoder_SPI1_MOSI
39	PE9	I/O	TIM1_CH1	Mag_Encoder_A_TIM1_CH1
41	PE11	I/O	TIM1_CH2	Mag_Encoder_A_TIM1_CH2
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
52	PB13	I/O	SPI2_SCK	BLDC_Data_SPI2_SCK
53	PB14 *	I/O	GPIO_Output	BLDC_Data_SPI2_GPIO
54	PB15	I/O	SPI2_MOSI	BLDC_Data_SPI2_MOSI

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	PD14	I/O	UART9_RX	BLDC_CMD_UART9_RX
62	PD15	I/O	UART9_TX	BLDC_CMD_UART9_TX
71	PA12 *	I/O	GPIO_Output	LED_GPIO_Output
72	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
81	PD0	I/O	UART4_RX	
82	PD1	I/O	UART4_TX	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723VGTx
Datasheet	DS13313_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

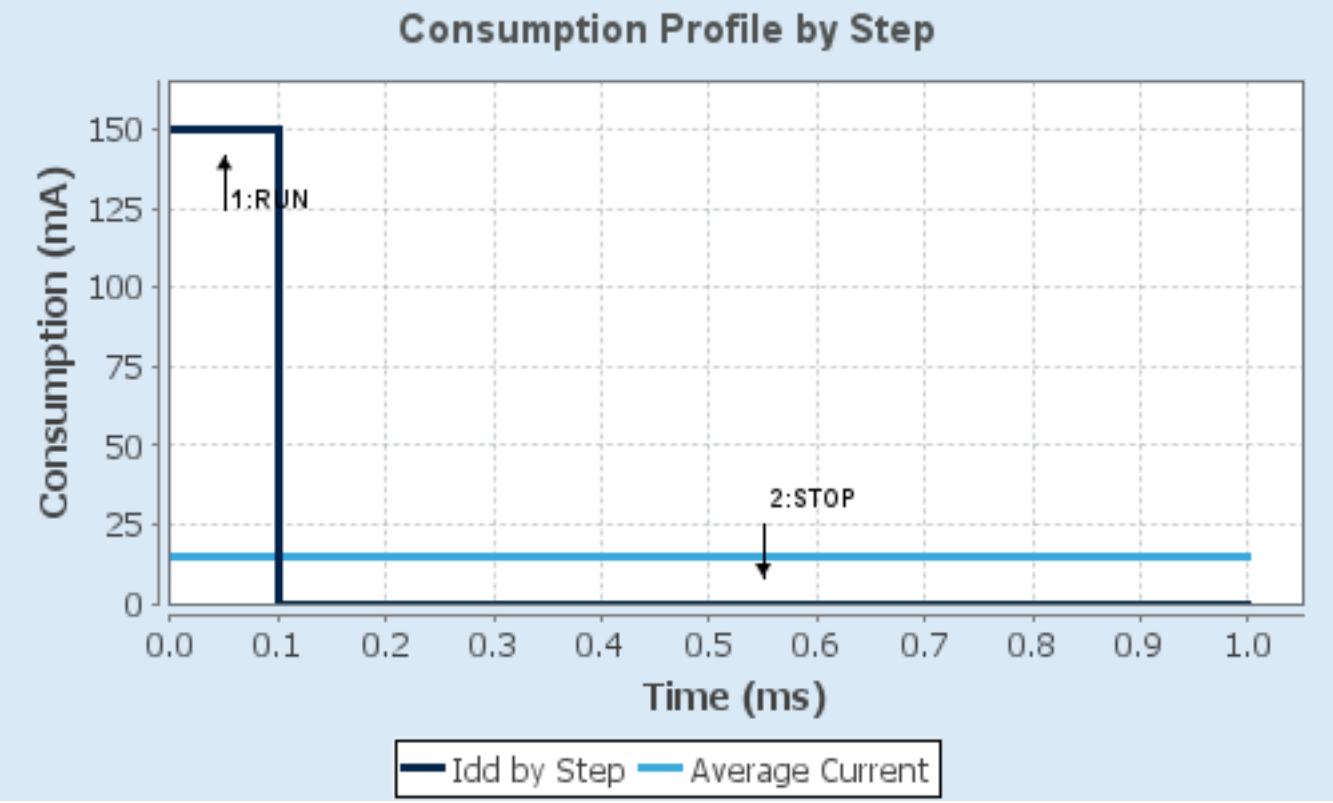
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS_OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	104.75	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	Biarticular_Jumper_BLDC_Driver_H7
Project Folder	H:\OneDrive\bsm\Github\Biarticular-jumper\2. Software\1. Robot Controller\0.
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_SPI2_Init	SPI2
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2
7	MX_TIM7_Init	TIM7
8	MX_TIM4_Init	TIM4
9	MX_UART4_Init	UART4
10	MX_SPI1_Init	SPI1
11	MX_ADC3_Init	ADC3

Rank	Function Name	Peripheral Instance Name
12	MX_TIM5_Init	TIM5
13	MX_UART9_Init	UART9

3. Peripherals and Middlewares Configuration

3.1. ADC3

mode: IN0

IN1: IN1 Single-ended

3.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 8-bit resolution ***
Scan Conversion Mode	Enabled
Data Alignment	Right alignment
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	Oversampling ratio 2x
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Sampling Mode	Normal
Rank	1
Channel	Channel 0
Sampling Time	2.5 Cycles
Offset Number	No offset
Offset Sign	Offset Sign Negative
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	2.5 Cycles
Offset Number	No offset
Offset Sign	Offset Sign Negative
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

3.2. CORTEX_M7

3.2.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode	**Enabled ***

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled
MPU Region Base Address	**0x0 ***
MPU Region Size	4GB
MPU SubRegion Disable	**0x87 ***
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	DISABLE
MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

3.3. DEBUG

Debug: Serial Wire

3.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.4.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

3.5. SPI1

Mode: Full-Duplex Master

3.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**2.864583 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.6. SPI2

Mode: Transmit Only Master

3.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**2.864583 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.7. SYS

Timebase Source: SysTick

3.8. TIM1

Combined Channels: Encoder Mode

3.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**3999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.9. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

3.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 32 bits value)	**499 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.10. TIM4

Clock Source : Internal Clock

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**254 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

3.11. TIM5

Clock Source : Internal Clock

3.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**274 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**999999999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

3.12. TIM7

mode: Activated

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2749 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.13. UART4

Mode: Asynchronous

3.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.14. UART9

Mode: Asynchronous

3.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	Current_A_ADC3_IN0
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	Current_B_ADC3_IN1
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_SPI1_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_SPI1_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_SPI1_MOSI
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Data_SPI2_SCK
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Data_SPI2_MOSI
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_A_TIM1_CH1
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_A_TIM1_CH2
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Motor_PWM_A_TIM2_CH1
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Motor_PWM_B_TIM2_CH2
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_Motor_PWM_C_TIM2_CH3
UART4	PD0	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART9	PD14	UART9_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_CMD_UART9_RX
	PD15	UART9_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLDC_CMD_UART9_TX
GPIO	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BLDC_Motor_nSLEEP_GPIO_Output
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BLDC_Motor_nFAULT_GPIO_Input
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Mag_Encoder_SPI1_nCS_GPIO_Output
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BLDC_Data_SPI2_GPIO
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GPIO_Output

4.2. DMA configuration

DMA request	Stream	Direction	Priority
UART9_RX	DMA2_Stream0	Peripheral To Memory	Low
ADC3	DMA1_Stream0	Peripheral To Memory	Low
SPI2_TX	DMA1_Stream2	Memory To Peripheral	Low

UART9_RX: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC3: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI2_TX: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

4.3. BDMA configuration

nothing configured in DMA service

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
TIM4 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
TIM7 global interrupt	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 stream0 global interrupt	unused		
DMA1 stream2 global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
SPI1 global interrupt	unused		
UART4 global interrupt	unused		
DMA2 stream0 global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
UART9 global interrupt	unused		

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

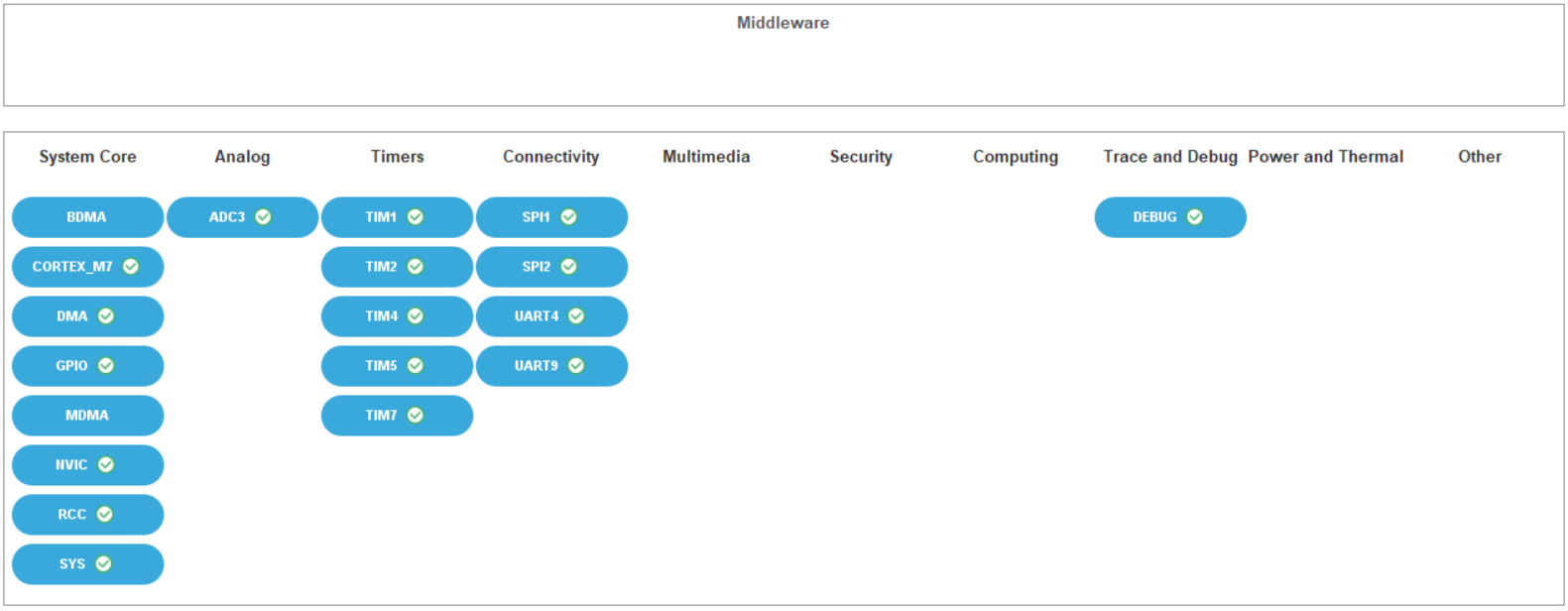
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM4 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
TIM7 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h72x-3x_line_product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
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