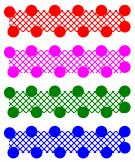
CONTENT INDEXING

01. INDEX
02.Change List
03.Block Diagram
05.Power Tree-RK816-3
10.PX3-SE Power
11.PX3-SE MISC&USB
12.PX3-SE DDR Controler
13.PX3-SE Flash/SD Controler
17.PX3-SE Display
18.PX3-SE GPIO
19.PX3_SE_CIF
20.Power-RK816-3
21.POWER_IN
30.RAM-DDR3 2x16bit
40.Memory-Nand Flash(OPTION)
41.Memory-eMMC Flash
42.Memory-SPI_FLASH(OPTION)
45.CVBS_IN TP2825(OPTION)
46.CVBS_IN ADV7181D
50.LCD LVDS
51.LCD MIPI(OPTION)
60.WIFI/BT MODULE
61.GPS MODULE
70.PX3 CODEC/CVBS OUT/HDMI
71.EXTERNAL CODEC
72.VOICE PROCESSOR
73.AUDIO PA
80.SENSOR
81.TF card
82.HDMI
83.I2C TO UART
85.USB HUB
88.KEYPAD
99.MARK

PCB POWER WIRE WIDTH INDICATE

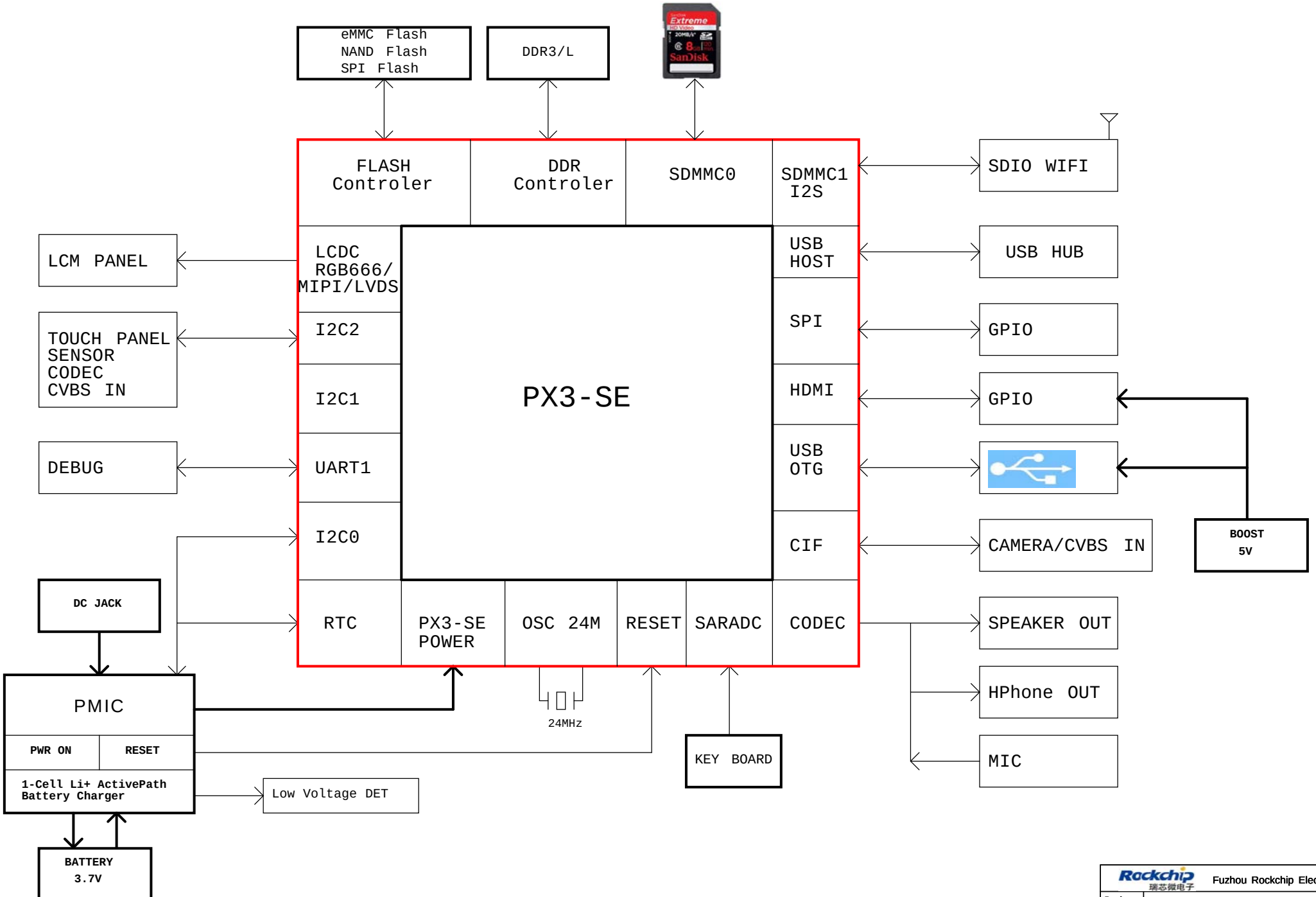


above 80 miles
above 50 miles
above 30 miles
above 16 miles
No indicate
Under needs

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	PX3-SE_IVN_REF_V10		
File:	INDEX		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	1 of 23

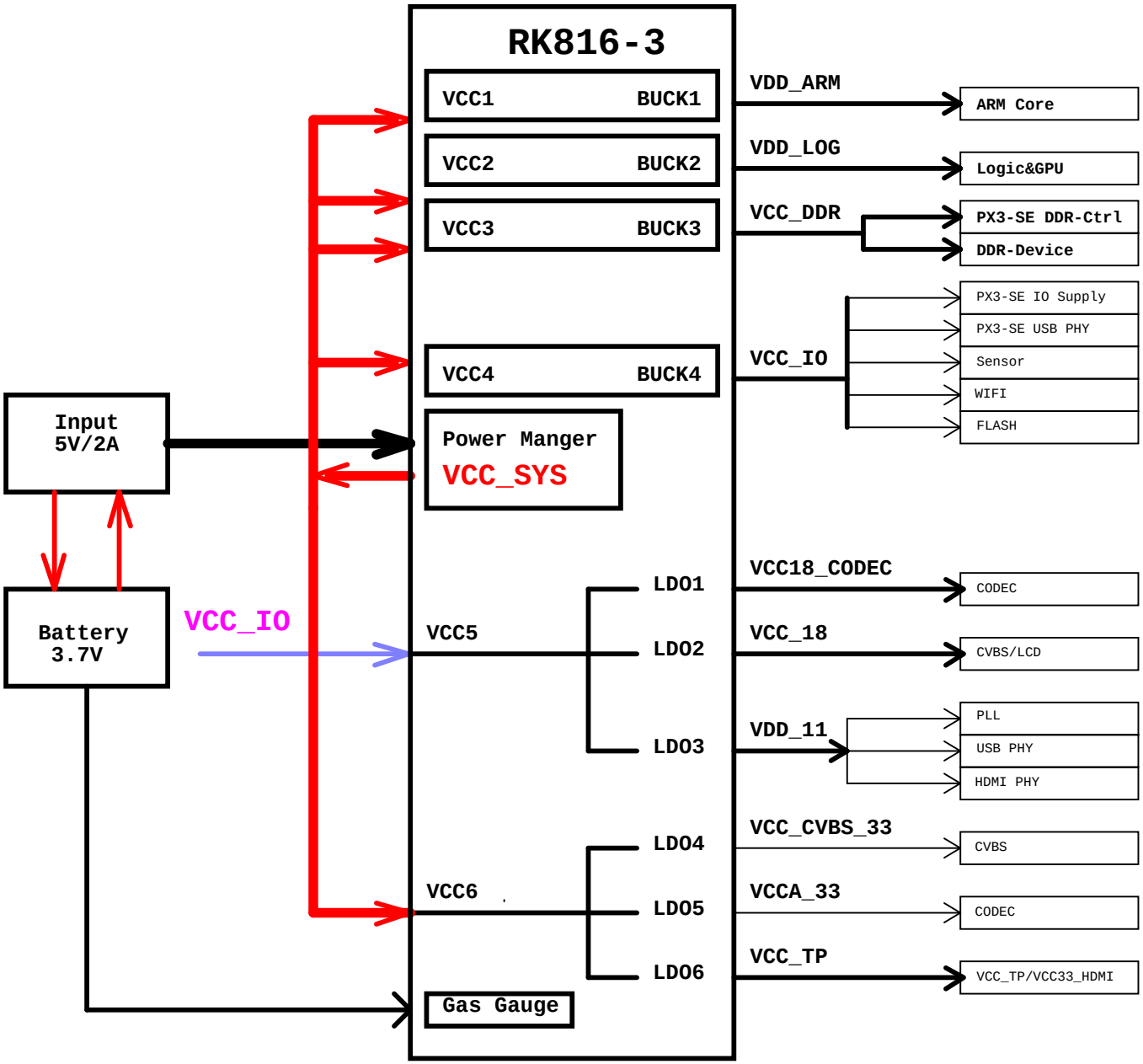
Version	Date	Author	Change Note	Note
V1.0	20170226	ZHM	First Edit	

Fuzhou Rockchip Electronics	
Project:	PX3-SE_IVN_REF_V10
File:	Change List
Date: Friday, June 29, 2018	Rev: V1.0
Designed by: ZHM	Sheet: 2 of 23



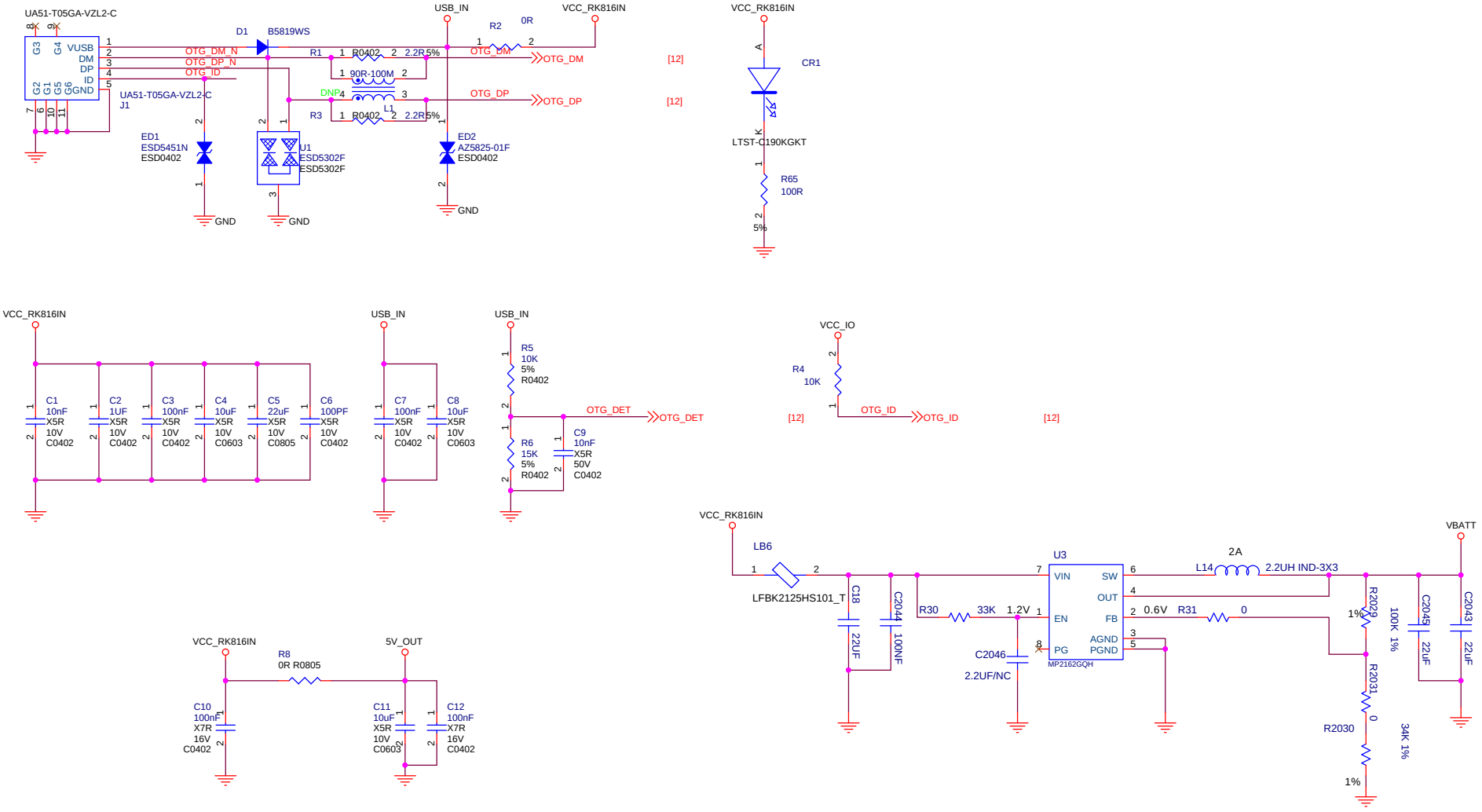
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	PX3-SE_IVN_REF_V10
File:	BLOCK Diagram
Date:	Friday, June 29, 2018
Rev:	V1.0
Designed by:	ZHM
Sheet:	3 of 23

POWER DIAGRAM



PMU Channel	TIMER (2mS)	default ON/OFF	default voltage	PX3-SE
DCDC1	solt:2	ON	1.1V	VDD_ARM
DCDC2	solt:1	ON	1.1V	VDD_LOG
DCDC4	solt:1	ON	3.3V	VCC_IO/VCCIO_WL/VCC_SD FLASH/VCC_LCD
DCDC3	solt:3	ON	DDR3 1.5V DDR3L 1.35V LPDDR 1.245V	VCC_DDR
VLDO1	X	OFF		VCC18_CODEC
VLDO2	solt:1	ON	1.8V	VCC_18
VLDO3	solt:1	ON	1.1V	VDD_11
VLDO4	X	OFF	3.3V	VCC_CVBS_33
VLDO5	solt:4	ON	3.3V	VCCA_33
VLDO6	solt:4	ON	3.3V	VCC_TP
RESET	58mS	ON	OD	RESET

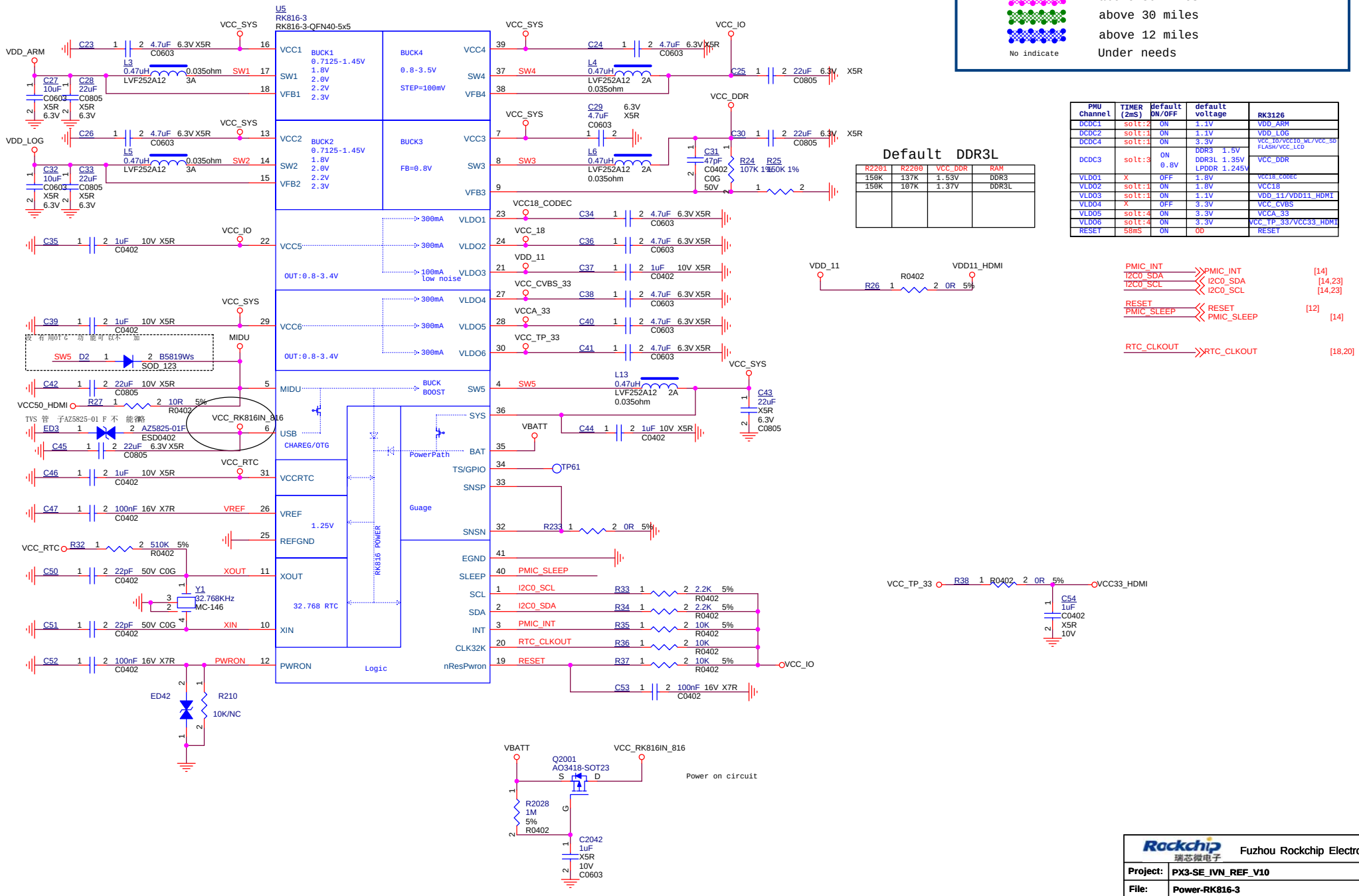
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	Power Tree-RK816-3		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	4 of 23



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Friday, June 29, 2018	Sheet 5 of 23	

PCB POWER WIRE WIDTH INDICATE

above 80 miles
above 50 miles
above 30 miles
above 12 miles
No indicate Under needs



Default DDR3L

R2201	R2200	VCC_DDR	RAM
150K	137K	1.53V	DDR3
150K	107K	1.37V	DDR3L

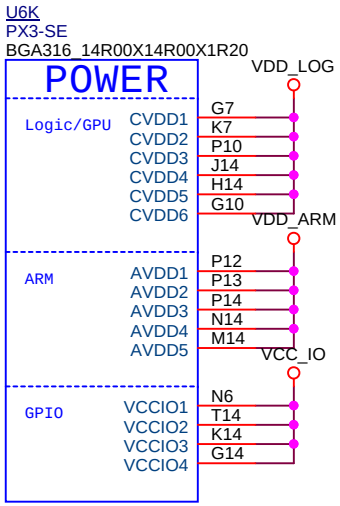
PMU Channel	TIMER (2mS)	default ON/OFF	default voltage	RK3126
DCDC1	solt:2	ON	1.1V	VDD_ARM
DCDC2	solt:1	ON	1.1V	VDD_LOG
DCDC4	solt:1	ON	3.3V	VCC_IO/VCCIO_WL/VCC_SD FLASH/VCC_LCD
DCDC3	solt:3	ON 0.8V	DDR3 1.5V DDR3L 1.35V LPDDR 1.245V	VCC_DDR
VLDO1	X	OFF	1.8V	VCC18_CODEC
VLDO2	solt:1	ON	1.8V	VCC18
VLDO3	solt:1	ON	1.1V	VDD_11/VDD11_HDMI
VLDO4	X	OFF	3.3V	VCC_CVBS
VLDO5	solt:4	ON	3.3V	VCCA_33
VLDO6	solt:4	ON	3.3V	VCC_TP_33/VCC33_HDMI
RESET	58mS	ON	OD	RESET

PMIC_INT [14]
I2C0_SDA [14,23]
I2C0_SCL [14,23]
RESET [12]
PMIC_SLEEP [14]
RTC_CLKOUT [18,20]

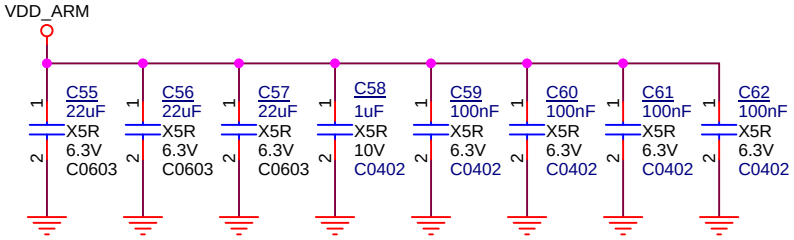
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

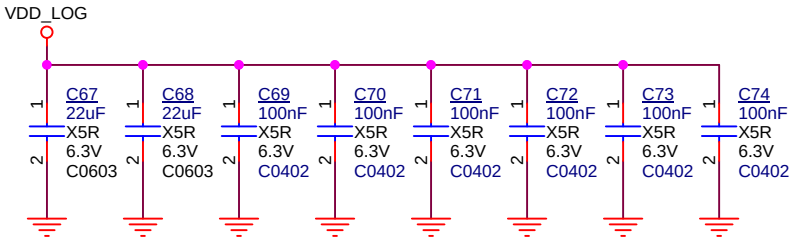
Project:	PX3-SE_IVN_REF_V10		
File:	Power-RK816-3		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	6 of 23

PX3-SE-K

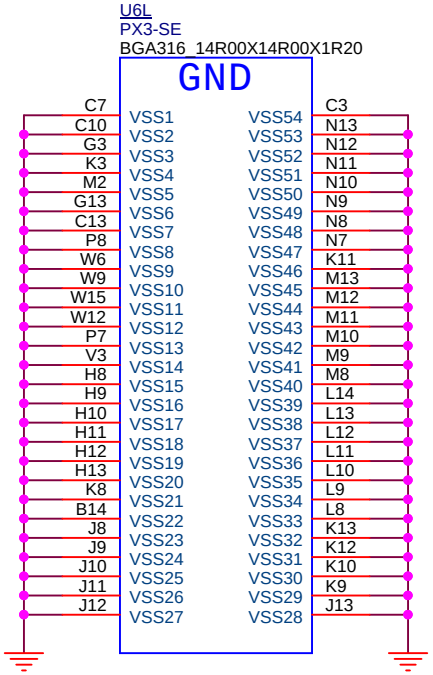


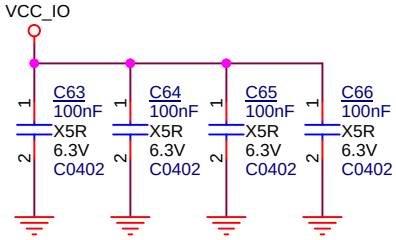
Note:
Place these filter capacitors under CPU.





PX3-SE-L





Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3-SE POWER		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	7 of 23

PX3-SE-J

U6J
PX3-SE
BGA316_14R00X14R00X1R20

Memory

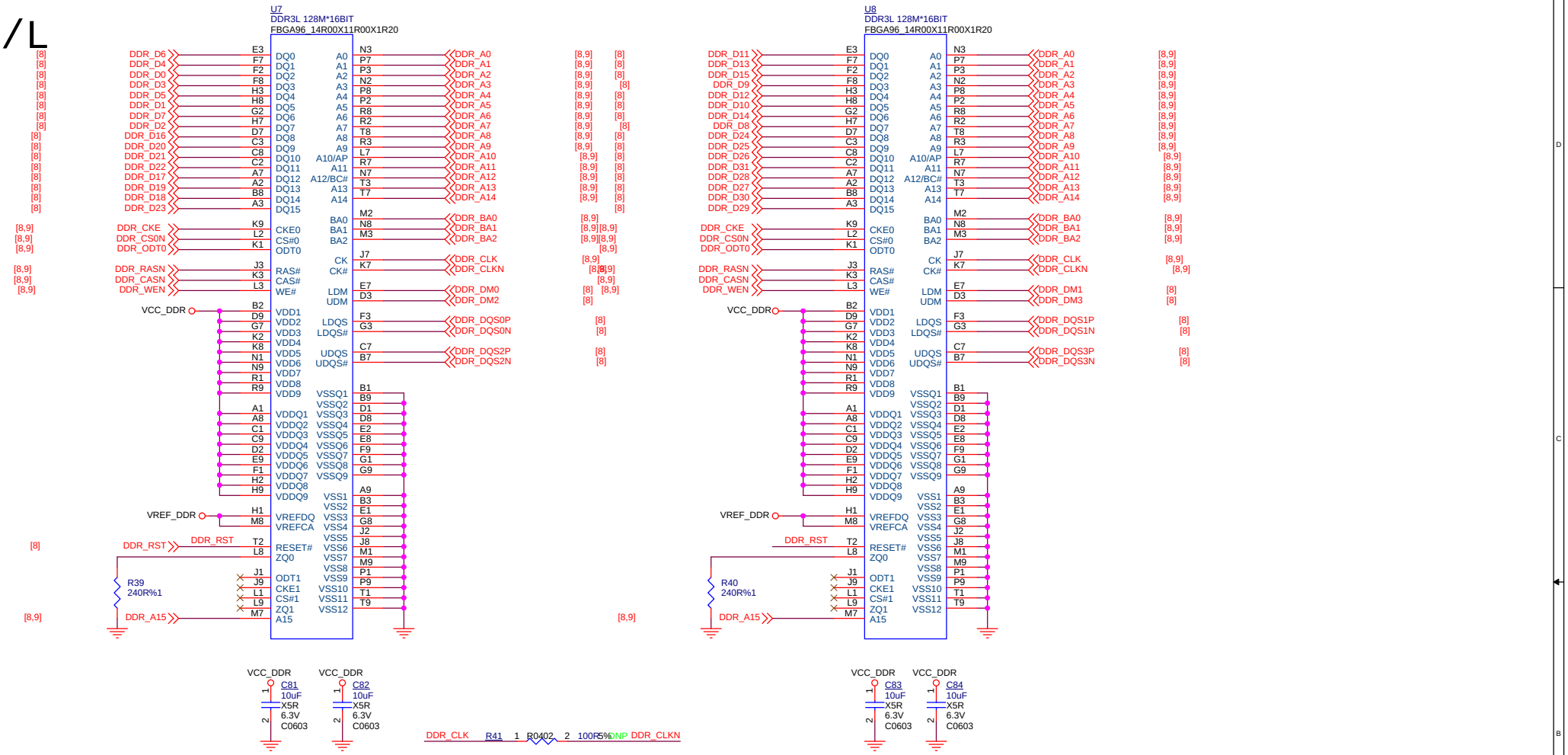
[9]	DDR_D0	A14	DDR_DQ0	DDR_A0	D1	DDR_A0	[9]
[9]	DDR_D1	F8	DDR_DQ1	DDR_A1	A4	DDR_A1	[9]
[9]	DDR_D2	F11	DDR_DQ2	DDR_A2	E2	DDR_A2	[9]
[9]	DDR_D3	A7	DDR_DQ3	DDR_A3	D2	DDR_A3	[9]
[9]	DDR_D4	B10	DDR_DQ4	DDR_A4	A2	DDR_A4	[9]
[9]	DDR_D5	D10	DDR_DQ5	DDR_A5	E5	DDR_A5	[9]
[9]	DDR_D6	B13	DDR_DQ6	DDR_A6	F7	DDR_A6	[9]
[9]	DDR_D7	C8	DDR_DQ7	DDR_A7	E4	DDR_A7	[9]
[9]	DDR_DM0	B7	DDR_DQM0	DDR_A8	D8	DDR_A8	[9]
[9]	DDR_DQS0P	A8	DDR_DQS0	DDR_A9	E1	DDR_A9	[9]
[9]	DDR_DQS0N	B8	DDR_DQS0n	DDR_A10	C4	DDR_A10	[9]
				DDR_A11	C5	DDR_A11	[9]
				DDR_A12	B4	DDR_A12	[9]
				DDR_A13	G1	DDR_A13	[9]
				DDR_A14	B5	DDR_A14	[9]
				DDR_A15	A5	DDR_A15	[9]
[9]	DDR_D8	G6	DDR_DQ8				
[9]	DDR_D9	G5	DDR_DQ9				
[9]	DDR_D10	F2	DDR_DQ10	DDR_BA0	D7	DDR_BA0	[9]
[9]	DDR_D11	H6	DDR_DQ11	DDR_BA1	E8	DDR_BA1	[9]
[9]	DDR_D12	H3	DDR_DQ12	DDR_BA2	D3	DDR_BA2	[9]
[9]	DDR_D13	J2	DDR_DQ13				
[9]	DDR_D14	K2	DDR_DQ14	DDR_CSN0	A1	DDR_CS0N	[9]
[9]	DDR_D15	K1	DDR_DQ15	DDR_CSN1	B6	TP1 TP_0.5	
[9]	DDR_DM1	H4	DDR_DQM1	DDR_ODT0	B2	DDR_ODT0	[9]
				DDR_ODT1	G2		
[9]	DDR_DQS1P	H1	DDR_DQS1				
[9]	DDR_DQS1N	H2	DDR_DQS1n	DDR_CLK	B1	DDR_CLK	[9]
				DDR_CLKn	C2	DDR_CLKN	[9]
[9]	DDR_D16	A10	DDR_DQ16	DDR_CKE	B3	DDR_CKE	[9]
[9]	DDR_D17	C11	DDR_DQ17				
[9]	DDR_D18	B9	DDR_DQ18	DDR_RASn	E3	DDR_RASN	[9]
[9]	DDR_D19	E11	DDR_DQ19	DDR_CASn	E7	DDR_CASN	[9]
[9]	DDR_D20	E10	DDR_DQ20	DDR_WEn	D5	DDR_WEN	[9]
[9]	DDR_D21	B12	DDR_DQ21				
[9]	DDR_D22	F10	DDR_DQ22	DDR_RESETn	F6	DDR_RST	[9]
[9]	DDR_D23	A13	DDR_DQ23				
[9]	DDR_DM2	D11	DDR_DQM2				
[9]	DDR_DQS2P	A11	DDR_DQS2				
[9]	DDR_DQS2N	B11	DDR_DQS2n				
[9]	DDR_D24	K4	DDR_DQ24	DDR_VDD1	M7	VCC_DDR	
[9]	DDR_D25	L4	DDR_DQ25	DDR_VDD2	L7		
[9]	DDR_D26	G4	DDR_DQ26	DDR_VDD3	J7		
[9]	DDR_D27	K5	DDR_DQ27	DDR_VDD4	H7		
[9]	DDR_D28	H5	DDR_DQ28	DDR_VDD5	G8		
[9]	DDR_D29	K6	DDR_DQ29	DDR_VDD6	G9		
[9]	DDR_D30	L5	DDR_DQ30	DDR_VDD7	G11		
[9]	DDR_D31	L6	DDR_DQ31	DDR_VDD8	G12		
[9]	DDR_DM3	L3	DDR_DQM3				
[9]	DDR_DQS3P	L1	DDR_DQS3				
[9]	DDR_DQS3N	L2	DDR_DQS3n				

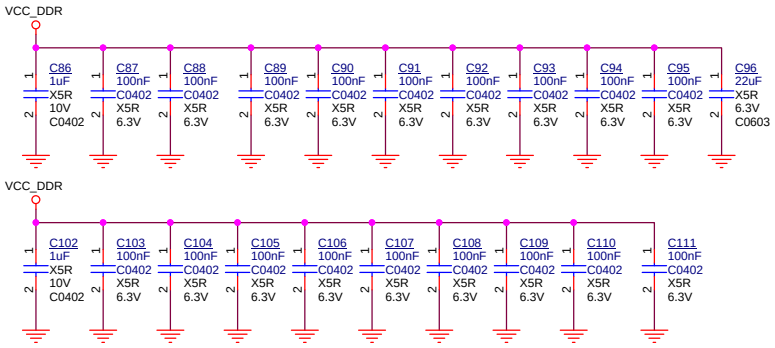
VCC_DDR

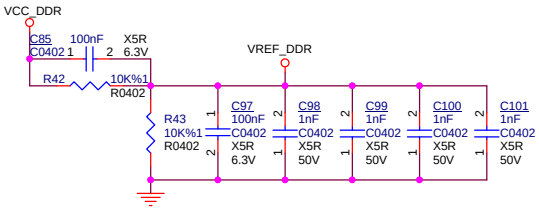
C75 10uF X5R 6.3V C0603
C76 1uF X5R 10V C0402
C77 100nF X5R 6.3V C0402
C78 100nF X5R 6.3V C0402
C79 100nF X5R 6.3V C0402
C80 100nF X5R 6.3V C0402

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3-SE DDR Controler		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	8 of 23

DDR3/L



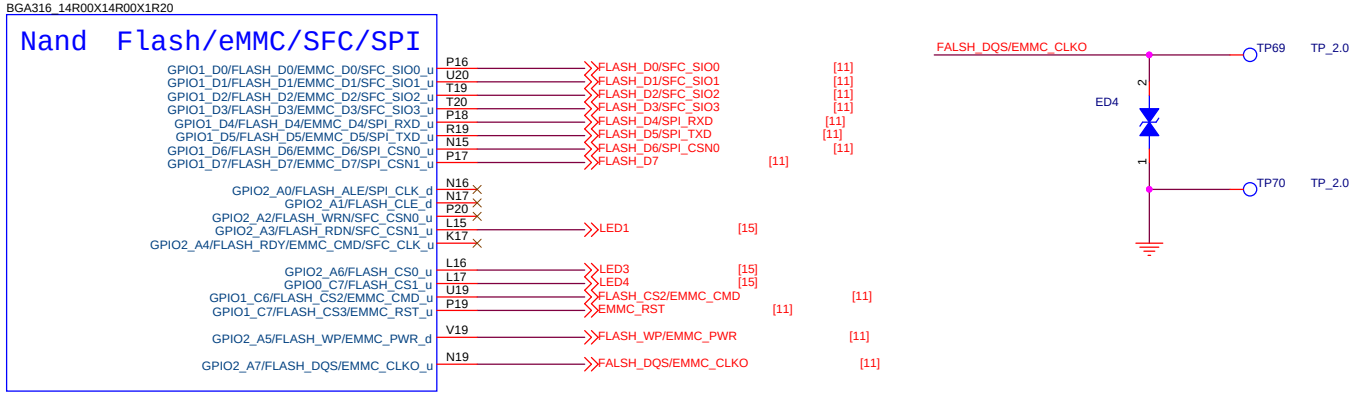




Fuzhou Rockchip Electronics			
Project:	PX3-SE_IVN_REF_V10		
File:	RAM-DDR3 2x16bit		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	9 of 23

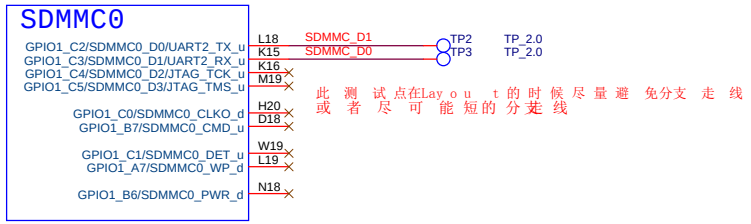
PX3-SE-E

U6E
PX3-SE
BGA316_14R00X14R00X1R20



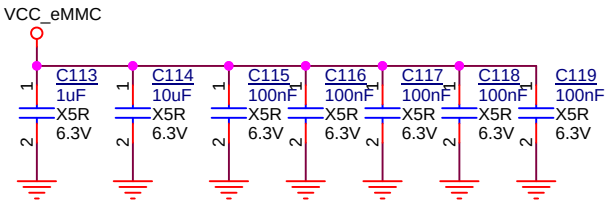
PX3-SE-D

U6D
PX3-SE



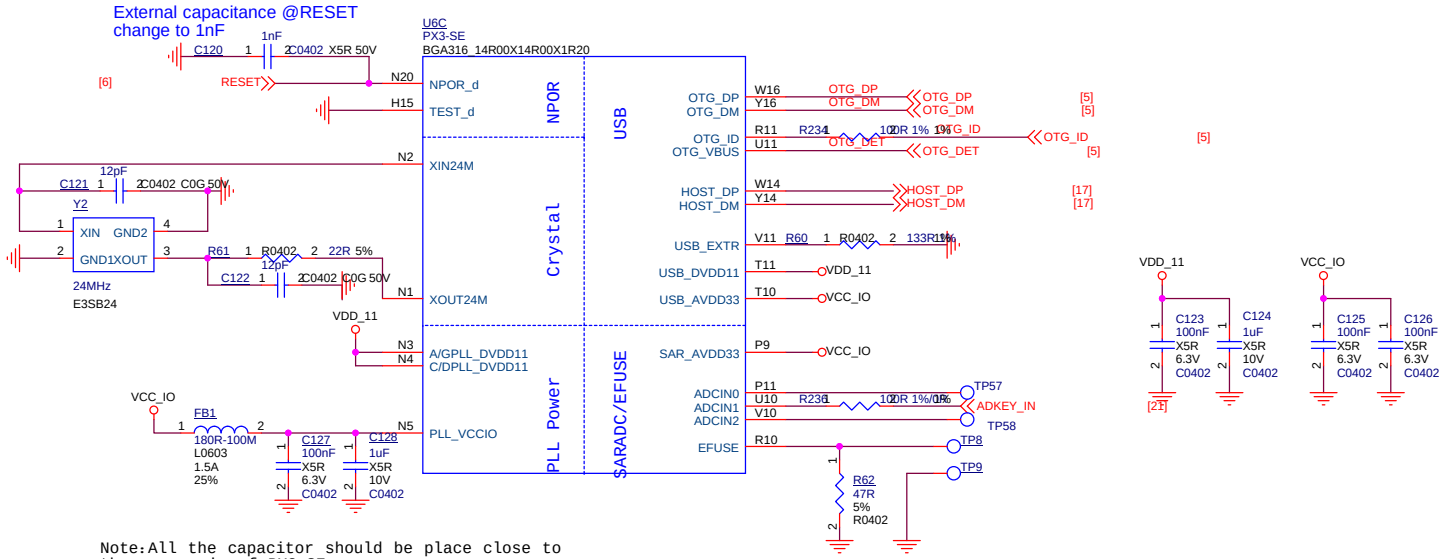
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3-SE Flash/SD Controler		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	10 of 23

eMMC FLASH



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	Memory-eMMC Flash		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	11 of 23

PX3-SE-C



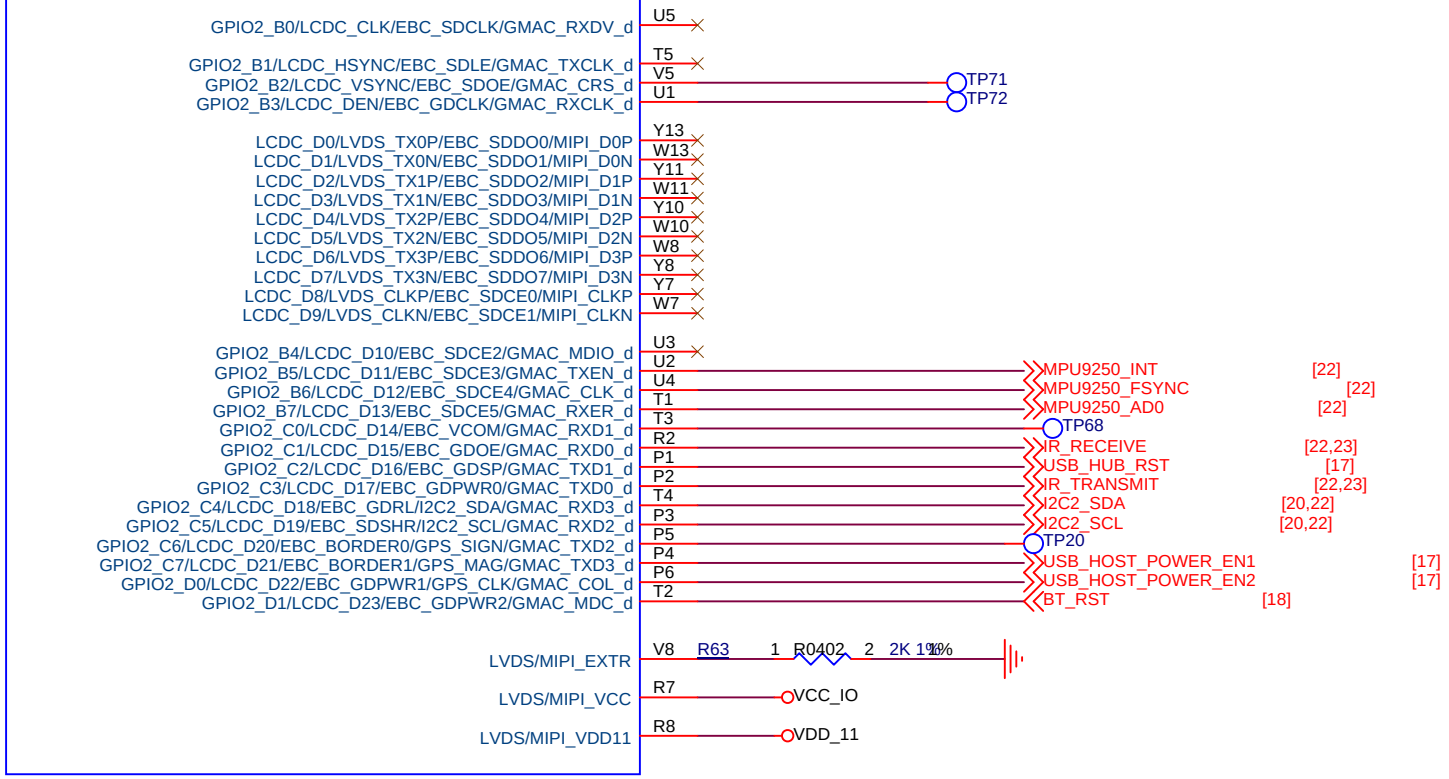
Note:All the capacitor should be place close to the power pin of PX3-SE。

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	11.PX3-SE MISC&USB		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	12 of 23

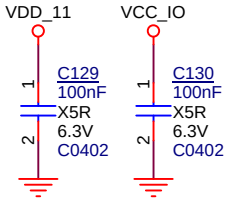
U6A
PX3-SE
BGA316_14R00X14R00X1R20

PX3-SE-A

LCDC/LVDS/MIPI/GMAC/EMAC

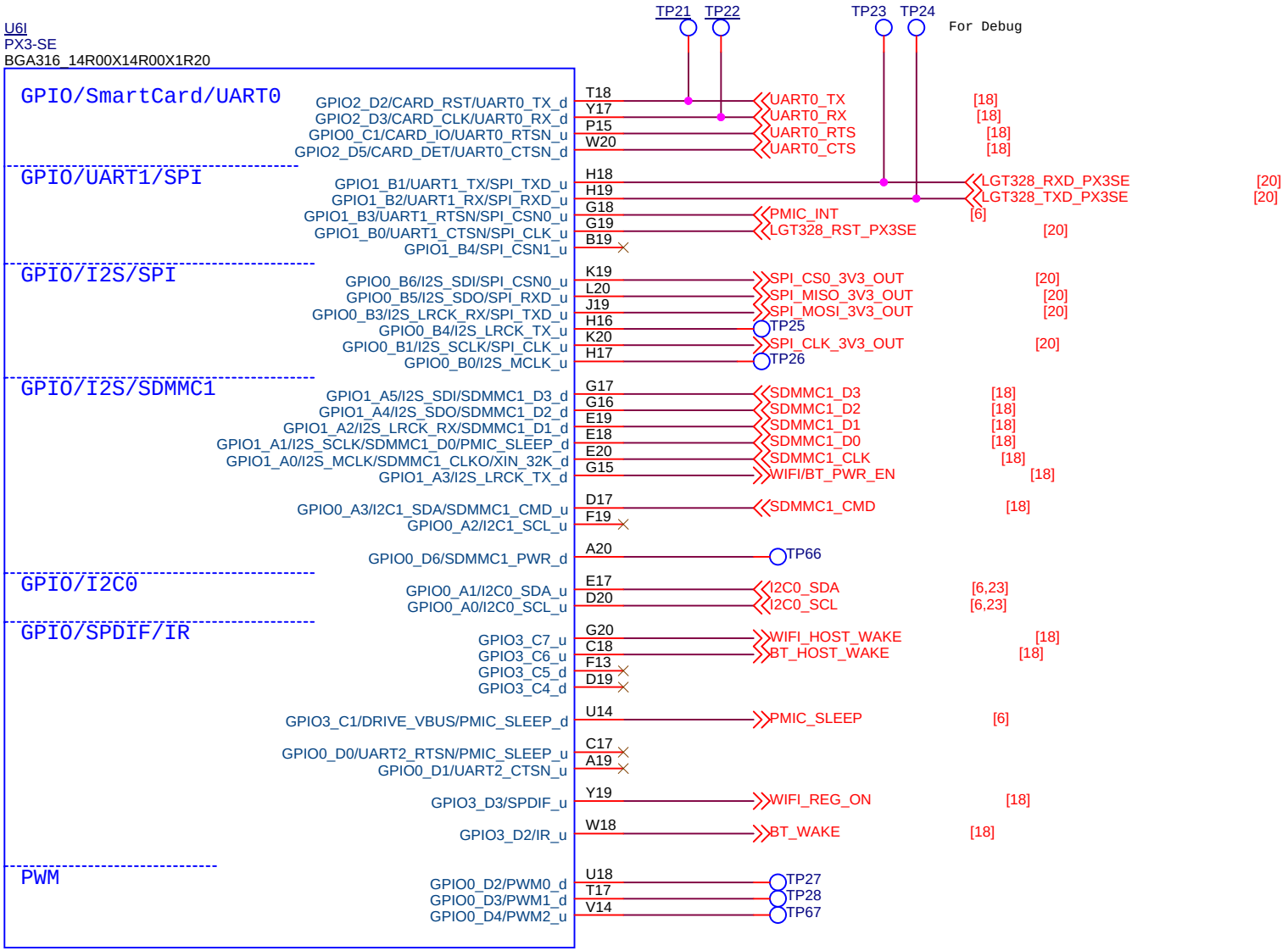


Correspondence between LCDC DATA and RGB			
LCDC_D0	B2	LCDC_D9	G5
LCDC_D1	B3	LCDC_D10	G6
LCDC_D2	B4	LCDC_D11	G7
LCDC_D3	B5	LCDC_D12	R2
LCDC_D4	B6	LCDC_D13	R3
LCDC_D5	B7	LCDC_D14	R4
LCDC_D6	G2	LCDC_D15	R5
LCDC_D7	G3	LCDC_D16	R6
LCDC_D8	G4	LCDC_D17	R7



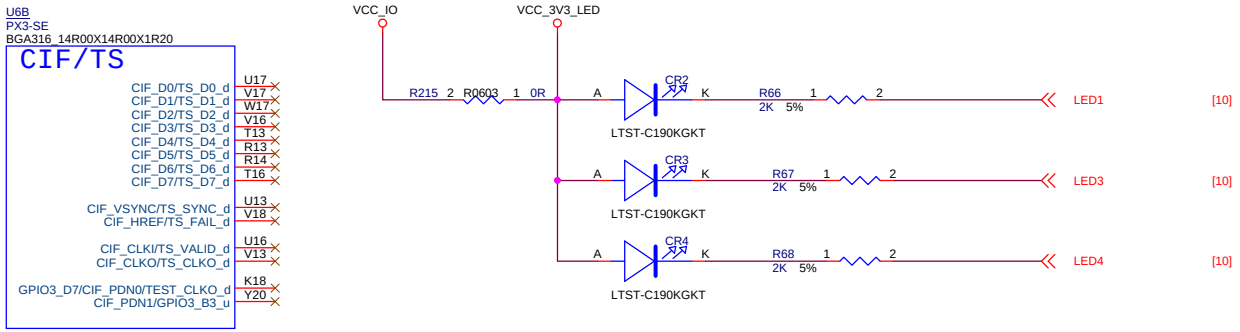
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3-SE Display		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	13 of 23

PX3-SE-I

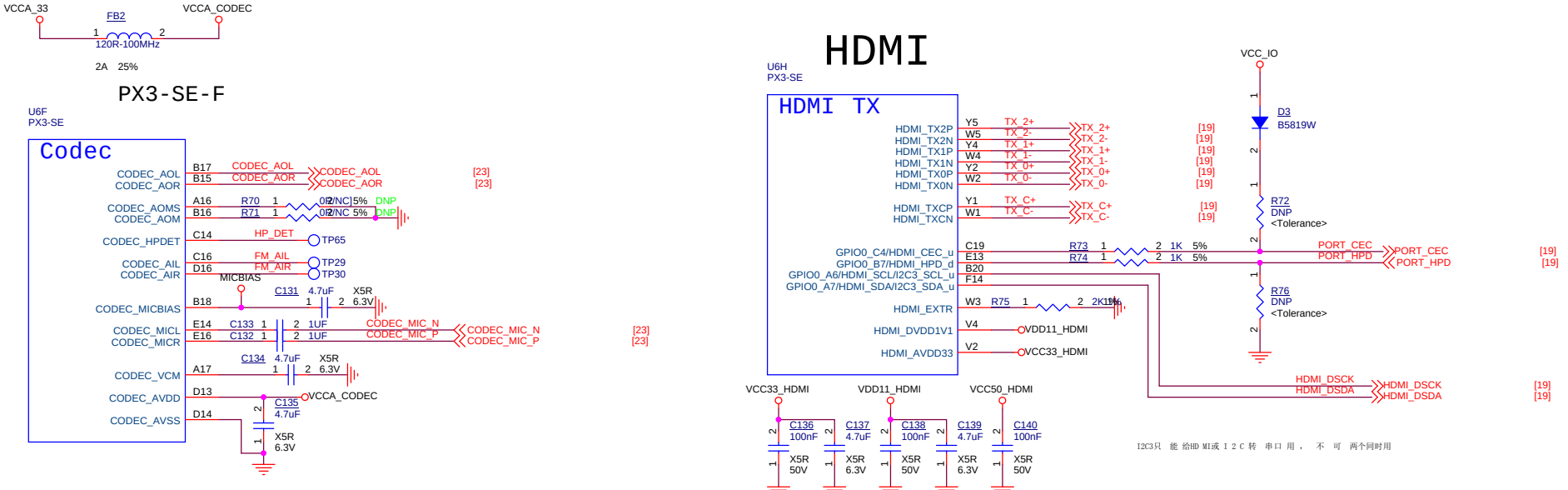


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3-SE GPIO		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	14 of 23

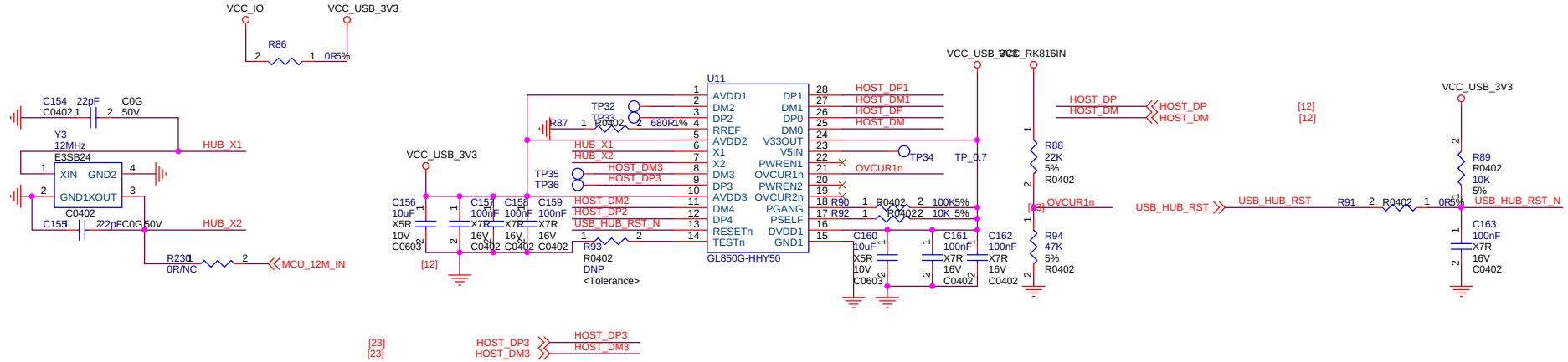
PX3-SE-B

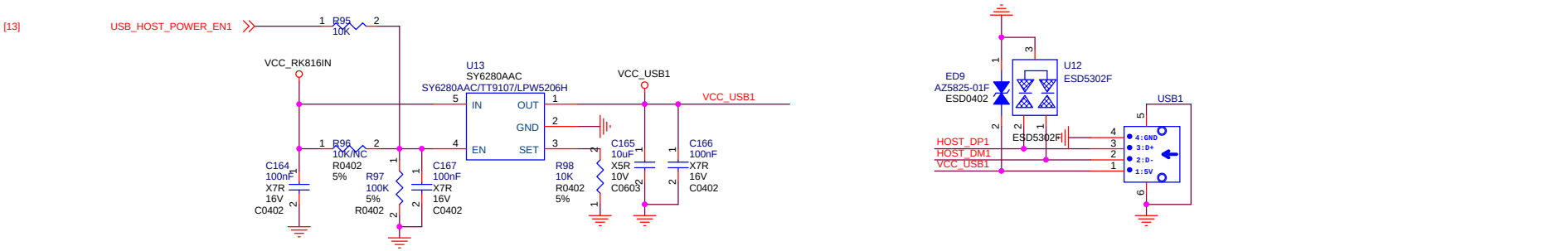


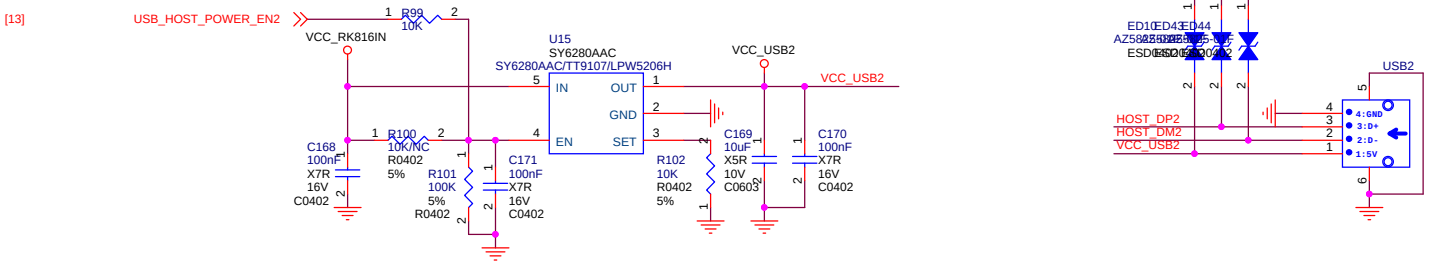
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3_SE_CIF		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	15 of 23



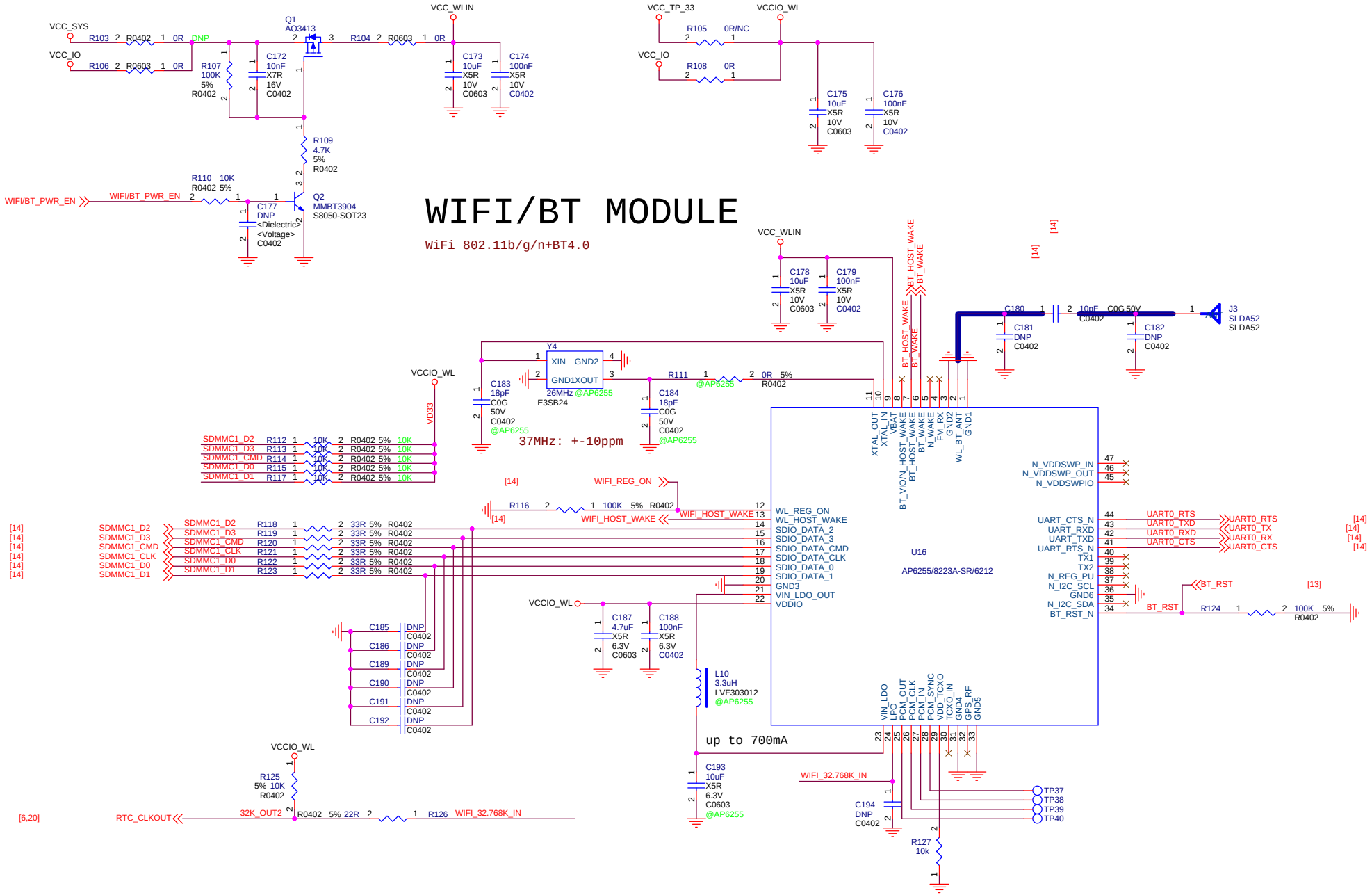
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	PX3 CODEC/CVBS OUT/HDMI		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	16 of 23

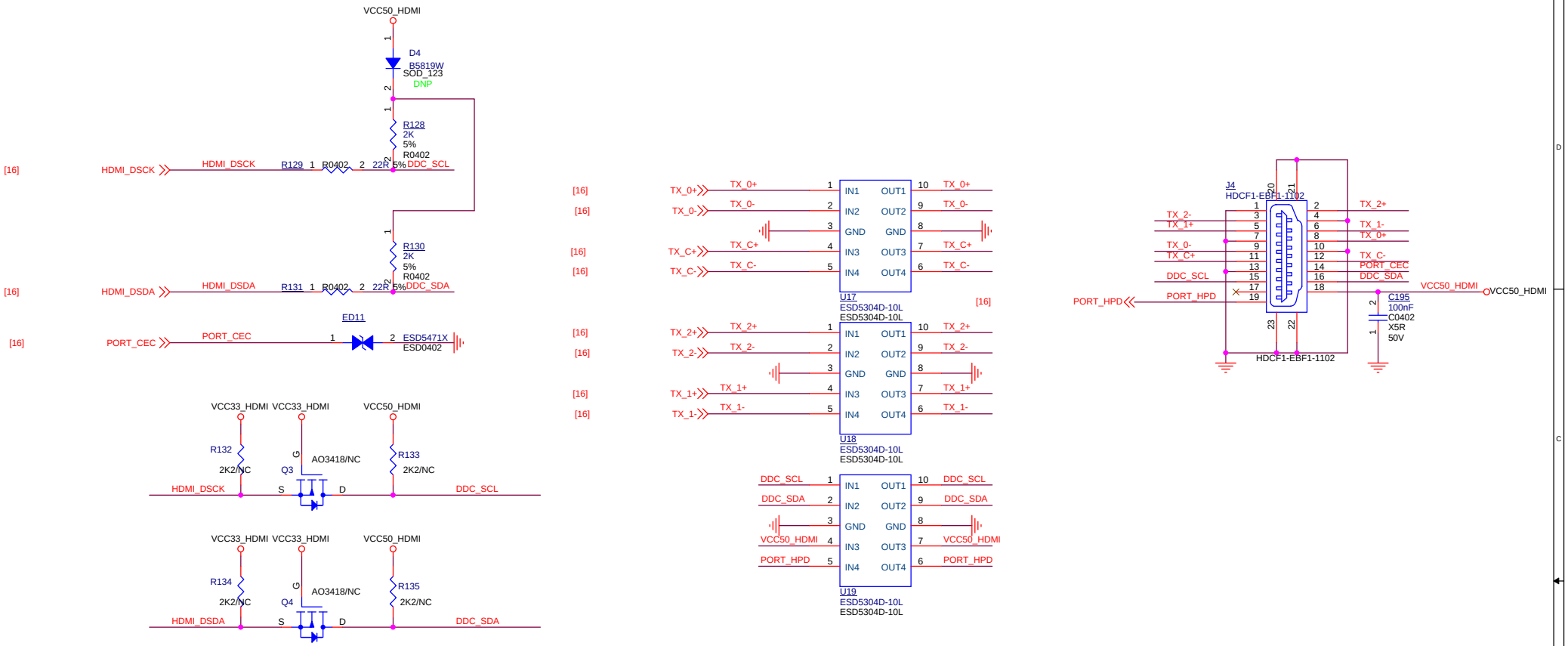




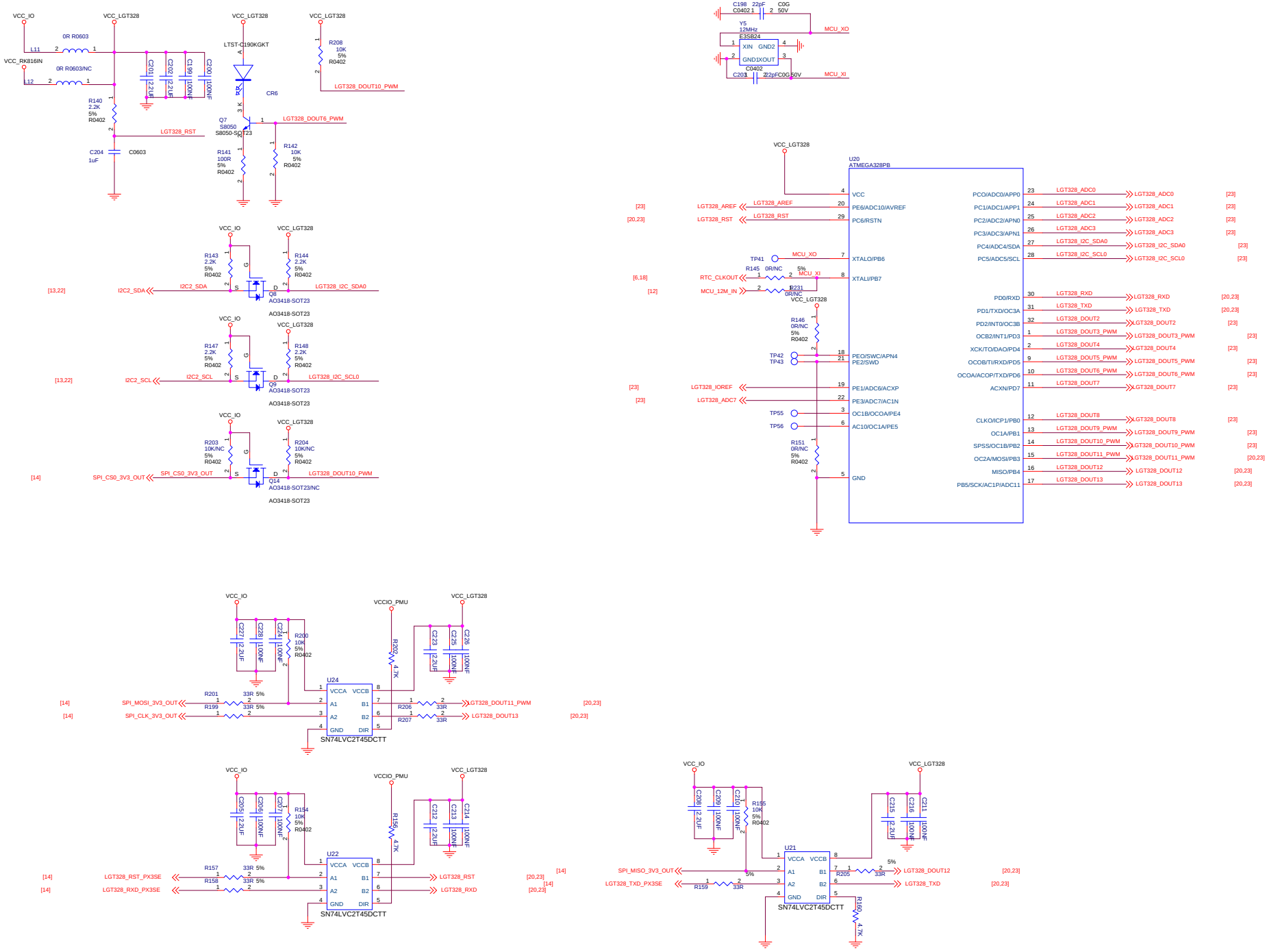


Fuzhou Rockchip Electronics			
Project:	PX3-SE_IVN_REF_V10		
File:	USB HUB		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	17 of 23

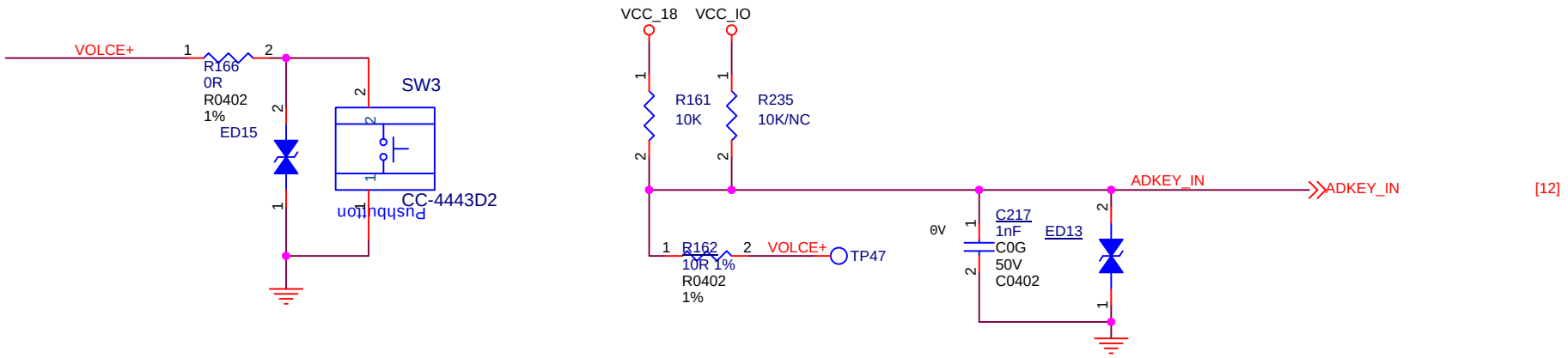

WIFI/BT MODULE
WiFi 802.11b/g/n+BT4.0
VCC_SYS
VCC_IO
VCC_WLIN
VCCIO_WL
VCC_TP_33
WIFI/BT_PWR_EN
Q1 AO3413
Q2 MMBT3904 S8050-SOT23
R103 2 R0402 1 0R DNP
R104 2 R0603 1 0R
R106 2 R0603 1 0R
R105 0R/NC
R108 0R
R107 100K 5% R0402
R109 4.7K 5% R0402
R110 10K R0402 5%
C172 10nF X7R 16V C0402
C173 10uF X5R 10V C0603
C174 100nF X5R 10V C0402
C175 10uF X5R 10V C0603
C176 100nF X5R 10V C0402
C177 DNP <Dielectric> <Voltage> C0402
C178 10uF X5R 10V C0603
C179 100nF X5R 10V C0402
C180 1 2 10pF C0G 50V C0402
C181 DNP C0402
C182 DNP C0402
J3 SLDA52 SLDA52
Y4 XIN GND2 GND1XOUT
26MHz @AP6255
E3SB24
C183 18pF C0G 50V C0402 @AP6255
C184 18pF C0G 50V C0402 @AP6255
R111 1 @AP6255 2 0R 5% R0402
37MHz: +-10ppm
VD33
SDMMC1_D2 R112 10K R0402 5% 10K
SDMMC1_D3 R113 10K R0402 5% 10K
SDMMC1_CMD R114 10K R0402 5% 10K
SDMMC1_D0 R115 10K R0402 5% 10K
SDMMC1_D1 R117 10K R0402 5% 10K
WIFI_REG_ON
R116 2 1 100K 5% R0402
WIFI_HOST_WAKE
BT_HOST_WAKE
BT_WAKE
SDMMC1_D2 R118 2 33R 5% R0402
SDMMC1_D3 R119 2 33R 5% R0402
SDMMC1_CMD R120 2 33R 5% R0402
SDMMC1_CLK R121 2 33R 5% R0402
SDMMC1_D0 R122 2 33R 5% R0402
SDMMC1_D1 R123 2 33R 5% R0402
C185 DNP C0402
C186 DNP C0402
C189 DNP C0402
C190 DNP C0402
C191 DNP C0402
C192 DNP C0402
C187 4.7uF X5R 6.3V C0603
C188 100nF X5R 6.3V C0402
L10 3.3uH LVF303012 @AP6255
up to 700mA
C193 10uF X5R 6.3V C0603 @AP6255
C194 DNP C0402
R125 5% 10K R0402
R126 WIFI_32.768K_IN
32K_OUT2
RTC_CLKOUT
R127 10k
U16
AP6255/8223A-SR/6212
WL_REG_ON
WL_HOST_WAKE
SDIO_DATA_2
SDIO_DATA_3
SDIO_DATA_CMD
SDIO_DATA_CLK
SDIO_DATA_0
SDIO_DATA_1
GND3
VIN_LDO_OUT
VDDIO
XTAL_OUT
XTAL_IN
VBAT
BT_VIO/N_HOST_WAKE
BT_HOST_WAKE
BT_WAKE
N_WAKE
FM_RX
GND2
WL_BT_ANT
GND1
N_VDDSWP_IN
N_VDDSWP_OUT
N_VDDSWPIO
UART_CTS_N
UART_RXD
UART_TXD
UART_RTS_N
TX1
TX2
N_REG_PU
N_I2C_SCL
GND6
N_I2C_SDA
BT_RST_N
UART0_RTS
UART0_TX
UART0_RX
UART0_CTS
BT_RST
R124 1 2 100K 5% R0402
VIN_LDO
LPO
PCM_OUT
PCM_CLK
PCM_IN
PCM_SYNC
TCXO_VDD
TCXO_IN
GND4
GPS_RF
GND5
WIFI_32.768K_IN
TP37
TP38
TP39
TP40
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: PX3-SE_IVN_REF_V10
File: WIFI/BT
Date: Friday, June 29, 2018
Rev: V1.0
Designed by: ZHM
Sheet: 18 of 23



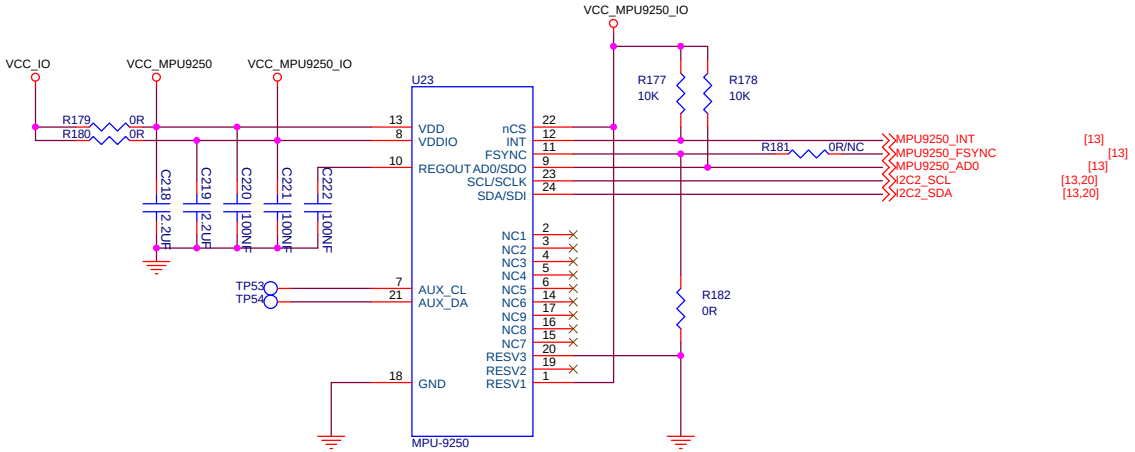
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	HDMI		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	19 of 23



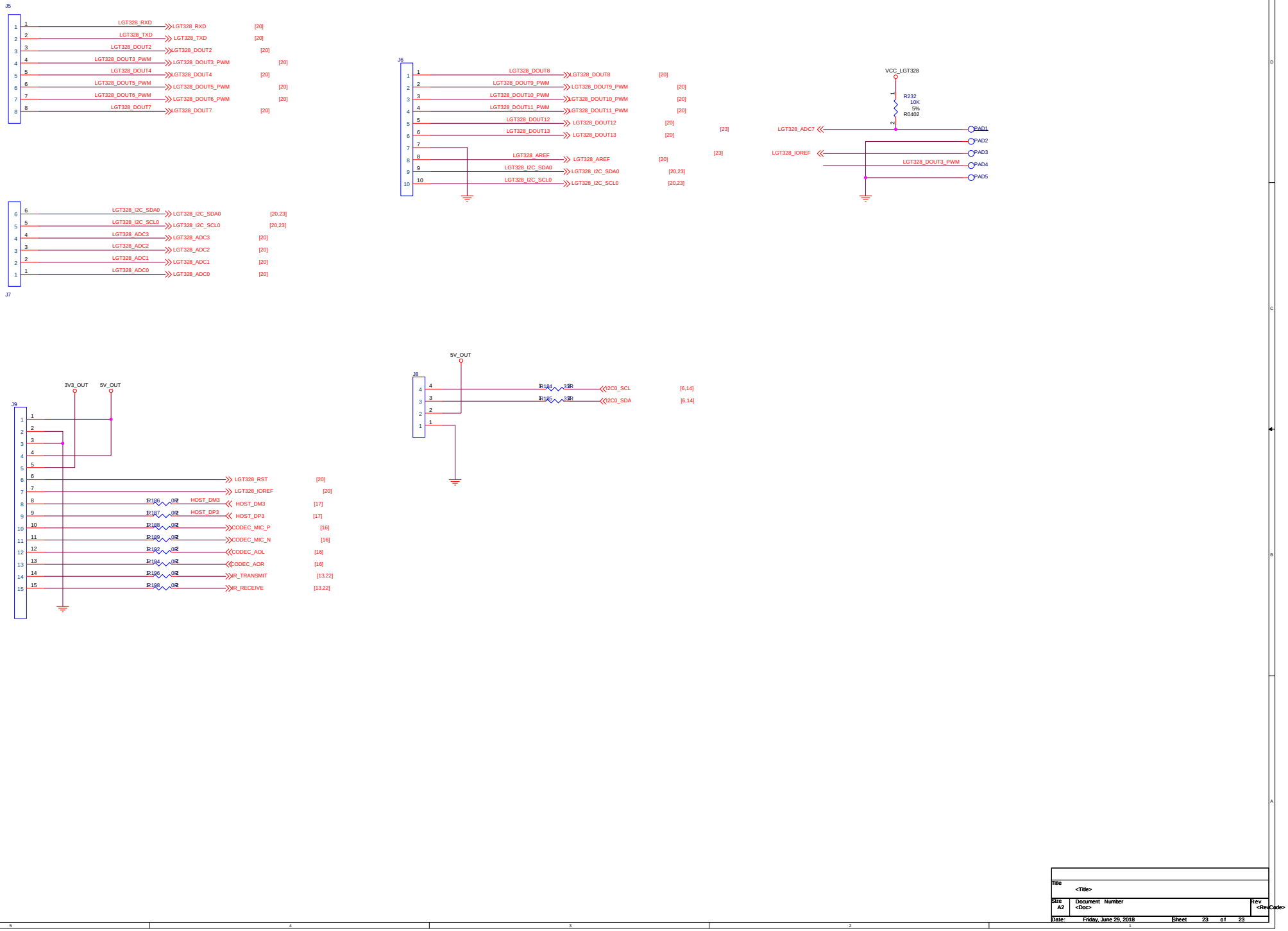
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	HDMI		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	20 of 23



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	MARK		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	21 of 23



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX3-SE_IVN_REF_V10		
File:	MARK		
Date:	Friday, June 29, 2018	Rev:	V1.0
Designed by:	ZHM	Sheet:	22 of 23


J5
LGT328_RXD
LGT328_TXD
LGT328_DOUT2
LGT328_DOUT3_PWM
LGT328_DOUT4
LGT328_DOUT5_PWM
LGT328_DOUT6_PWM
LGT328_DOUT7
[20]
J6
LGT328_DOUT8
LGT328_DOUT9_PWM
LGT328_DOUT10_PWM
LGT328_DOUT11_PWM
LGT328_DOUT12
LGT328_DOUT13
LGT328_AREF
LGT328_I2C_SDA0
LGT328_I2C_SCL0
[20,23]
[23]
VCC_LGT328
R232
10K
5%
R0402
LGT328_ADC7
LGT328_IOREF
LGT328_DOUT3_PWM
PAD1
PAD2
PAD3
PAD4
PAD5
J7
LGT328_ADC3
LGT328_ADC2
LGT328_ADC1
LGT328_ADC0
5V_OUT
J8
I2C0_SCL
I2C0_SDA
[6,14]
3V3_OUT
J9
LGT328_RST
LGT328_IOREF
HOST_DM3
HOST_DP3
CODEC_MIC_P
CODEC_MIC_N
CODEC_AOL
CODEC_AOR
XR_TRANSMIT
XR_RECEIVE
[13,22]
Title
<Title>
Size
A2
Document Number
<Doc>
Rev
<RevCode>
Date:
Friday, June 29, 2018
Sheet
23
of
23