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OI.II Calu	39

RK3368H_Tablet_REF_V1.0

I2C address(7Bit)

1: I2C0 POWER

RK818-1 0x1c **SYR827** 0x40 XZ3216 0x60 HYM8563 0x51

2: I2C1 CODEC

ES8316 0x20 ALC5631 0x38

3: I2C2 Touch Panel CT363 0x1b FT5506 **GSL3680** 0x40

4: I2C3 Camera

OV2659 0x30

OV8858

5: I2C4 Sensor

CM3218 0x10,0x0c LSM330TR G:0x6a,A:0x1e

MMA8452Q 0x1d

MPU6500 0x34 1: DN **附** 不 贴。 LIS3DH 0x19

2:如果 Value 和option 是哪 说明是预留还贴。

Note: 器件参数说明

LSM303D 0x1d

择 eMMC时, op tion是@MMC都 要贴;@Mand 不贴 奴选 择 Mand时, op tion是Mand都 要贴:@stw// C 7贴

頻光 择 RTL8 7 25模组,那么 option是 DMMS 2 12格器件 不 贴 頻光 择 AP620类组 时, 那么 option是 DMMS 2 12格器件 要 贴上

Bill of Materials

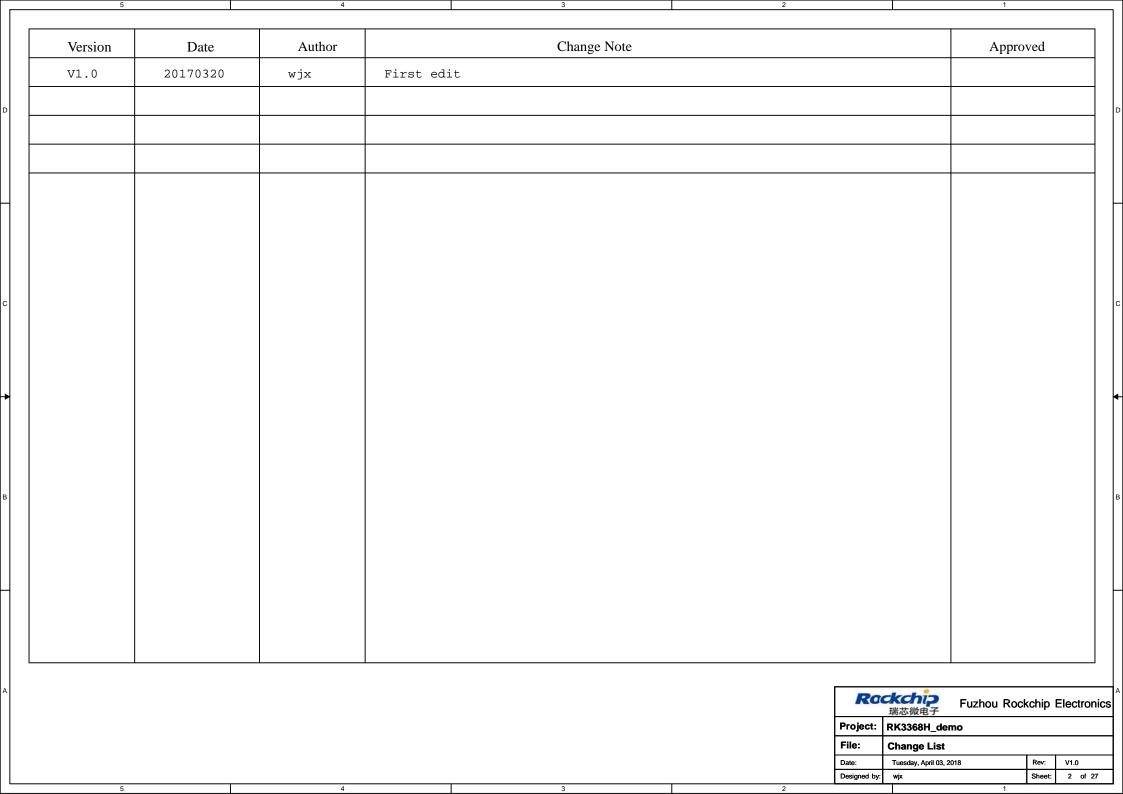
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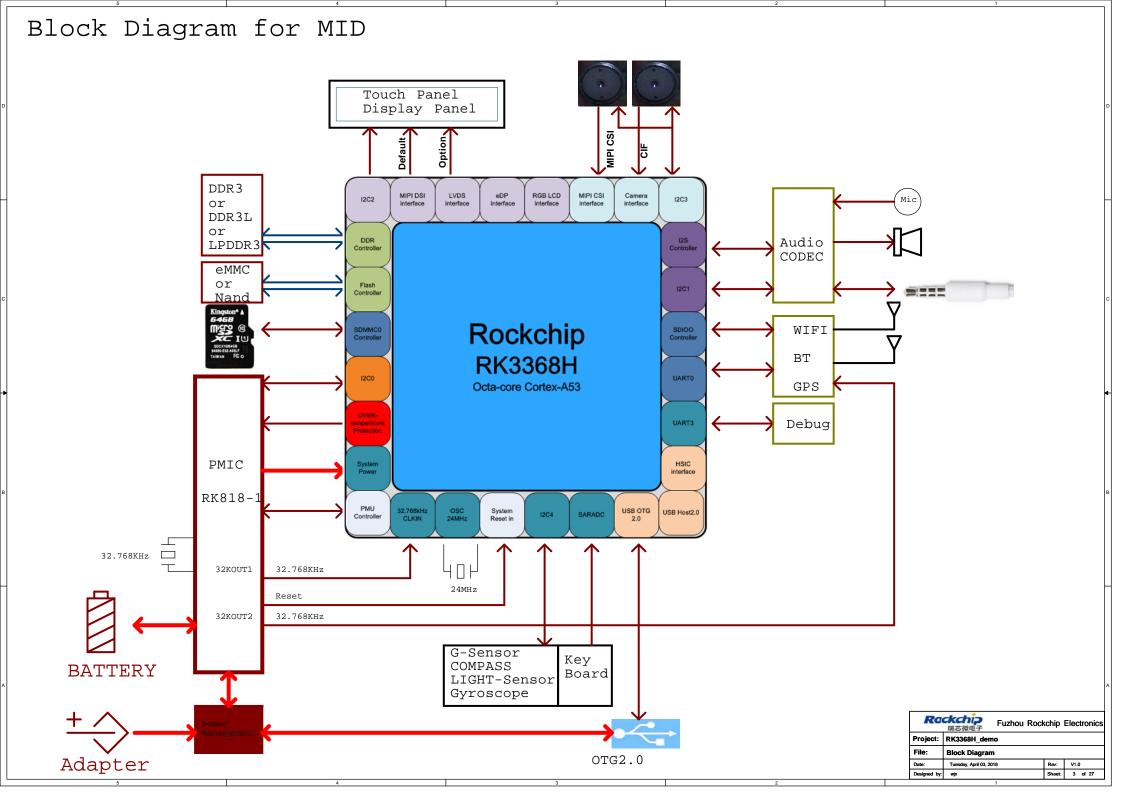
Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption Combined property string:

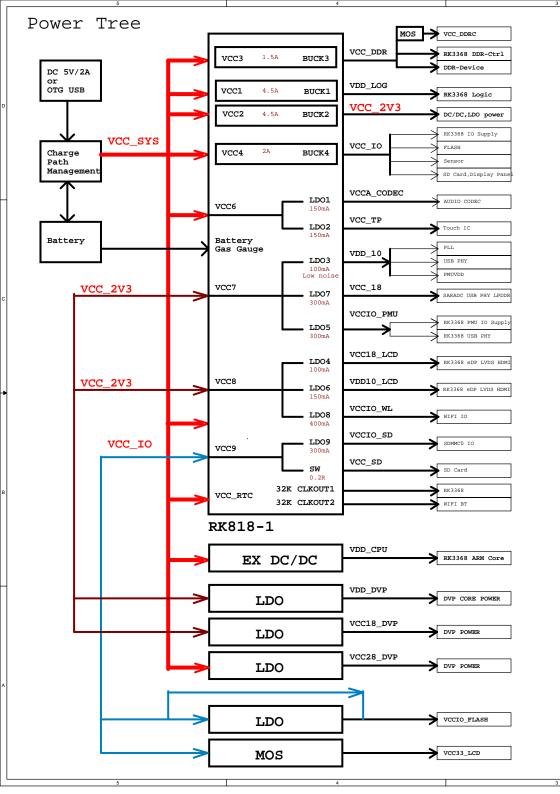
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Project: RK3368H der

MARK



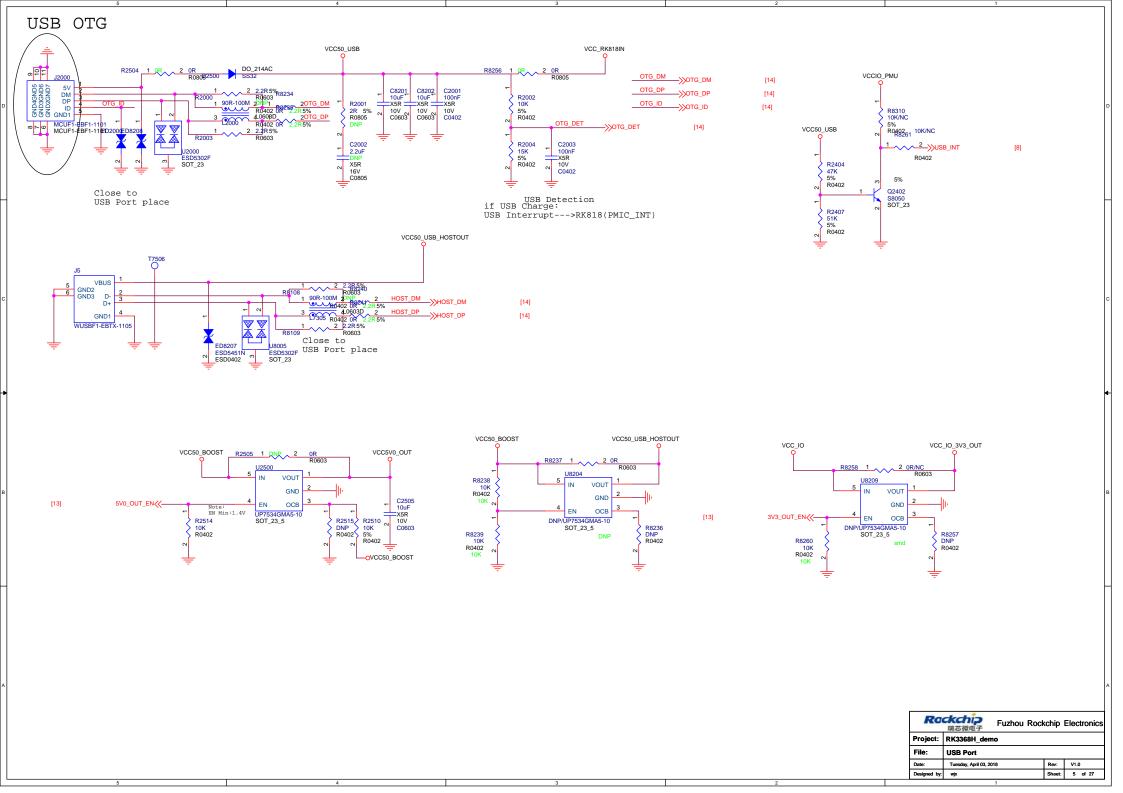


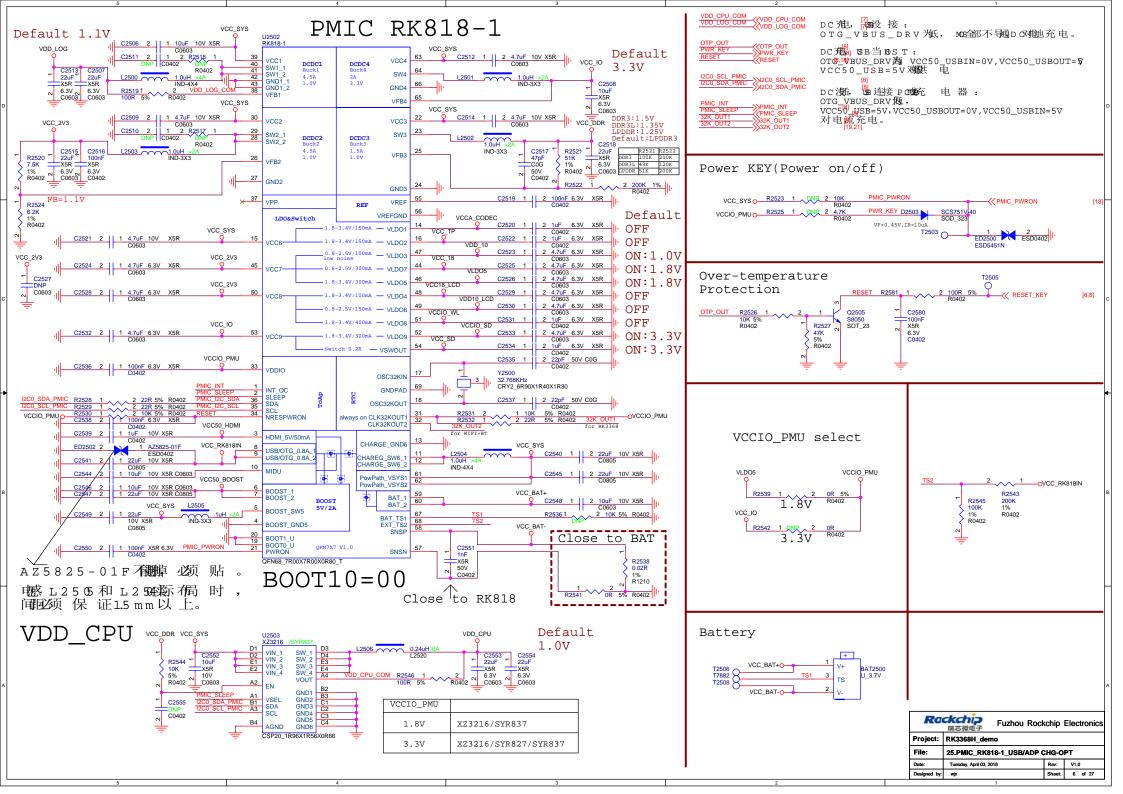


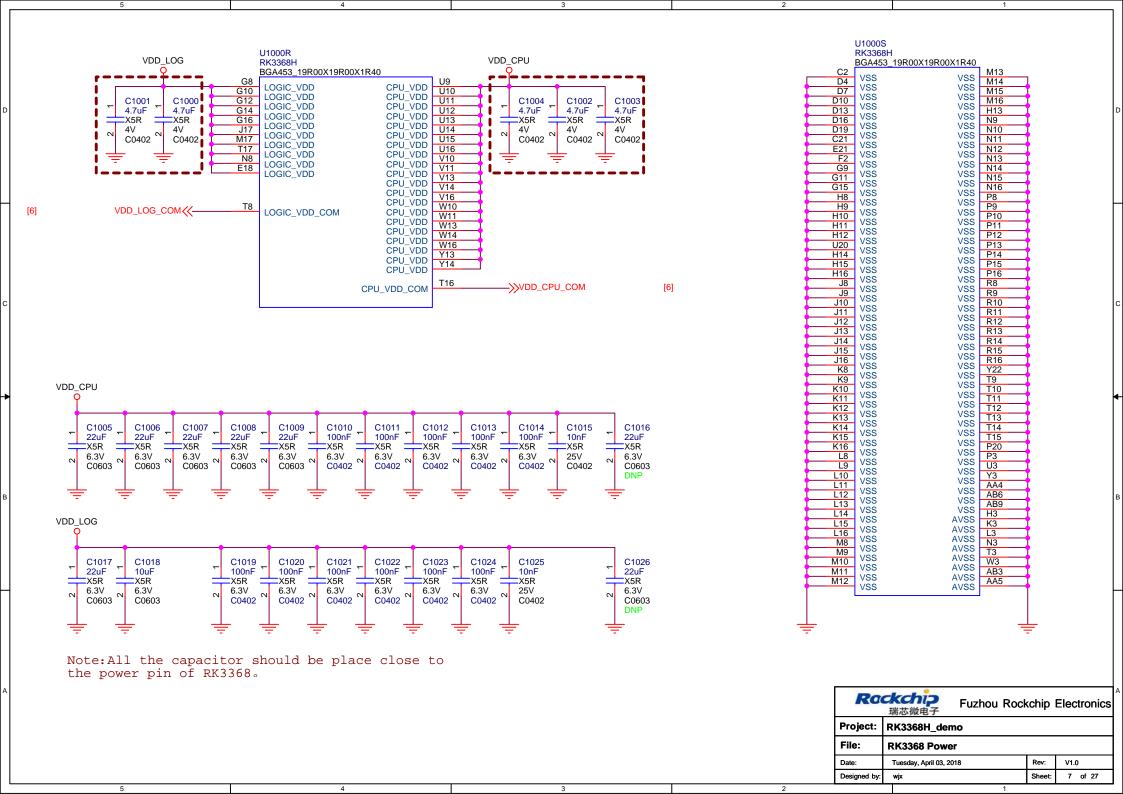
Power up Timing

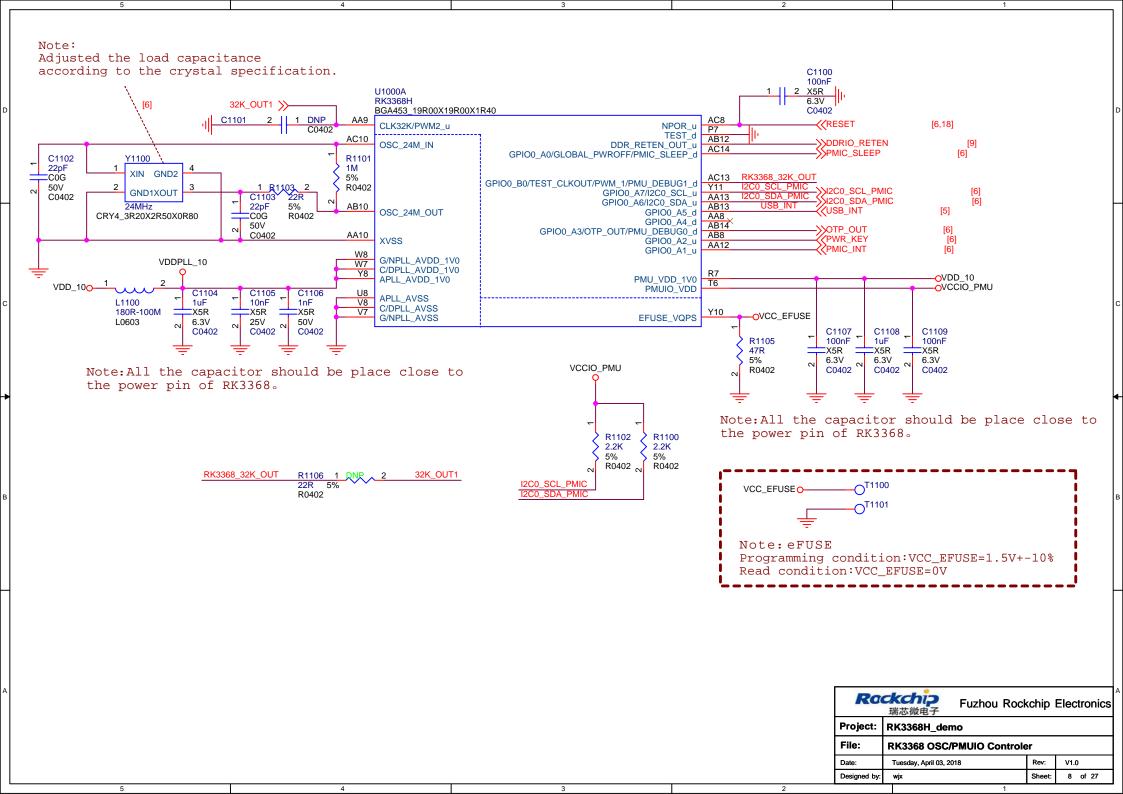
Power up '	l'ımıng			
PowerName	PMIC Channel	timer(2mS)	Default voltage	Normal voltage
VCC_2V3	DCDC2	Slot:1	2.3V	2.3V
VDD_10	VLD03	Slot:2	1.0V	1.0V
VDD_LOG	DCDC1	Slot:3	1.1v	DVFS
VCC_DDR	DCDC3	Slot:3	1.25V	1.25V
VDD_CPU	EX DCDC	Slot:3A	1.0V	DVFS
VCC_18	VLD07	Slot:3	1.8V	1.8V
VCCIO_PMU	VLD05	Slot:4	1.8V	1.8V
VCC_IO	DCDC4	Slot:4	3.3V	3.3V
VCCIO_FLASH	EX LDO(1.8V or VCC_IO) Slot:4A	1.8V or 3.3V	1.8V or 3.3V
VCCIO_SD	VLDO9	Slot:5	3.3V	1.8V or 3.3V
VCC_SD	VSWOUT1	Slot:5	3.3V	3.3V
Reset	(16*2mS)+50m	3		
VDD10_LCD	VLD06	OFF	0V	1.0V
VCC18_LCD	VLDO4	OFF	0V	1.8V
VCC33_LCD	EX MOS	OFF	0V	3.3V
VCCA_CODEC	VLD01	OFF	0V	3.0V
VCC_TP	VLDO2	OFF	0V	3.3V
AGGIO_MT	VLDO8	OFF	0V	1.8V
VDD_DVP	EX LDO	OFF	0V	1.2V or 1.5V
VCC18_DVP	EX LDO	OFF	0V	1.8V
VCC28_DVP	EX LDO	OFF	0V	2.8V

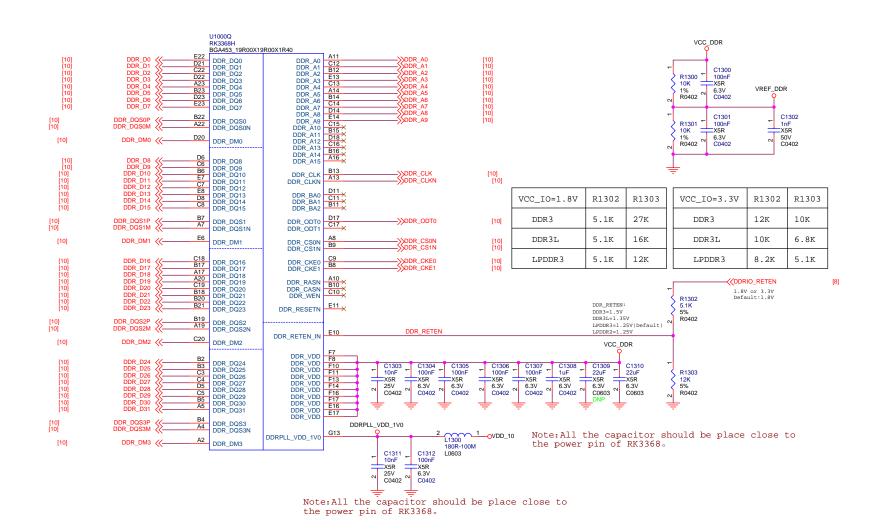
Ro	ckchip 瑞芯微电子	Fuzhou	Rockchip	Electronics
Project:	RK3368H_demo			
File:	Power tree-RK818-1			
Date:	Tuesday, April 03, 2	018	Rev:	V1.0
Designed by:	wjx		Sheet:	4 of 27





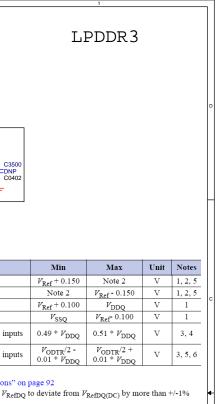






File: RK3368H_demo
File: RK3368 DDR Controler

Date: Tuesday, April 03, 2018 Rev: V1.0
Designed by: wk Sheet: 9 of 27



DRAM-LPDDR3-178P-Default

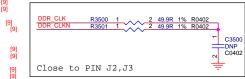
Rev: V1.0 Sheet:

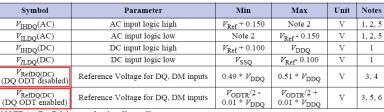
10 of 27

Tuesday, April 03, 2018

Date:

Designed by: wjx





NOTE 1 For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

NOTE 2 See "Overshoot and Undershoot Specifications" on page 92

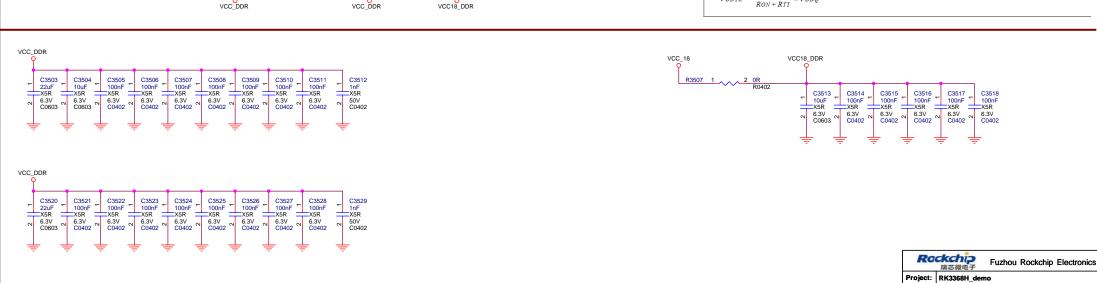
NOTE 3 The ac peak noise on V_{RefDO} may not allow V_{RefDO} to deviate from V_{RefDO(DC)} by more than +/-1% V_{DDO} (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. $V_{\rm DDQ}/2$ +/- 12 mV.

NOTE 5 For reference: approx. V_{ODTR}/2 +/- 12 mV.

NOTE 6 Ron and Rodt nominal mode register programmed values are used for the calculation of Vodtr.

$$VODTR = \frac{2RON + RTT}{RON + RTT} \times VDDQ$$



DDR_A1 N2 DDR_A2 N3

DDR_A3 M3

DDR_A5 E3

DDR A6

DDR_A7

DDR A8

DDR_CLK

DDR_CLKn

DDR_CKEO DDR_CKE

DDR_ODT

DDR 700

DDR_ZQ1

DDR_VREFCA

NU1 A2 X NU2 A12 X A13 X NU4 B1 X NU5 B13 X NU6 NU7 T13 X NU8 NU9 NU9 NU10 NU10 X NU10 NU12 X NU11 NU12 X N

C4 K9 R3 NC1 NC2 NC3

H4

DDR_VREFDQ J11 OVREF_DDR

VREF DDR

OVREF DDR

C3501

X5R

50V C0402

VREF DDRC(DDR VREFDO)

DQ ODT disabled and enabled

-(PMIC_SLEEP

[6,8]

DDR_A2

DDR_A4

DDR_A6

SDDR A7

SDDR A9

->>DDR_CS0N ->>DDR_CS1N

->>DDR_CKE0 ->>DDR_CKE1

->>DDR_ODT0

2 240R 1%

R0402

DDR_CLK

DDR_CLKN

DDR_CLKN

DDR_D0 DDR_D1

DDR_D2 DDR_D3 DDR_D4 DDR_D5

DDR_D13 DDR_D8 DDR_D11

DDR_D14

DDR_D17 DDR_D18 DDR_D19

DDR_D20

DDR_D21 DDR_D22

DDR_D23 DDR_D24 DDR_D25 DDR_D26 DDR_D27

DDR_D28 DDR_D29 DDR_D30 DDR_D31

DDR DQS0P

DDR_DQS0M DDR_DQS1P

DDR DOS2P DDR_DQS2M

DDR_DM0 <<

DDR_DM1
DDR_DM2

DDR_D0 N10 DDR_D1 N11 DDR_D2

DDR_D3 DDR_D4

DDR_D5 DDR_D6

DDR_D7

DDR D12

DDR_D13

DDR_D14 DDR_D15

DDR D16/NC

DDR_D17/NC

DDR_D18/NC DDR_D19/NC

DDR_D20/NC

DDR D21/NC R10 DDR_D21/NC DDR_D22/NC

DDR_D23/NC DDR_D24/NC

DDR_D25/NC DDR_D26/NC

DDR D27/NC B11 DDR_D27/NC DDR_D28/NC B9 DDR_D29/NC

DDR_D29/NC DDR_D30/NC

DDR_D31/NC

DDR_DQS0

DDR DOS2r

DDR_DQS3

DDR_DM0

DDR DM1

DDR_DQS3n

DDR_DM2/NC DDR_DM3/NC

G10 DDR_DQS01
G11 DDR_DQS1
P10 DDR_DQS1
P11 DDR_DQS2

U3500

Note: All the capacitor should be place close to

the power pin of LPDDR3.

FBGA178 13R00X11R50X1R20

F11 DDR_D7
F10 DDR_D8
DDR_D9
DDR_D10
E11 DDR_D11

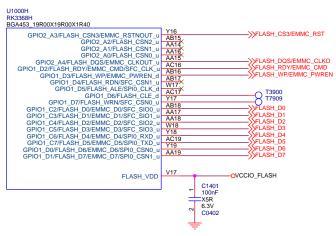
M10 M11

E10 E9 D9 T8

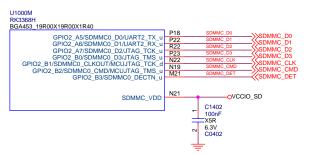
B8

D10

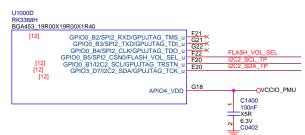
LPDDR3 FILTER



Note:All the capacitor should be place close to the power pin of RK3368.



Note:All the capacitor should be place close to the power pin of RK3368.



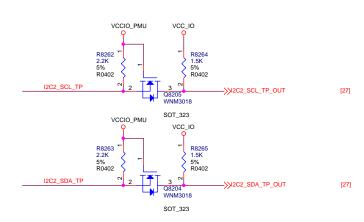
Note:All the capacitor should be place close to the power pin of RK3368.



	Driver	$T \cap$	CLI
T. TIMOTT	DTTACT	$\pm O$	

FLASH_VOL_SEL	FLASH_IO Voltage
1.8V or 3.3V	1.8V Driver IO
0V	3.3V Driver IO





Rockchip Fuzhou Rockchip Electronics				
Project:	RK3368H_demo			
File:	RK3368 FLASH/SDMMC Controler			
Date:	Tuesday, April 03, 2018	Rev:	V1.0	
Designed by:	wjx	Sheet:	11 of 27	

eMMC VCC_IO VCCIO_FLASH FLASH D0 R3900 1 DNP 2 0R 5% R0402 FLASH D2 FLASH_D3 U3900 IN OUT **GND** ΕN BP FLASH_D4 C3900 C3902 C3903 PT5108E23E-18 100nF FLASH_D5 10uF C3901 10uF /WL2801E-18 X5R X5R DNP X5R SOT_23_5 C0402 6.3V 6.3V 6.3V C0603 C0603 C0402 Note: FLASH_RDY/EMMC_CMD 2 10K 5% R0402 [11] Close to eMMC or Nand Flash VCCIO_FLASH U4000 FLASH D0 НЗ AA5 C4000 C4001 C4002 FLASH DO DATA0 VCCQ1 FLASH D1 H4 AA3 100nF 100nF 100nF FLASH D1 VCCQ2 DATA1 FLASH_D2 H5 X5R Y4 X5R X5R [11] FLASH_D2 DATA2 VCCQ3 FLASH_D3 J2 W4 6.3V 6.3V 6.3V FLASH D3 7 7 DATA3 VCCQ4 C0402 @eMMC J3 J4 K6 C0402 C0402 111 FLASH_D4 DATA4 VCCQ5 ____C0402 ___@eMMC [11] FLASH_D5 DATA5 FLASH D6 J5 [11] FLASH D6 DATA6 VCC1 FLASH_D7 VCC_IO J6 T10 FLASH_D7 [11] DATA7 VCC2 N5 VCC3 FLASH RDY/EMMC CMD W5 M6 CMD VCC4 FLASH_DQS/EMMC_CLKO\\ FLASH_DQS/EMMC_CLKO R4001 1 QeMMC2 33R 5% W6 CLK VSS1 R10 P5 C4003 C4004 VSS2 FLASH_WP/EMMC_PWREN U5 100nF 100nF FLASH WP/EMMC PWREN RST n VSS3 R8247 M7 X5R X5R VSS4 K2 H6 6.3V 6.3V FLASH_CS3/EMMC_RST << VDDi VSS5 C0402 C0402 VSS6 = @eMMC = @eMMC × R5 R4002 C4005 DNP **RCLK** DNP 100nF AA6 VSSQ1 VSSQ2 R0402 R0402 М9 AA4 X5R T4000 VSF1 @eMMC 6.3V M10 Y5 @eMMC VSF2 VSSQ3 T4001 C0402 N10 Y2 T4002 VSF3 VSSQ4 U10 K4 VSF4 VSSQ5 T4003 [11,12] BGA169 18R00X14R00X1R20 Note: All the capacitor should be place close to the power pin of eMMC.

->>FLASH_DQS/EMMC_CLKO T3902 () T3903 O

Note:

[11,12]

[11]

[11]

VCCIO FLASH

RP4000

10K @eMMC RP4 0408

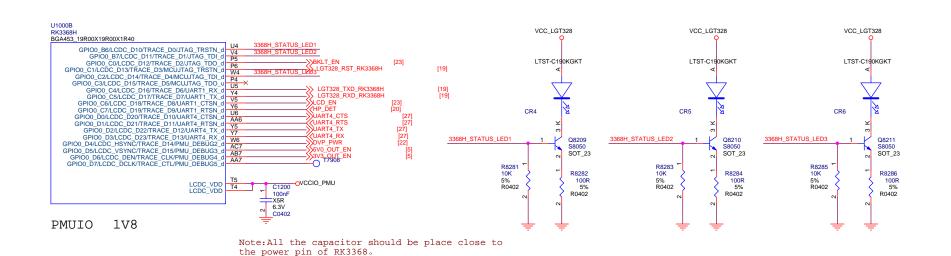
6

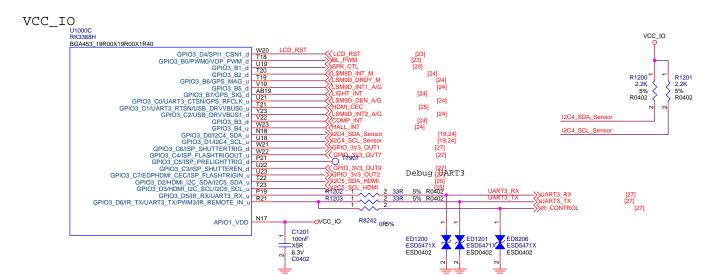
10K @eMMC RP4_0408

3 ~~~

Reserve PAD for eMMC or tSD Update.

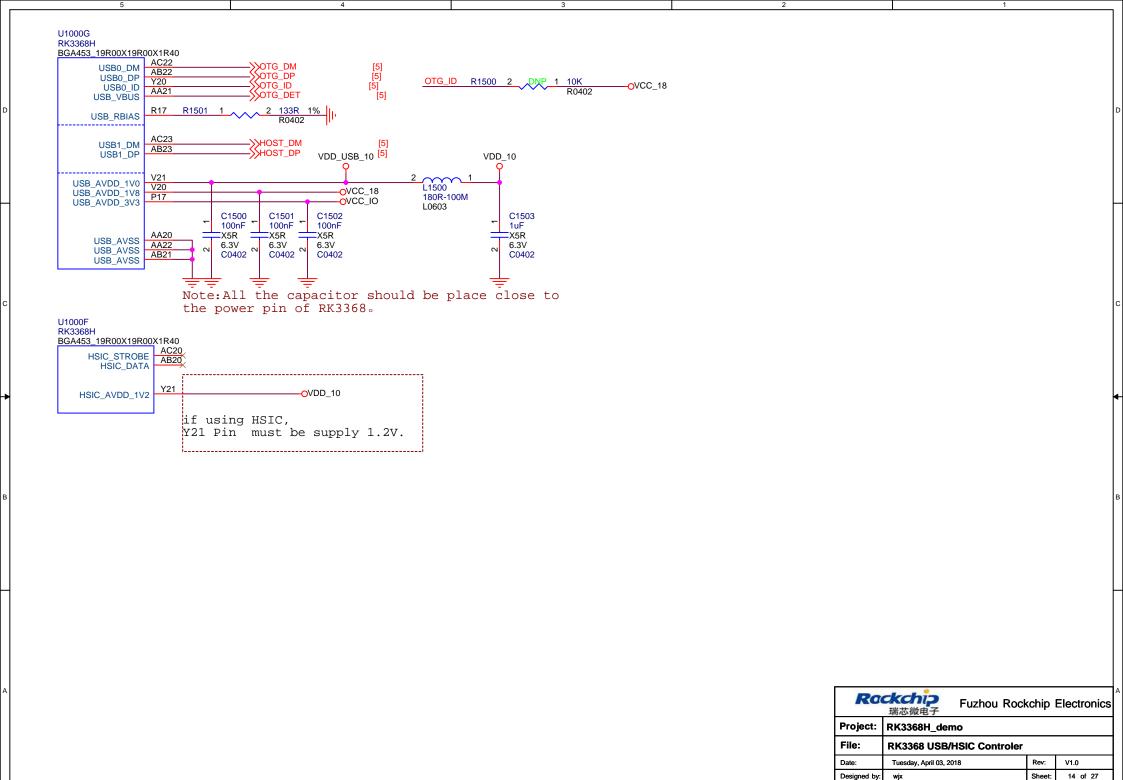
Ra	ckchip 瑞芯微电子	Fuzhou	Rock	chip	Electronics
Project:	RK3368H_den	no			·
File:	Flash-eMMC-Default				
Date:	Tuesday, April 03, 20	118		Rev:	V1.0
Designed by:	wjx			Sheet:	12 of 27





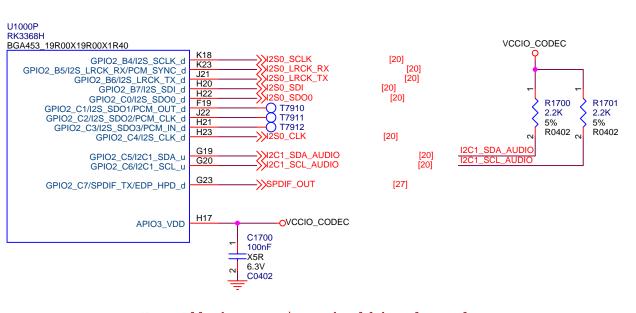
Note: All the capacitor should be place close to the power pin of RK3368.

KChip 瑞芯微电子 Fuzhou	Rockchip	Electronics	
RK3368H_demo			
RK3368 GPIO Interface			
Tuesday, April 03, 2018	Rev:	V1.0	
wjx	Sheet:	13 of 27	
	孫志微电子 RK3368H_demo RK3368 GPIO Interface Tuesday, April 03, 2018	屬芯價电子 RK3368H_demo RK3368 GPIO Interface Tuesday, April 03, 2018 Rev:	

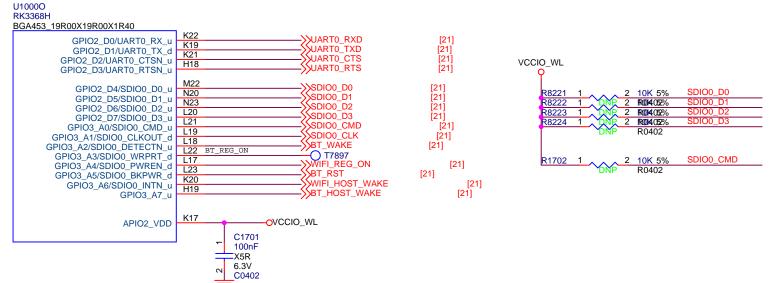


wjx

Sheet:

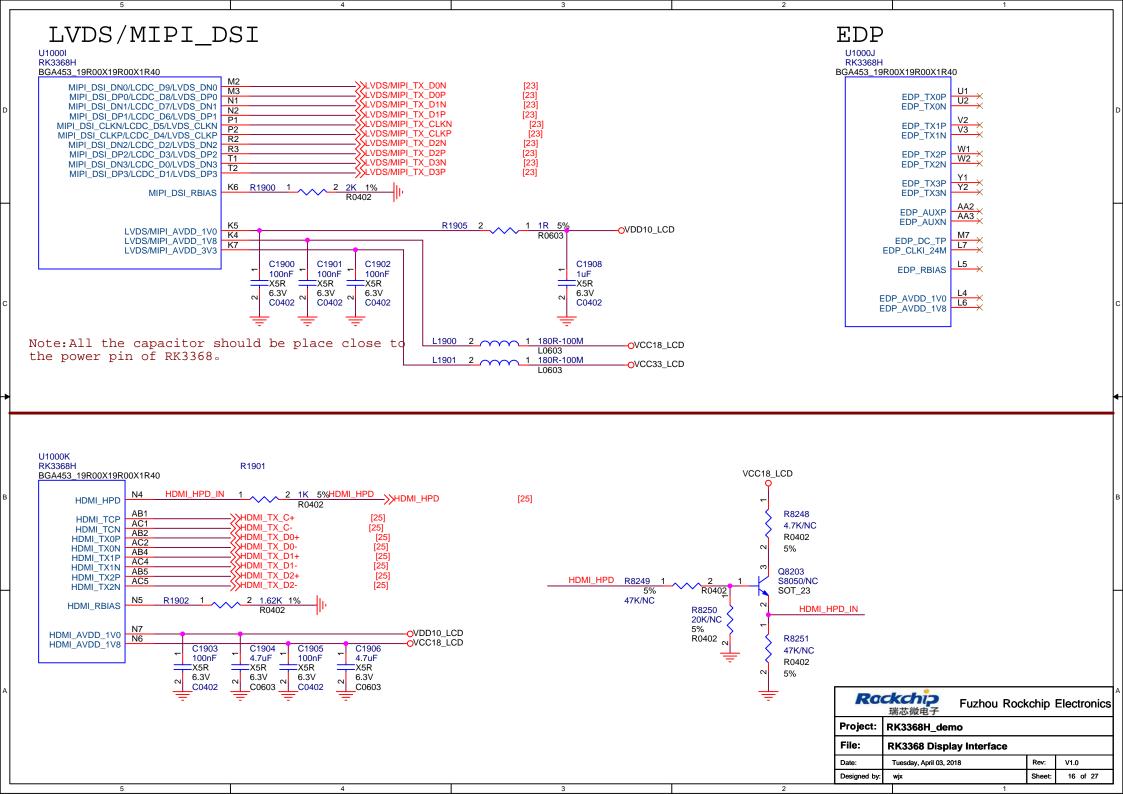


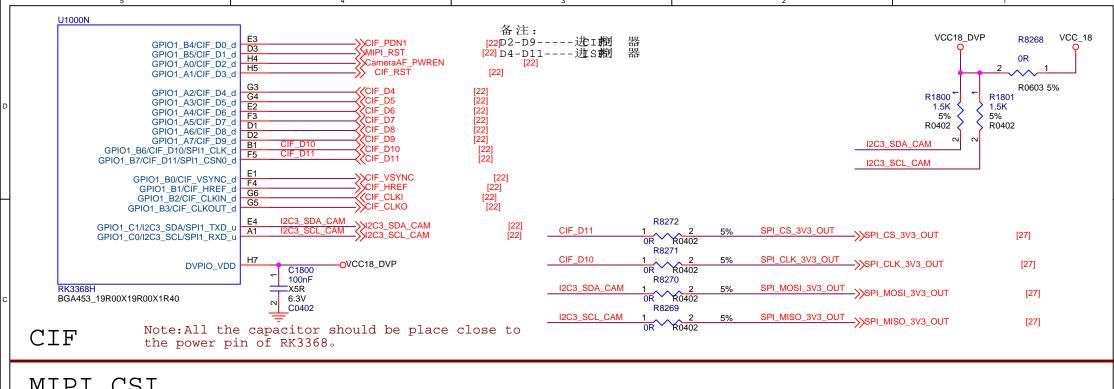
Note: All the capacitor should be place close to the power pin of RK3368.



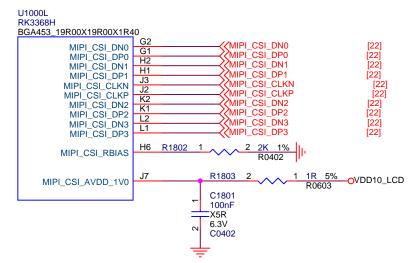
Note: All the capacitor should be place close to the power pin of RK3368.

Rockchip Fuzhou Rockchip Electronics				
Project:	RK3368H_demo			
File:	RK3368 SDIO0/UART0/I2C1			
Date:	Tuesday, April 03, 2018	Rev:	V1.0	
Designed by:	wjx	Sheet:	15 of 27	



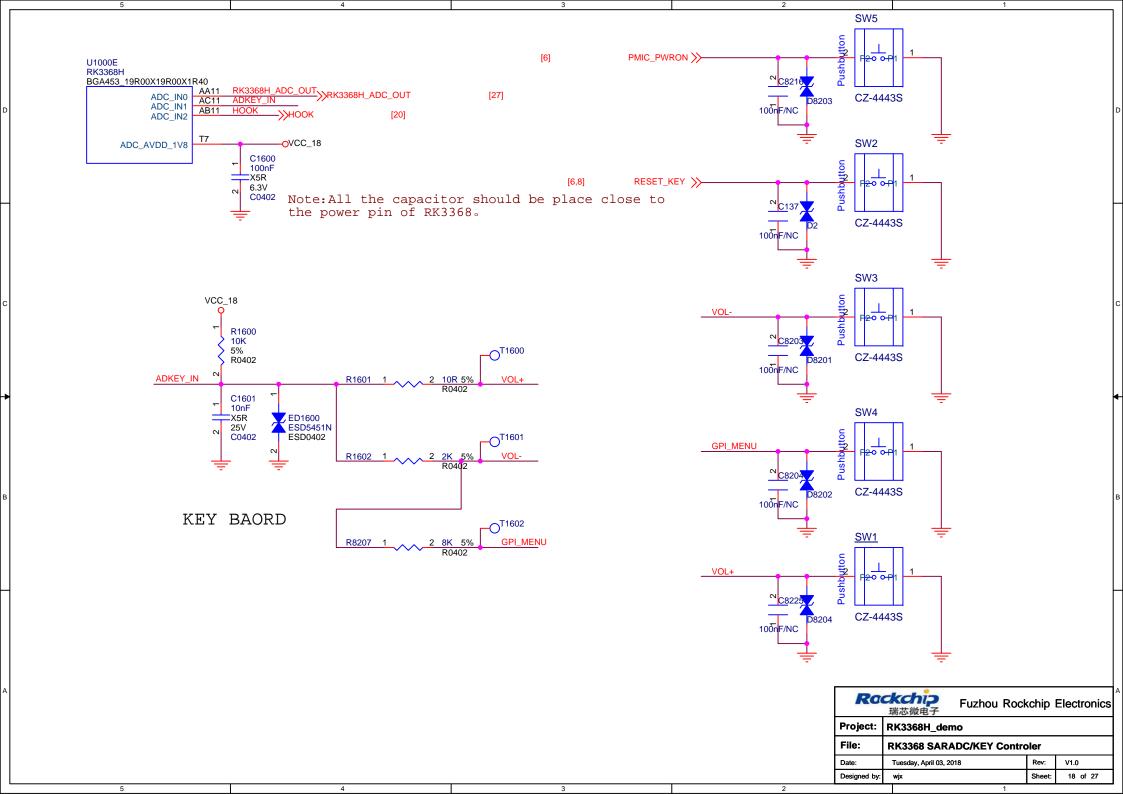


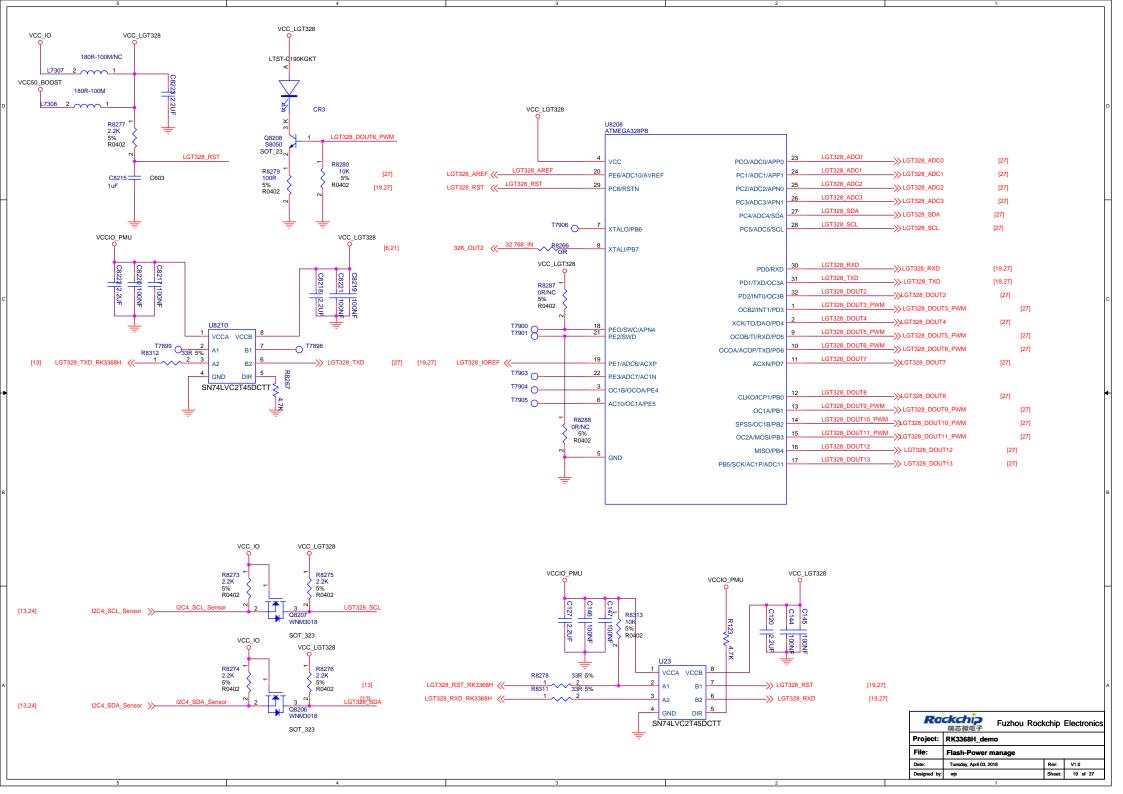
MIPI CSI

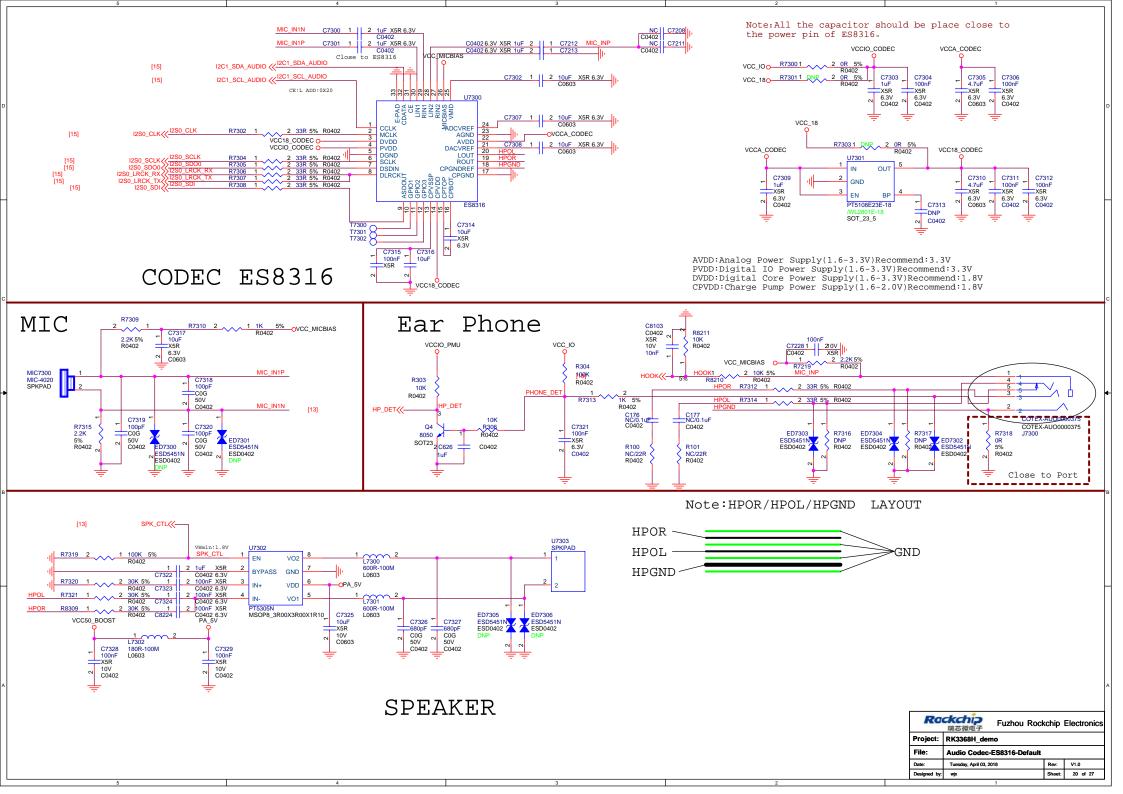


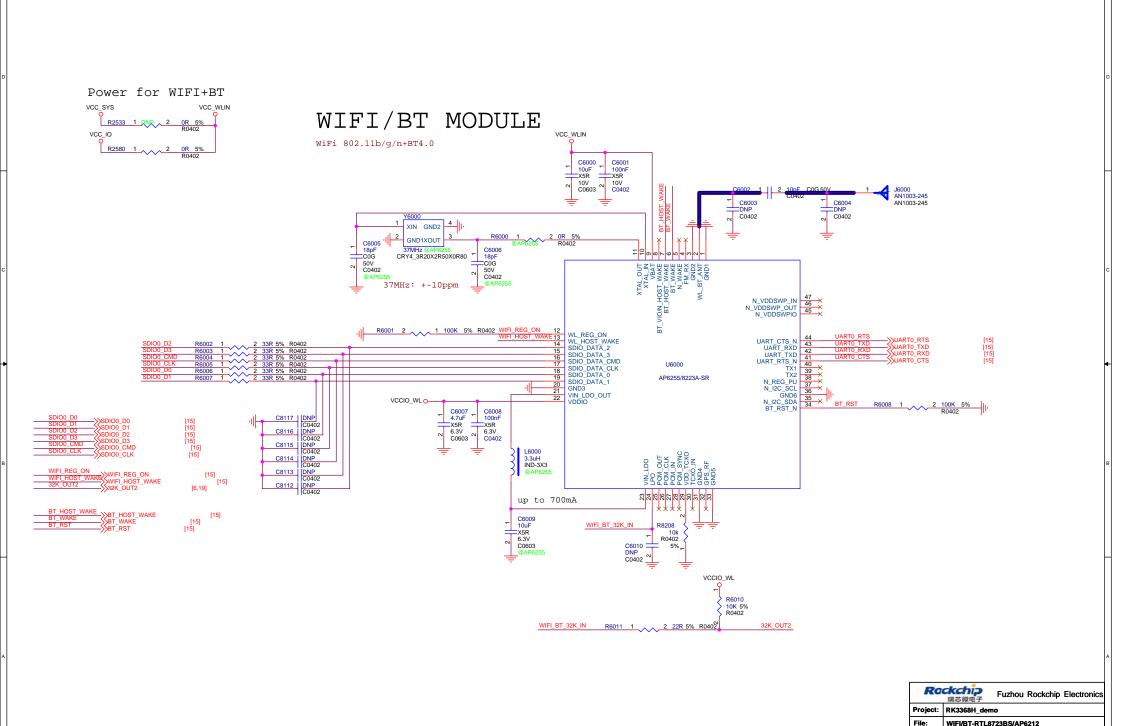
Note: All the capacitor should be place close to the power pin of RK3368.

Ro	はない Fuzhou F 瑞芯微电子	Rockchip	Electronics	
Project:	RK3368H_demo			
File:	RK3368 DVP/MIPICSI Interface			
Date:	Tuesday, April 03, 2018	Rev:	V1.0	
Designed by:	wjx	Sheet:	17 of 27	
_	1			







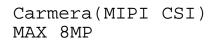


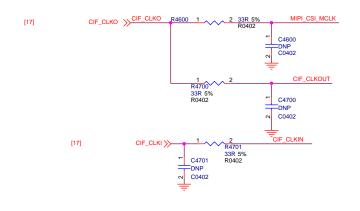
Tuesday, April 03, 2018

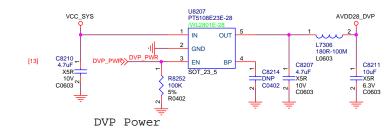
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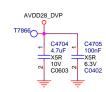
Rev: V1.0 Sheet:

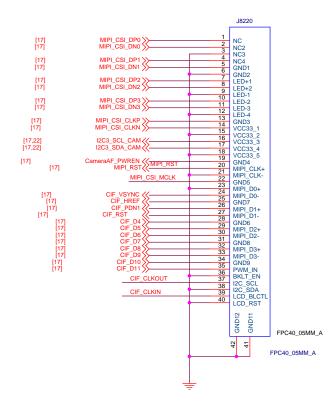
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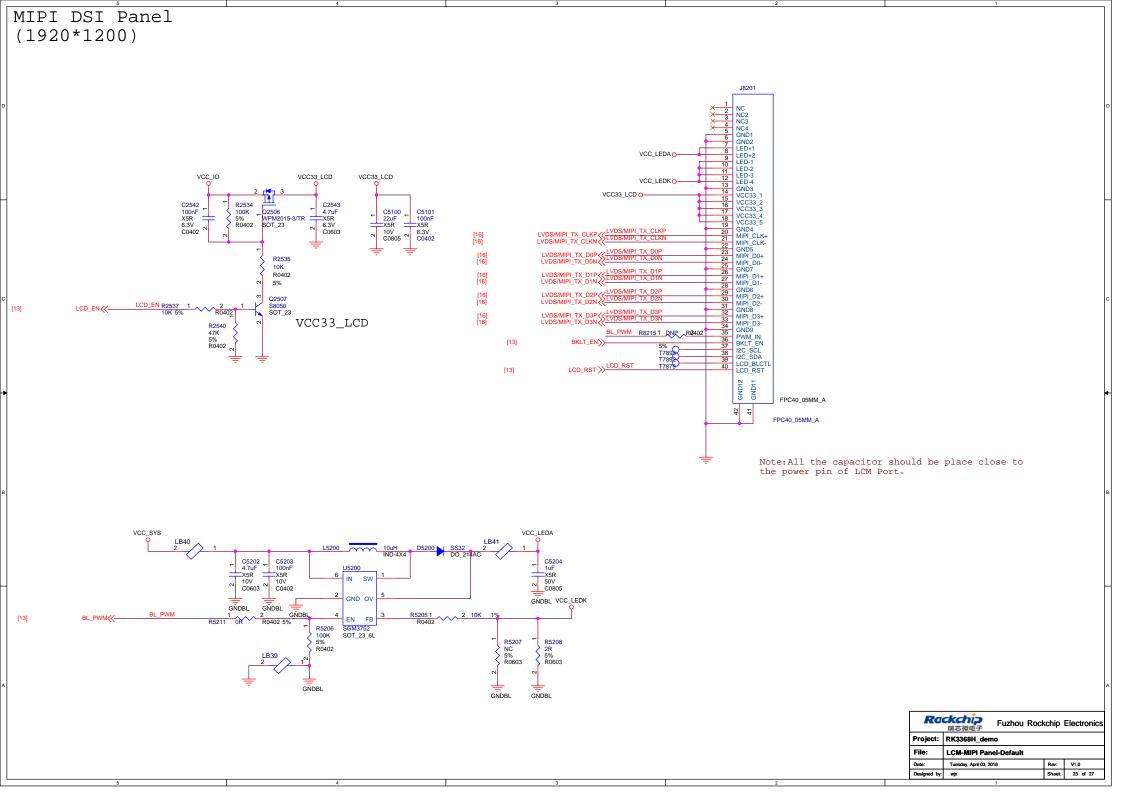


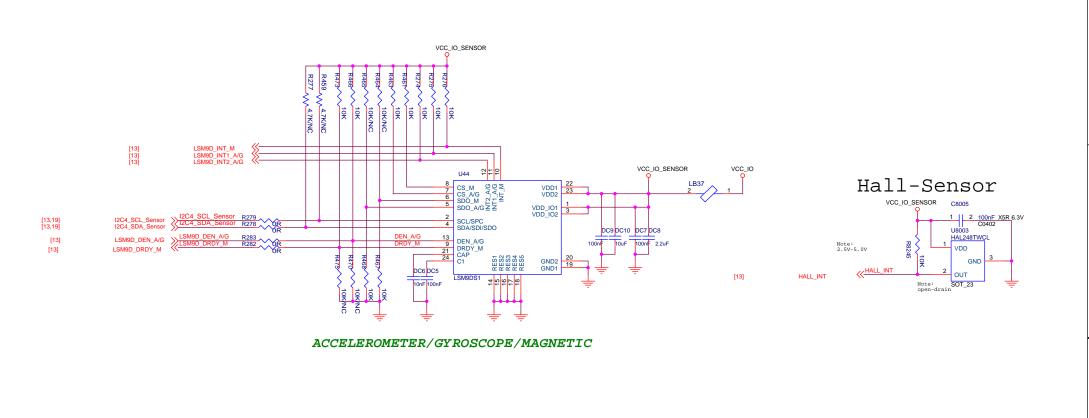


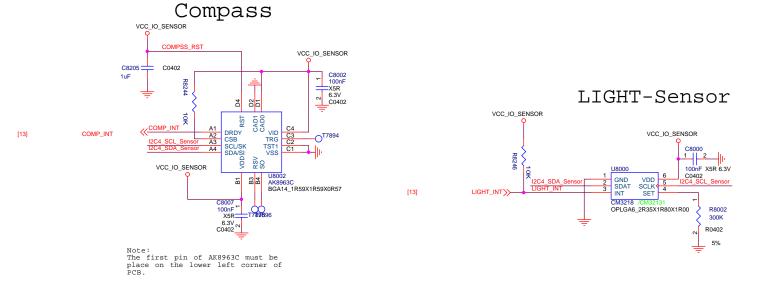


Note:All the capacitor should be place close to the power pin of Camera Port $\!\!\!\!^{\circ}$

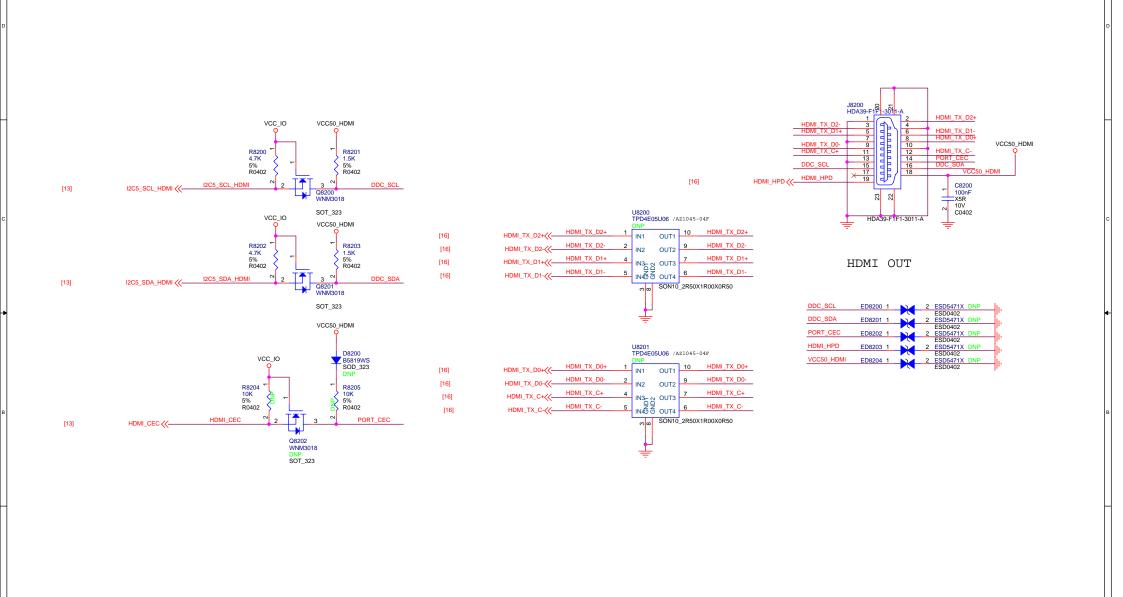
Ro	ckchip 瑞芯微电子	Fuzhou	Rockchip	Electronics
Project:	RK3368H_der	no		
File:	Camera-MIPI CSI			
Date:	Tuesday, April 03, 2	018	Rev:	V1.0
Designed by:	wjx		Sheet:	22 of 27







Ro	Rockchip 端芯微电子 Fuzhou Rockchip Electronics				
Project:	RK3368H_demo				
File:	Sensor/VIB				
Date:	Tuesday, April 03, 2018	Rev:	V1.0		
Designed by:	wjx	Sheet:	24 of 27		



Ra	Rockchip 端芯微电子		Rockch	ip	Electronics
Project:	RK3368H_demo				
File:	HDMI OUT Port				
Date:	Tuesday, April 03, 2	018	Re	v:	V1.1
Designed by:	Zhangdz		Sh	eet:	25 of 27
		1			

