Design of a high speed 4-bit Carry Look-Ahead Adder

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Abstract—**Adders are very important components of ALU and making adders faster and more efficient will lead to lower run-time of computer programs. There are many adders of which the CLA adders are the fastest. In this paper the CLA architecture implemented computes carry out terms without using the conventional method of using carry-propagate and carry-generate signals.**

Keywords—*Adders, CLA.*

I. REFERENCE CIRCUIT DETAILS

Figure-1[1] shows the architecture of unconventional 4-bit Carry Look-Ahead adder without the carry propagate and carry generate signals directly used for carry bit generation. In this architecture all the input signals are directly connected to the CLA circuits for carry bit generation. The sum bit is generated using the design same as the conventional design.

In order to generate the carry bits using CLA circuit by only using the input signals (A_i, B_i and C_0), it is necessary to use the simplified Boolean equation of carry bit which is given as follows:

$$C_1 = A_0B_0 + C_0(A_0 + B_0)$$

Figure-2 shows the improvement in the timing delays. It shows the decrease in rising and falling delays of this CLA architecture when compared to the conventional CLA architecture.
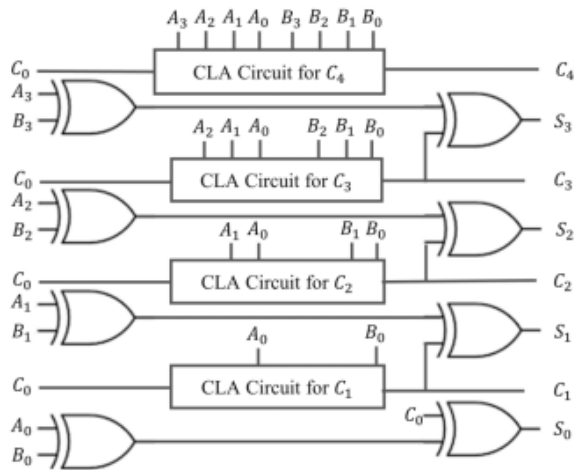

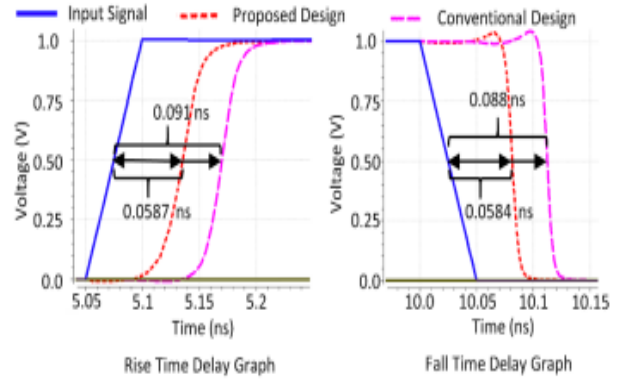Figure 1 (Reference Circuit Diagram)

Figure 2 (Reference waveform)

II. PROPAGATION DELAY AND POWER ESTIMATION

The proposed design of the 4-bit CLA architecture consumes 7.47 µW of average power and propagation delay of 0.0586 ns. The simulation has been conducted utilizing Cadence design and simulation tools with the technology node of 45 nm. The source voltage used is 1 V. [2]

III. REFERENCE PAPERS/ JOURNALS

[1] Mehedi Hasan, Abdul Hasib Siddique, Abdal Haque Mondol, Mainul Hossain, Hasan U. Zaman, Sharnali Islam. "High Performance Design of a 4-bit Carry Look-Ahead Adder in Static CMOS Logic". Article in Indonesian Journal of Electrical Engineering and Informatics (IJEEI) · December 2020

[2] Mehedi Hasan, Abdul Hasib Siddique, Abdal Haque Mondol, Mainul Hossain, Hasan U. Zaman, Sharnali Islam. "High Performance Design of a 4-bit Carry Look-Ahead Adder in Static CMOS Logic". Article in Indonesian Journal of Electrical Engineering and Informatics (IJEEI) · December 2020