INDIAN INSTITUTE OF INFORMATION TECHNOLOGY BHAGALPUR

VLSI MANUAL LAB REPORT

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1. *Input & Output characteristics of NMOS using EDA Tool.*
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3. *DC Analysis of CMOS Inverter*
4. *Transient Analysis of CMOS Inverter*
5. *NAND and NOR Gates using PMOS & NMOS.*

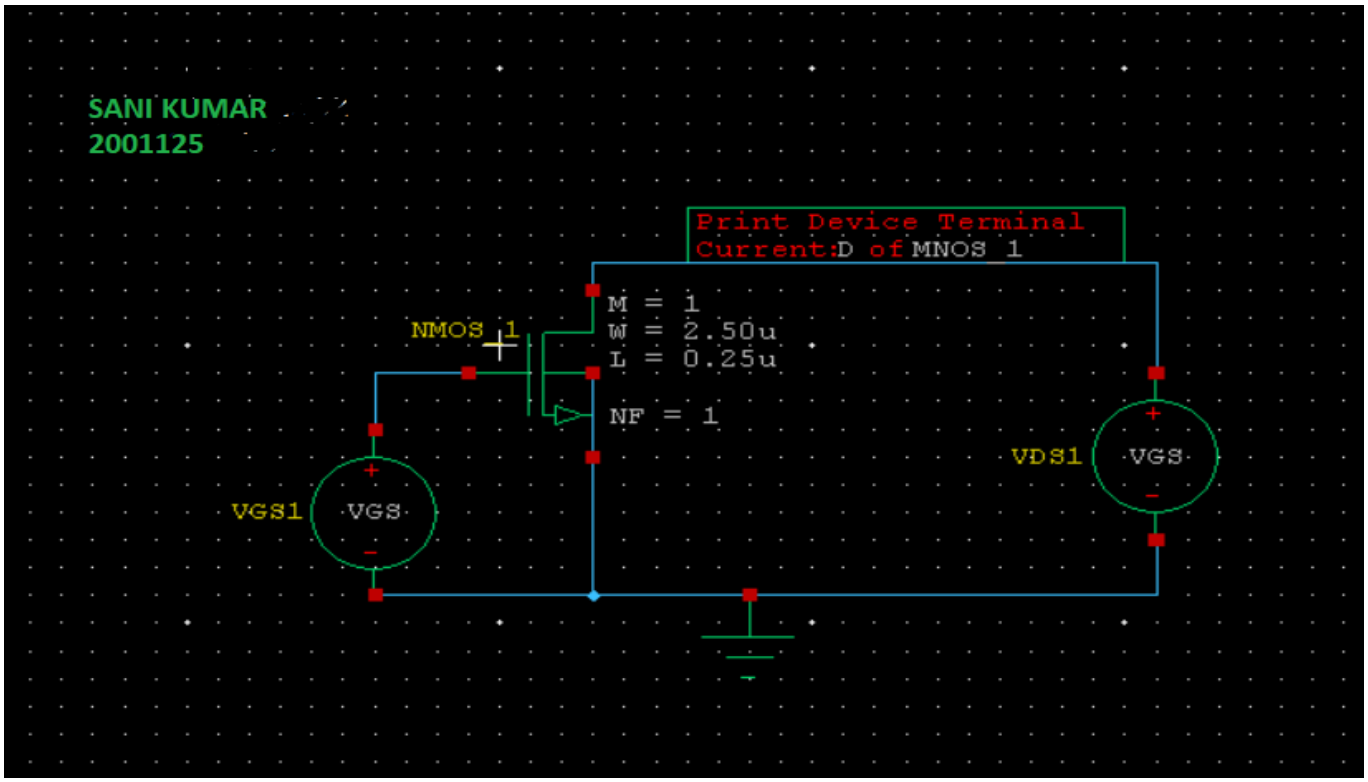
Experiment 1

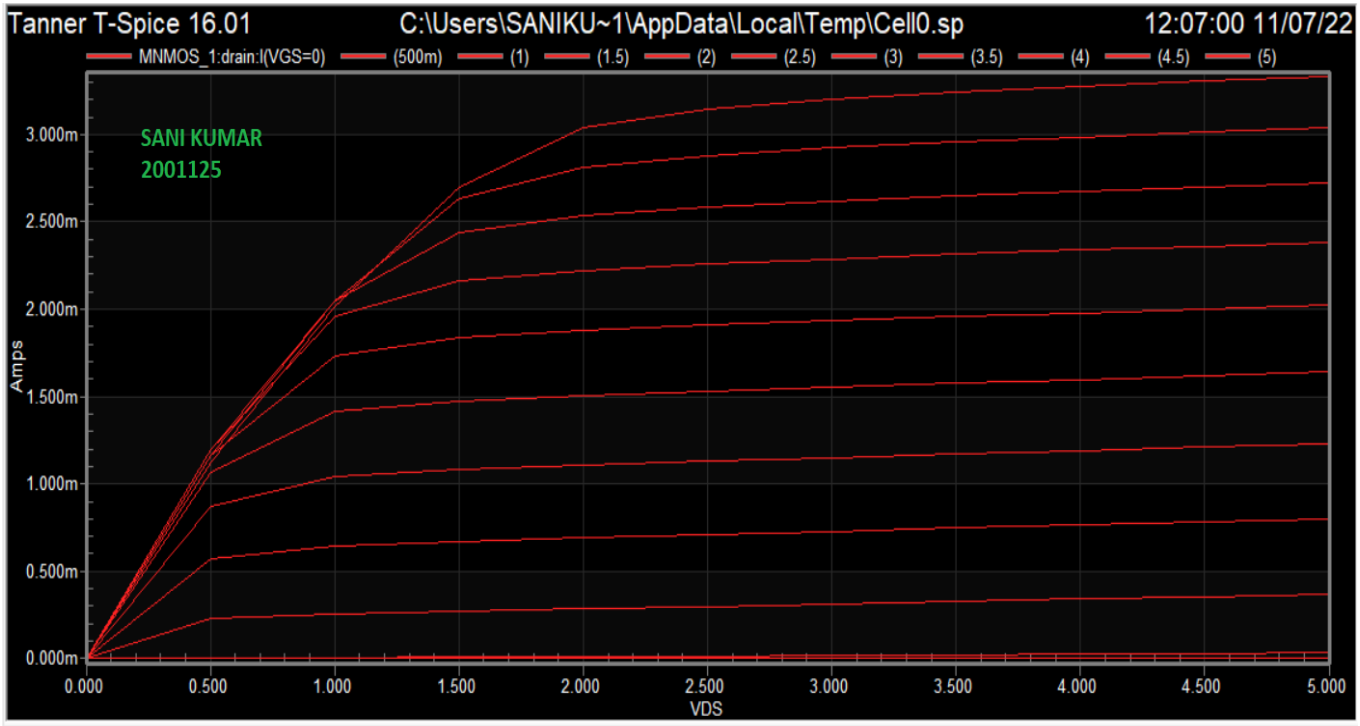
Aim- To analyse input and output characteristics of NMOS using EDA tool.

Software Required- Tanner EDA tool.

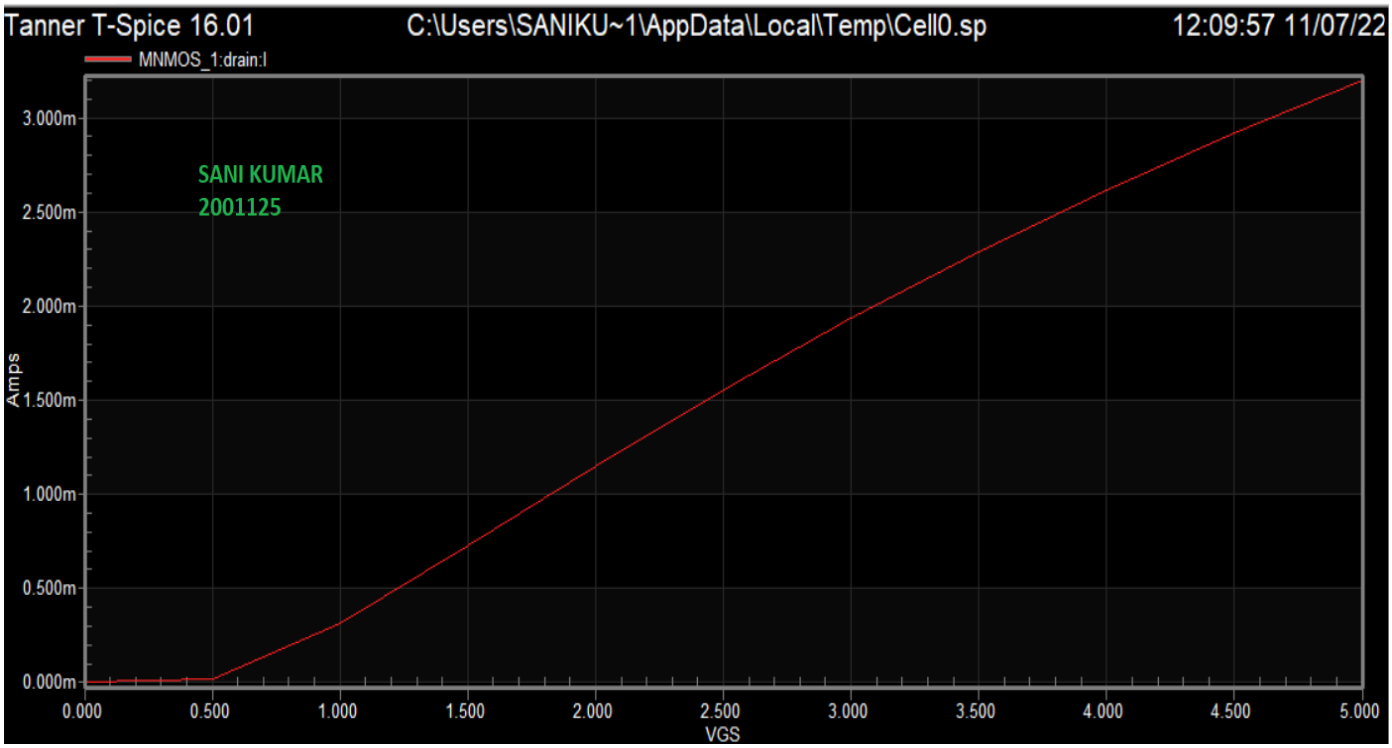
Theory- N type MOSFET is form by taking p substrate and two high doped n is diffused in this p substrate. These two are taking as drain and source. Between drain and source channel is formed. NMOS is in the cut off region when gate to source voltage (Vgs) is negative. So for enhancement mode Vgs is greater than threshold voltage.

Diagram:-





Output characteristic



Input characteristic

Conclusion- Hence, by taking V_{gs} constant we got the above output characteristics.

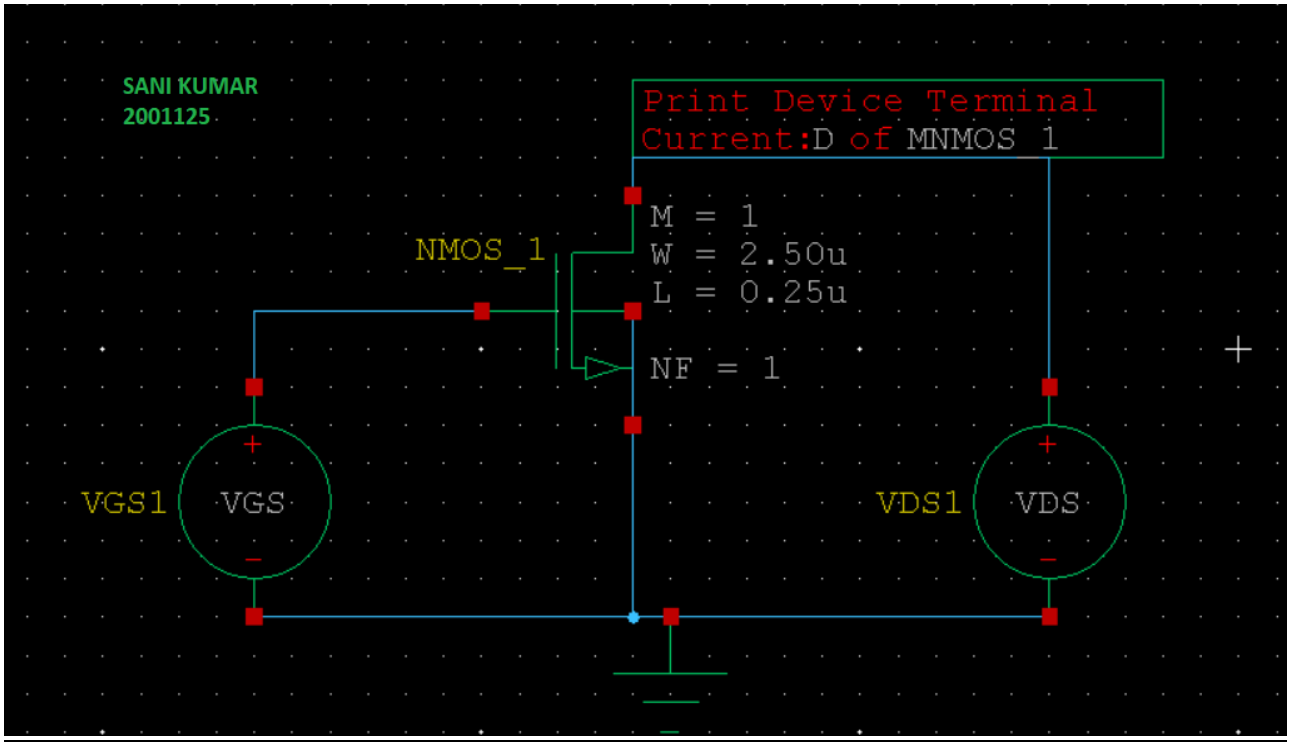
Experiment 2

Aim- To analyse input and output characteristics of PMOS using EDA tool.

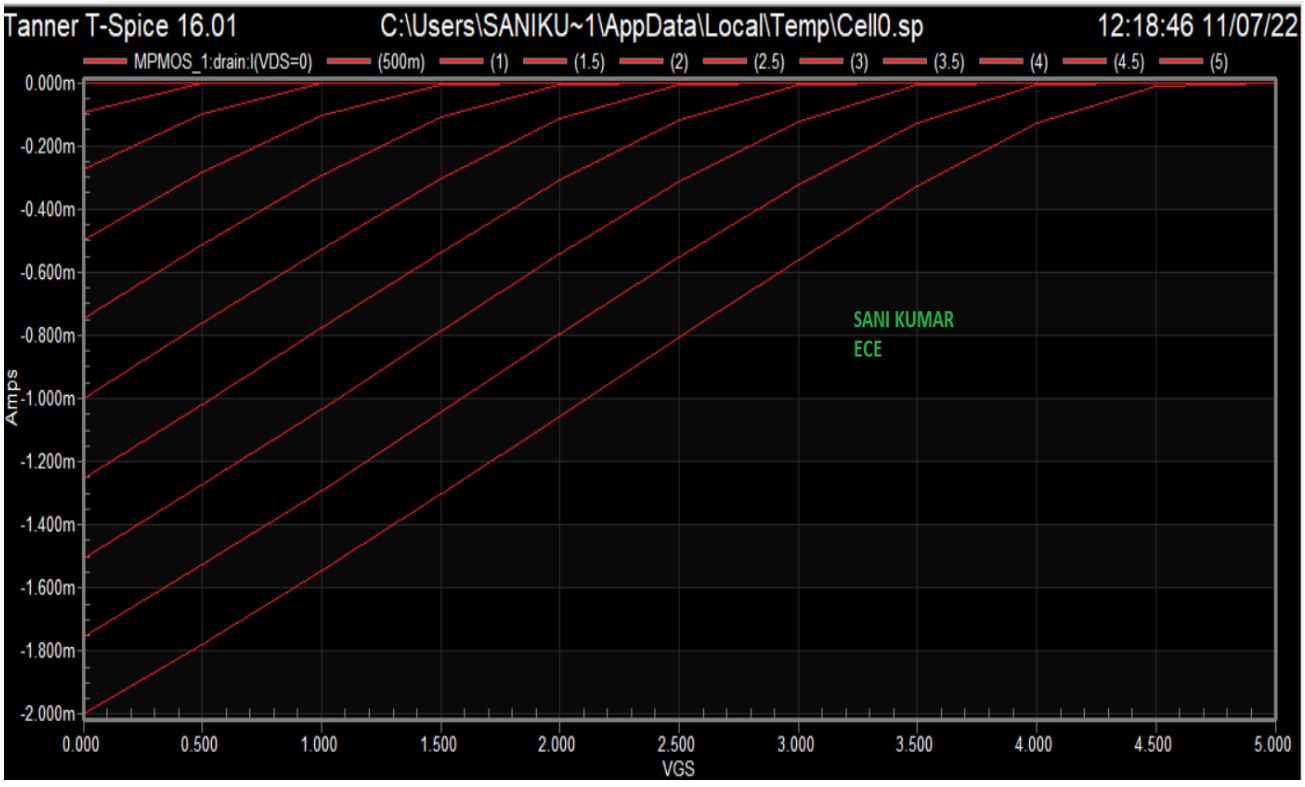
Software Required- Tanner EDA tool.

Theory- PMOS is behaving just opposite to NMOS. PMOS is made by taking N type substrate and doped TWO high doped P in N type substrate. PMOS is working when gate to source voltage is negative. So in this analysis we apply negative voltage to gate and drain.

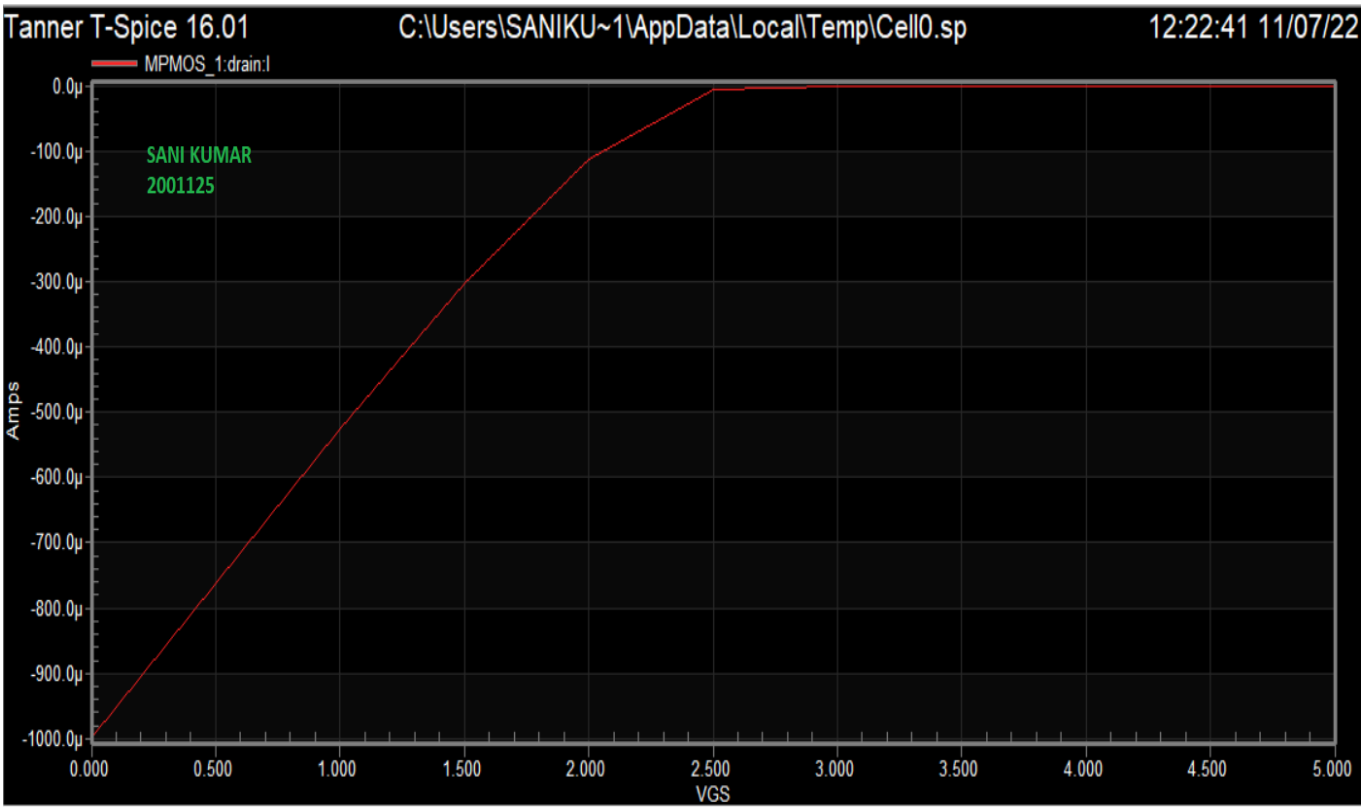
Circuit Diagram-



Output-



Output Characteristic



Conclusion- Hence, by taking V_{ds} constant we get the above desired curve.

Experiment 3

Aim- DC analysis of CMOS inverter using Tanner EDA tool.

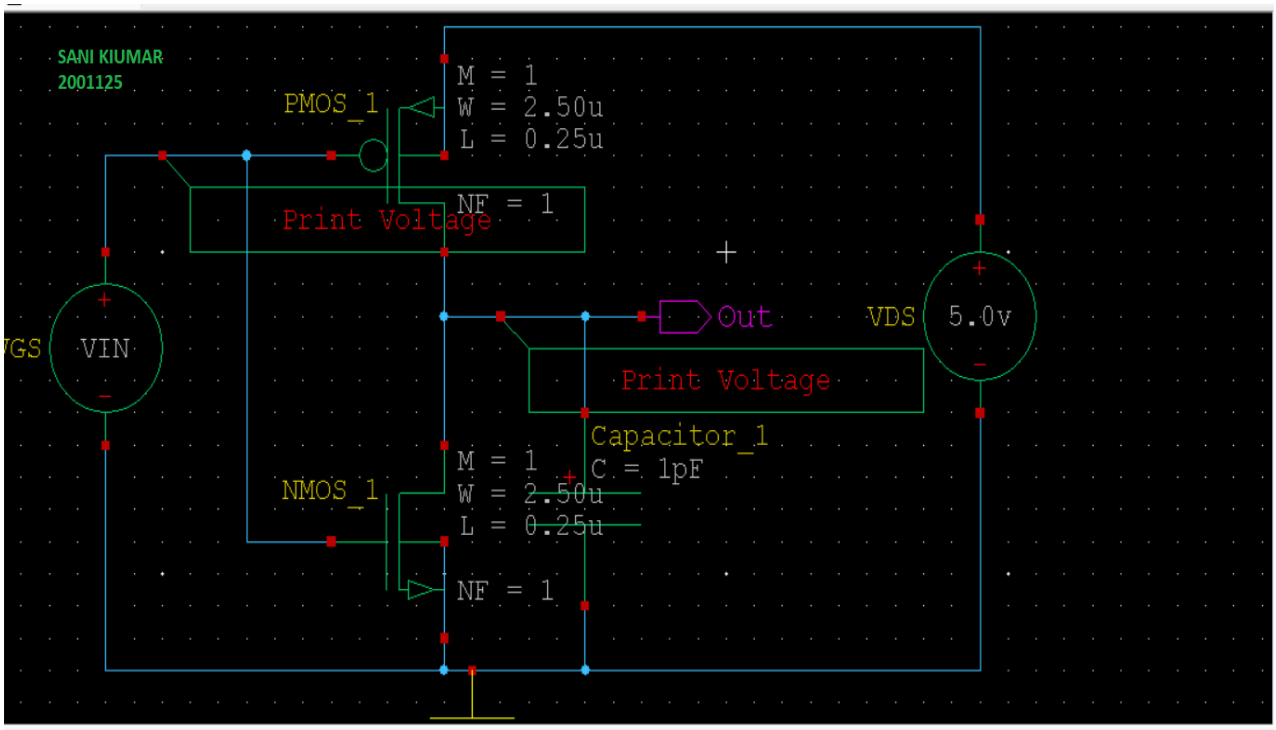
Software Required- Tanner EDA tool.

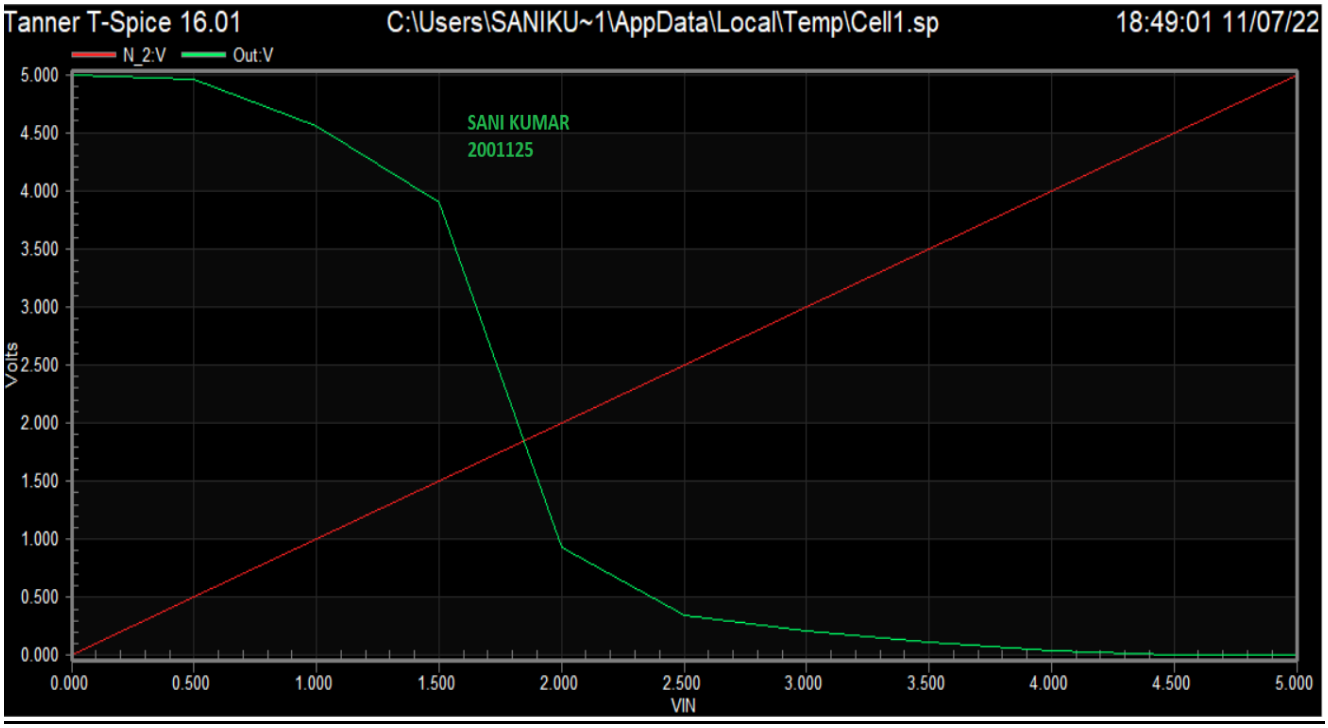
Theory- A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, where VIN is connected to the gate terminals and VOUT is connected to the drain terminals. It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS

and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter's operations can be seen very easily.

Circuit Diagram and Output-

1.





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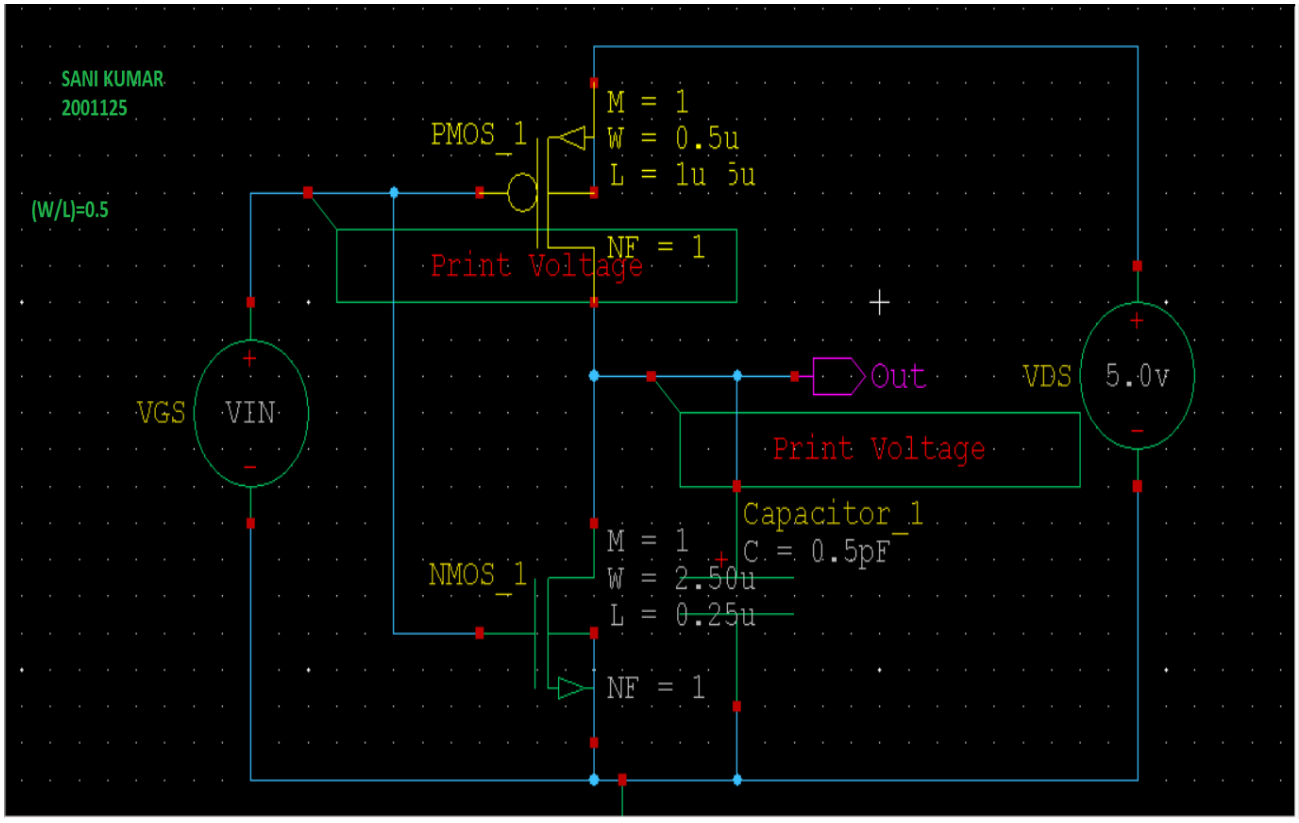
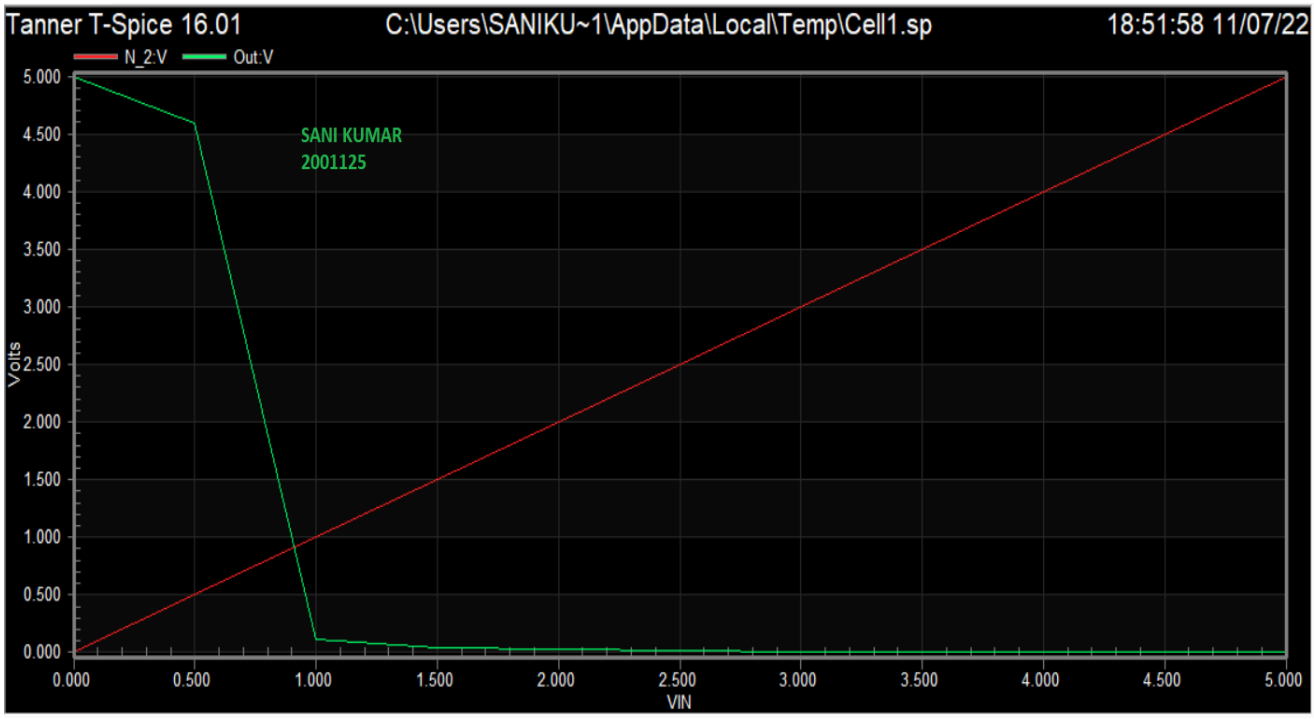
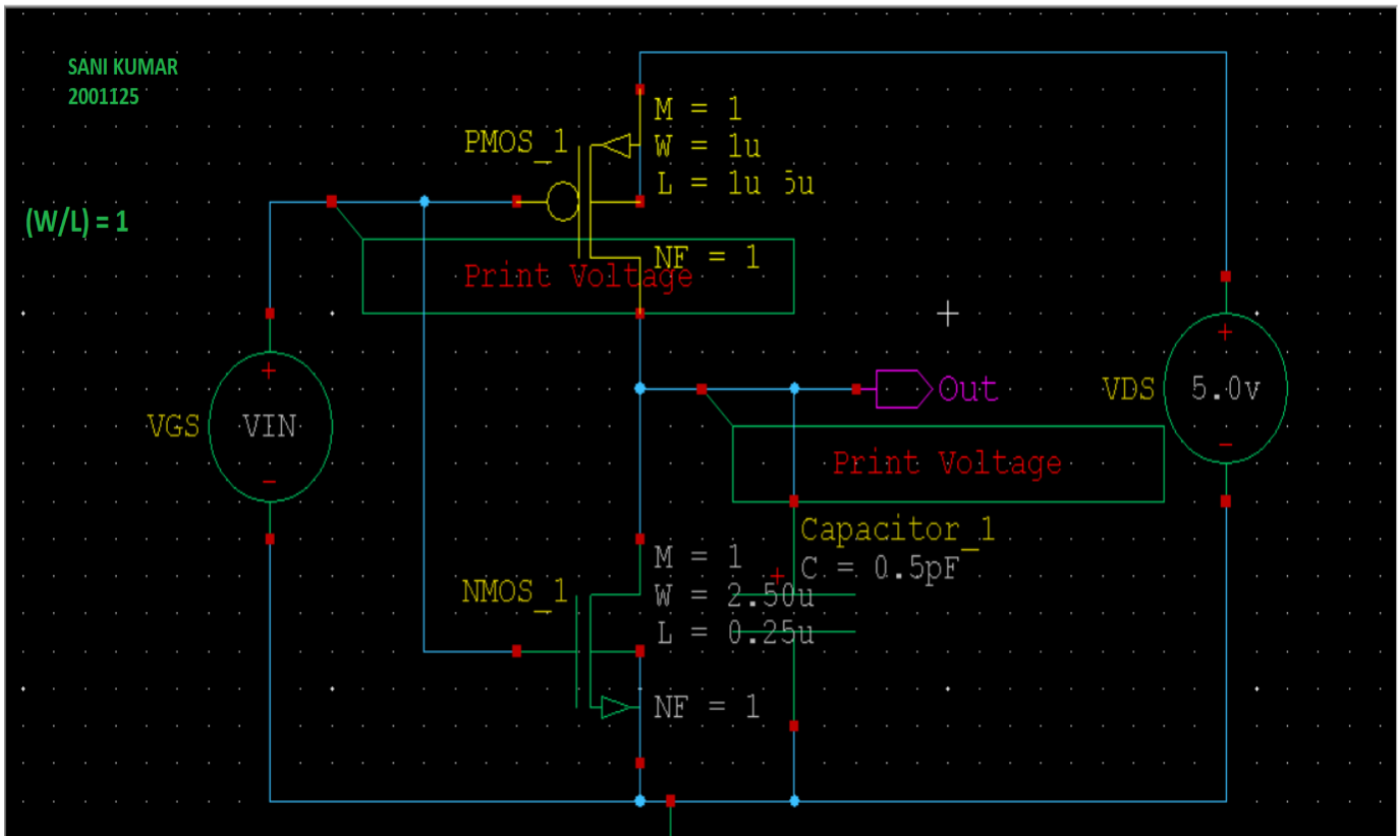
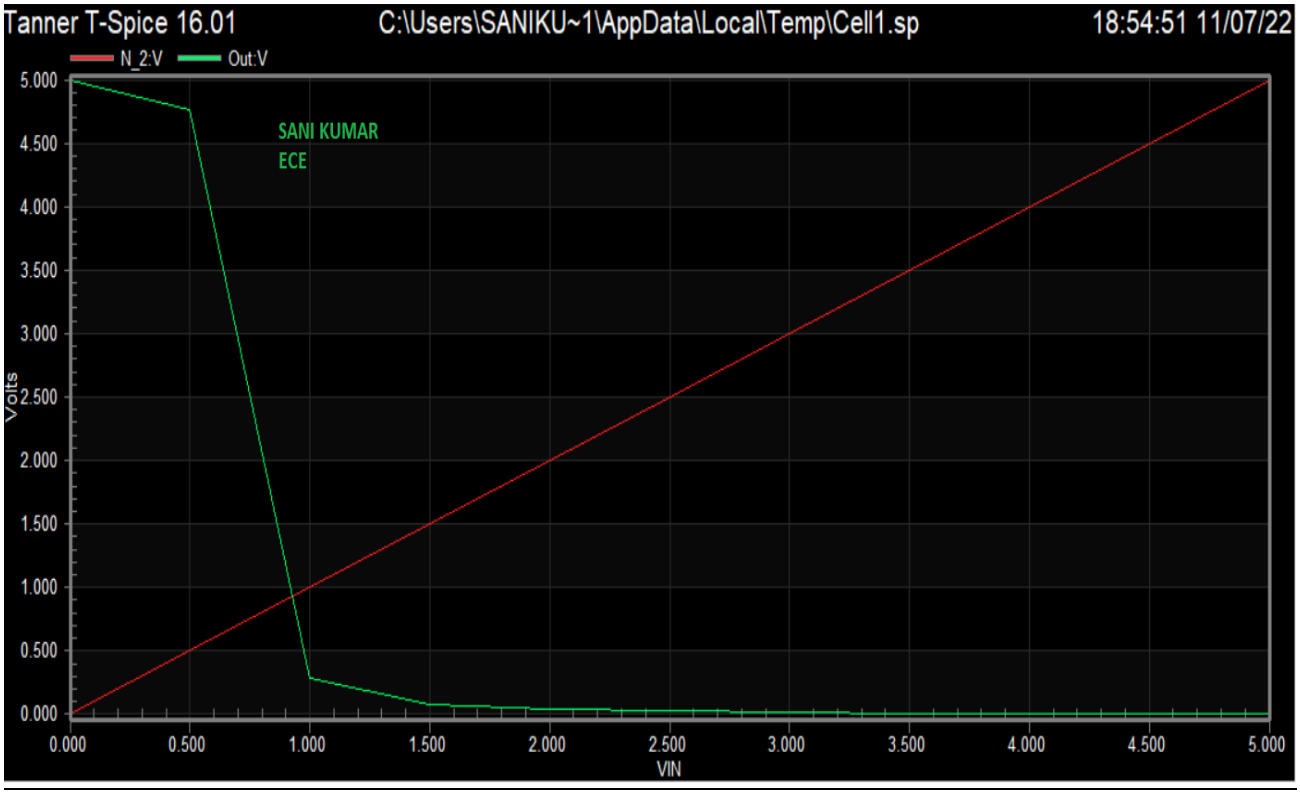

SANI KUMAR
2001125
(W/L)=0.5
PMOS_1
M = 1
W = 0.5u
L = 1u 5u
NF = 1
Print Voltage
VGS
VIN
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.5pF
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1


Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
18:51:58 11/07/22
N_2:V
Out:V
SANI KUMAR
2001125
Volts
VIN
5.000
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
0.500
0.000

3.


SANI KUMAR
2001125
(W/L) = 1
PMOS_1
M = 1
W = 1u
L = 1u
NF = 1
Print Voltage
VGS
VIN
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.5pF
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1


Tanner T-Spice 16.01
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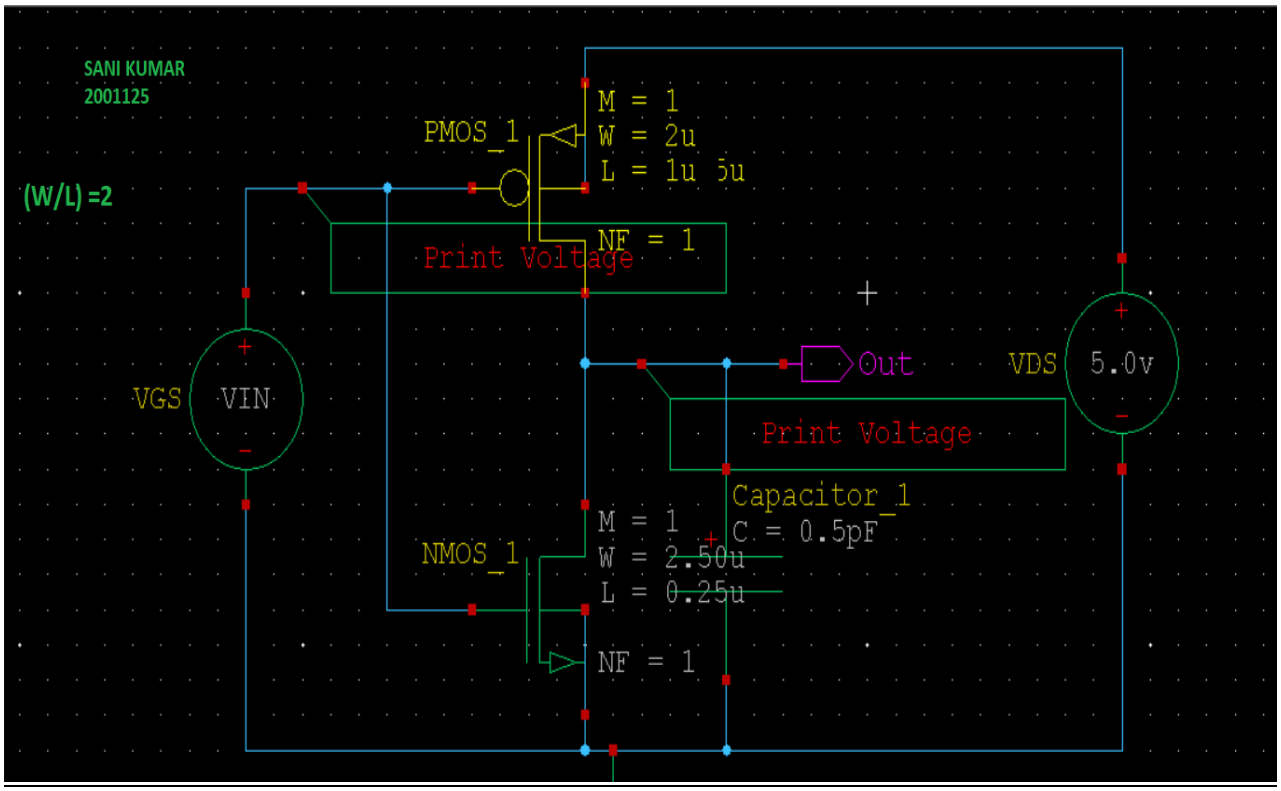
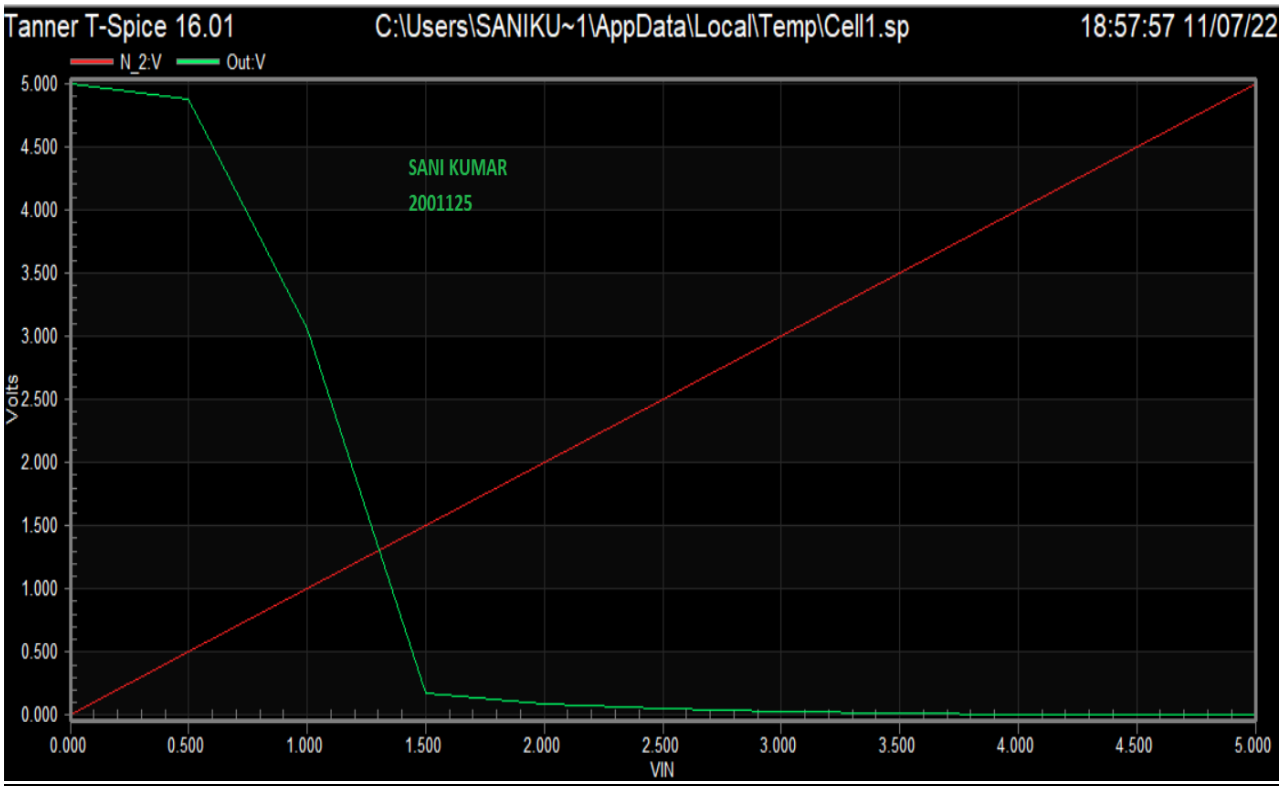
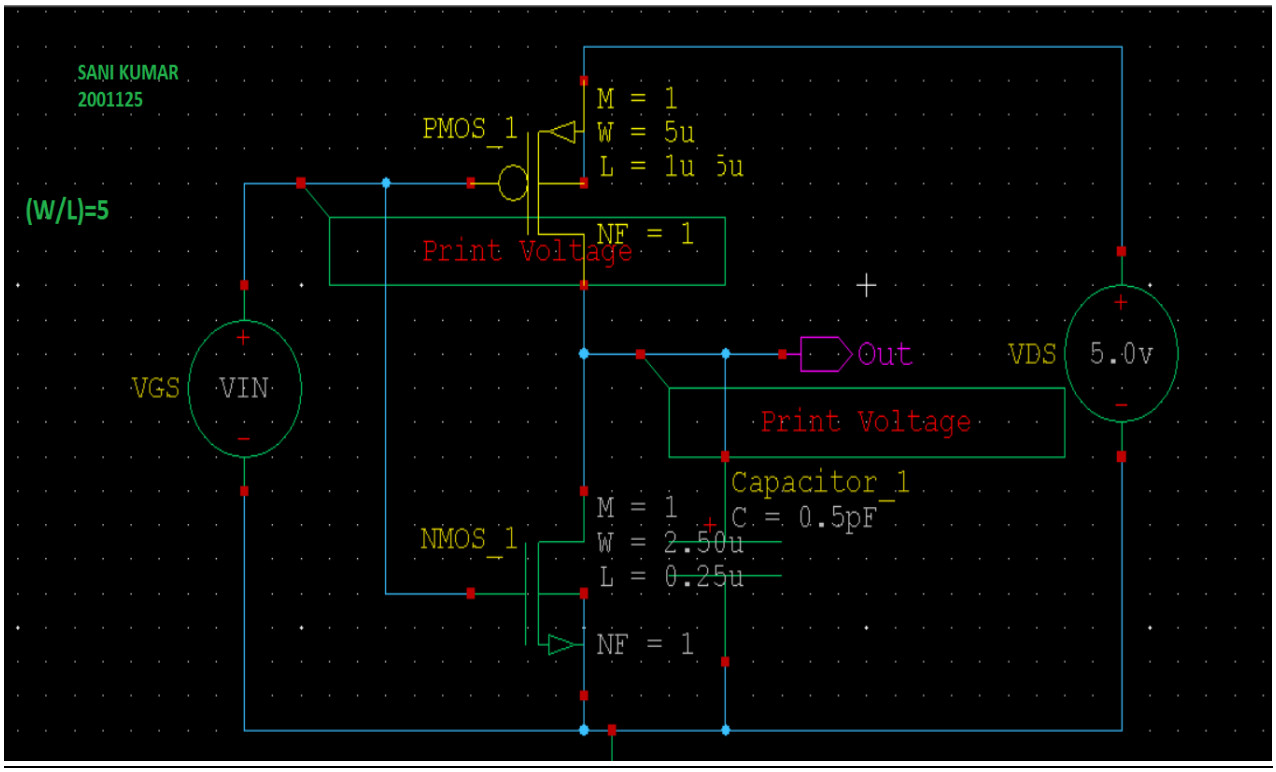
18:54:51 11/07/22
N_2:V
Out:V
SANI KUMAR
ECE
Volts
VIN
0.000
0.500
1.000
1.500
2.000
2.500
3.000
3.500
4.000
4.500
5.000

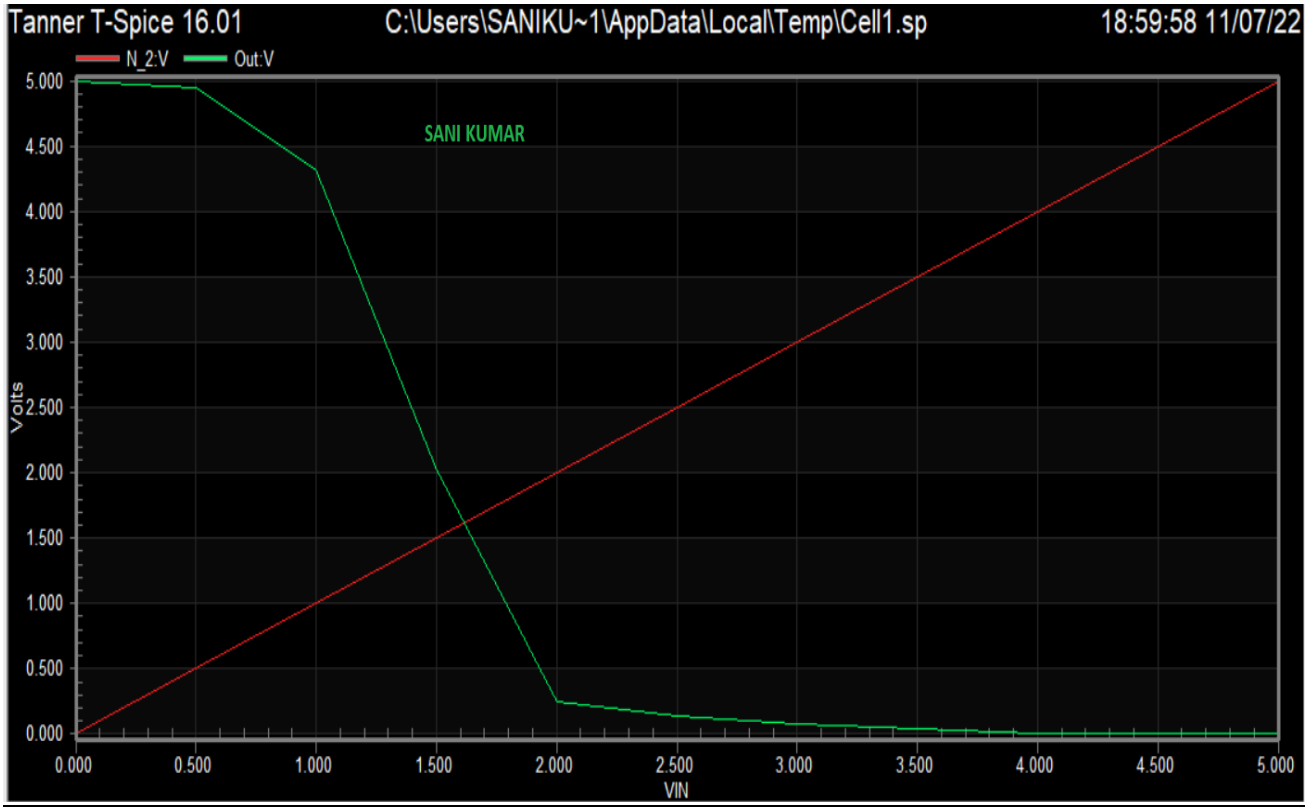
4.


SANI KUMAR
2001125
(W/L) =2
PMOS_1
M = 1
W = 2u
L = 1u 5u
NF = 1
Print Voltage
VGS
VIN
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.5pF
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1

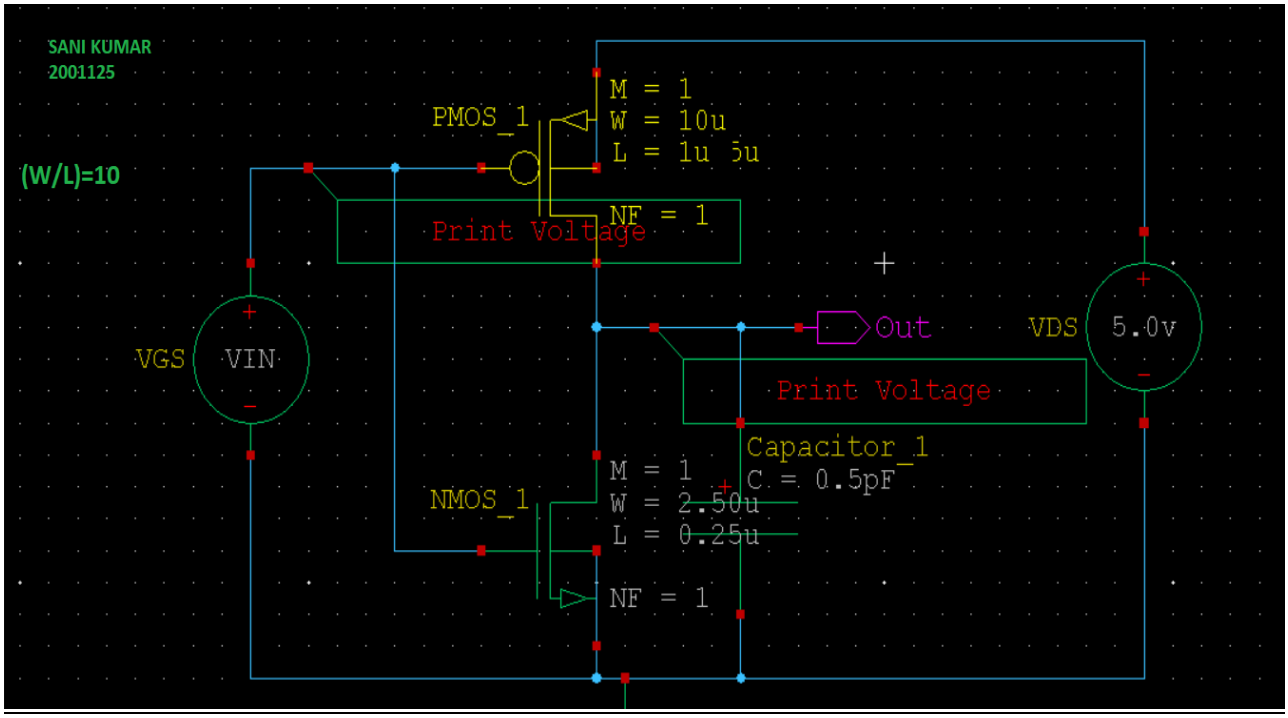

Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
18:57:57 11/07/22
N_2:V
Out:V
SANI KUMAR
2001125
Volts
VIN
0.000
0.500
1.000
1.500
2.000
2.500
3.000
3.500
4.000
4.500
5.000

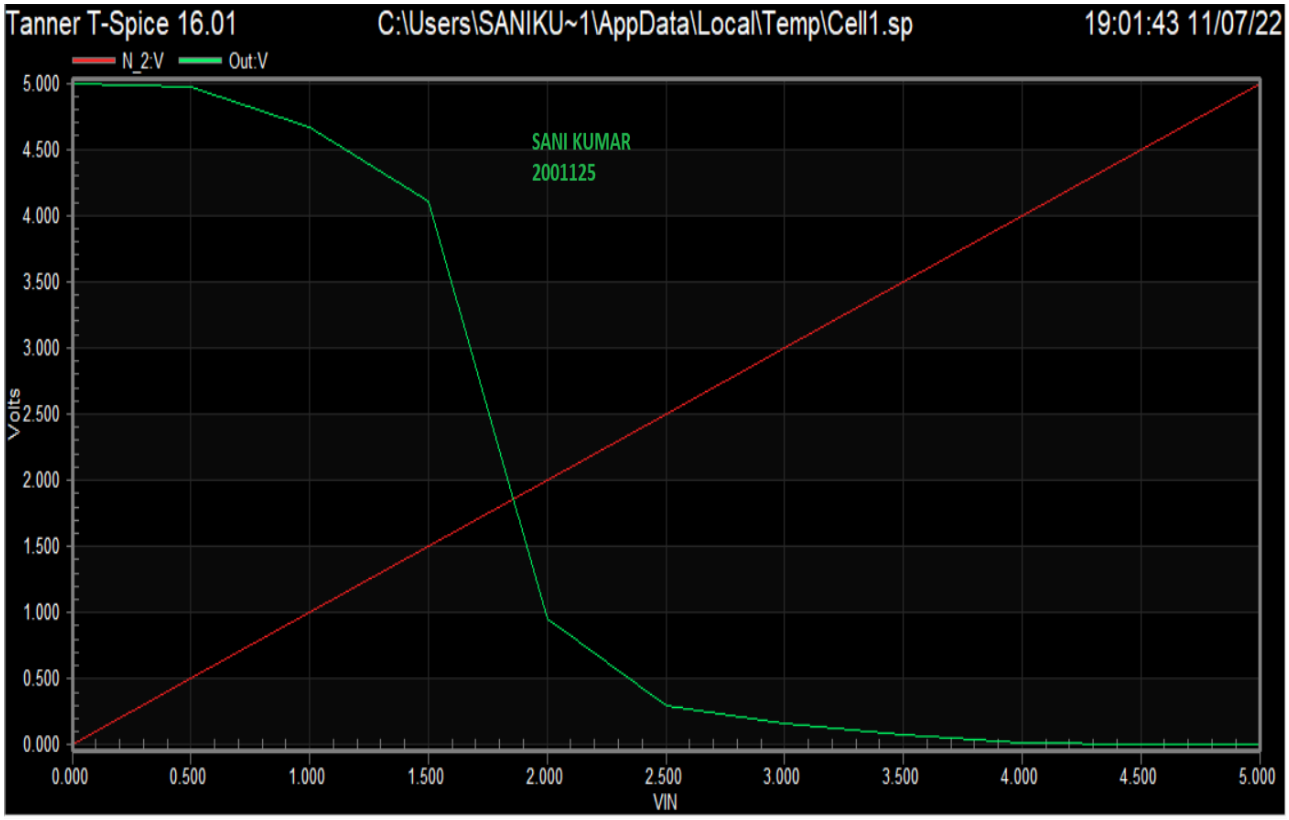
5.


SANI KUMAR
2001125
(W/L)=5
PMOS_1
M = 1
W = 5u
L = 1u 5u
NF = 1
Print Voltage
VGS
VIN
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.5pF
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1


Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
18:59:58 11/07/22
N_2:V
Out:V
SANI KUMAR
Volts
VIN
0.000
0.500
1.000
1.500
2.000
2.500
3.000
3.500
4.000
4.500
5.000

6.


SANI KUMAR
2001125
(W/L)=10
PMOS_1
M = 1
W = 10u
L = 1u 5u
NF = 1
Print Voltage
VGS
VIN
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.5pF
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1



Conclusion- Hence, we performed the DC analysis of CMOS inverter

Experiment 4

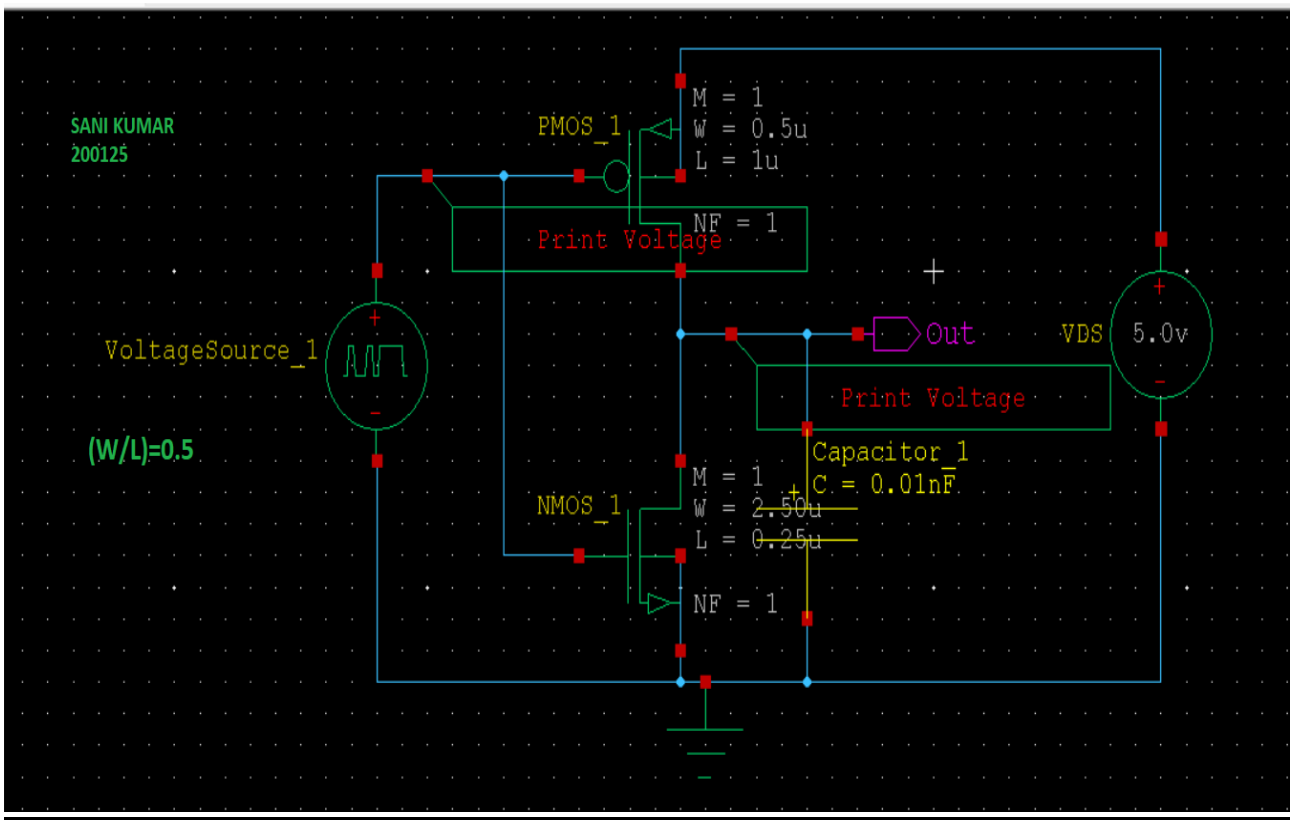
Aim- Transient analysis of CMOS inverter using Tanner EDA tool.

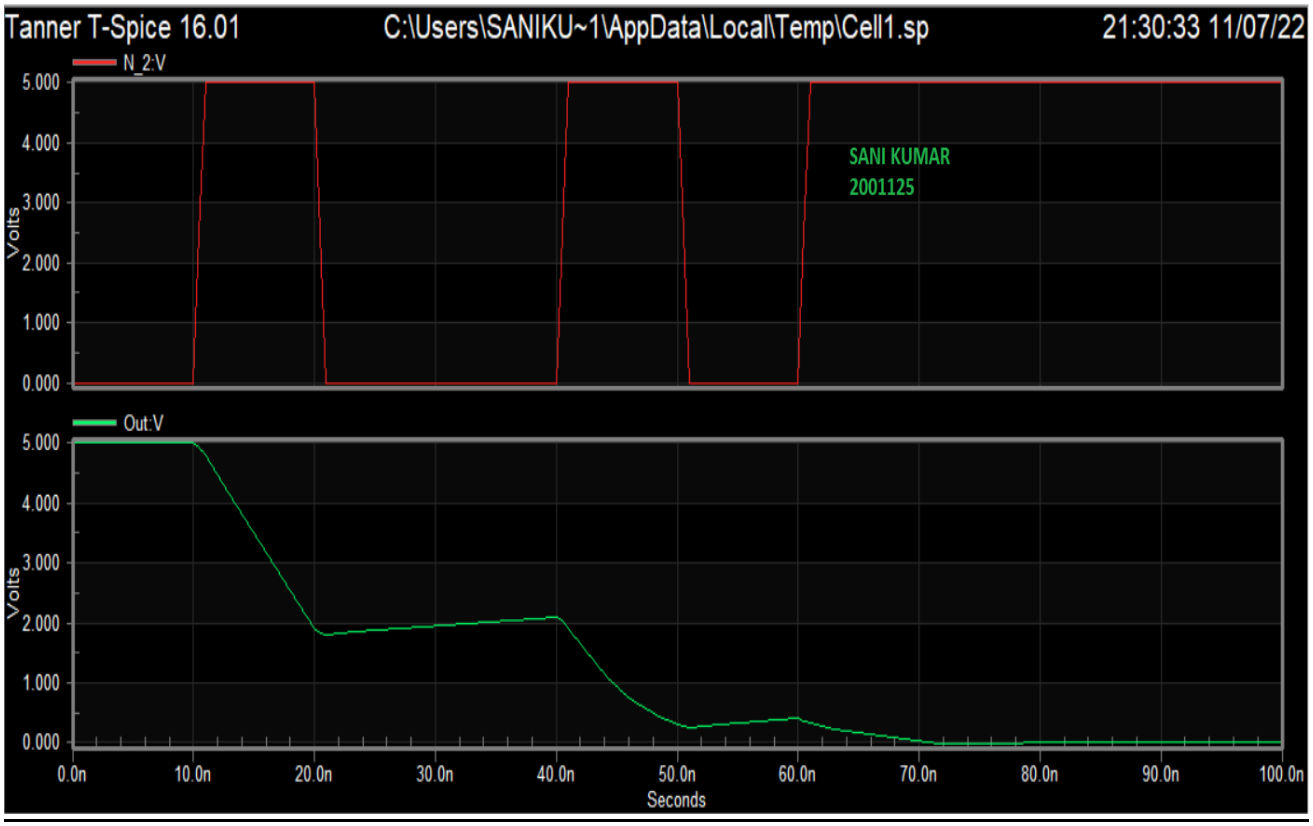
Software Required- Tanner EDA tool.

Theory- A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, where VIN is connected to the gate terminals and VOUT is connected to the drain terminals. It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter's operations can be seen very easily.

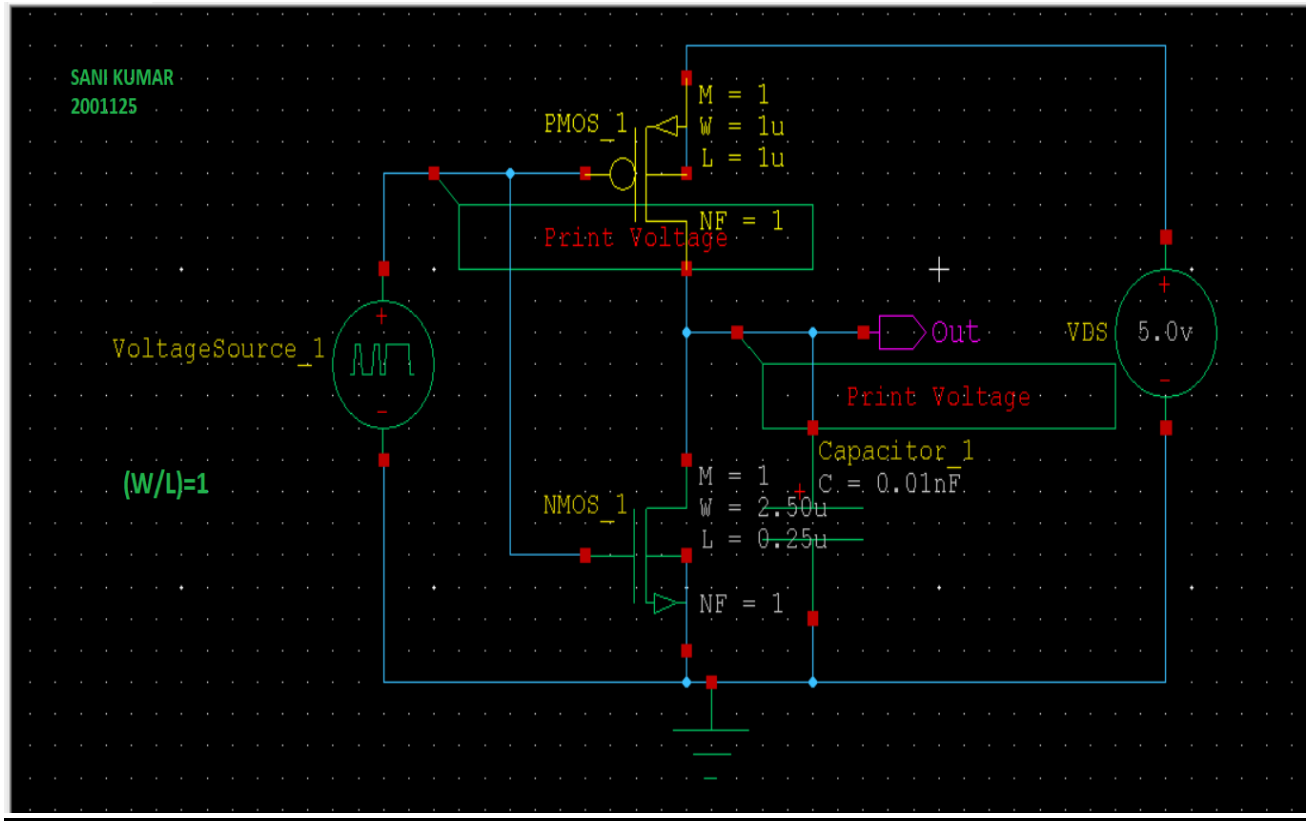
Circuit Diagram and Output-

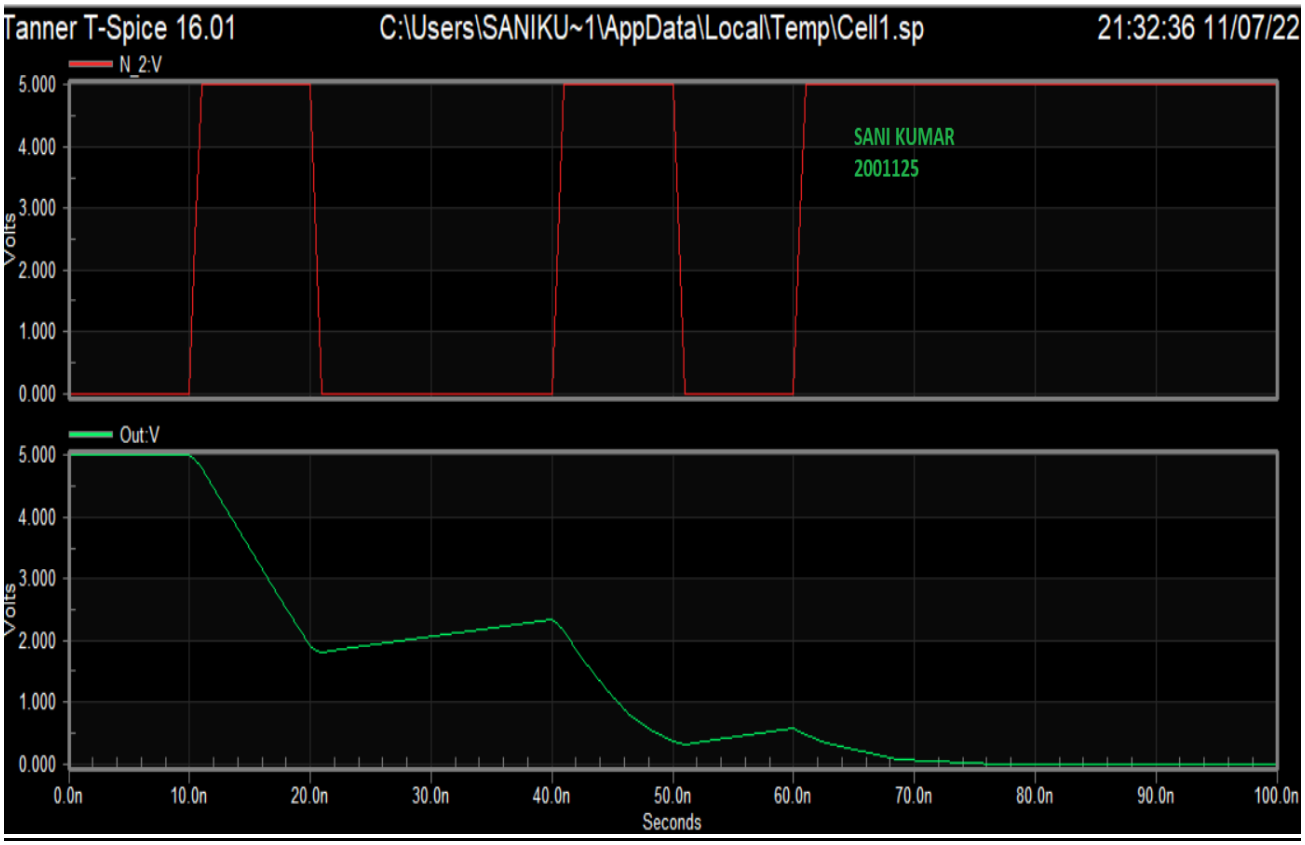
1.



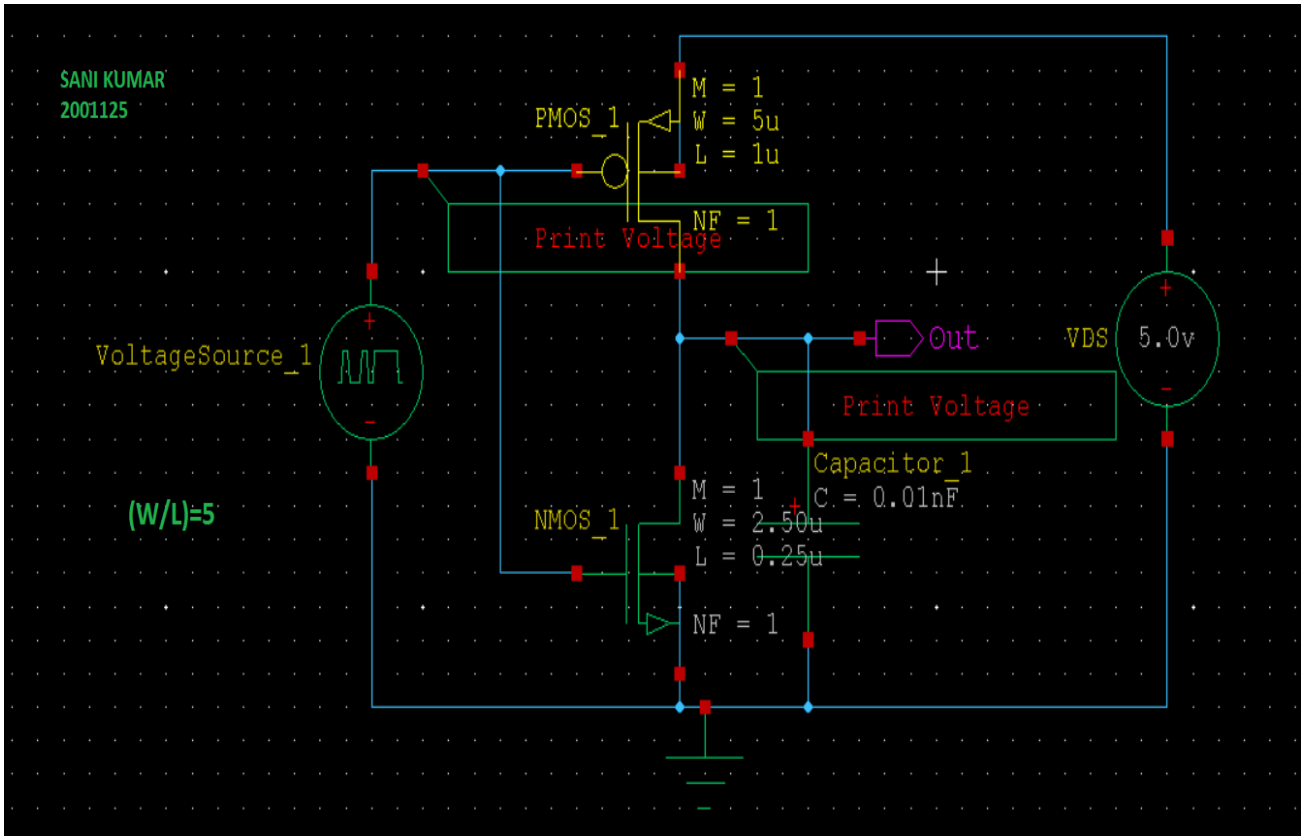

Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
21:30:33 11/07/22
N_2:V
Out:V
Volts
SANI KUMAR
2001125
5.000
4.000
3.000
2.000
1.000
0.000
0.0n
10.0n
20.0n
30.0n
40.0n
50.0n
60.0n
70.0n
80.0n
90.0n
100.0n
Seconds

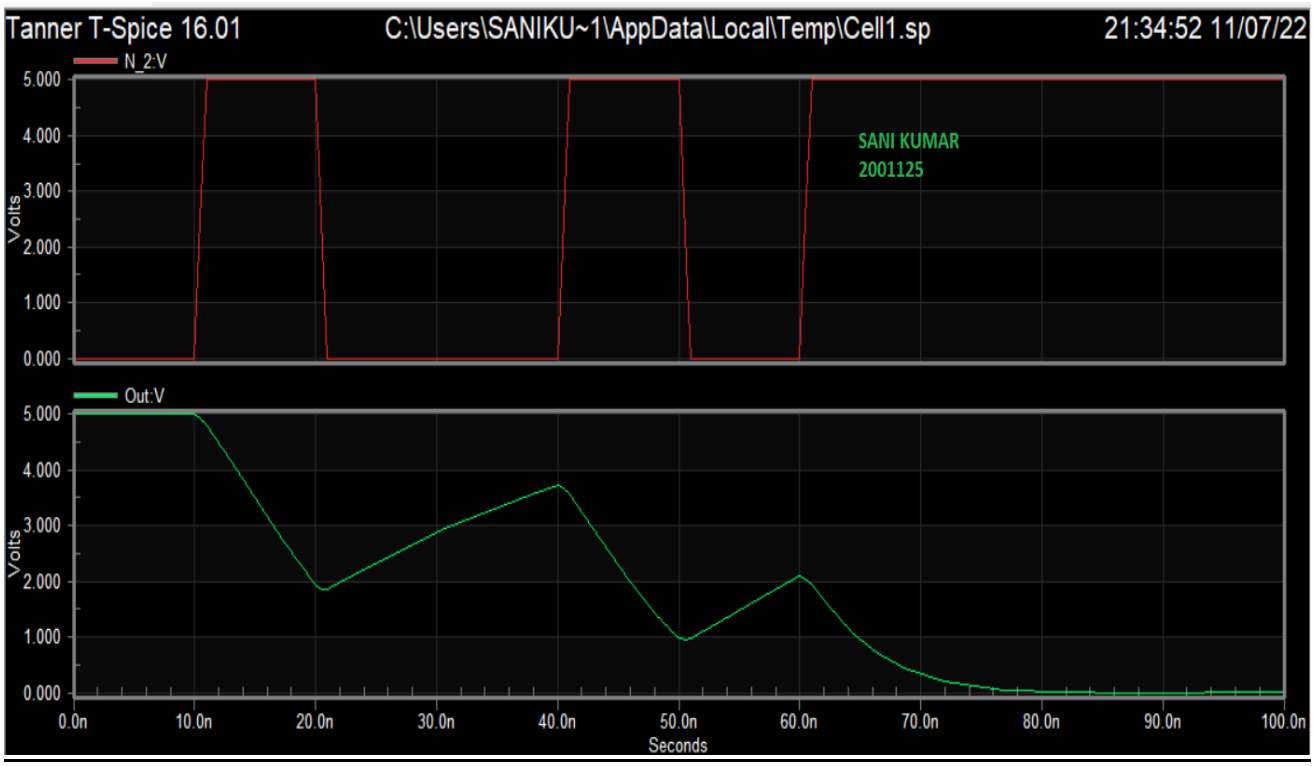
2.


SANI KUMAR
2001125
PMOS_1
M = 1
W = 1u
L = 1u
NF = 1
Print Voltage
VoltageSource_1
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.01nF
(W/L)=1
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1

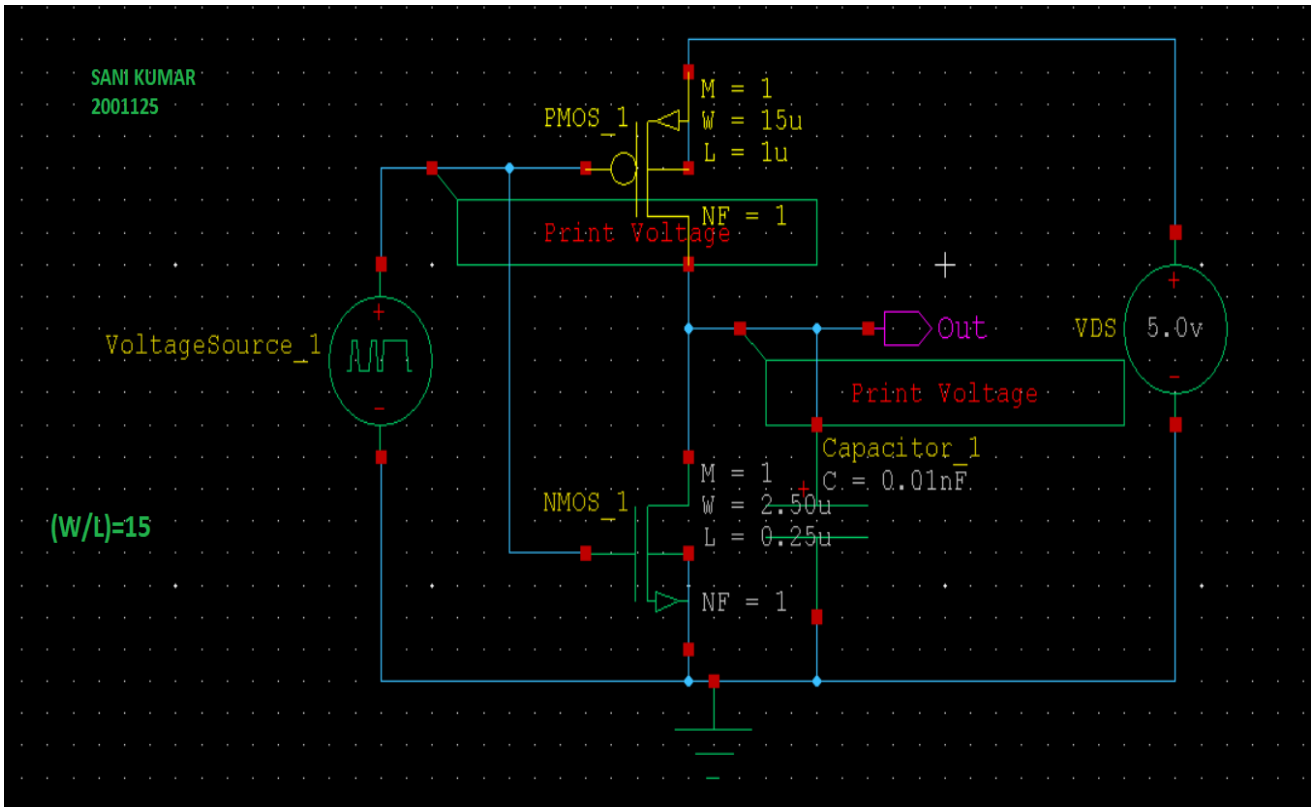

Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
21:32:36 11/07/22
N_2:V
SANI KUMAR
2001125
Volts
5.000
4.000
3.000
2.000
1.000
0.000
Out:V
0.0n
10.0n
20.0n
30.0n
40.0n
50.0n
60.0n
70.0n
80.0n
90.0n
100.0n
Seconds

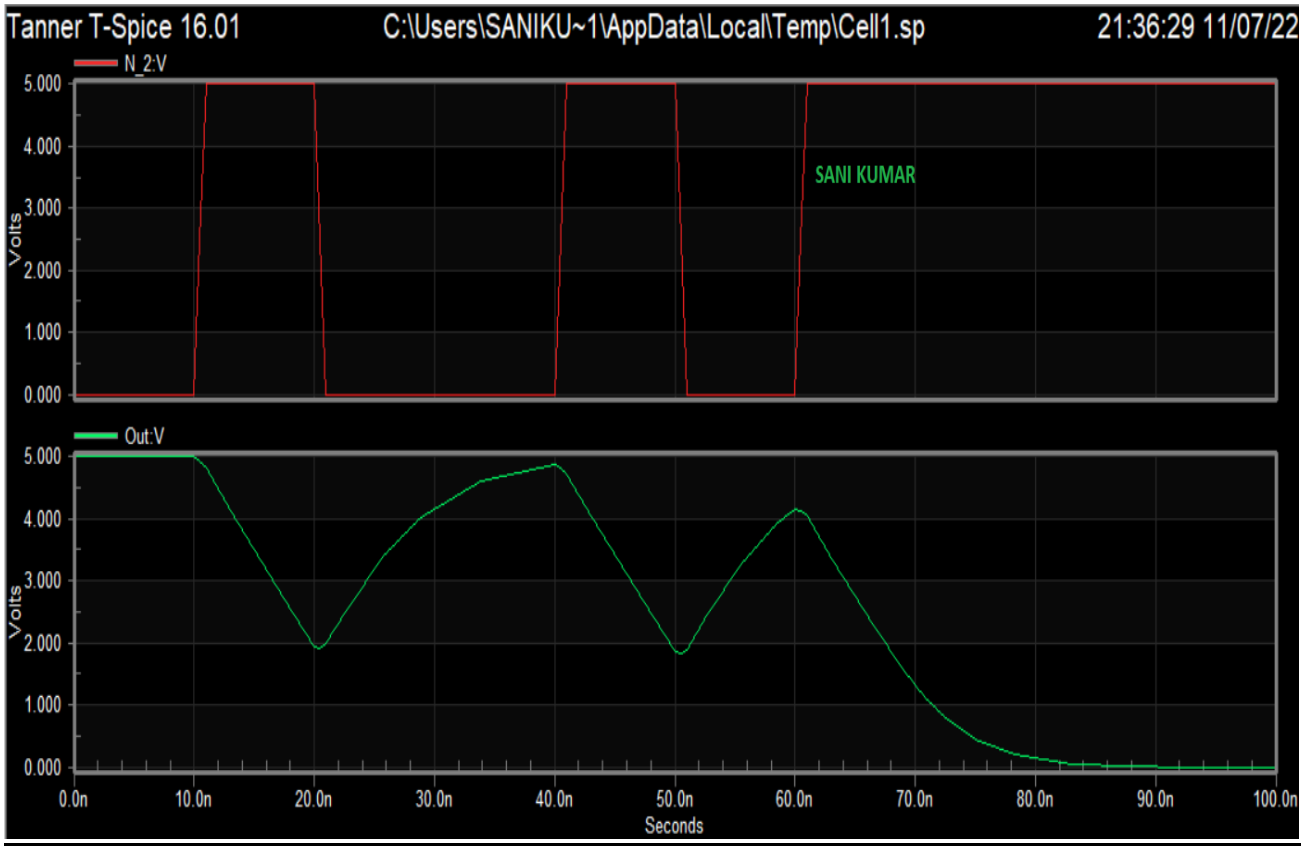
3.


SANI KUMAR
2001125
PMOS_1
M = 1
W = 5u
L = 1u
NF = 1
Print Voltage
VoltageSource_1
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.01nF
(W/L)=5
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1


Tanner T-Spice 16.01
C:\Users\SANIKU~1\AppData\Local\Temp\Cell1.sp
21:34:52 11/07/22
N_2:V
SANI KUMAR
2001125
Volts
Out:V
Seconds
0.0n
10.0n
20.0n
30.0n
40.0n
50.0n
60.0n
70.0n
80.0n
90.0n
100.0n

4.


SANI KUMAR
2001125
PMOS_1
M = 1
W = 15u
L = 1u
NF = 1
Print Voltage
VoltageSource_1
Out
VDS
5.0v
Print Voltage
Capacitor_1
C = 0.01nF
M = 1
W = 2.50u
L = 0.25u
NMOS_1
NF = 1
(W/L)=15



Conclusion- Hence, we performed the Transient analysis of CMOS inverter.

Experiment 5

Aim- NAND and NOR Gates using PMOS and NMOS using Tanner EDA tool.

Software Required- Tanner EDA tool.

Theory- NAND: *Figure 2* shows a CMOS two-input NAND gate. P-channel transistors Q1 and Q2 are connected in parallel between +V and the output terminal. N-channel transistors Q3 and Q4 are connected in series between the output terminal and ground.

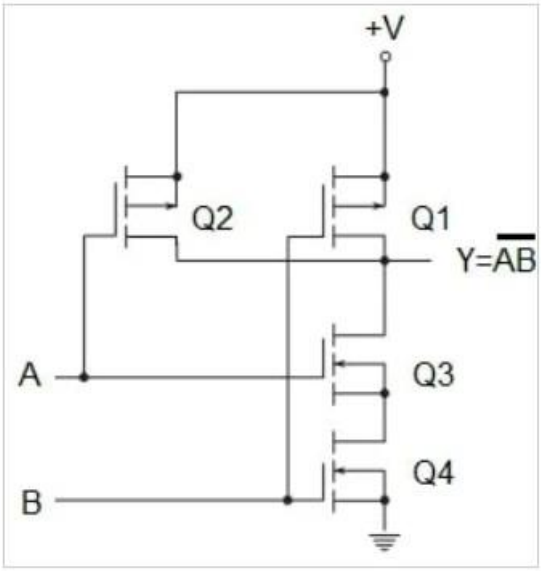


Figure 2

With Q3 and Q4 transistors ”on” and Q1 and Q2 transistors “off,” the output is a logic 0. This condition happens when both inputs, A and B, are logic 1, confirming the lowest row in the above truth table.

With logic 0 in inputs A and B, Q3 and Q4 transistors are “off,” and Q1 and Q2 transistors are “on,” producing a logic 1 output. This is consistent with the first row of the truth table.

When one of the inputs is a logic “1” and the other one is a logic “0”, either Q3 is “off” and Q2 is “on” or Q4 is “off” and Q1 is “on.” The output in both cases is a logic “1,” validating the second and the third rows of the truth table.

NOR- The output of a NOR gate is logic 1 with logic 0 in both inputs. The outcomes for other input combinations are logic 0.

Figure 3 shows a CMOS two-input NOR gate. P-channel transistors Q1 and Q2 are connected in series between +V and the output terminal. N-channel transistors Q3 and Q4 are connected in parallel between the output and ground.

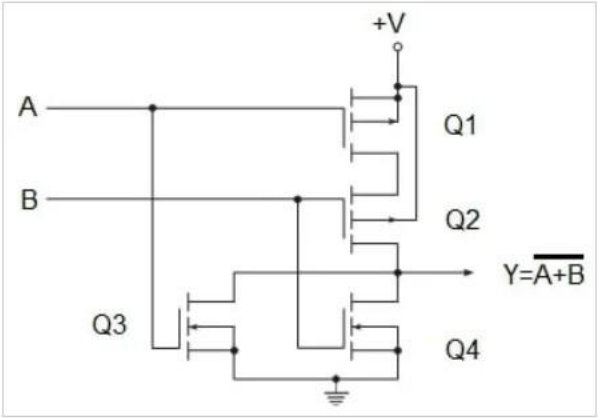


Figure 3. A CMOS two-input NOR gate.

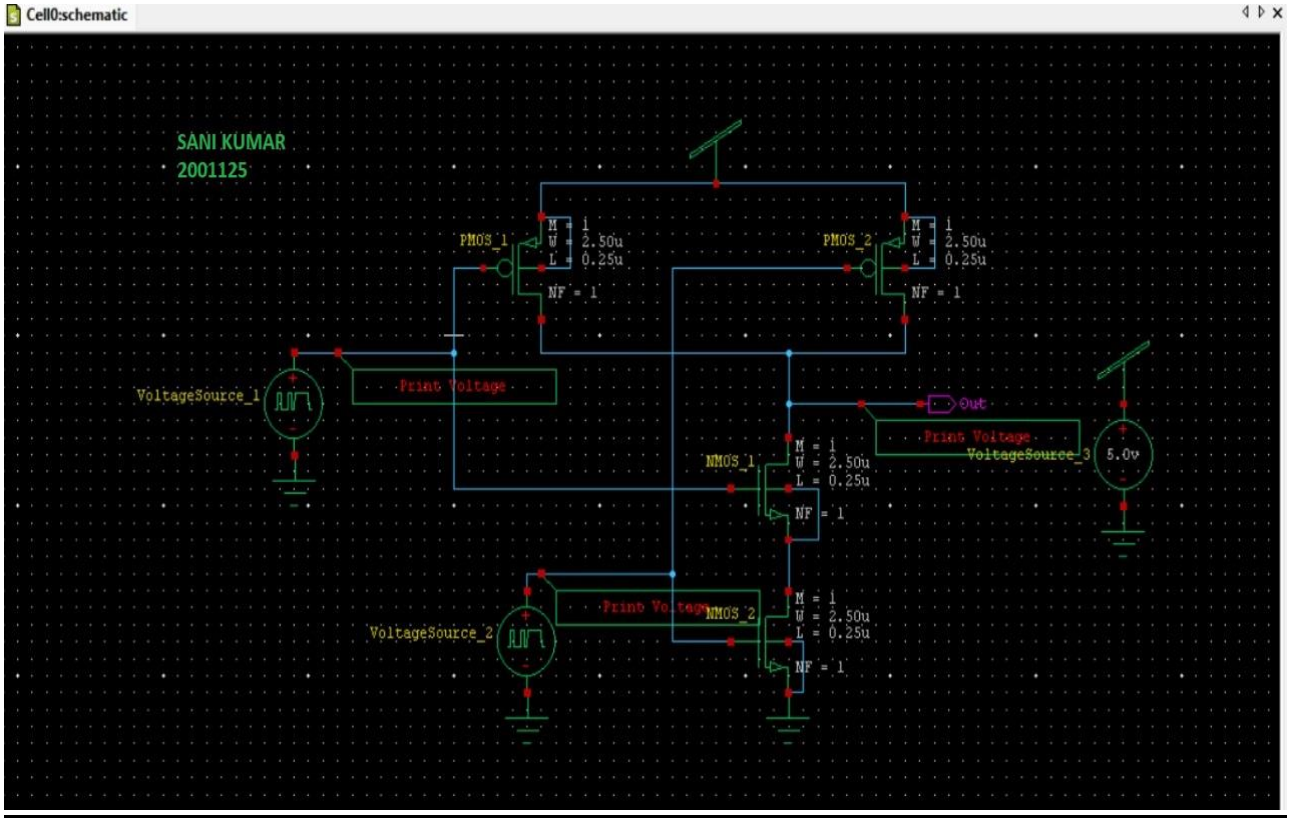
When both inputs, A and B, are logic 0, Q1 and Q2 are “on,” and Q3 and Q4 are “off,” and the output is logic 1. This confirms the first row of the truth table above.

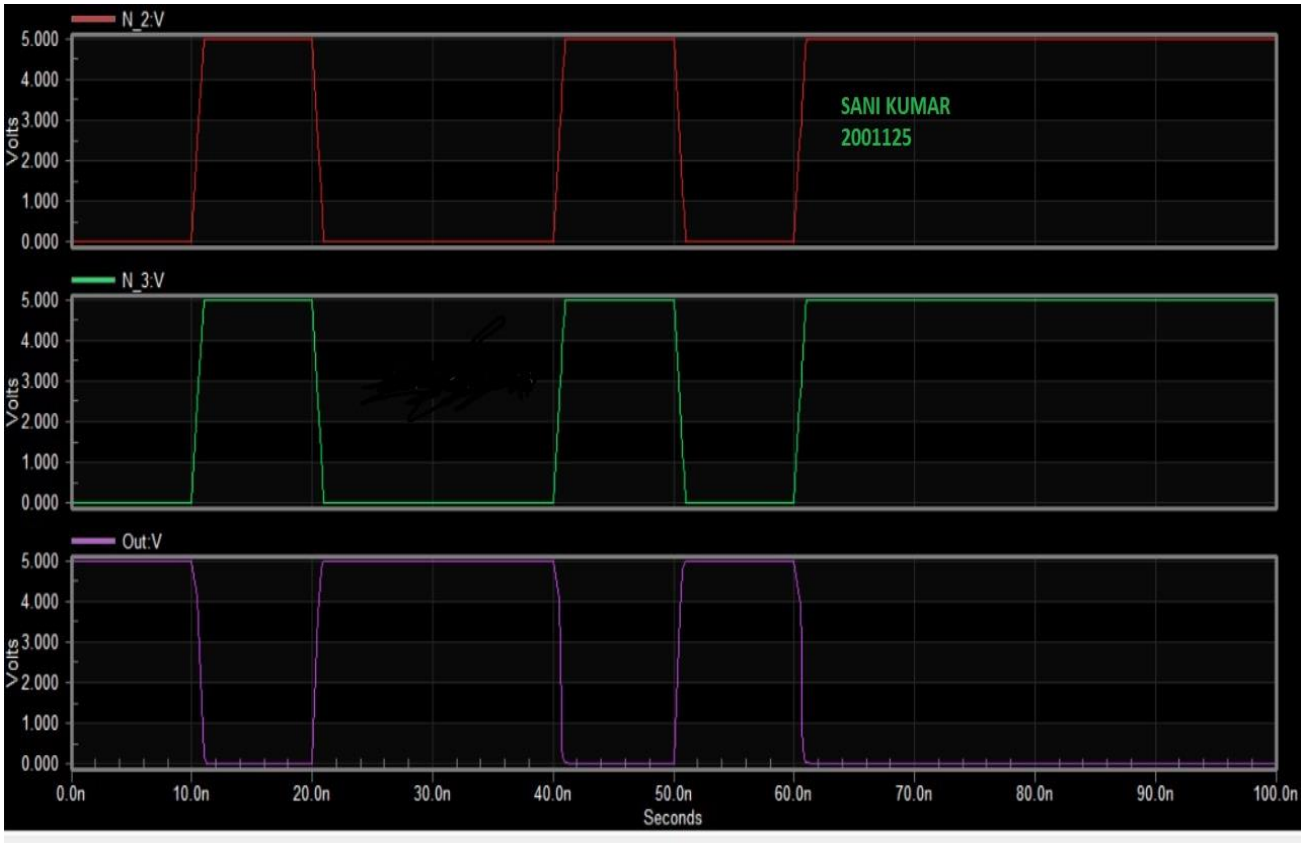
With both inputs logic 1, Q3 and Q4 are “on,” and Q1 and Q2 are “off,” producing a logic 0 output that confirms the last row of the truth table.

For the two remaining input combinations, either Q1 is “off” and Q3 is “on” or Q2 is “off” and is Q4 “on”. In these cases, the output is logic 0 which is consistent with the above truth table.

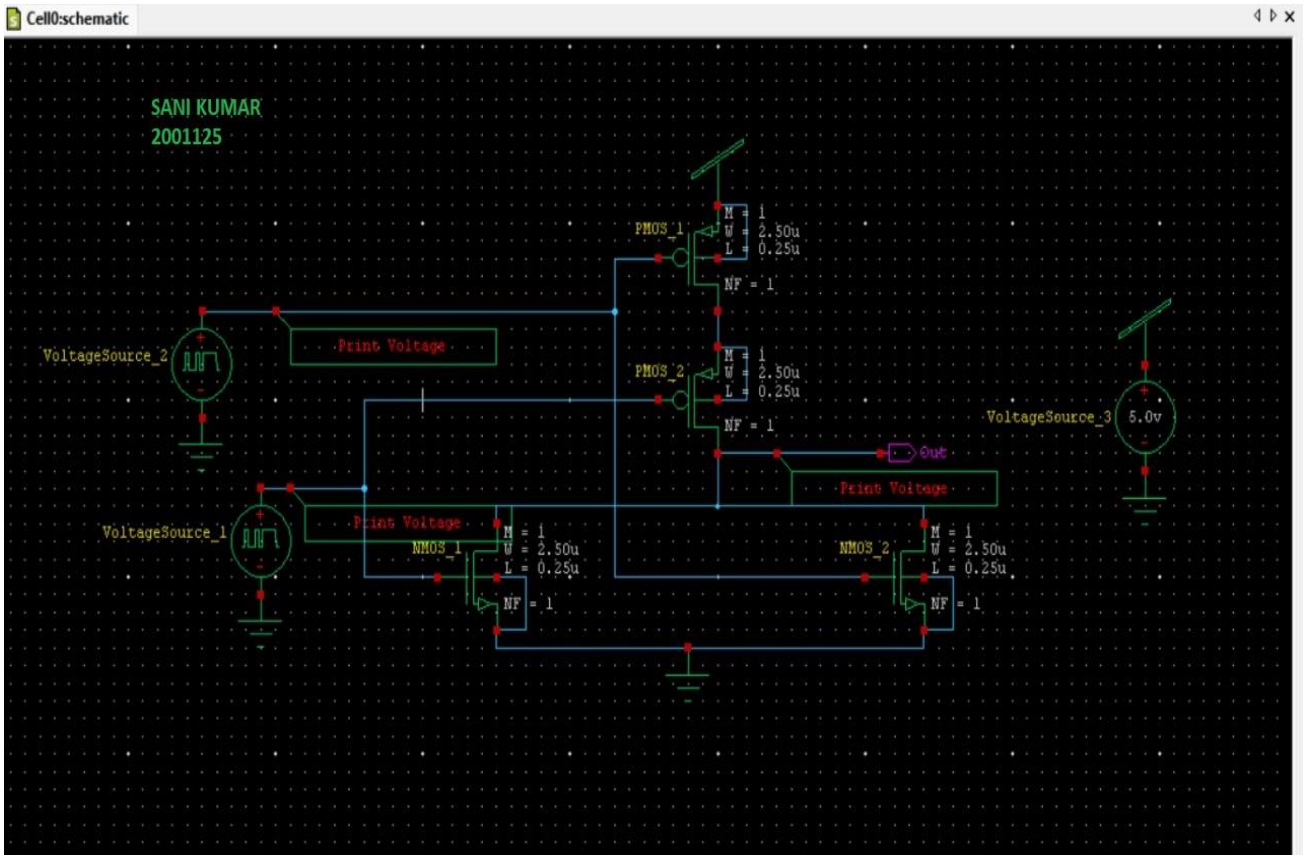
Circuit Diagram:

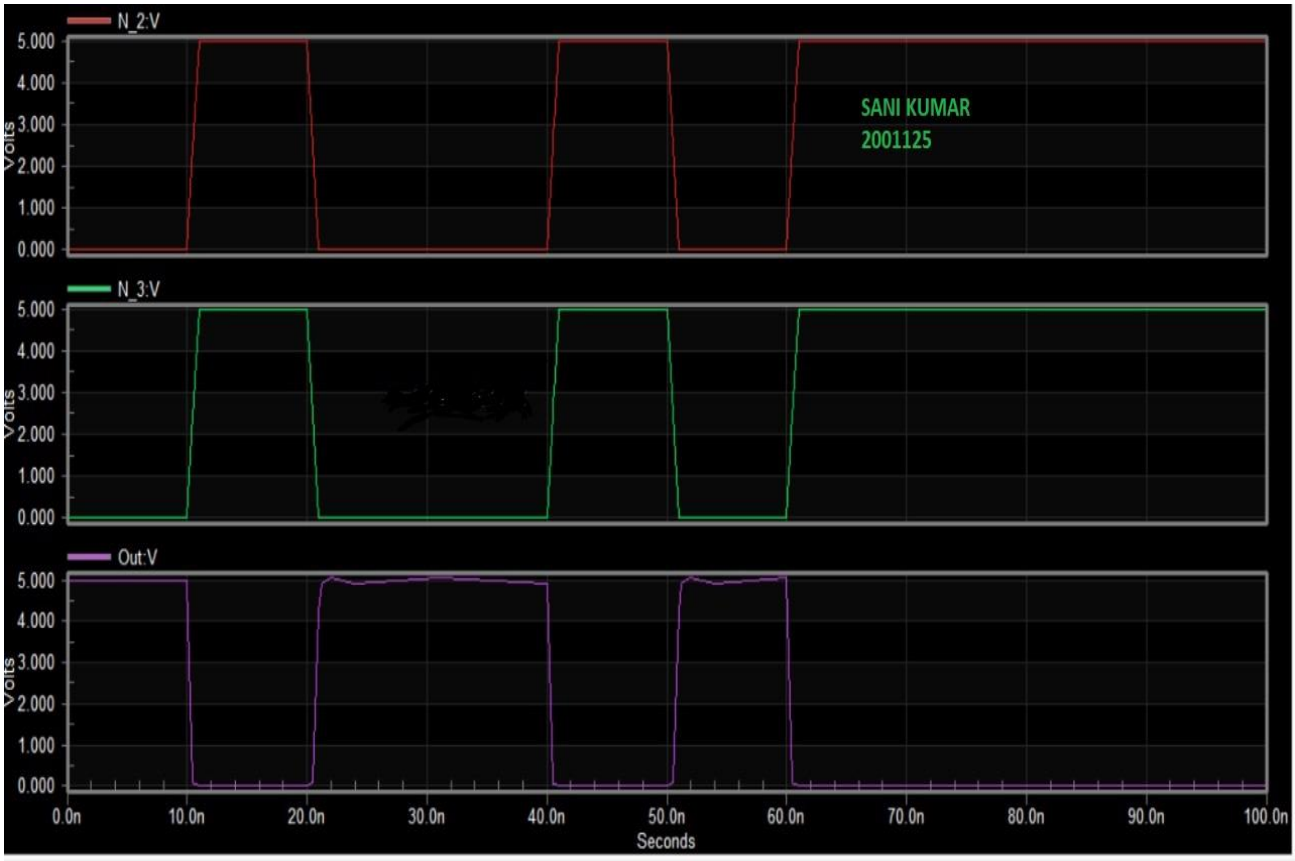
1.NAND Gate-





NOR Gate:


Cell0:schematic
SANI KUMAR
2001125
PMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1
PMOS_2
M = 1
W = 2.50u
L = 0.25u
NF = 1
VoltageSource_2
Print Voltage
VoltageSource_3
5.0v
Out
Print Voltage
VoltageSource_1
Print Voltage
NMOS_1
M = 1
W = 2.50u
L = 0.25u
NF = 1
NMOS_2
M = 1
W = 2.50u
L = 0.25u
NF = 1



Conclusion: Hence NAND and NOR gate was realised using PMOS and NMOS by the use of Tanner EDA Tool and desired output was obtained.