NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125

भारतीय सूचना प्रौद्योगिकी संस्थान भागलपुर

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY BHAGALPUR

(An Institute of National Importance under Act of Parliament)

VLSI LAB MANUAL REPORT

NAME :- SANI KUMAR

ROLL NO. – 2001125

DEP. – ECE

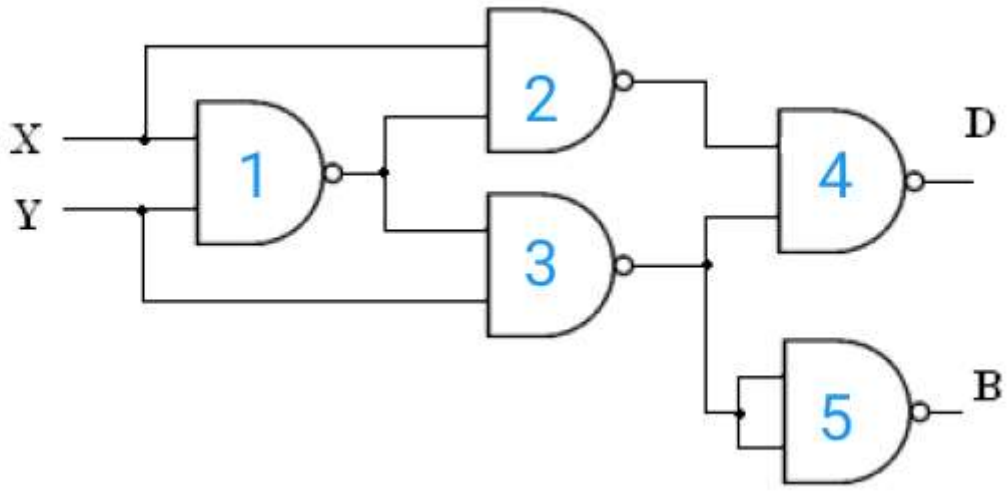
SUMMITED TO:- **RAJAN SIR**

NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125

EXPERIMENT -6

AIM :- Half Adder using NAND Gate

THEORY:- Half adder is a combinational circuit that performs the simple addition of two single-bit binary numbers and produces a 2-bit number. The LSB of the result is the Sum (usually represented as Sum or S_0 or $\sum_0$) and the MSB is the Carry (usually represented as C_{OUT}).



TRUTH TABLE-

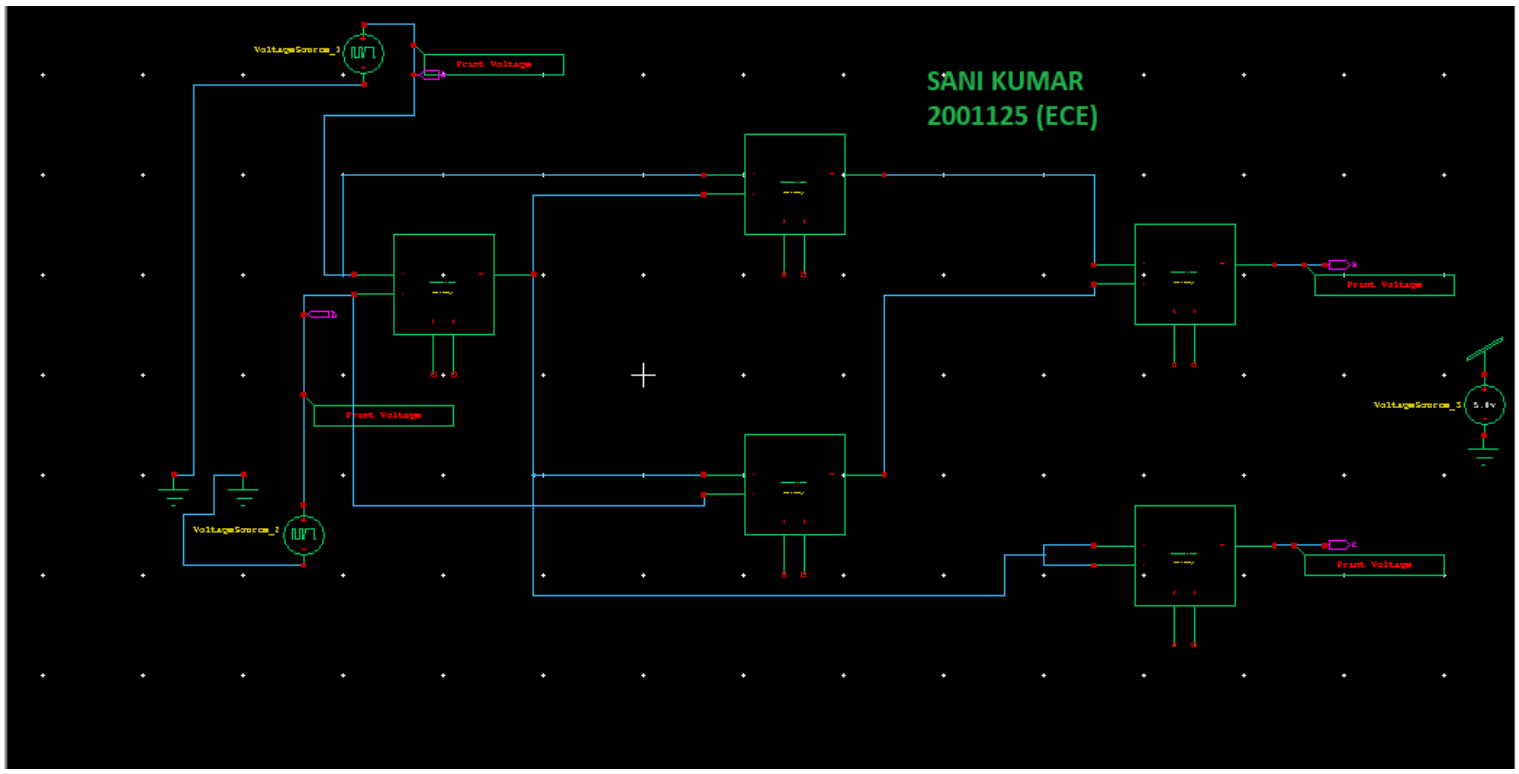
INPUT		OUTPUT	
A	B	Sum	
0	0	0	
0	1	**1**	
1	0	**1**	
1	1	0	

NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**

PROCEDURE

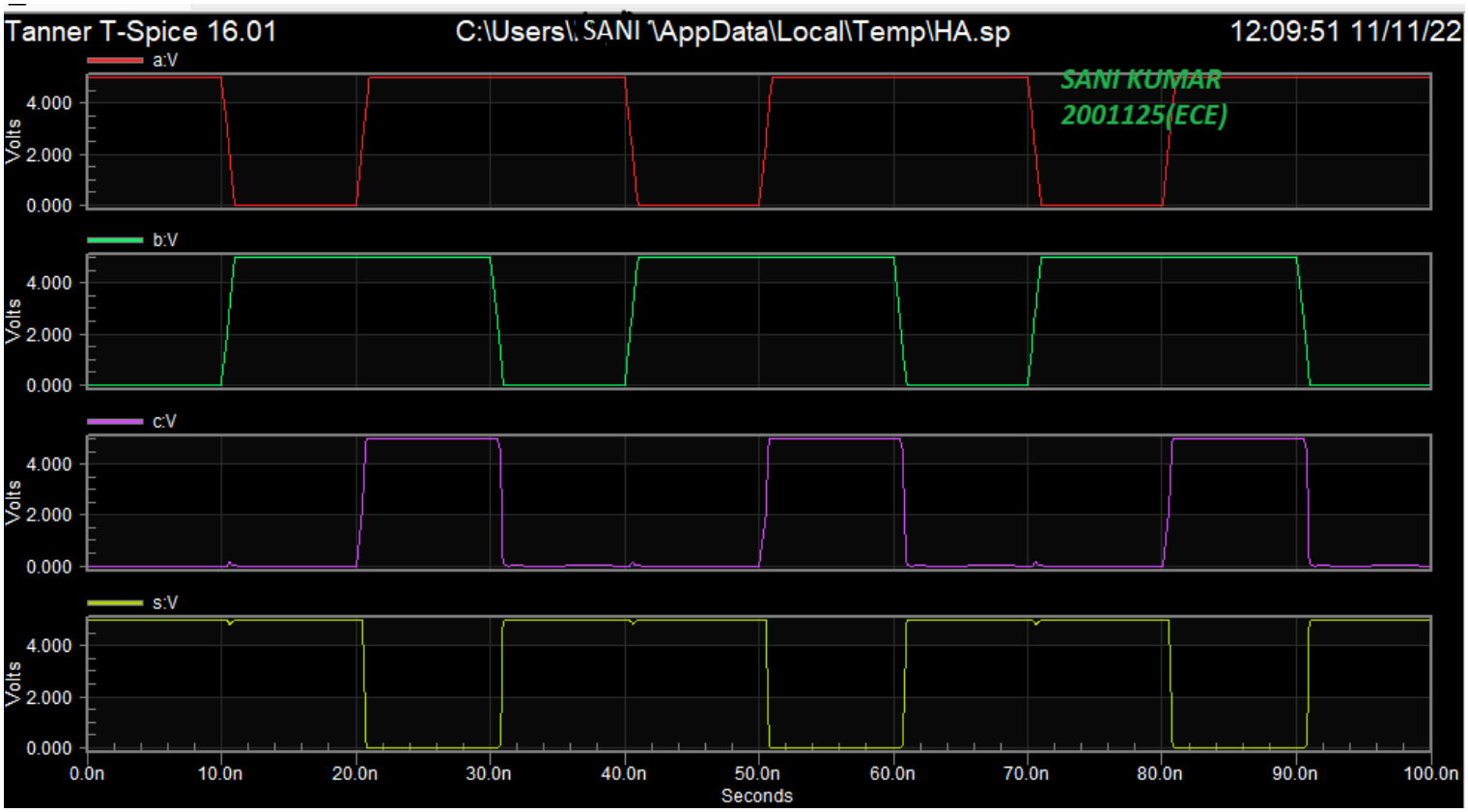
1. Draw the schematic of the HALF ADDER using the NAND gate.
2. Perform Transient Analysis of the HALF ADDER circuit.
3. Obtain the output waveform from W-edit.
4. Obtain the spice code using T-edit.

Circuit diagram-



OUTPUT-

NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**



AIM

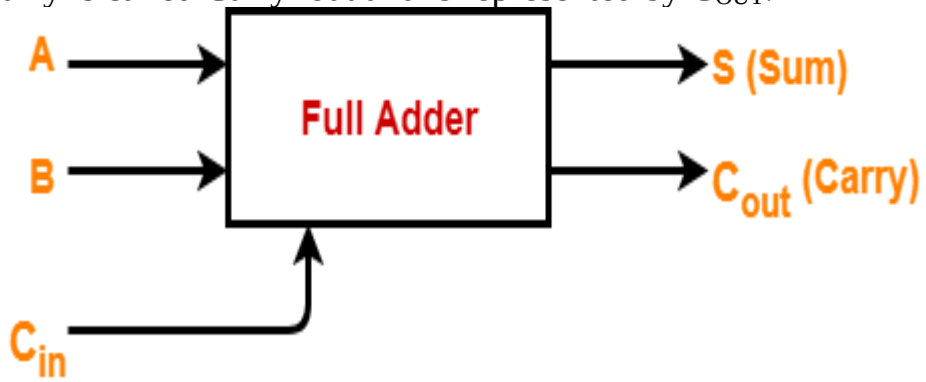
. Full Adder using NAND Gate

APPARATUS REQUIRED:

NAND GATE(COMPLEX CMOS CIRCUIT), BIT VOLTAGE, GROUND, VDD

THEORY:

Full adder is a digital circuit used to calculate the sum of three binary bits, which is the main difference between this and half adder. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called Carry–in, generally represented by C_{IN}. It calculates the sum of three bits along including the carry. The output carry is called Carry–out and is represented by C_{OUT}.



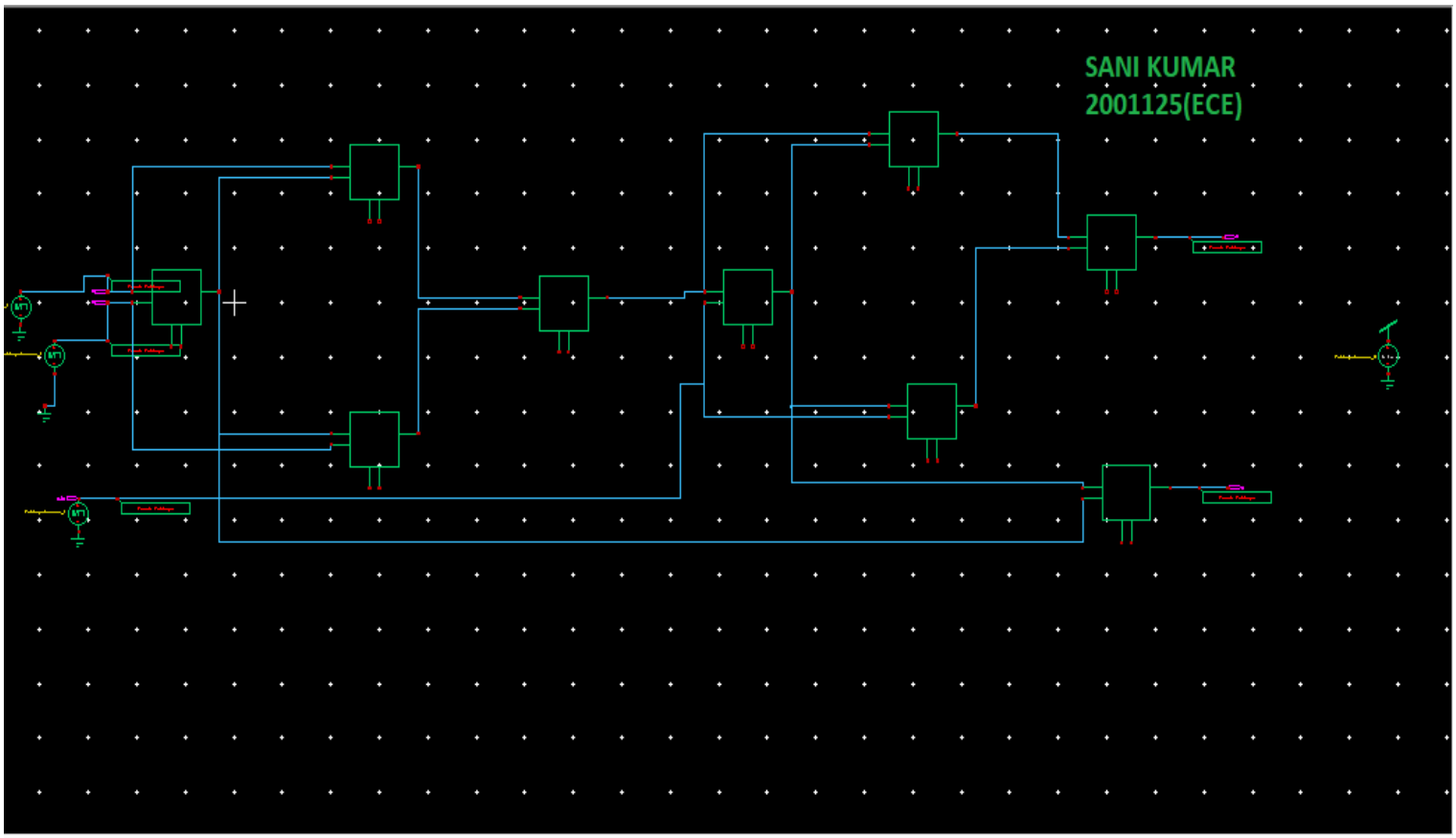
NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125

TRUTH TABLE-

Inputs			Outputs	
A	**B**	**C_{in}**	**C_{out} (Carry)**	**S (Sum)**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

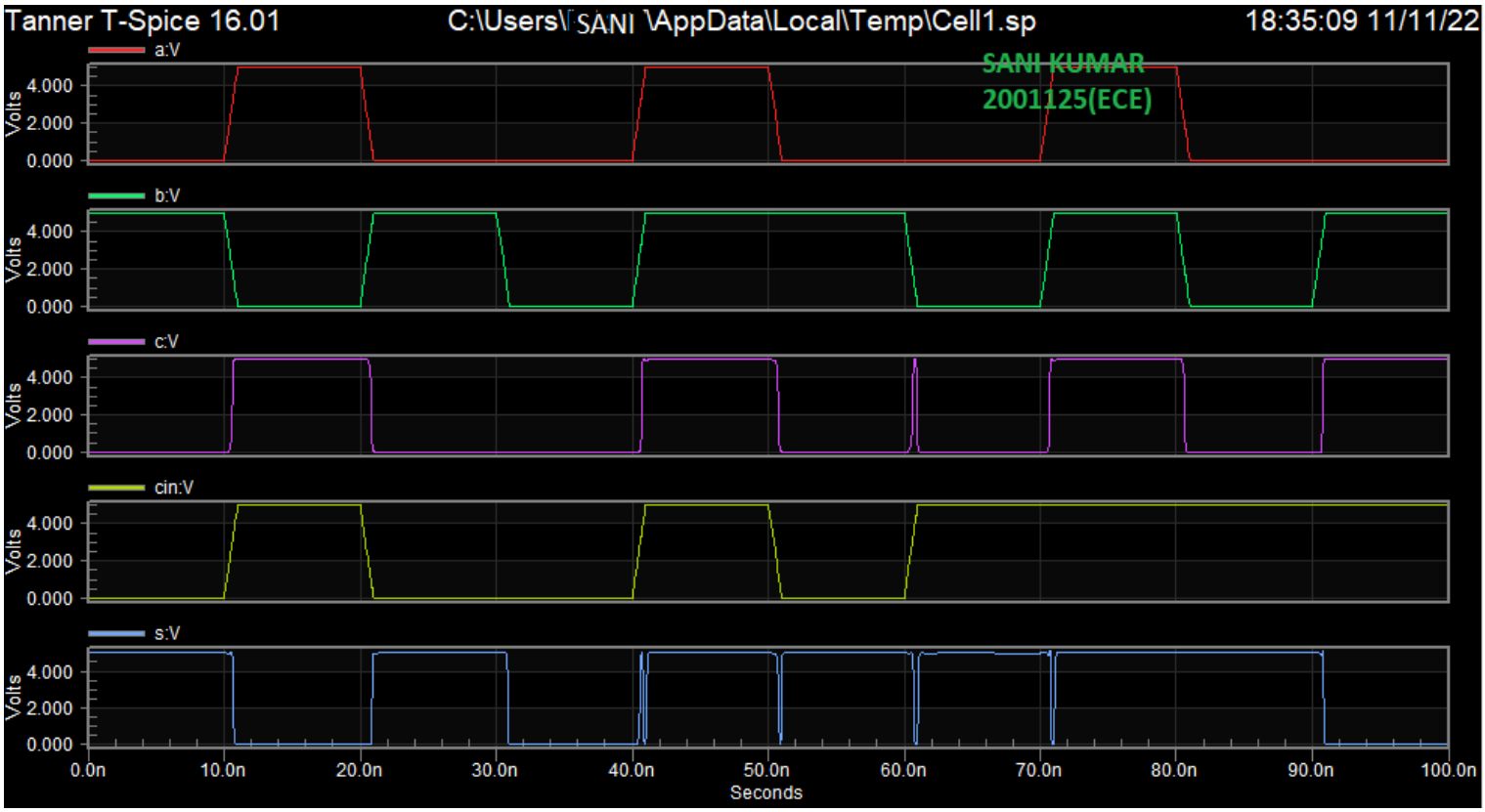
Circuit diagram-

NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125



Output-

NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125



EXPERIMENT 7

AIM

4:1 Multiplexer using NAND Gate

APPARATUS REQUIRED:

NAND GATE(COMPLEX CMOS CIRCUIT), BIT VOLTAGE, GROUND, VDD,

THEORY:

Building 4x1 mux directly from NAND gates: The logical equation of a 4x1 multiplexer is given as:

Y = (S1' S0' A + S1' S0 B + S1 S0' C + S1 S0 D)

where S1 and S0 are the selects of the multiplexer and A, B, C and D are the multiplexer inputs.

Now, using De-morgan's law (**m + n = (m'n')'**)

The above equation turns into,

Y = ((S1' S0' A)' (S1' S0 B)' (S1 S0' C)' (S1 S0 D)')'
In other words,

Y = NAND (NAND(S1',S0',A),NAND(S1',S0,B),NAND(S1,S0',C),NAND(S1,S0,D))

S0	S1	Output
0	0	A
0	1	B
1	0	C
1	1	D

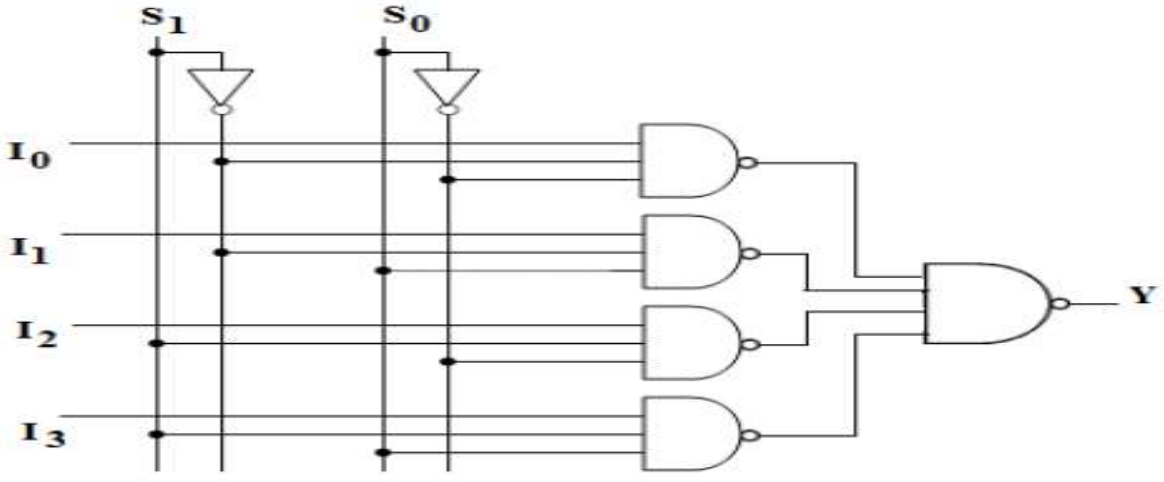
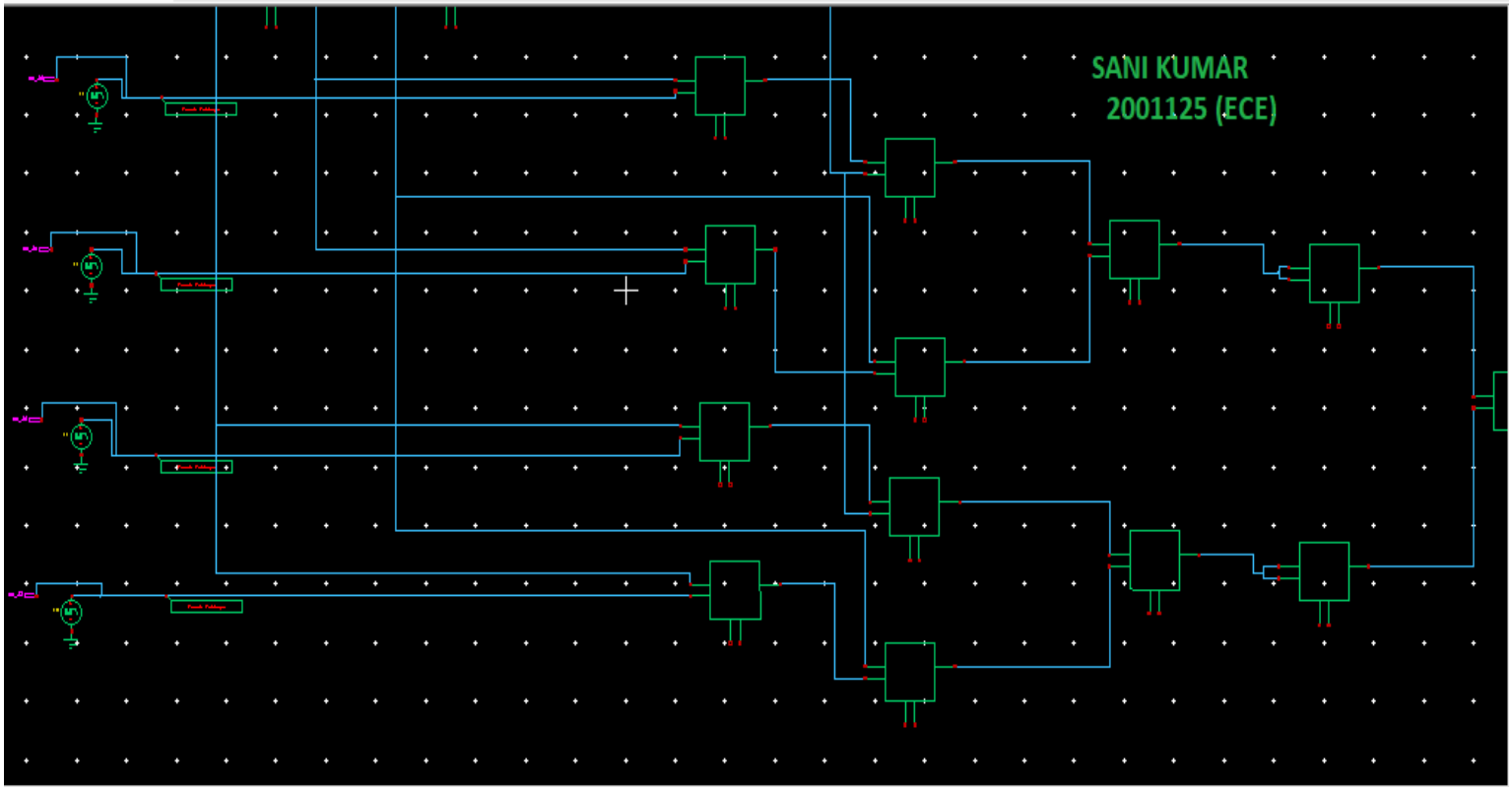


Fig. 1: 4x1 Multiplexer

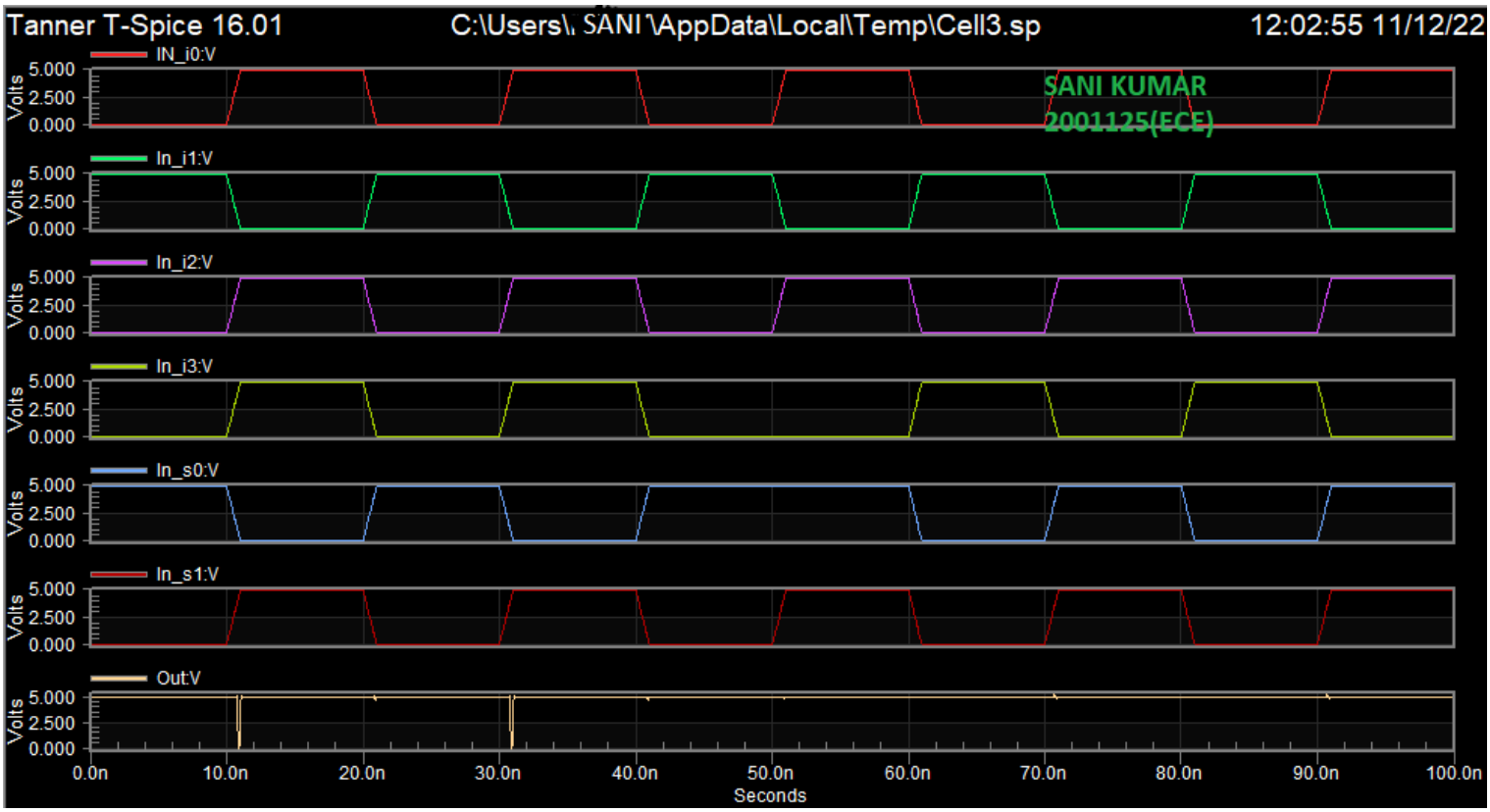
NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125

Circuit diagram-



Output-

NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125



EXPERIMENT 8

AIM

DC and transient analysis of dynamic logic circuit.

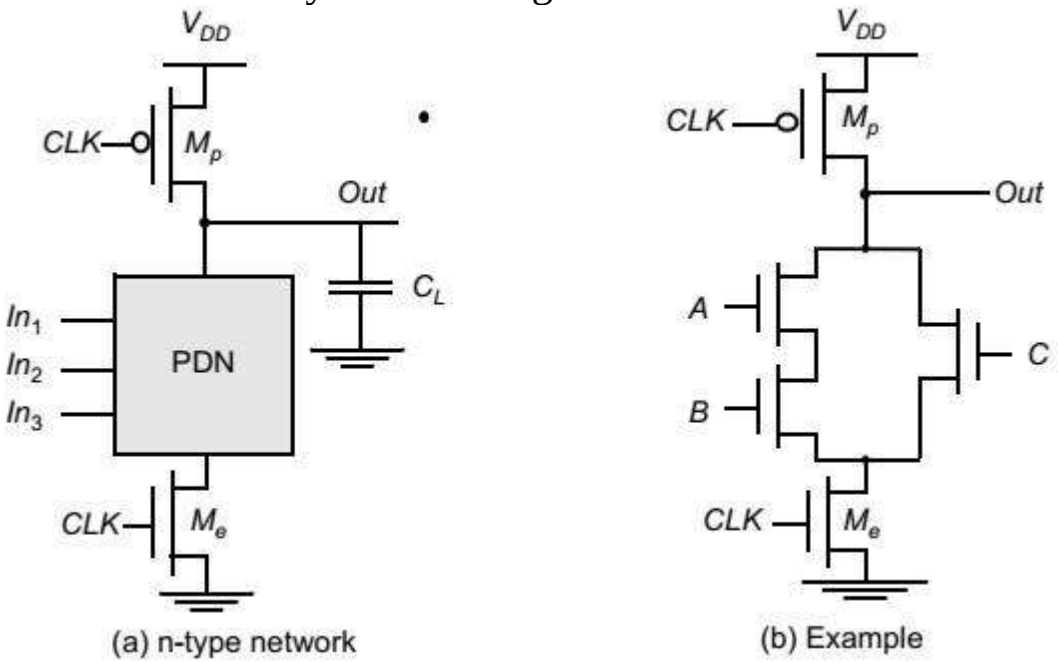
APPARATUS REQUIRED:

PMOS, NMOS, VDD, GROUND,OUTPUT INPUT PORT

THEORY:

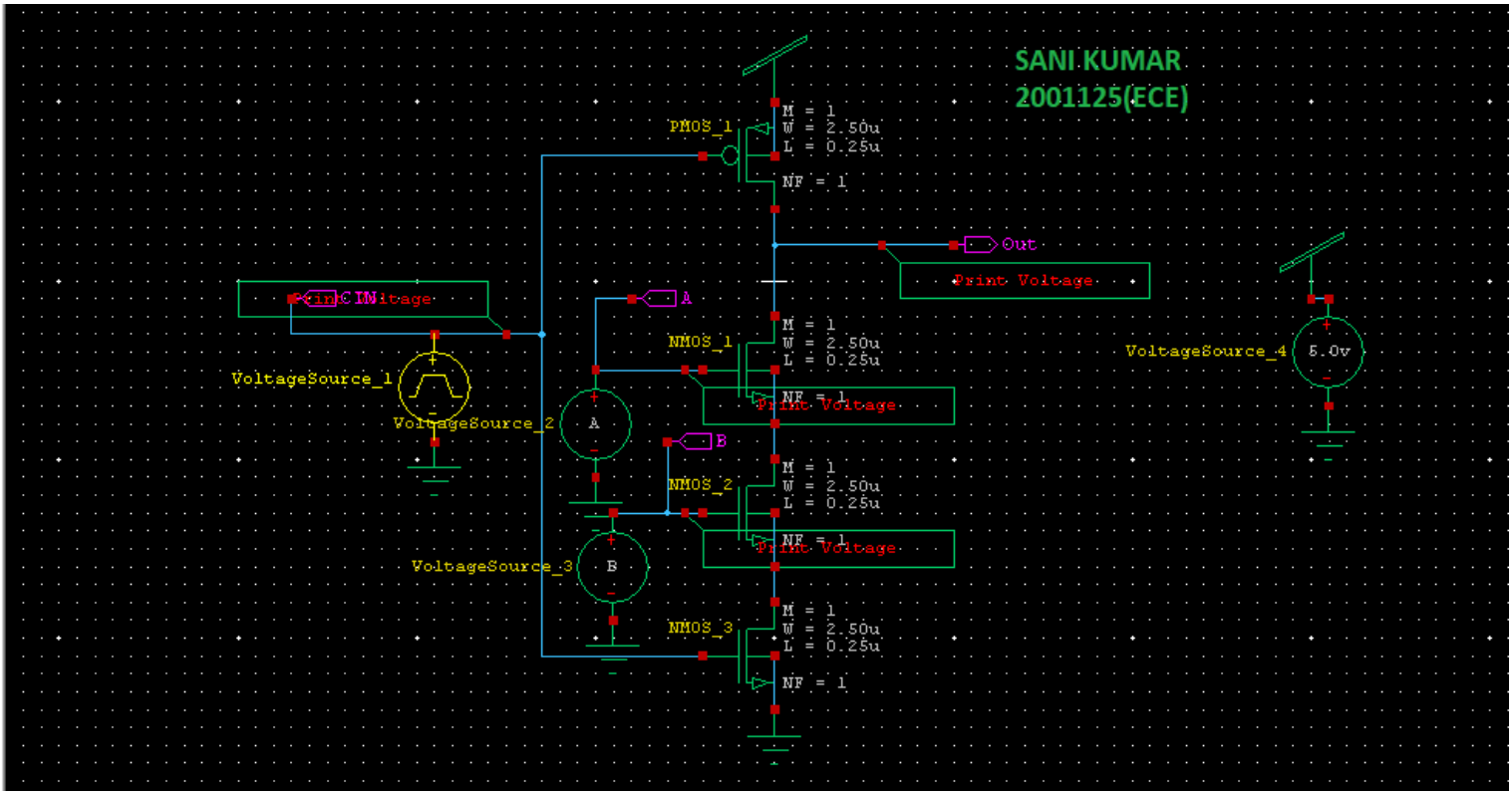
Dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes. In this section, an alternate logic style called dynamic logic is presented that obtains a similar result, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of precharge and conditional evaluation phases. The basic construction of an (n-

type) dynamic logic gate is shown in Figure. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.

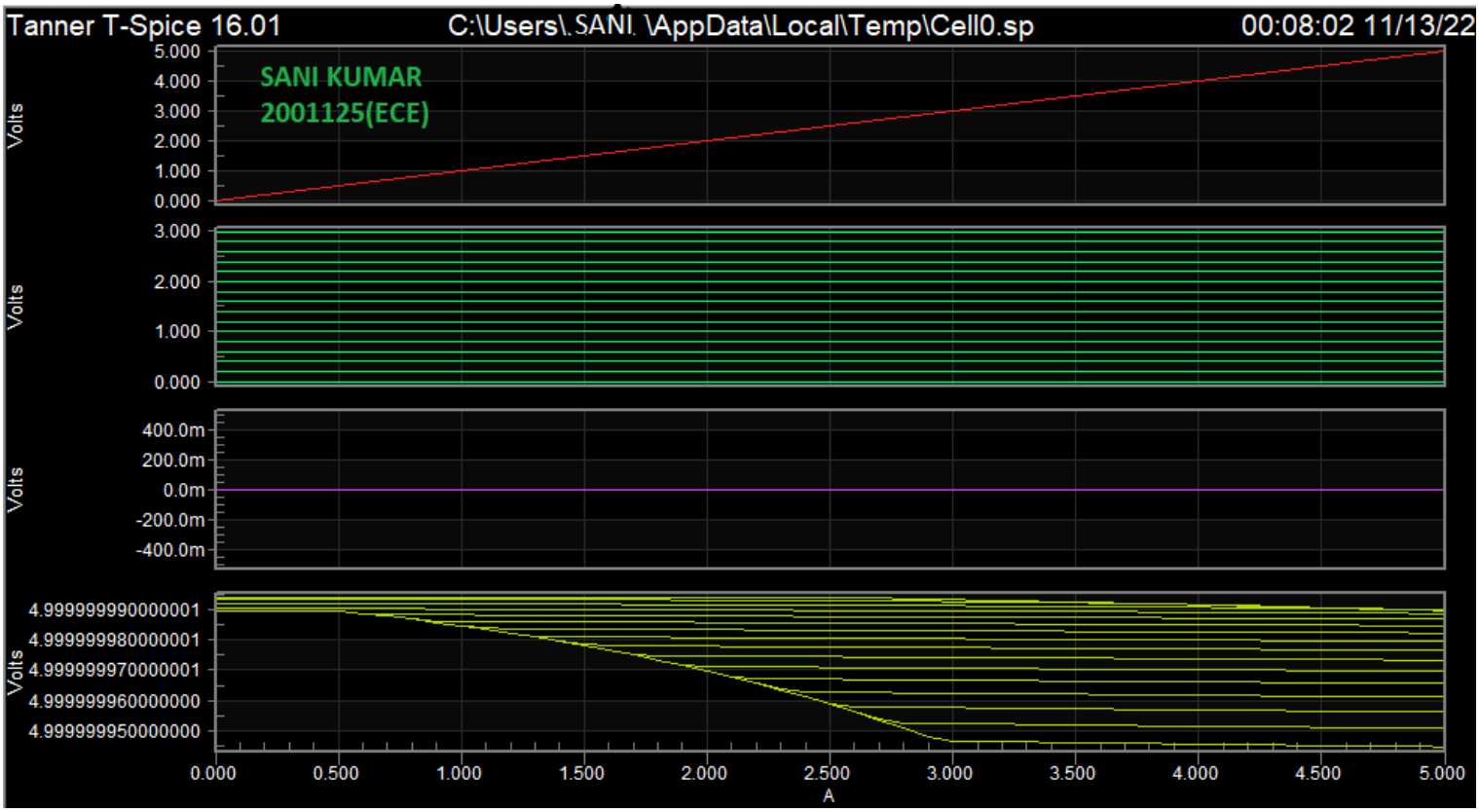


Circuit diagram-

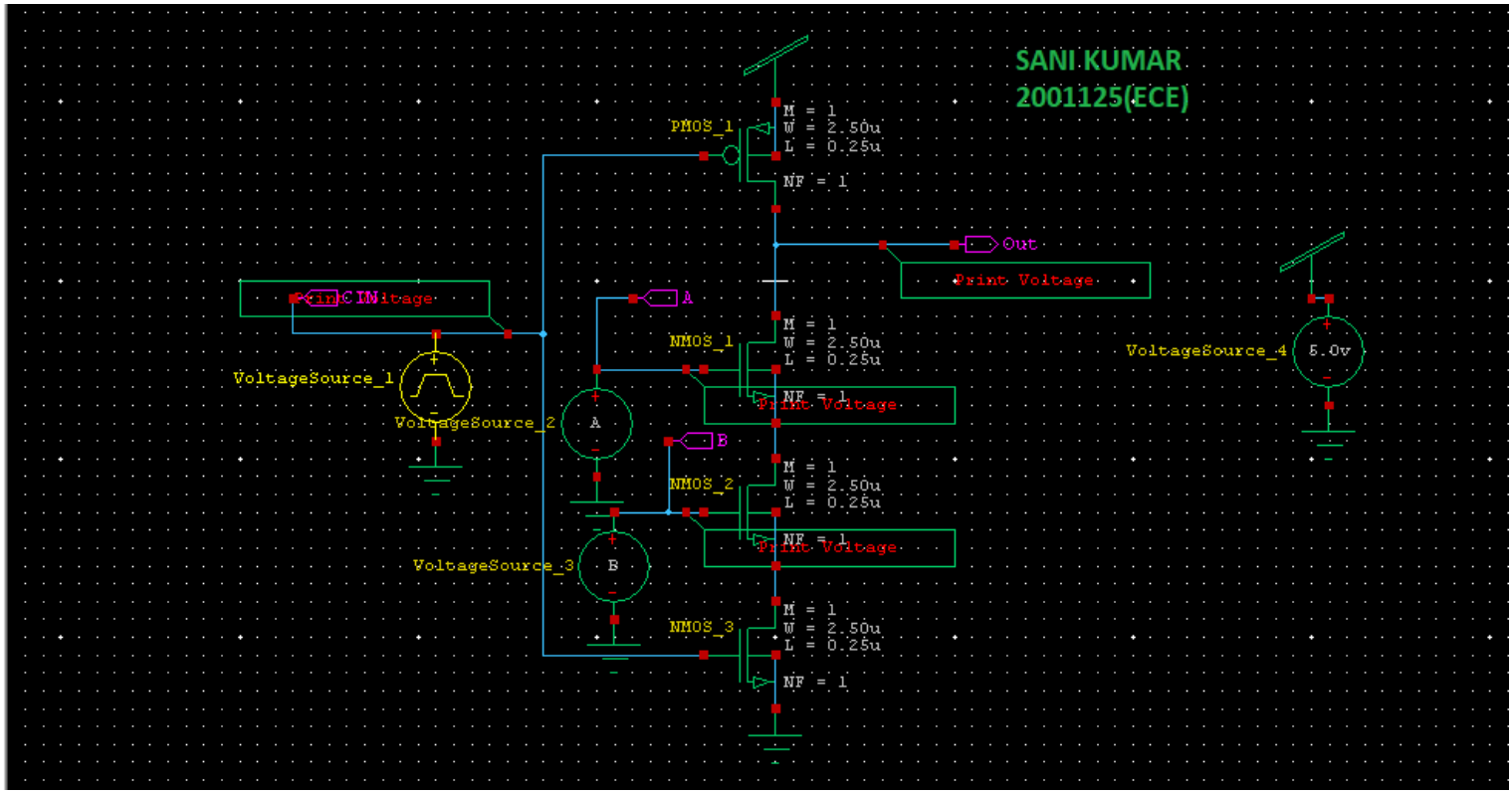
DC ANALYSIS



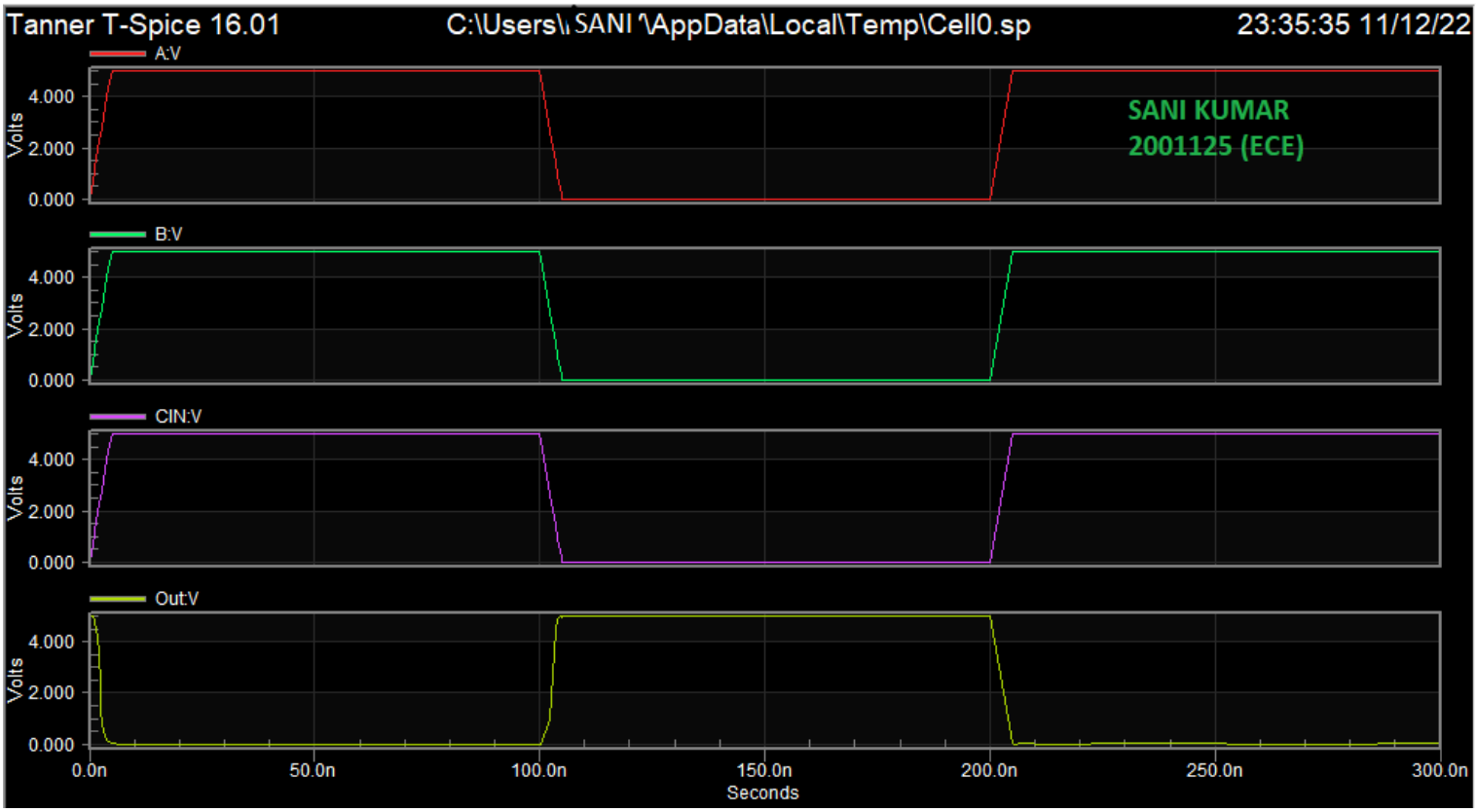
NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**



TRANSIENT ANALYSIS-



NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**



AIM

DC and transient analysis of RATIOED logic circuit.

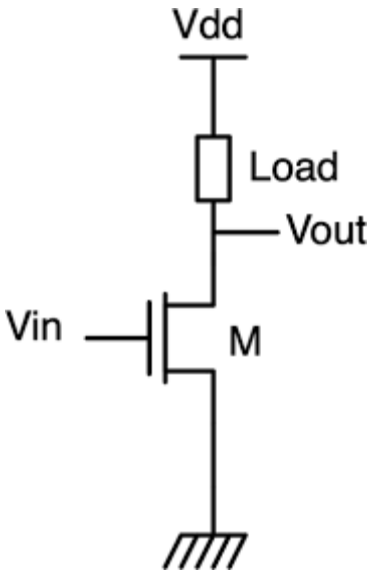
APPARATUS REQUIRED:

PMOS, NMOS, VDD, GROUND,OUTPUT INPUT PORT

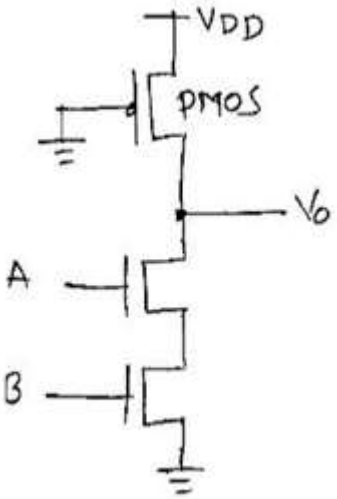
THEORY:

Ratioed circuits use weak pull-up devices and stronger pull- down devices. They reduce the input capacitance and hence improve logical effort by eliminating large pMOS transistors loading the inputs but depend on the correct ratio of pull-up to pull-down strength.

NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125



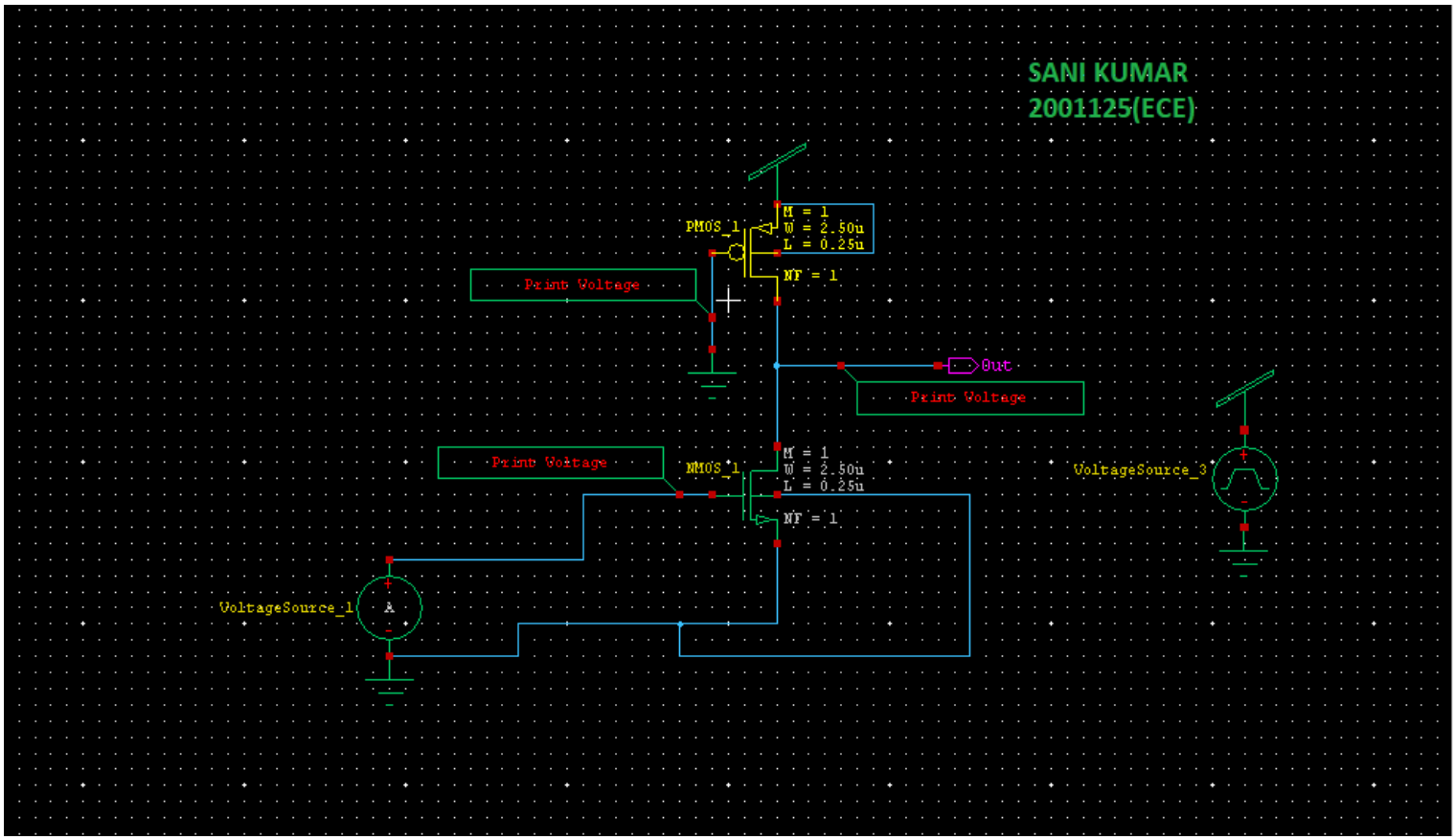
A	B	Vo
0	0	1
0	1	1
1	0	1
1	1	0

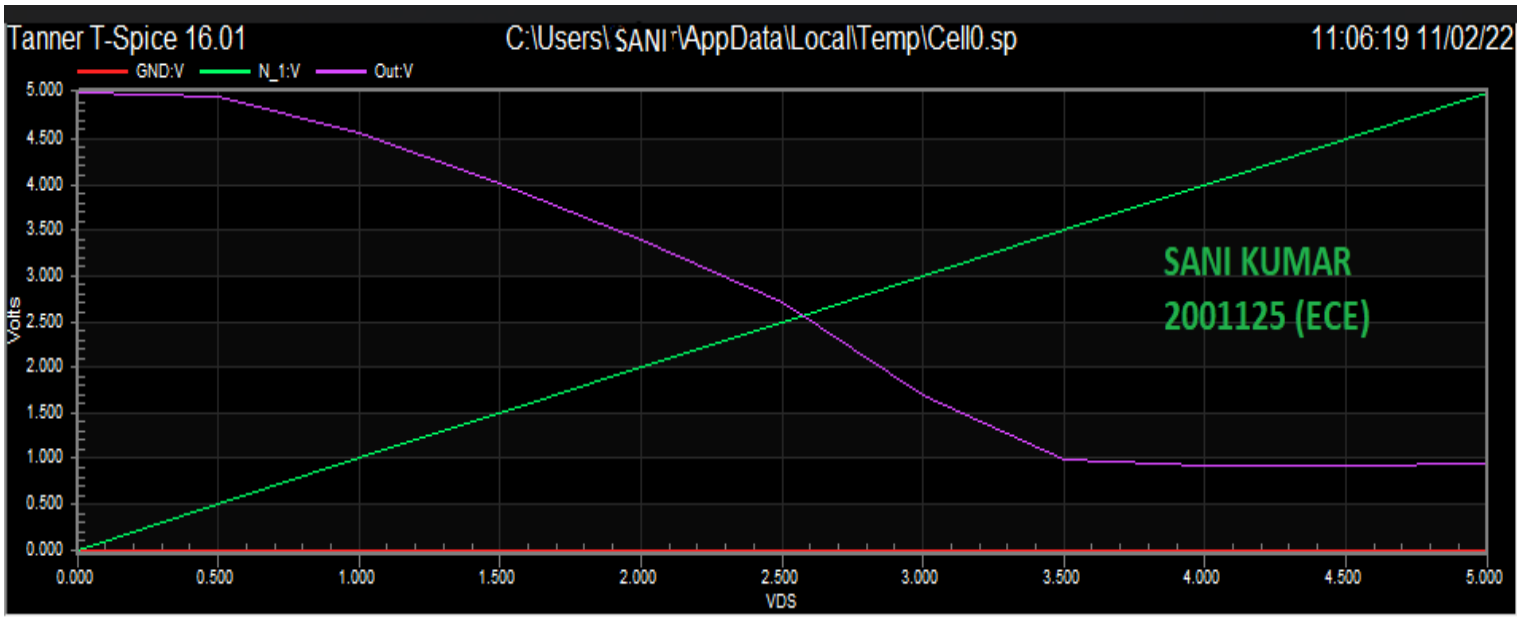


DC ANALYSIS-

CIRCUIT DIAGRAM –

NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**

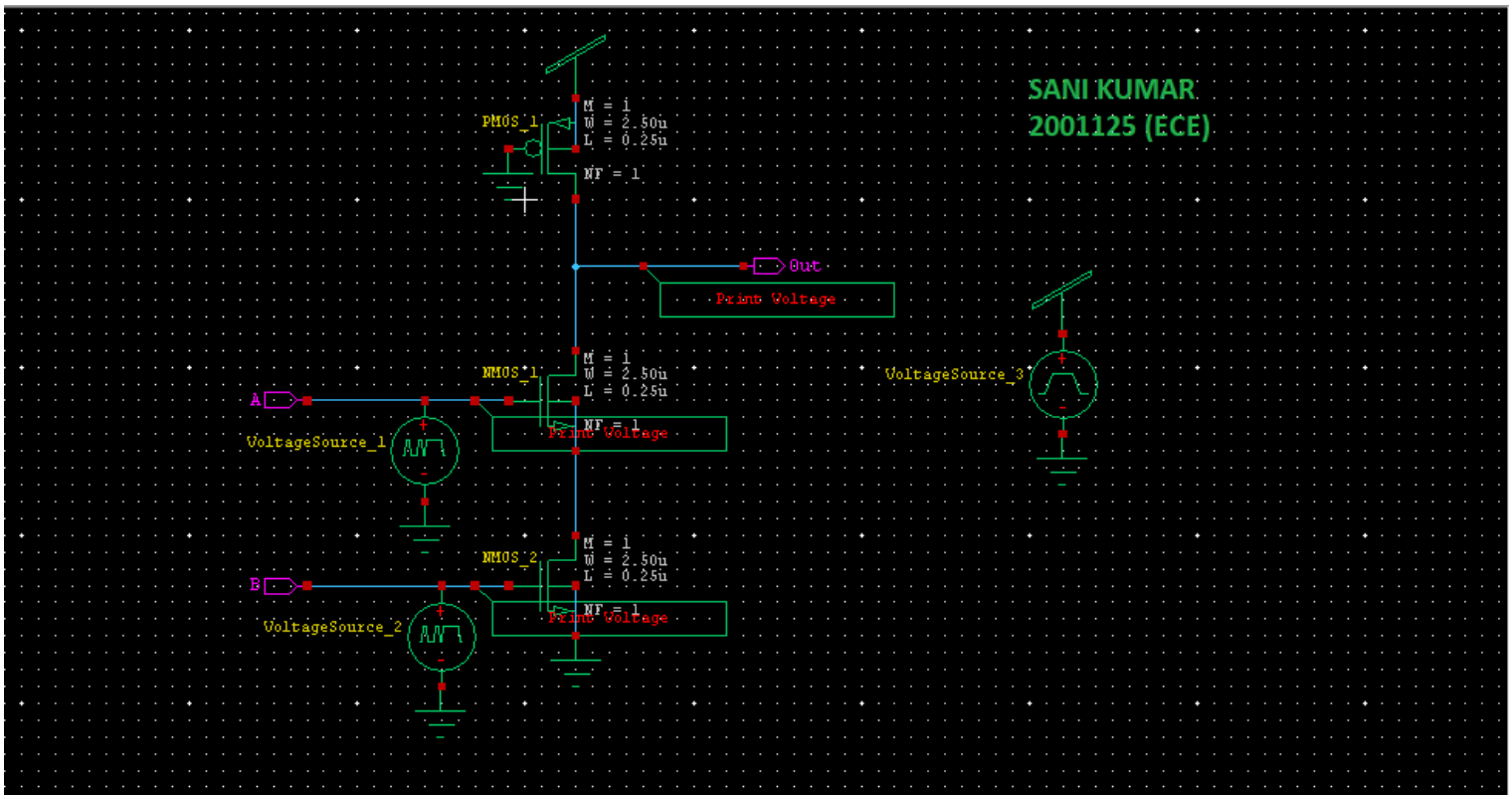


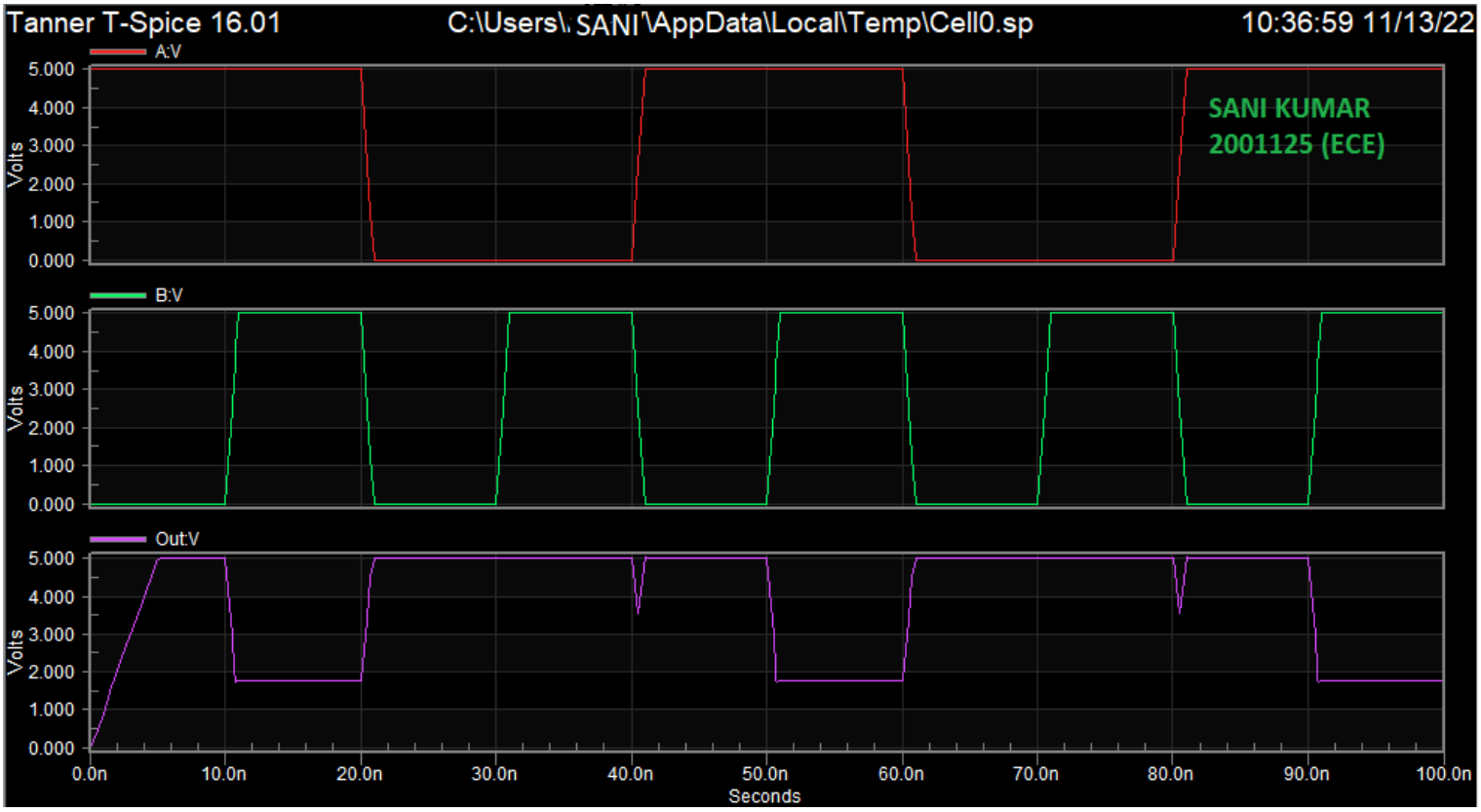


TRANSIENT ANALYSIS-

Circuit diagram-

NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**





NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125

EXPERIMENT 9

AIM

DC and transient analysis of RATIOED logic circuit.

APPARATUS REQUIRED:

PMOS, NMOS, VDD, GROUND,OUTPUT INPUT PORT

THEORY:

A transmission gate is an electronic element and good non mechanical relay built with CMOS technology. It is made by parallel combination of nMOS and pMOS transistors with the input at the gate of one transistor (C) being complementary to the input at the gate () of the other.

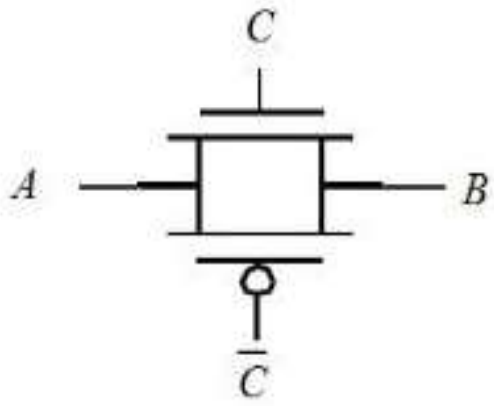
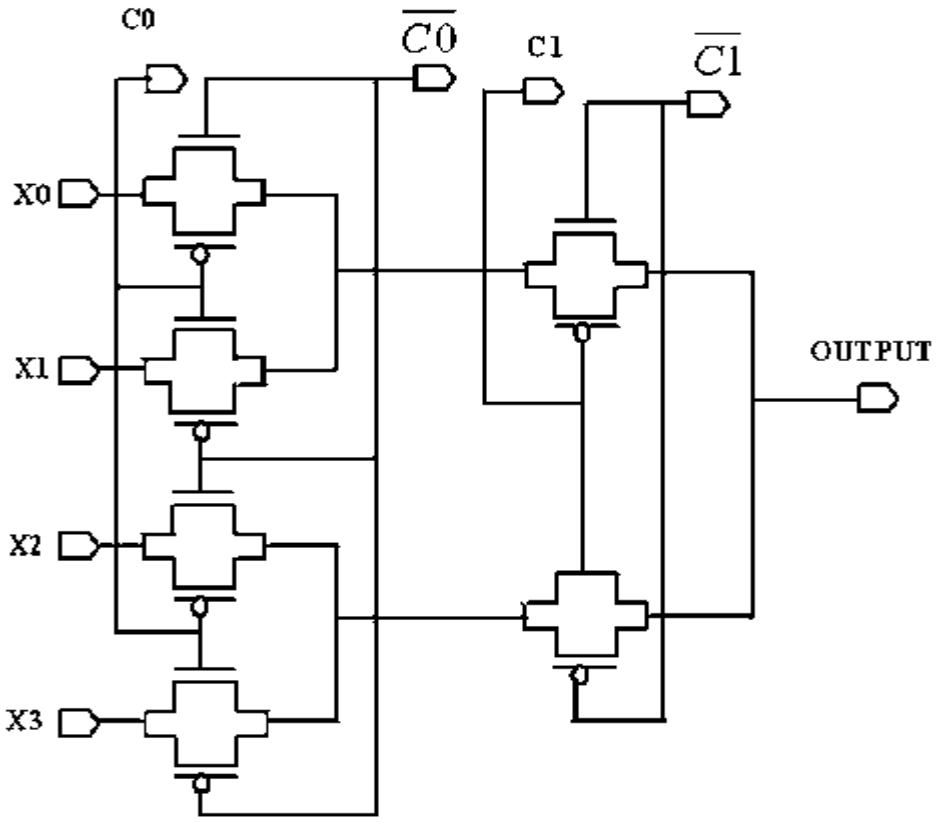


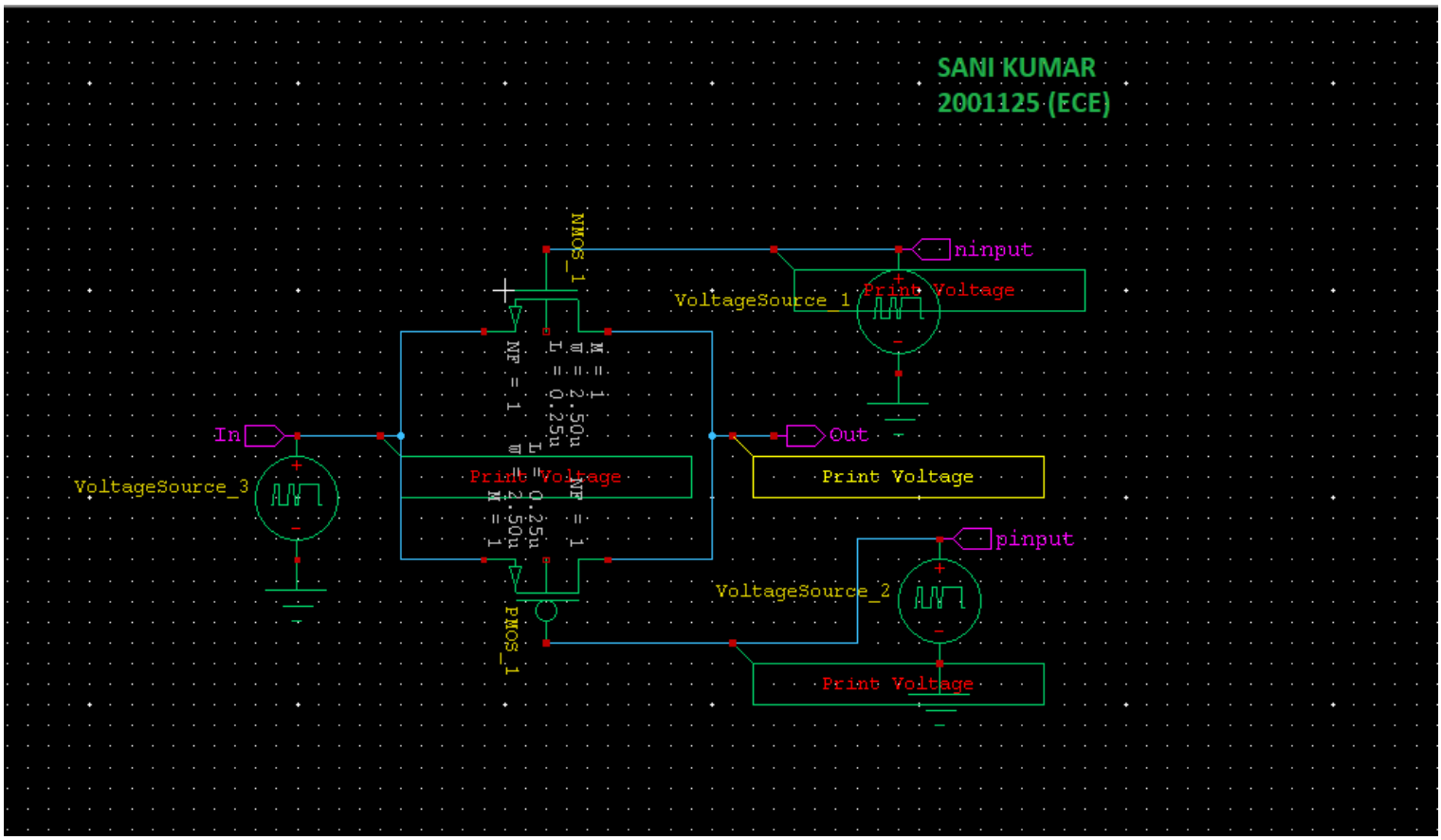
Fig.4: Symbol for tranmission gate

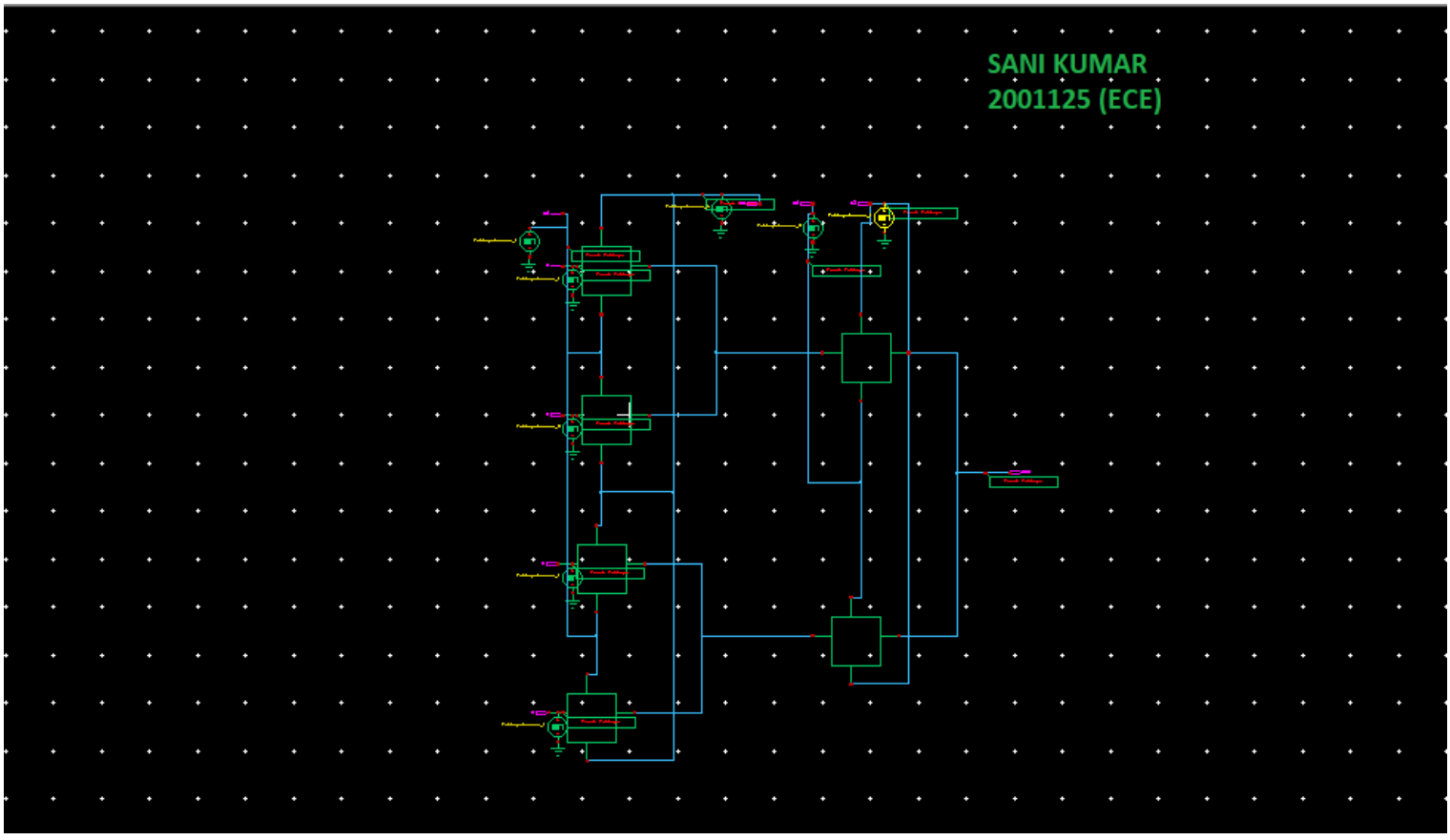
NAME :- SANI KUMAR BRANCH :- ECE ROLL NO. :- 2001125



Transmission gate construction –

NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**





NAME :- SANI KUMAR **BRANCH :- ECE** **ROLL NO. :- 2001125**

OUTPUT :-