Delay Pedal Circuit- PT2399 based

Sanidhya Anand (19d170027)

Madhumitha S (19d170013)

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Project Report

This circuit is of a three-knob delay pedal, used very commonly by guitarists and other musicians in the music industry. It is based on the Boy-In-Well pedal, which itself uses a 9V source and a PT2399* Integrated Circuit chip to function. The circuit has three control functionalities (handled by potentiometers):

1. Time knob- Controls the amount of time between signal repeats. Itself based on a VCO or a Voltage Controlled Oscillator built into the IC, this knob can smoothly roll between delay times of 30ms and 340ms.
2. Repeats knob- Controls the number of repeats (which is feedback from the original signal) reaching the output buffer after mixing with the wet signal.
3. Level knob- Controls the volume of the wet signal, which is the tails of the delay.

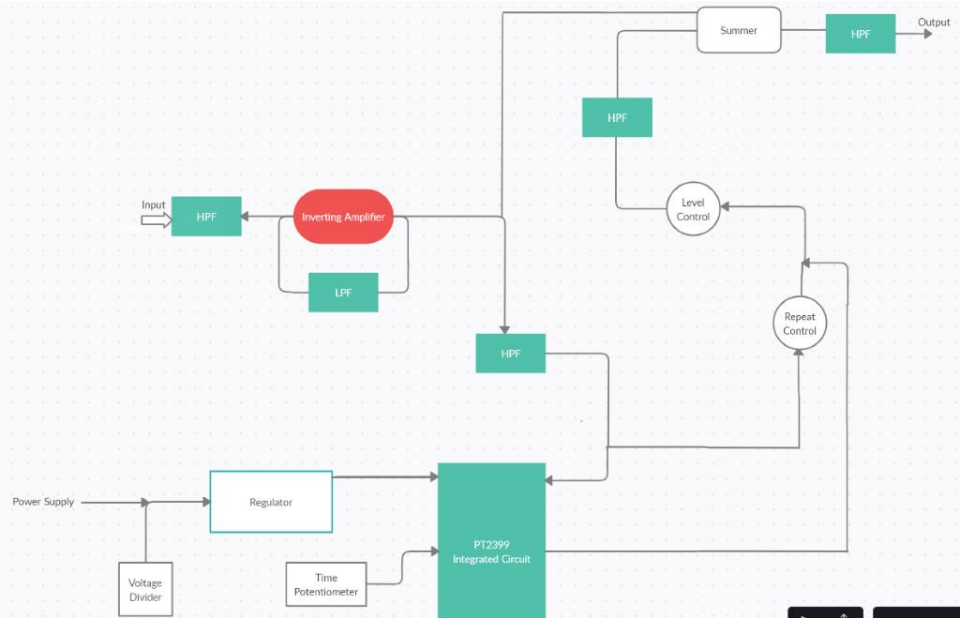
*Internal components of PT2399 are not diagrammatically shown in this report.

The entire circuit is powered by a regulated +9V adapter power supply. Reverse polarity connections of the adapter are prevented by a diode connected to ground. The basic job of the entire circuit can be divided into four parts:

1. Input Buffer and Gain stage
2. Power Supply
3. PT2399 Delay Line stage
4. Output Buffer

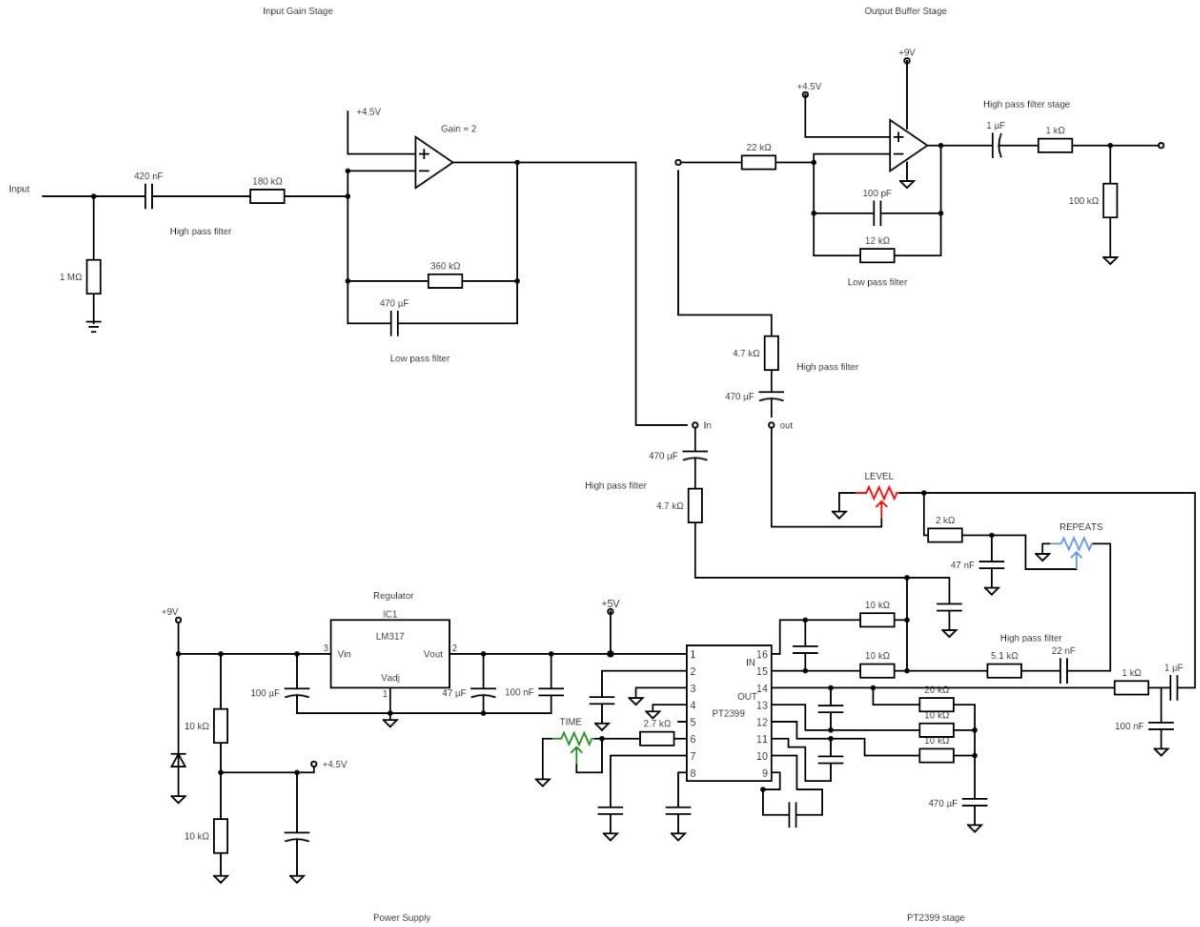
These four components of the circuit are connected to each other through various filters to remove unwanted low frequency paralytic oscillation noise and shrill unwanted high frequencies whenever needed. These filters are often represented by HPF (High Pass Filter) and LPF (Low Pass Filter). A High Pass filter gradually *removes* frequencies **BELOW** a certain cutoff value, while a Low Pass Filter gradually *removes* frequencies **ABOVE** a certain cutoff value. Hence these are used to solve the respective aforementioned abnormalities.

Block Diagram



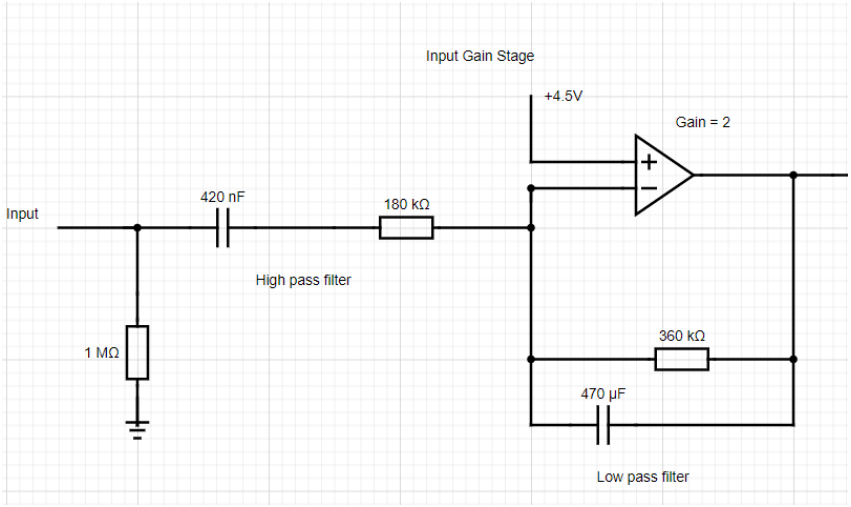
Summary of the device

The input signal to the circuit is in the form of a sound waveform. The magnetic pickups of a guitar detect vibration of the metallic strings through disturbance in the created magnetic field. These then output the waveform through a DC jack which is connected to the delay pedal circuit through a 6.35mm stereo socket. The signal has now entered the first stage of the circuit, which is the Input Gain stage. It goes through an inverting amplifier which provides a gain of ~2. This signal now splits into two parts. The first part goes into the output adder/summer op-amp topology. The second part of the circuit again splits into two, one part going into the repeat control to decide the number of feedback signals in the output, while the second part goes into the actual PT2399 IC, where it passes through multiple filters, a VCO, a delay line, and then a modulating-demodulating circuit. This output is now delayed by the time interval set by the VCO-time potentiometer combination, which acts as a clock. This output then enters the level control, which decides how loud the delayed signal (wet signal) is. Finally, they enter the output buffer stage which acts as a summer for the first part of the input (dry signal) and the delayed wet signal. This final summed voltage output is the output sound waveform.



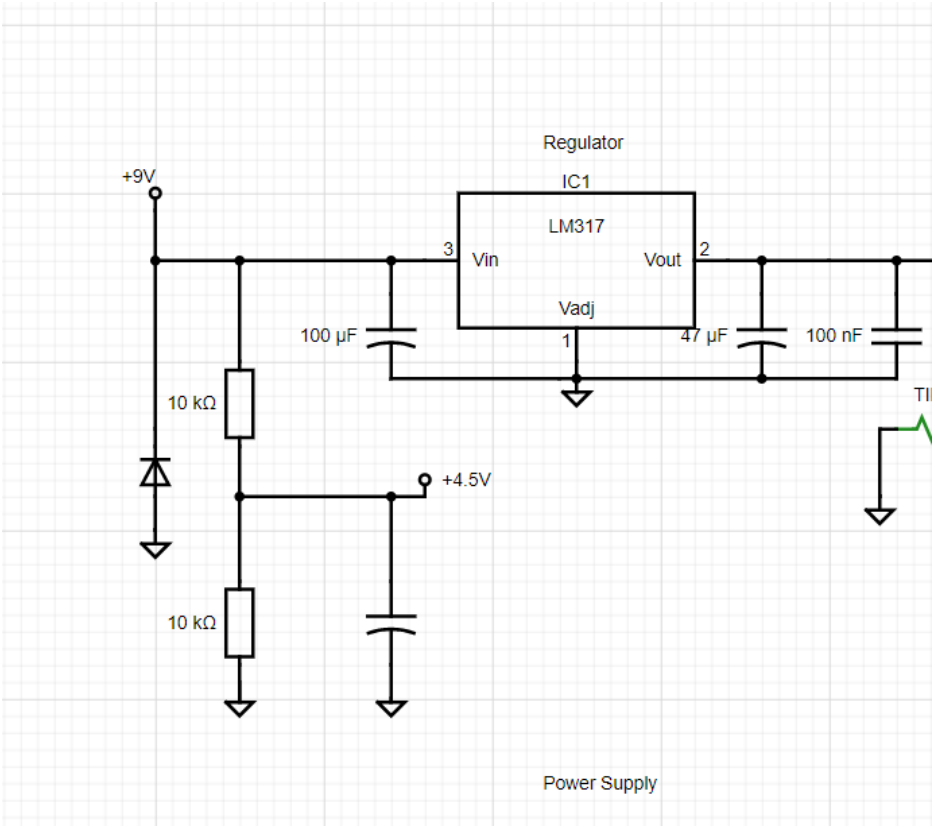
Input Buffering Amplifier (Inverting)

The input signal to the inverting amplifier passes through an HPF, which has a cut off frequency around 4Hz to remove DC and any low frequency parasitic oscillation in an idle circuit. The input resistance, due to the 1M Ohm resistor is of the order of 9.9 x 10^5 Ohm, thus preventing any spikes in the input sound (anti-pop resistor). It also ensures that the source of the signal which are the guitar pickups do not become overloaded. The voltage gain of the amplifier can be written as the negative of the value of the division of the LPF resistance by the external resistance, which in this case comes out to be –360k/180k = -2, in an inverting topology of the op amp. The capacitor connected in parallel with the op amp topology acts as an LPF, which mellows out the higher frequencies in the input signal. This cuts off any high frequency harmonics that occur from a distorted signal coming due to the buffering amplifier's gain. The cutoff frequency generally takes a value around 9.4 kHz.



Power Supply

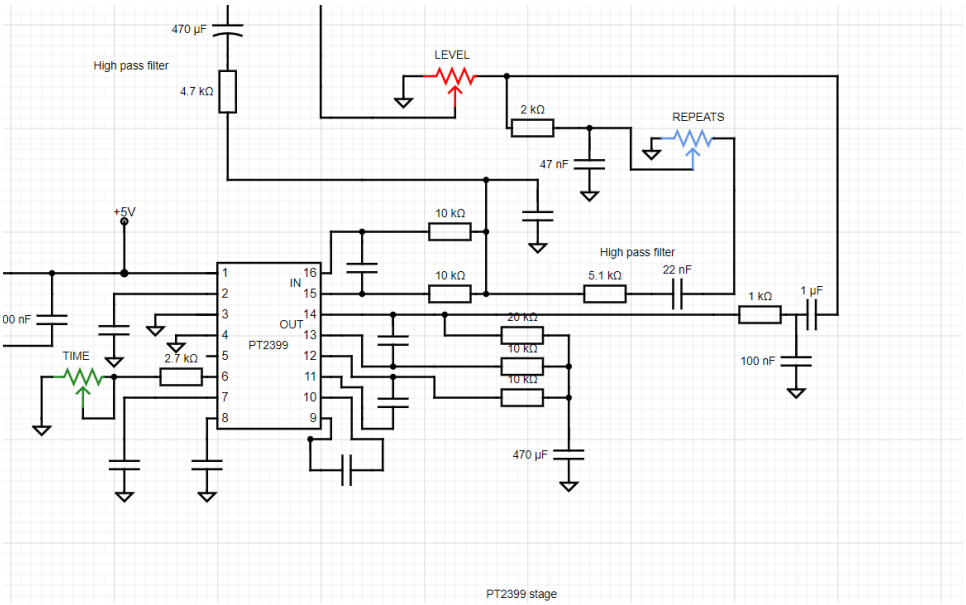
The power supply is what provides electrical power and a bias voltage to the entire circuitry. The diode protects the pedal in case the 9V DC adapter is connected in reverse polarity. The voltage divider formed by the two 10k Ohm resistors outputs a 4.5V voltage (9*10k/ (10k+10k)). This 4.5V is used as a bias voltage/virtual ground for the entire circuit. The IC shown is a 5V linear regulator and it removes any ripples from the input power supply voltage waveform with the help of the 100uf capacitor, thus outputting a constant voltage. The 5V path should be kept short to prevent any DC noise.



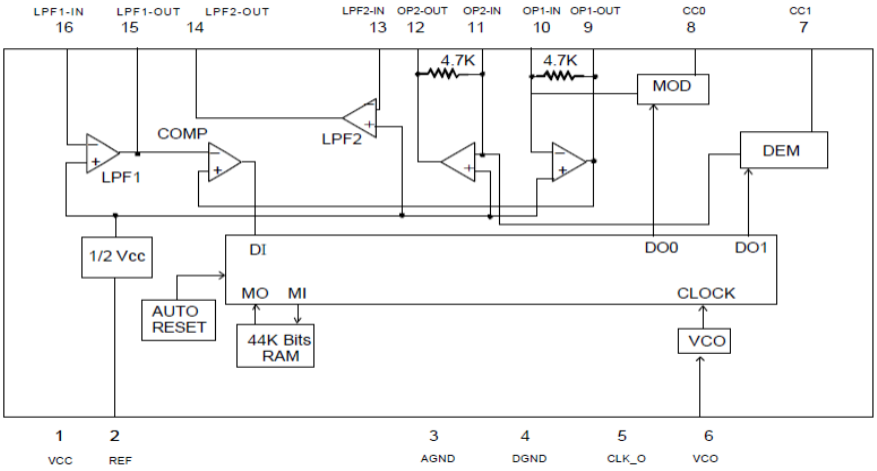
PT2399 Stage

The PT2399 is a 16 pin IC, with the first pin receiving power supply of regulated 5V DC (Vcc). This stage takes the prepared buffered audio signal and delays it before outputting. The IC takes into input the buffered signal through an HPF, and encounters the junction between the Rep eats potentiometer and the IN **pin 1** of the IC. This Repeats Potentiometer controls how much of the input signal enters the IC. The larger the value at the potentiometer, the lower is the input signal to the comparing op amp built into the IC. This comparator compares the input signal (connected to the negative voltage) with the modulated delayed signals. The higher the input signal, higher would be the amount of clock cycles for which the op amp sends an output to the delay line, thus increasing the number of repeats. The delay line is controlled by a Voltage Controlled Oscillator acting as a Clock, while this VCO is in turn controlled by the Time potentiometer at **Pin 6**. This arrangement generally gives a value of between 30 to 600 milliseconds for the delay time (clock ping time) as the VCO outputs a square wave with frequency based off the delay time. This square wave can be outputted through **Pin 5**, which can in turn be connected to a microcontroller or a tap-tempo device to set the time between delays by fixing the frequency of the square wave. Thus, it is possible to override the VCO with an external device. Delay times above 340ms lead to considerable distortion in the wet signal, hence generally keeping that as the upper limit.

If the resistance from Pin 6 to the ground is less than 2k Ohm, during the power-on of the PT2399, the chip may latch up, causing the chip to crash and stop functioning. Thus a 2.7k Ohm resistor is used to prevent this.



Coming back to the input signal, it passes through an LPF with cutoff frequency around 4300 Hz. This is so that no processing of the high frequency harmonics happens, as high-pitched delays sound unpleasant to the listener. This input signal reaches the first op-amp within the IC, which amplifies the difference between itself and the reference Voltage at **Pin 2**. This reference Voltage (2.5V) is equal to half of Vcc (5V) as there is a Voltage divider between Pin 1 and Pin 2 of uniform resistances. The output of the op-amp then becomes the negative terminal input of the comparator, which compares it with the

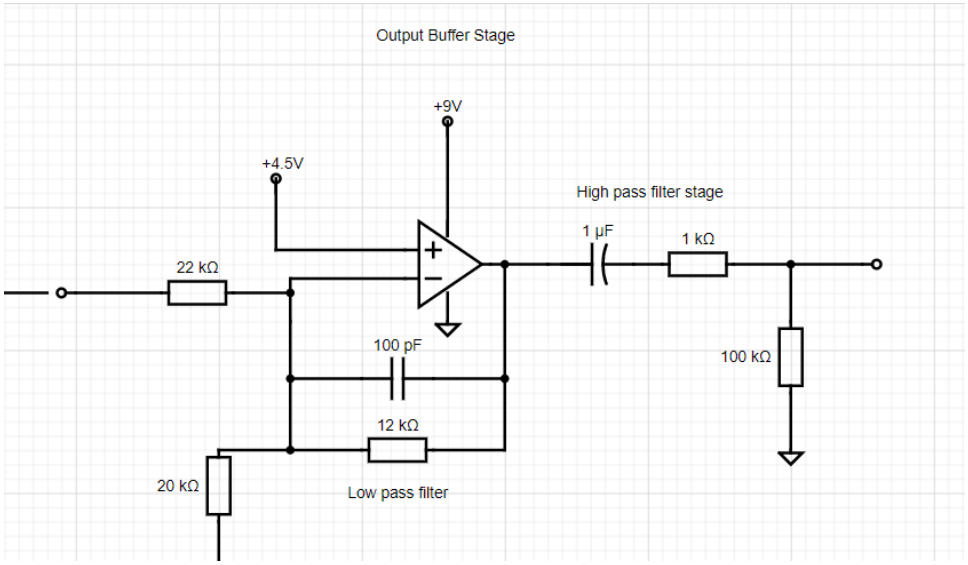


PT2399 Delay Block Diagram

output of the amplified signal coming from the Modulator, which is initially zero. The comparator gives a high output to the delay line, which now itself inputs to the modulator. The Modulator is set in a Multi Feedback Topology. This circuit basically repeatedly compares the increasing delayed signal at the positive terminal of the comparator with the input signal until it becomes greater, and the comparator outputs low, stopping the delay cycle. Thus, controlling the input signal (via the Repeats potentiometer), controls the amount of repeats in the delay signal. Furthermore, all the delayed signals go through a demodulator, whose output is then sent to another op-amp. The final output of this op-amp is the output delay signal. This output delay signal then runs through the LPF at **Pin 13** and **Pin 14** and another HPF to finally remove any unwanted noise.

Now, the level potentiometer controls the peak of this signal (wet signal). The final output of the PT2399 stage has been reached.

Output Buffer Stage



The Output Buffer is designed to attenuate the magnitude of the high frequencies with respect to the mid-low frequencies. The filter takes the unnatural sounding pre-emphasized audio and turns it back into its original response.

The op-amp is configured as a summing amplifier. The dry signal coming over 22k Ohm resistor has a little more resistance than the wet signal coming in over 20k Ohm resistor, making the mix ratio 1.1:1 in favor of the wet signal. This can be calculated using Kirchoff's current law on the junction between the summer and the summing resistances. With another potentiometer at the wet resistance, delay pedals vary the mix ratio of the two signals. This final output is our desired result after passing through an HPF to remove any noise from the op-amp.

Disclaimer Points

1. Grounding capacitors at ICs are not specified in value. This is due to ambiguity for different uses.
2. Value of capacitances in filters at the IC can safely be taken as 0.022 micro-Farad.