HW_3: Physical Design

Physical Design of Integrated Circuits
ECE 510
Spring 2019

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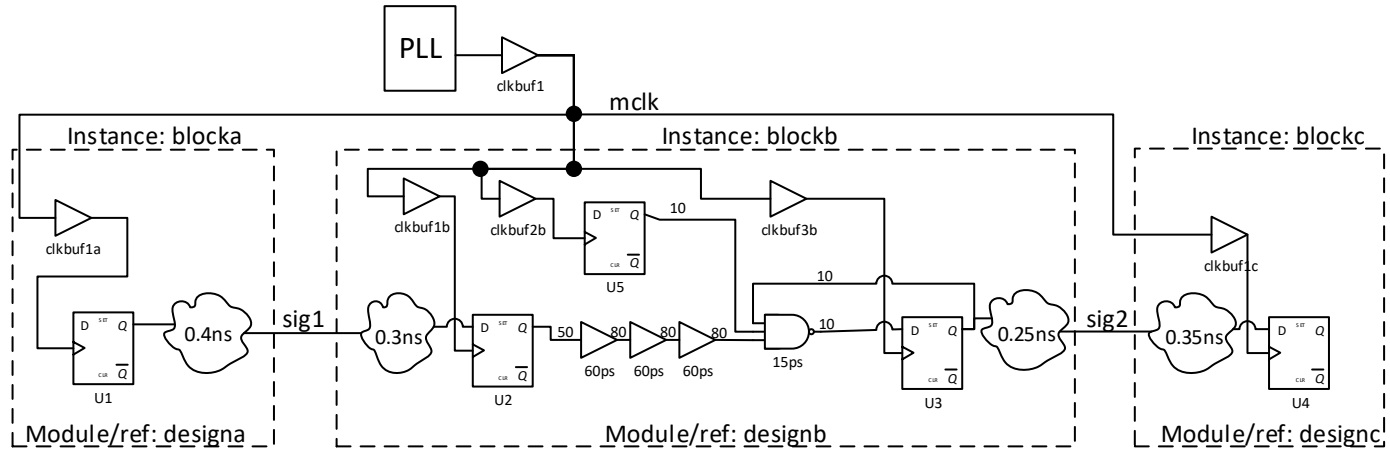
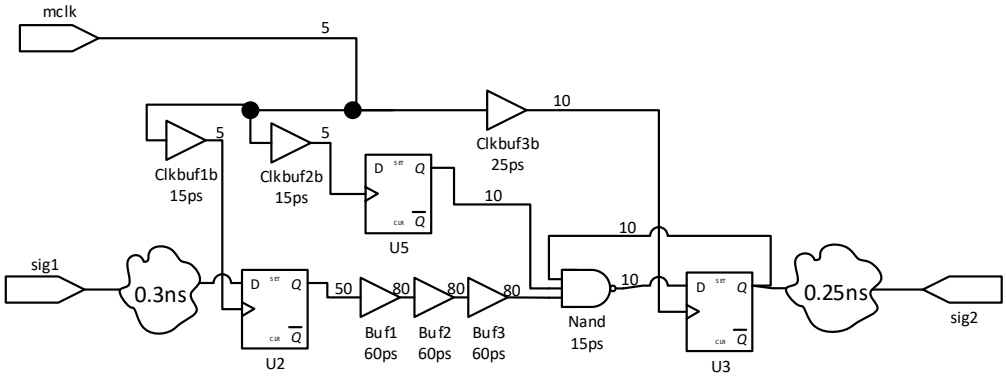
Full Chip Picture with PLL, Block A, Block B, and Block C



Block B by itself



Static Timing Analysis Questions Circuit

Extra hold margin 10ps
FF CP->Q = 80ps, setup = 30ps, hold = 20ps
clock period is 700ps with a 50/50 duty cycle
Source latency from PLL to mclk port is 70ps.
PLL jitter supplying mclk is 60ps
Net and combinational cell delays are indicated above in ps.

Before clock trees are built, the expected clock latency was 40 and skew was 30 with an endpoint transition of 100ps.

PART 1

For Block B, give the input constraints for Sig1 (delay and approximate drive constraints):

Input delay would be sum of clk-to-Q for U1 and logic delay:

set_input_delay [expr 0.4 + 0.08] [all_inputs] -clock mclk

No specific *driving cell* is specified. We can assume a cell INVXI or drive value of 0.1:

set_driving_cell -lib_cell INVX1 [all_inputs]

set_drive 0.1 sig1

For Block B, give the output constraints for Sig2 (delay and approximate load constraints)

Output delay will be sum of logic delay in block c and setup time for U4:

set_output_delay [expr 0.35 + 0.03] [all_outputs] -clock mclk

No load values given in problem statement. Assuming *load* value to be 0.1:

set_load 0.1 [all_outputs]

What are the clock constraints for pre-cts:

Creating clock of period 700 and 50% duty:

create_clock -name mclk -period 0.7 -waveform { 0.0 0.35 }

The *setup uncertainty* is jitter plus potential future clock skew:

Set_clock_uncertainty -setup -0.09 mclk

Clock latency.

The set_clock_latency -source is for the portion outside your block to the input port. This is given to be 70

set_clock_latency -source 0.07

The set_clock_latency without the source option is for the future clock skew within your block given as 40

set_clock_latency 0.04 mclk

Clock Transition given as 100ps

set_clock_transition 0.1 mclk

What are the clock constraints for post-cts:

Creating clock of period 700 and 50% duty:

create_clock -name mclk -period 0.7 -waveform { 0.0 0.35 }

The *setup uncertainty post cts* is jitter given as 60ps:

set_clock_uncertainty -setup -0.06 mclk

The *hold uncertainty* is Extra hold margin give as 10ps:

set_clock_uncertainty -hold 0.01 mclk

The set_clock_latency portion inside block is no longer used and it is propagated/calculated on the real values:

Remove_clock_latency mclk

The latency portion outside the block remains in post-cts:

Set_clock_latency -source 0.07

Remove_clock_transition mclk

Set_propogated_clock mclk

PART 2a (Ideal pre-cts Clocks)

PRECTS constraints. Ignore the clock buffer delays and only use the ideal clock numbers.
Datapath is using the indicated numbers.
SETUP PATH

```
Startpoint: U2
Endpoint: U3
Path Type: max

Point                                    Incr    Path
-----------------------------------------------------
clock mclk (rise edge)                   0.0   0.0
clock network delay (ideal)              0.11  0.11        sum of latencies 70+40ps
U2/CLK                                   0.0   0.11
U2/Q                                     0.08  0.19        clock to Q 80ps
buf1/O                                   0.11  0.30        50 +60ps
buf2/O                                   0.14  0.44        80 +60ps
buf3/O                                   0.14  0.58        80 +60ps
nand3/O                                  0.095 0.675       80 +15ps
U3/D                                     0.01  0.685       10ps net delay
data arrival time                              0.685

Clock mclk (rise edge)                   0.7   0.7         clock period 700ps
clock network delay (ideal)              0.11  0.81        sum of latencies 70+40ps
U3/CLK                                   0.0   0.81
clock uncertainty                       -0.09  0.72        -(jitter + skew)
library setup time                      -0.03  0.69        set up time 30ps
data required time                             0.69
-----------------------------------------------------
data required time                               0.690
data arrival time                                0.685
-----------------------------------------------------
slack(MET)                                      0.005
```

PART 2b (Propagated post-cts Clocks)

POST CTS constraints. Propagate the real values of the clocks
SETUP PATH

```
Startpoint: U2
Endpoint: U3
Path Type: max

Point                                    Incr    Path
-----------------------------------------------------
clock mclk (rise edge)                   0.00  0.0
clock network delay (propagated)         0.095 0.095       70 + (5+15+5)
U2/CLK                                   0.0   0.095
U2/Q                                     0.08  0.175       clock to Q 80ps
buf1/O                                   0.11  0.285       50 +60ps
buf2/O                                   0.14  0.425       80 +60ps
buf3/O                                   0.14  0.565       80 +60ps
nand3/O                                  0.095 0.660       80 +15ps
U3/D                                     0.01  0.670
data arrival time                              0.670

Clock mclk (rise edge)                   0.70  0.70        clock period 700ps
clock network delay (propagated)         0.11  0.81        70 + (5+25+10)
U3/CLK                                   0.0   0.81
clock uncertainty                       -0.06  0.75        -(jitters)
library setup time                      -0.03  0.72        set up time 30ps
data required time                             0.72
-----------------------------------------------------
data required time                             0.720
data arrival time                              0.670
-----------------------------------------------------
slack(MET)                                     0.05
```

Part 3 (Propagated post-cts Clocks)

POST CTS constraints. Propagate the real values of the clocks
HOLD PATH

```
Startpoint: U5
Endpoint: U3
Path Type: min

Point                                    Incr    Path
-----------------------------------------------------
clock mclk (rise edge)                   0.0     0.0
clock network delay (propagated)         0.095   0.095       70 + (5+15+5)
U5/CLK                                   0.0     0.095
U5/Q                                     0.08    0.175       clock to Q 80ps
nand/O                                   0.025   0.200       10+15ps
U3/D                                     0.01    0.210       10ps
data arrival time                                0.210

clock mclk (rise edge)                   0.0     0.0         hold-same edge
clock network delay (propagated)         0.11    0.11        70 + (5+25+10)
U3/CLK                                   0.0     0.11
clock uncertainty                        0.01    0.12        extra hold margin 10ps
library hold time                        0.02    0.14        hold =20ps
data required time                               0.14
-----------------------------------------------------
data required time                                0.14
data arrival time                                 0.21
-----------------------------------------------------
slack(VIOLATED)                                  -0.07
```