[[1]](#footnote-1)

Project: Routing in Physical Design

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**Abstract:**   
This project takes in RTL or netlist and transforms into a placed and routed layout using Synopsys IC Compiler. Routing involves wiring the cells together using traces on the various metal layers, with the vias providing connections between the metal layers. The general reporting includes values for cell counts, cell areas, setup and hold timing, clock skew and layout details.

**I] Indicate who is working on which topics**.

|  |  |  |
| --- | --- | --- |
|  | Project Task | Owner |
| 1 | Look up commands needed for getting data to be including for general reporting. | Kesha, Sanika, Byron, Srijana |
| 2 | Routing Critical Nets using route\_zrt\_group: Write a proc named as below which will use make the tool (ICC) to use specified routing layers for the top N (user given) paths or for a path with given start/end points | Kesha, Sanika |
| 3 | Compare usage of route\_zrt\_group command with the proc written | Kesha, Sanika |
| 4 | Routing Corridor: Using any design with a HIP or macro, show how you routing to go around the HIP | Srijana, Byron |
| 5 | Route guide: Write a proc that will generate a routing shape as follows; consider a buffer in the left side and another at the right side to begin with. The length of the horizontal and vertical segments are given by user along with the layer themselves; depending the max cap and max transition requirements, more buffers may have to be added after the routing shape is generated | Srijana, Byron |

**II] Indicate which parts of the user manuals have what you need and what commands you are researching.**

Zroute -Ch 6 ICC Implementation User Guide

* Routing Corridors: Page 6-35 to 6-38
* Routing Critical Nets: Page 6-76
* Routing Blockages: Page 6-38 (metal layer)
* Setting the routing constraints: Page 6-15
* Routing the secondary power and ground pins: Page 6-79

For skew groups,

report skew group, Query\_QOR\_snapshot in the manual

Set\_clock\_tree\_options -target -skew, set\_clock\_tree\_options -clock\_trees -max\_buffer\_levels,

query\_qor\_snapshot -name max\_logic\_level

For Layout, DRC query and Report critical area.

Report\_critical\_area -fault\_type open|short, get\_drc\_errors

**III] Indicate a time frame for each part and when it needs to come together**

* Wednesday, May 15- Finalize design with area utilization of 80% without considering HIPS and MACROS.
* Thursday, May 23- Complete 50% of the design.
* Saturday, June 1st- Complete 90% of the Project work except the documentation.
* Thursday, June 6th – Final completion with documentation of the project.

**IV] Indicate what early work has been done**. **Some actual progress is expected so that you will finish in time.**

* We are looking into user guide for finding the commands for each of the table in reporting excel sheet.
* We have finalized the design with 80% of area utilization without considering the HIPS and MACROS.
* Studying how to write proc.

**References:**

* IC Compiler Implementation User Guide

1. [↑](#footnote-ref-1)