CUMMINS COLLEGE OF ENGINEERING FOR WOMEN

(An Autonomous Institute affiliated to Savitribai Phule Pune University)

Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of positive and negative numbers declared in an array of signed decimal 10 numbers in the program. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1005H, SS:200AH and SP: 0257H
(03 Marks)

Unit-2

Q No 2 a) What is the significance of different bits in the control word register in 8255? (04 Marks) (5)

What is the role of D7 bit in CWR of 8255? (01 Marks)

Unit-3

Q No 3 a) A) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. While Decoding I2, I2 was found as a branch Instruction. What Branch Prediction algorithm steps are required? (04 Marks) (7)

B) List the features of Pentium Processor. (03 Marks)

Unit-4

Q No 4 a) What is the maximum size of GDT? Justify. (3)

Unit-5

Q No 5 a) A) How a TSS descriptor can cause a task switch? (05 Marks) (15)

B) What are Interrupts? And how are they handled by Pentium? (05 Marks)

What is the significance of following fields in TSS? – i) T bit, ii) Link to the old TSS descriptor and iii) I/O map base address (05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C1 writes L1			
C2 reads L1			
C2 writes L1			
C1 reads L1			

(04 Marks)

B) Assume that there are 4 cores and 70% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) What is the need of multicore architecture? List types of multiprocessors.
(04 Marks)

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3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add 5 Hex numbers from an array. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:2004H, ES:2005H and DI: 024FH
(03 Marks)

Unit-2

Q No 2 a) A) Give the errors that may get generated during communication using 8251 with examples. (5)
(03 Marks)

B) Compare Asynchronous and Synchronous modes of communication.
(02 Marks)

Unit-3

Q No 3 a) Pentium can fetch two instructions simultaneously. State True or False, justify your answer. List any 2 features of Pentium Processor. (7)
(04 Marks)

What is an active queue and Passive queue? When Passive queue activated?
(03 Marks)

Unit-4

Q No 4 a) There is a 32 bit segment Descriptor in Pentium. True or false? Justify. (3)

Unit-5

Q No 5 a) A) What is the significance of static and dynamic fields in a TSS. List any 2 contents of static and dynamic fields of Pentium TSS. (15)
(05 Marks)

B) MOV AX,1000H
CLI
POP BX
ADD CX, BX
DIV CX

If an external interrupt occurs while ADD instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts.
(05 Marks)

C) There are four applications currently executing in a system. How many minimum numbers of GDT(s), LDT(s) and IDT(s) can be present in the system? What will be their maximum size?
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add signed 5 decimal numbers from an array. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1004H, DS:2007H and SI: 0269H
(03 Marks)

Unit-2

Q No 2 a) What is the significance of different bits in the control word register in 8255? (5)
(04 Marks)

What is the role of D7 bit in CWR of 8255?
(01 Marks)

Unit-3

Q No 3 a) A) State the difference between 8086 Microprocessor and Pentium Microprocessor. (7)
(04 Marks)

B) Deeper the Pipeline-Deeper the Branching problem. State True or False, justify your answer.
(03 Marks)

Unit-4

Q No 4 a) There is a 32 bit segment Descriptor in Pentium. True or false? Justify. (3)

Unit-5

Q No 5 a) A) MOV AX, 1000H (15)
STI
POP BX
SUB CX, BX
DIV CX
If an external interrupt occurs while SUB instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts.
(05 Marks)

B) What is the maximum number of interrupts allowed in Pentium protected mode? Explain any two exceptions found in Pentium.
(05 Marks)

C) With a neat diagram explaining how IDTR locates IDT in memory.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to display a 2 digit number in Accumulator in decimal format. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. ES:1004H, DS:2006H and DI: 02FFH (03 Marks)

Unit-2

Q No 2 a) What is the significance of different bits in the control word register in 8255? (04 Marks) (5)

What is the role of D7 bit in CWR of 8255? (01 Marks)

Unit-3

Q No 3 a) A) There can be a 256 entry Branch Target Buffer (BTB) in Pentium System. State True or False, justify your answer. List the features of Pentium Processor. (04 Marks) (7)

B) For two consecutive instructions I4 and I5, what are Instruction Pairing/issue algorithm steps? (03 Marks)

Unit-4

Q No 4 a) Prove that v86 address formation consists of base address + offset address with example. (3)

Unit-5

Q No 5 a) A) What is multitasking? Clear the concept of time sharing with proper illustration. (05 Marks) (15)

B) How an interrupt can cause a task switch in Pentium? (05 Marks)

C) Draw and explain the Privilege Levels in the Pentium processor with example. (05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Instructions :

1. All questions are compulsory.
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3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of positive and negative numbers declared in an array of 10 Hex numbers in the program. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:F006H, DS:2006H and SI: 0F09H
(03 Marks)

Unit-2

Q No 2 a) What is the significance of different bits in the control word register in 8255? (5)
(04 Marks)

What is the role of D7 bit in CWR of 8255?
(01 Marks)

Unit-3

Q No 3 a) A) Pentium is a Two way Superscalar System. State True or False, justify your answer. List the features of Pentium Processor. (7)
(04 Marks)

B) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. To Complete the I1 and I2 instruction Decoding, what Instruction Pairing/issue algorithm steps are required?
(03 Marks)

Unit-4

Q No 4 a) There is a 32 bit segment Descriptor in Pentium. True or false? Justify. (3)

Unit-5

Q No 5 a) A) What is multitasking? Clear the concept of time sharing with proper illustration. (15)
(05 Marks)

B) How an interrupt can cause a task switch in Pentium?
(05 Marks)

C) Draw and explain the Privilege Levels in the Pentium processor with example.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P2 reads C1
ii) P3 writes C1 and P2 reads C2
iii) P2 writes C1 and P3 writes C2
iv) P1 and P3 read C1
(04 Marks)

B) Assume that there are 2 cores and 30% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Which type of processor is SoC ? What are the advantages of SoC?
(04 Marks)

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Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of even and odd numbers in an array of 10 decimal numbers declared in the program. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:C004H, DS:A006H and IP: 0A07H
(03 Marks)

Unit-2

Q No 2 a) A) Compare Mode 0 and Mode 2 of 8253. (5)
(03 Marks)

B) Give applications of Mode 0 and 2.
(02 Marks)

Unit-3

Q No 3 a) A) Pentium is a Two way Superscalar System. State True or False, justify your answer. List the features of Pentium Processor. (7)
(04 Marks)

B) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. To Complete the I1 and I2 instruction Decoding, what Instruction Pairing/issue algorithm steps are required?
(03 Marks)

Unit-4

Q No 4 a) In the real mode of Pentium it generates a 20 bit physical address. State true or false. (3)
Justify your answer.

Unit-5

Q No 5 a) A) MOV AX, 1000H (15)
STI
POP BX
SUB CX, BX
DIV CX
If an external interrupt occurs while SUB instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts.
(05 Marks)

B) What is the maximum number of interrupts allowed in Pentium protected mode? Explain any two exceptions found in Pentium.
(05 Marks)

C) With a neat diagram explaining how IDTR locates IDT in memory.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Instructions :

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Unit-1

Q No 1 a) A) Write an assembly language program to add 5 Hex numbers from an array. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:2004H, ES:2005H and DI: 024FH (03 Marks)

Unit-2

Q No 2 a) A) Give the importance of various bits in the control word of 8253. (04 Marks) (5)

B) Write the applications of 8253. (01 Marks)

Unit-3

Q No 3 a) A) There can be a 256 entry Branch Target Buffer (BTB) in Pentium System. State True or False, justify your answer. List the features of Pentium Processor. (04 Marks) (7)

B) For two consecutive instructions I4 and I5, what are Instruction Pairing/issue algorithm steps? (03 Marks)

Unit-4

Q No 4 a) Pentium supports two types of protection in memory management unit. Identify these types and give your opinion on them. (3)

Unit-5

Q No 5 a) A) MOV AX, 1000H (15)
STI
POP BX
SUB CX, BX
DIV CX

If an external interrupt occurs while SUB instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts. (05 Marks)

B) What is the maximum number of interrupts allowed in Pentium protected mode? Explain any two exceptions found in Pentium. (05 Marks)

C) With a neat diagram explaining how IDTR locates IDT in memory. (05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P2 reads C1
ii) P3 writes C1 and P2 reads C2
iii) P2 writes C1 and P3 writes C2
iv) P1 and P3 read C1
(04 Marks)

B) Assume that there are 2 cores and 30% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Which type of processor is SoC ? What are the advantages of SoC?
(04 Marks)

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Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of even and odd numbers in an array of 10 decimal numbers declared in the program. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:C004H, DS:A006H and IP: 0A07H
(03 Marks)

Unit-2

Q No 2 a) A) Justify the roles of different bits in mode definition format of 8251. (5)
(04 Marks)

B) 8251 is used for which type of communication.
(01 Marks)

Unit-3

Q No 3 a) A) Instruction and Data caches in Pentium are Two way Set Associative. State True or False, justify your answer. (04 Marks) (7)

B) Give the difference between Pipelining of 8086 Microprocessor and Pentium Microprocessor. (03 Marks)

Unit-4

Q No 4 a) There can be 1024 page tables in a Pentium system. State true or false. Justify your answer. (3)

Unit-5

Q No 5 a) A) What is the significance of static and dynamic fields in a TSS. List any 2 contents of static and dynamic fields of Pentium TSS. (05 Marks) (15)

B) MOV AX,1000H
CLI
POP BX
ADD CX, BX
DIV CX

If an external interrupt occurs while ADD instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts. (05 Marks)

C) There are four applications currently executing in a system. How many minimum numbers of GDT(s), LDT(s) and IDT(s) can be present in the system? What will be their maximum size? (05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C2 writes L1			
C2 reads L1			
C1 writes L1			
C1 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 25% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Compare i5 and i7 processors.
(04 Marks)

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Unit-1

Q No 1 a) A) Write an assembly language program to display a 2 digit number in Accumulator in decimal format. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. ES:1004H, DS:2006H and DI: 02FFH (03 Marks)

Unit-2

Q No 2 a) A) Give the importance of various bits in the control word of 8253. (04 Marks) (5)

B) Write the applications of 8253. (01 Marks)

Unit-3

Q No 3 a) A) There can be a 256 entry Branch Target Buffer (BTB) in Pentium System. State True or False, justify your answer. List the features of Pentium Processor. (04 Marks) (7)

B) For two consecutive instructions I4 and I5, what are Instruction Pairing/issue algorithm steps? (03 Marks)

Unit-4

Q No 4 a) There can be 1024 page tables in a Pentium system. State true or false. Justify your answer. (3)

Unit-5

Q No 5 a) A) How a TSS descriptor can cause a task switch? (05 Marks) (15)

B) What are Interrupts? And how are they handled by Pentium? (05 Marks)

What is the significance of following fields in TSS? – i) T bit, ii) Link to the old TSS descriptor and iii) I/O map base address (05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C1 writes L1			
C2 reads L1			
C2 writes L1			
C1 reads L1			

(04 Marks)

B) Assume that there are 4 cores and 70% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) What is the need of multicore architecture? List types of multiprocessors.
(04 Marks)

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Instructions :

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Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of even and odd numbers in an array of 10 decimal numbers declared in the program. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:C004H, DS:A006H and IP: 0A07H
(03 Marks)

Unit-2

Q No 2 a) A) Compare the BSR and I/O mode of 8255. (5)
(03 Marks)

B) Configure 8255 to interface with ADC using Port B in mode 0.
(02 Marks)

Unit-3

Q No 3 a) A) Elaborate features of Pentium Processor. (7)
(04 Marks)

B) Compare 2 stage Pipeline of 8086 Microprocessor with 5 stage pipeline of Pentium Microprocessor.
(03 Marks)

Unit-4

Q No 4 a) Pentium supports two types of protection in memory management unit. Identify these types and give your opinion on them. (3)

Unit-5

Q No 5 a) A) What is multitasking? Clear the concept of time sharing with proper illustration. (15)
(05 Marks)

B) How an interrupt can cause a task switch in Pentium?
(05 Marks)

C) Draw and explain the Privilege Levels in the Pentium processor with example.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Instructions :

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Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of positive and negative numbers declared in an array of 10 Hex numbers in the program. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:F006H, DS:2006H and SI: 0F09H
(03 Marks)

Unit-2

Q No 2 a) A) Give the importance of various bits in the control word of 8253. (04 Marks) (5)

B) Write the applications of 8253.
(01 Marks)

Unit-3

Q No 3 a) A) Pentium is a Two way Superscalar System. State True or False, justify your answer. List the features of Pentium Processor. (7)
(04 Marks)

B) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. To Complete the I1 and I2 instruction Decoding, what Instruction Pairing/issue algorithm steps are required?
(03 Marks)

Unit-4

Q No 4 a) There can be 1024 page tables in a Pentium system. State true or false. (3)
Justify your answer.

Unit-5

Q No 5 a) A) Discuss various fields in a Task Gate Descriptor with a diagram. (15)
(05 Marks)

B) Describe an IDT table. What is the Limit of the IDT table? Justify.
(05 Marks)

C) What do you mean by privilege levels? How can system software change the Privilege level using Task Gate?
(05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C1 reads L1			
C2 writes L1			
C1 writes L1			
C2 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 65% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Differentiate Heterogenous and Homogenous Architectures with diagrams.
(04 Marks)

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Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add unsigned 5 decimal numbers from an array. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1004H, DS:2006H and IP: 00F7H
(03 Marks)

Unit-2

Q No 2 a) A) Justify the roles of different bits in mode definition format of 8251. (04 Marks) (5)

B) 8251 is used for which type of communication.
(01 Marks)

Unit-3

Q No 3 a) A) There can be a 256 entry Branch Target Buffer (BTB) in Pentium System. State True or False, justify your answer. List the features of Pentium Processor. (04 Marks) (7)

B) For two consecutive instructions I4 and I5, what are Instruction Pairing/issue algorithm steps? (03 Marks)

Unit-4

Q No 4 a) Prove that v86 address formation consists of base address + offset address with example. (3)

Unit-5

Q No 5 a) A) Discuss various fields in a Task Gate Descriptor with a diagram. (05 Marks) (15)

B) Describe an IDT table. What is the Limit of the IDT table? Justify. (05 Marks)

C) What do you mean by privilege levels? How can system software change the Privilege level using Task Gate? (05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i. P1 and P3 read C1
ii. P1 writes C1 and P2 reads C2
iii. P1 writes C1 and P2 writes C2
iv. P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 40% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) In a multiprocessor system, processors operate in parallel, and independently multiple caches may possess different copies of the same memory block. What is this problem called? Elaborate it in detail.
(04 Marks)

CUMMINS COLLEGE OF ENGINEERING FOR WOMEN

(An Autonomous Institute affiliated to Savitribai Phule Pune University)

Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to display a 2 digit number in Accumulator in decimal format. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. ES:1004H, DS:2006H and DI: 02FFH
(03 Marks)

Unit-2

Q No 2 a) A) Compare Mode 1 and Mode 3 of 8253. (03 Marks) (5)

B) Give applications of each mode.
(02 Marks)

Unit-3

Q No 3 a) A) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. While Decoding I2, I2 was found as a branch Instruction. What Branch Prediction algorithm steps are required? (04 Marks) (7)

B) List the features of Pentium Processor. (03 Marks)

Unit-4

Q No 4 a) Prove that v86 address formation consists of base address + offset address with example. (3)

Unit-5

Q No 5 a) A) What is the significance of static and dynamic fields in a TSS. List any 2 contents of static and dynamic fields of Pentium TSS. (05 Marks) (15)

B)
```
MOV AX,1000H
CLI
POP BX
ADD CX, BX
DIV CX
```
If an external interrupt occurs while ADD instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts. (05 Marks)

C) There are four applications currently executing in a system. How many minimum numbers of GDT(s), LDT(s) and IDT(s) can be present in the system? What will be their maximum size? (05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C2 writes L1			
C2 reads L1			
C1 writes L1			
C1 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 25% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Compare i5 and i7 processors.
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add unsigned 5 decimal numbers from an array. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1004H, DS:2006H and IP: 00F7H
(03 Marks)

Unit-2

Q No 2 a) A) Compare Mode 0 and Mode 2 of 8253. (03 Marks) (5)

B) Give applications of Mode 0 and 2.
(02 Marks)

Unit-3

Q No 3 a) A) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. While Decoding I2, I2 was found as a branch Instruction. What Branch Prediction algorithm steps are required? (7)
(04 Marks)

B) List the features of Pentium Processor.
(03 Marks)

Unit-4

Q No 4 a) Prove that v86 address formation consists of base address + offset address with example. (3)

Unit-5

Q No 5 a) A) There are five applications currently executing in a system. How many minimum numbers of GDT(s), LDT(s) and IDT(s) can be present in the system? What will be their maximum size? (15)
(05 Marks)

B) What is the significance of TSS in multitasking? Explain with-
a) Link to the old TSS descriptor
b) T bit
(05 Marks)

C) The I/O permission bitmap of a pentium TSS segment defines the right to use ports in the I/O address space. State True or false, justify your answer.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to display a 2 digit number in Accumulator in decimal format. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. ES:1004H, DS:2006H and DI: 02FFH
(03 Marks)

Unit-2

Q No 2 a) A) Justify the roles of different bits in mode definition format of 8251. (04 Marks) (5)

B) 8251 is used for which type of communication.
(01 Marks)

Unit-3

Q No 3 a) A) Instruction and Data caches in Pentium are Two way Set Associative. State True or False, justify your answer. (04 Marks) (7)

B) Give the difference between Pipelining of 8086 Microprocessor and Pentium Microprocessor. (03 Marks)

Unit-4

Q No 4 a) Prove that v86 address formation consists of base address + offset address with example. (3)

Unit-5

Q No 5 a) A) What is multitasking? Clear the concept of time sharing with proper illustration. (05 Marks) (15)

B) How an interrupt can cause a task switch in Pentium? (05 Marks)

C) Draw and explain the Privilege Levels in the Pentium processor with example. (05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (P1, P2 and P3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines C1 and C2. C1 gets copied by processor P2 and C2 by P3 for reading. What will be the states of C1 and C2 for the following events? (12)

i) P1 reads C1
ii) P2 writes C2 and P1 reads C1
iii) P2 writes C2 and P1 writes C1
iv) P3 reads C1

(04 Marks)

B) Assume that there are 4 cores and 50% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Write a note on issues with a multiprocessor system?
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to display a 2 digit number in Accumulator in decimal format. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. ES:1004H, DS:2006H and DI: 02FFH (03 Marks)

Unit-2

Q No 2 a) A) Compare Mode 1 and Mode 3 of 8253. (03 Marks) (5)

B) Give applications of each mode. (02 Marks)

Unit-3

Q No 3 a) A) Instruction and Data caches in Pentium are Two way Set Associative. State True or False, justify your answer. (04 Marks) (7)

B) Give the difference between Pipelining of 8086 Microprocessor and Pentium Microprocessor. (03 Marks)

Unit-4

Q No 4 a) Pentium supports two types of protection in memory management unit. Identify these types and give your opinion on them. (3)

Unit-5

Q No 5 a) A) Explain Task Linking with a suitable diagram. (15)
(05 Marks)

B) What are Exceptions? And how are they handled by Pentium?
(05 Marks)

C) Draw and explain a Hierarchy/Taxonomy of Pentium Interrupts.
(05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (PR1, PR2 and PR3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines LC1 and LC2. LC1 gets copied by processor PR2 and LC2 by PR3 for reading. What will be the states of LC1 and LC2 for the following events? (12)
i) PR1 writes LC1 and PR2 reads
ii) PR1 read LC2 and PR3 read LC1
iii) PR1 writes LC1 and PR2 writes LC2
iv) PR3 reads LC1
(04 Marks)

B) Assume that there are 4 cores and 80% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Differentiate I3 and I7 processors.
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to **count** the number of positive and negative numbers declared in an array of signed decimal 10 numbers in the program. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1005H, SS:200AH and SP: 0257H
(03 Marks)

Unit-2

Q No 2 a) A) Justify the roles of different bits in mode definition format of 8251. (04 Marks) (5)

B) 8251 is used for which type of communication.
(01 Marks)

Unit-3

Q No 3 a) A) Instruction and Data caches in Pentium are Two way Set Associative. State True or False, justify your answer. (04 Marks) (7)

B) Give the difference between Pipelining of 8086 Microprocessor and Pentium Microprocessor. (03 Marks)

Unit-4

Q No 4 a) What is the maximum size of GDT? Justify. (3)

Unit-5

Q No 5 a) A) Explain Task Linking with a suitable diagram. (05 Marks) (15)

B) What are Exceptions? And how are they handled by Pentium? (05 Marks)

C) Draw and explain a Hierarchy/Taxonomy of Pentium Interrupts. (05 Marks)

Unit-6

Q No 6 a) A) Consider a situation where there are three processors (PR1, PR2 and PR3) using dedicated L1 cache and shared main memory and use MESI protocol for cache coherence. Assume the events start with a copy of cache lines LC1 and LC2. LC1 gets copied by processor PR2 and LC2 by PR3 for reading. What will be the states of LC1 and LC2 for the following events? (12)

i) PR1 writes LC1 and PR2 reads
ii) PR1 read LC2 and PR3 read LC1
iii) PR1 writes LC1 and PR2 writes LC2
iv) PR3 reads LC1
(04 Marks)

B) Assume that there are 4 cores and 80% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Differentiate I3 and I7 processors.
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add unsigned 5 decimal numbers from an array. Write proper comments wherever necessary. (05 Marks) (8)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1004H, DS:2006H and IP: 00F7H
(03 Marks)

Unit-2

Q No 2 a) A) Compare Mode 0 and Mode 2 of 8253. (03 Marks) (5)

B) Give applications of Mode 0 and 2.
(02 Marks)

Unit-3

Q No 3 a) A) Pentium is a Two way Superscalar System. State True or False, justify your answer. List the features of Pentium Processor. (04 Marks) (7)

B) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. To Complete the I1 and I2 instruction Decoding, what Instruction Pairing/issue algorithm steps are required? (03 Marks)

Unit-4

Q No 4 a) Write a note on Page Table Directory and what is the role of PDBR? (3)

Unit-5

Q No 5 a) A) MOV AX, 1000H (15)
STI
POP BX
SUB CX, BX
DIV CX

If an external interrupt occurs while SUB instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts. (05 Marks)

B) What is the maximum number of interrupts allowed in Pentium protected mode? Explain any two exceptions found in Pentium. (05 Marks)

C) With a neat diagram explaining how IDTR locates IDT in memory. (05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C2 writes L1			
C2 reads L1			
C1 writes L1			
C1 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 25% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Compare i5 and i7 processors.
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add 5 Hex numbers from an array. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:2004H, ES:2005H and DI: 024FH
(03 Marks)

Unit-2

Q No 2 a) What is the significance of different bits in the control word register in 8255? (5)
(04 Marks)

What is the role of D7 bit in CWR of 8255?
(01 Marks)

Unit-3

Q No 3 a) A) Instruction and Data caches in Pentium are Two way Set Associative. State True or False, justify your answer. (04 Marks) (7)

B) Give the difference between Pipelining of 8086 Microprocessor and Pentium Microprocessor.
(03 Marks)

Unit-4

Q No 4 a) Pentium supports two types of protection in memory management unit. Identify these types and give your opinion on them. (3)

Unit-5

Q No 5 a) A) Explain Task Linking with a suitable diagram. (15)
(05 Marks)

B) What are Exceptions? And how are they handled by Pentium?
(05 Marks)

C) Draw and explain a Hierarchy/Taxonomy of Pentium Interrupts.
(05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C1 reads L1			
C2 writes L1			
C1 writes L1			
C2 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 65% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Differentiate Heterogenous and Homogenous Architectures with diagrams.
(04 Marks)

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Second Year Computer

MICROPROCESSOR ARCHITECTURES (CE2204)

Duration : 02:00 Hours | Max Marks : 50

Instructions :

1. All questions are compulsory.
2. Use of scientific calculator is allowed.
3. Draw diagrams wherever necessary.
4. Assume suitable data wherever necessary.

Unit-1

Q No 1 a) A) Write an assembly language program to add signed 5 decimal numbers from an array. Write proper comments wherever necessary. (8)
(05 Marks)

B) Find the physical address for the given contents of the registers of the 8086 microprocessor. CS:1004H, DS:2007H and SI: 0269H
(03 Marks)

Unit-2

Q No 2 a) A) Justify the roles of different bits in mode definition format of 8251. (5)
(04 Marks)

B) 8251 is used for which type of communication.
(01 Marks)

Unit-3

Q No 3 a) A) Pentium is a Two way Superscalar System. State True or False, justify your answer. List the features of Pentium Processor. (7)
(04 Marks)

B) I1 and I2 are two consecutive instructions given as an input to the 5 stage Instruction Pipeline of Pentium architecture. To Complete the I1 and I2 instruction Decoding, what Instruction Pairing/issue algorithm steps are required?
(03 Marks)

Unit-4

Q No 4 a) There can be 1024 page tables in a Pentium system. State true or false. (3)
Justify your answer.

Unit-5

Q No 5 a) A) What is the significance of static and dynamic fields in a TSS. List any 2 contents of static and dynamic fields of Pentium TSS. (15)
(05 Marks)

B) MOV AX,1000H
CLI
POP BX
ADD CX, BX
DIV CX

If an external interrupt occurs while ADD instruction is getting executed, will the instruction execute? Justify your answer. Differentiate Faults, Traps and Aborts.
(05 Marks)

C) There are four applications currently executing in a system. How many minimum numbers of GDT(s), LDT(s) and IDT(s) can be present in the system? What will be their maximum size?
(05 Marks)

Unit-6

Q No 6 a) A) Complete following table of 2 core system executing MESI and executing given sequence of operations. Assume that the cache line L1 is already copied in the dedicated cache of both the processors. (12)

Operation	Hit or Miss	L1 state in Core1	L1 state in Core2
C1 reads L1			
C2 writes L1			
C1 writes L1			
C2 reads L1			

(04 Marks)

B) Assume that there are 2 cores and 65% of a code has been parallelized. What is the amount of speed up achieved?
(04 Marks)

C) Differentiate Heterogenous and Homogenous Architectures with diagrams.
(04 Marks)