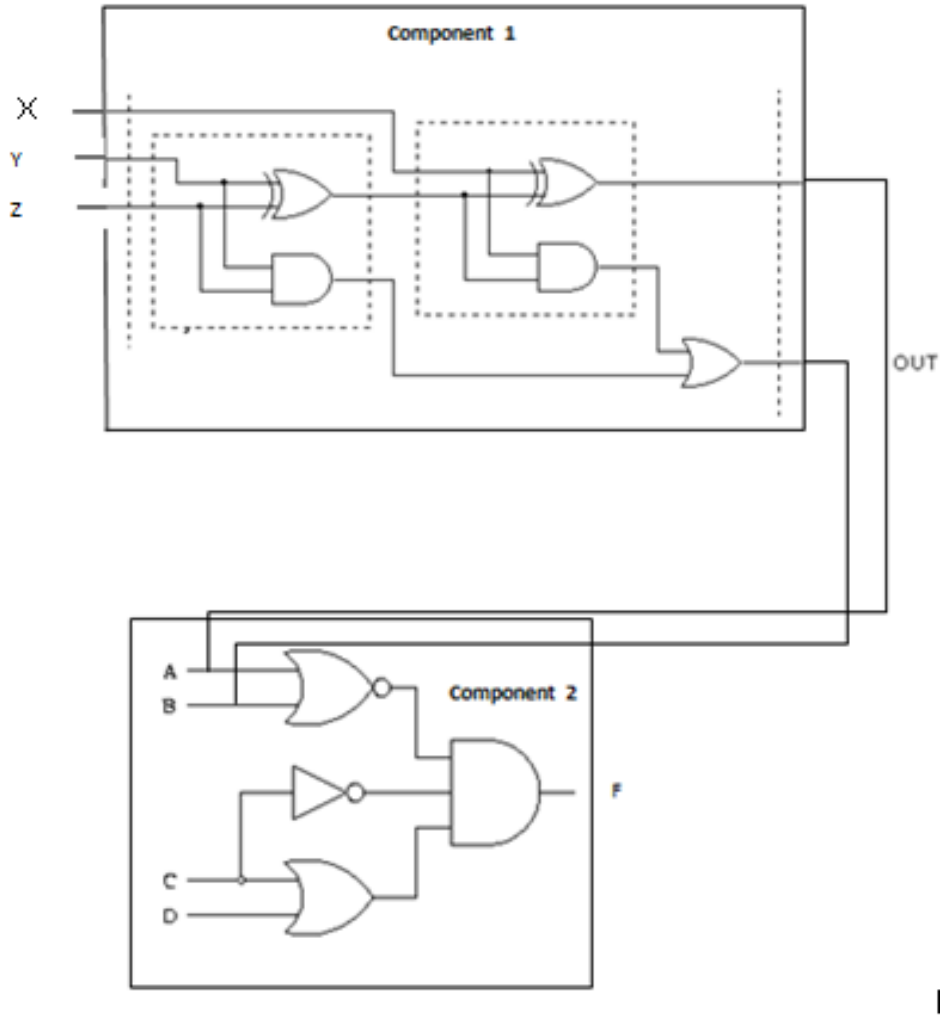
LAB 1: Mixed design using schematic and VHDL



Design the complete circuit above in one schematic file (*Primary inputs of the above circuit are: X, Y, Z, C and D; Primary Output is F*) in Quartus, where the component 1 should be coded in VHDL and component 2 designed in schematic.