LAB 3: Adder and Subtractor Unit

1. Objectives:

- In this lab you will build a 4-bit adder-subtractor unit (ASU).
- You are asked to prepare and compile a VHDL file to implement the 4-bit ASU.
- The decoded output of the three significant bits of the ASU will consist of a set of four different signals (ABCD-signals), which will be assigned individually. (See page 2 for various examples.)

2. Lab Preparation

1) Code a VHDL file to implement the ASU represented.

2) Minimize the logic expressions for your customized ABCD-signals. These minimized logic expressions are to be implemented as combinational circuit C in Figure 1 (shown below).

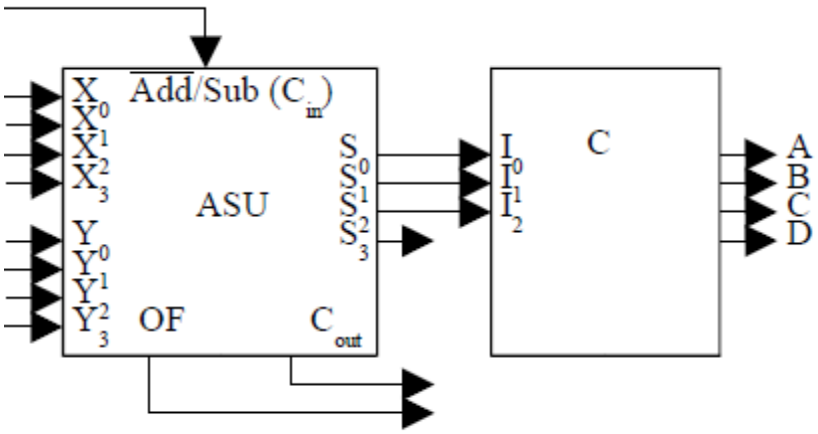

Figure 1

3) Modify the VHDL file obtained in 1) to implement the minimized logic expressions for ABCD signals.

4) Using Functional Simulator, verify the circuit described by the VHDL file obtained in 3). Observe the following signals: X3, X2, X1, X0, Y3, Y2, Y1, Y0, S3, S2, S1, S0, Cout, Cin.

Adder-Subtractor Decoded Outputs – Assignment Exercises

S			Ex.1				Ex.2				Ex.3				Ex.4				Ex.5				Ex.6				Ex.7			
2	1	0	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0	0	0	1	0	0	0	0	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	1	0	0	1	0	1	1	1
0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	1
0	1	1	1	1	1	0	1	0	0	1	1	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0	1	1	0	1
1	1	1	0	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
1	1	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0
1	0	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1	0	0	0	0

S			Ex.8				Ex.9				Ex.10				Ex.11				Ex.12				Ex.13				Ex.14			
2	1	0	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	1
0	0	1	0	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
0	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	1	0	0	1	0	1	1	1
1	1	1	0	0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0
1	1	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	0	1	0	0	1	1	1	1	0	0	1	1	1	0	1	1	0	0	0	0	0	1	1	0	1

S			Ex.15				Ex.16				Ex.17				Ex.18				Ex.19				Ex.20				Ex.21			
2	1	0	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0	1	1	0	1
0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	1	0	0	1	0	1	1	1
0	1	1	0	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	1
1	1	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0