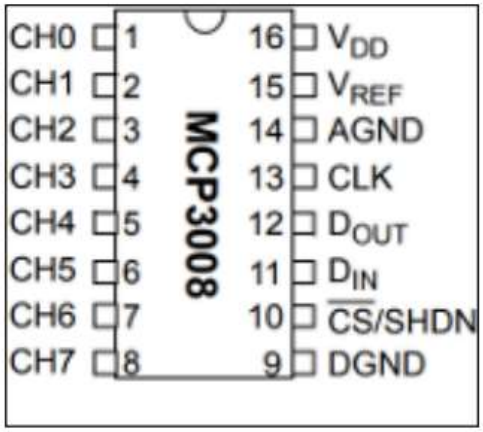
Foram Trivedi - 23B1269
Saniya Khinvasara - 23B1268

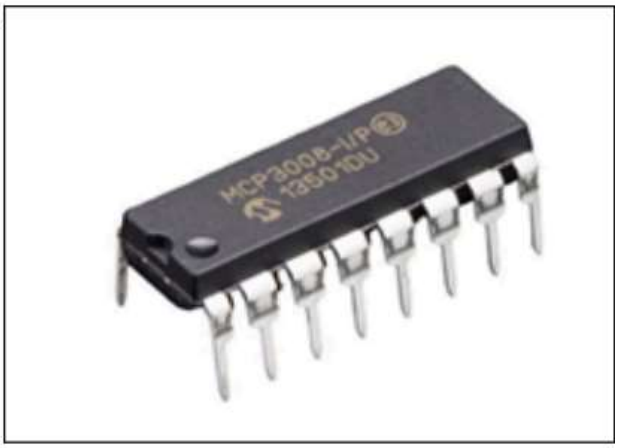
ADC to LCD via SPI

Design and Implementation of SPI-based Data Acquisition and LCD Display System using VHDL

ADC Module - MCP3008:

- The MCP3008 is a 10-bit analog-to-digital converter (ADC) from Microchip Technology, utilized as a peripheral module.
- The MCP3008 interfaces with the controller via the SPI protocol.
- It provides multiple input channels, enabling the precise digital representation of analog signals, ideal for applications requiring high accuracy in signal conversion.
- It offers 8 single-ended channels or 4 differential pairs, providing flexibility for multiple sensors.





ADC Working:

ADC converts input voltage to a corresponding digital value with respect to a reference Voltage. The calculations for the reference voltage 3.3V and input voltage 2V have been explained in calculations later.

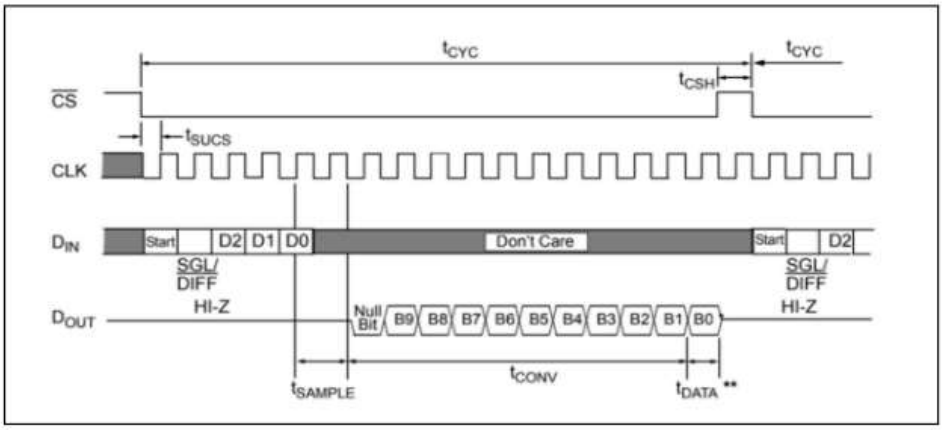
ADC configuration and SPI communication:

Clock Edges for Transmission: A total of 17 rising and falling edges are required on SCLK, with CS pulled low, for a single ADC cycle to send a 10-bit measurement to the master.

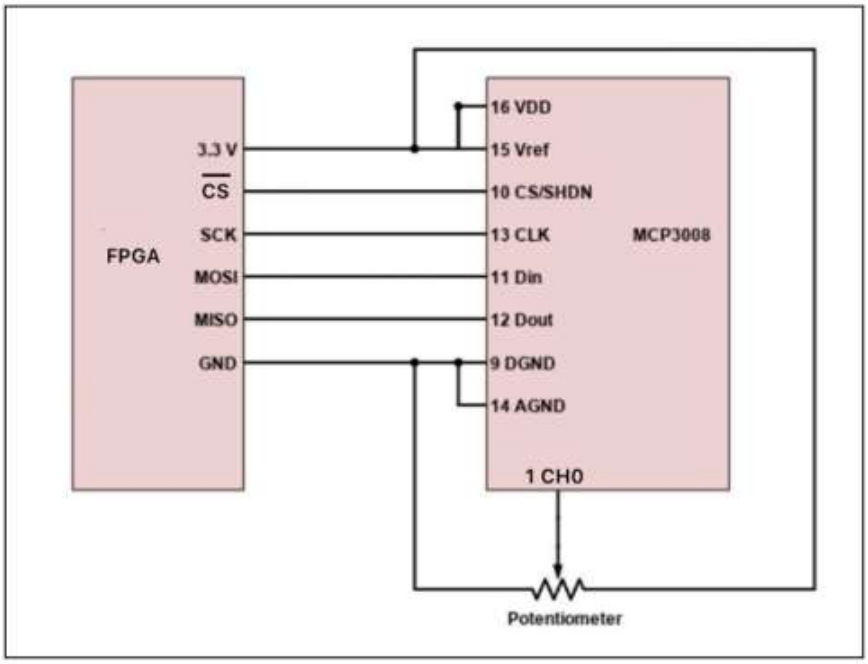
Channel Selection: To connect the potentiometer to CH0 in single-ended mode, the 4 bits

following the start bit are set to 1000. These bits configure the input type (single-ended) and select CH0.

Transmission starts at the 7th rising clock.



Circuit Design and Explanation:



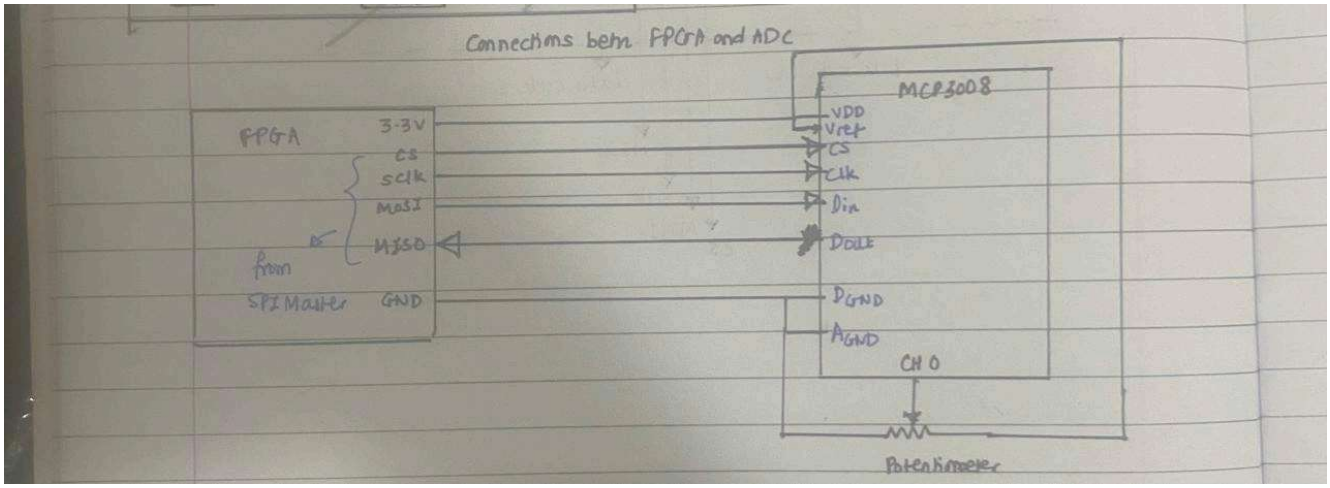
Signal Transmission: The master module sends CS, SCLK, and MOSI signals to the ADC.

Data Reception: The ADC responds by sending the MISO signal back to the master, which is stored in the "main received data" register.

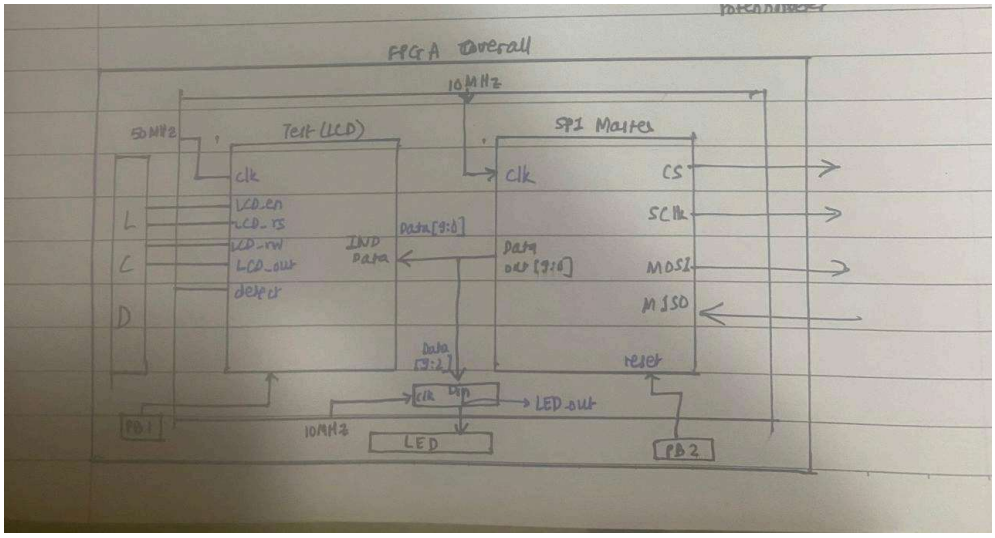
Data Transfer Completion: Once all 10 bits are transferred, the master pulls the "done" signal high, indicating data transfer is complete.

LCD Display Update: When the "done" signal is high, the register value is sent as the "inp" signal to the LCD module, configuring the LCD to display the digital output.

Block Diagram for connections between FPGA and ADC:



Block Diagram for FPGA:



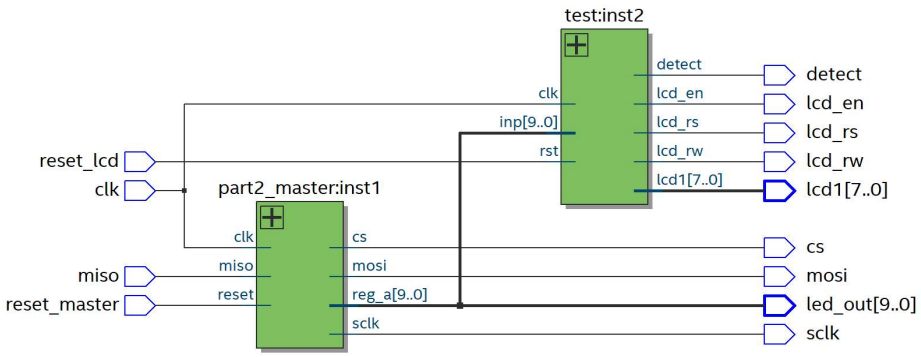
Pin Planning:

To	Direction	Location	I/O Bank	VREF Grou	Fitter Loca	I/O Standa	Reserved	Current St	Slew Rate	Differentia	Strict Preservation
clk	Input	PIN_26	2	B2_N0	PIN_26	2.5 V					
cs	Output	PIN_79	5	B5_N0	PIN_79	2.5 V					
lcd1[7]	Output	PIN_141	8	B8_N0	PIN_141	2.5 V					
lcd1[6]	Output	PIN_140	8	B8_N0	PIN_140	2.5 V					
lcd1[5]	Output	PIN_121	8	B8_N0	PIN_121	2.5 V					
lcd1[4]	Output	PIN_135	8	B8_N0	PIN_135	2.5 V					
lcd1[3]	Output	PIN_134	8	B8_N0	PIN_134	2.5 V					
lcd1[2]	Output	PIN_132	8	B8_N0	PIN_132	2.5 V					
lcd1[1]	Output	PIN_131	8	B8_N0	PIN_131	2.5 V					
lcd1[0]	Output	PIN_130	8	B8_N0	PIN_130	2.5 V					
lcd_en	Output	PIN_127	8	B8_N0	PIN_127	2.5 V					
lcd_rs	Output	PIN_122	8	B8_N0	PIN_122	2.5 V					
lcd_rw	Output	PIN_124	8	B8_N0	PIN_124	2.5 V					
led_out[9]	Output	PIN_60	3	B3_N0	PIN_60	2.5 V					
led_out[8]	Output	PIN_59	3	B3_N0	PIN_59	2.5 V					
led_out[7]	Output	PIN_58	3	B3_N0	PIN_58	2.5 V					
led_out[6]	Output	PIN_57	3	B3_N0	PIN_57	2.5 V					
led_out[5]	Output	PIN_56	3	B3_N0	PIN_56	2.5 V					
led_out[4]	Output	PIN_54	3	B3_N0	PIN_54	2.5 V					
led_out[3]	Output	PIN_52	3	B3_N0	PIN_52	2.5 V					
led_out[2]	Output	PIN_50	3	B3_N0	PIN_50	2.5 V					
miso	Input	PIN_77	5	B5_N0	PIN_77	2.5 V					
mosi	Output	PIN_75	5	B5_N0	PIN_75	2.5 V					
reset_lcd	Input	PIN_69	4	B4_N0	PIN_69	2.5 V					
reset_mas	Input	PIN_70	4	B4_N0	PIN_70	2.5 V					
sclk	Output	PIN_84	5	B5_N0	PIN_84	2.5 V					

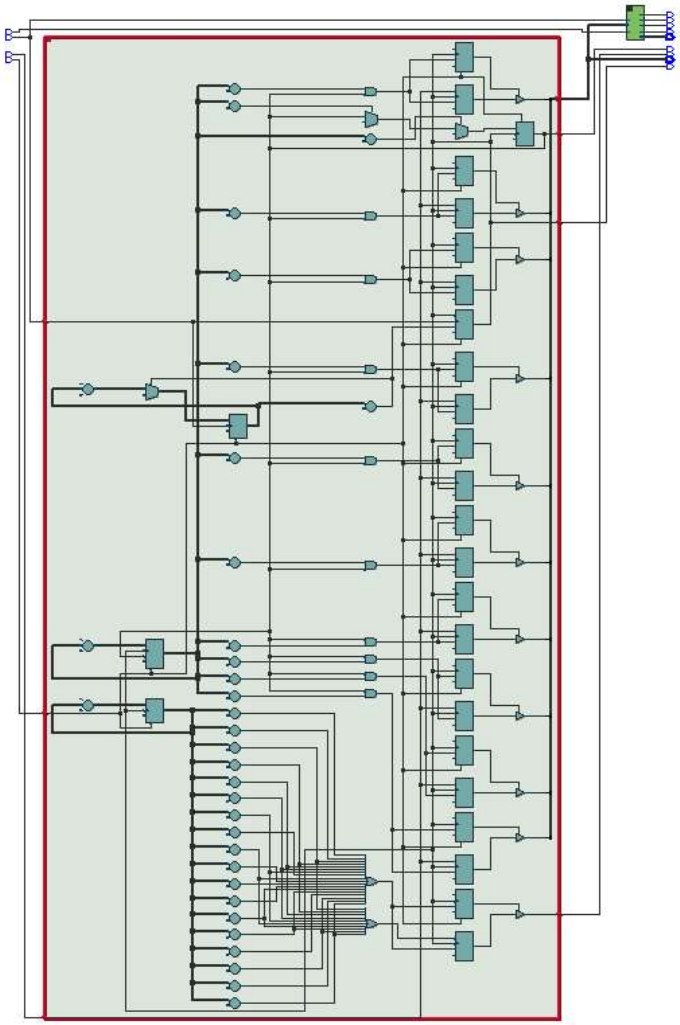
Results

Netlist Viewer:

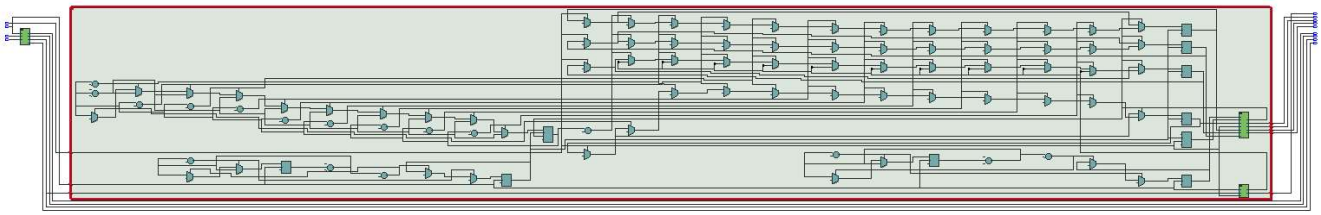
Toplevel



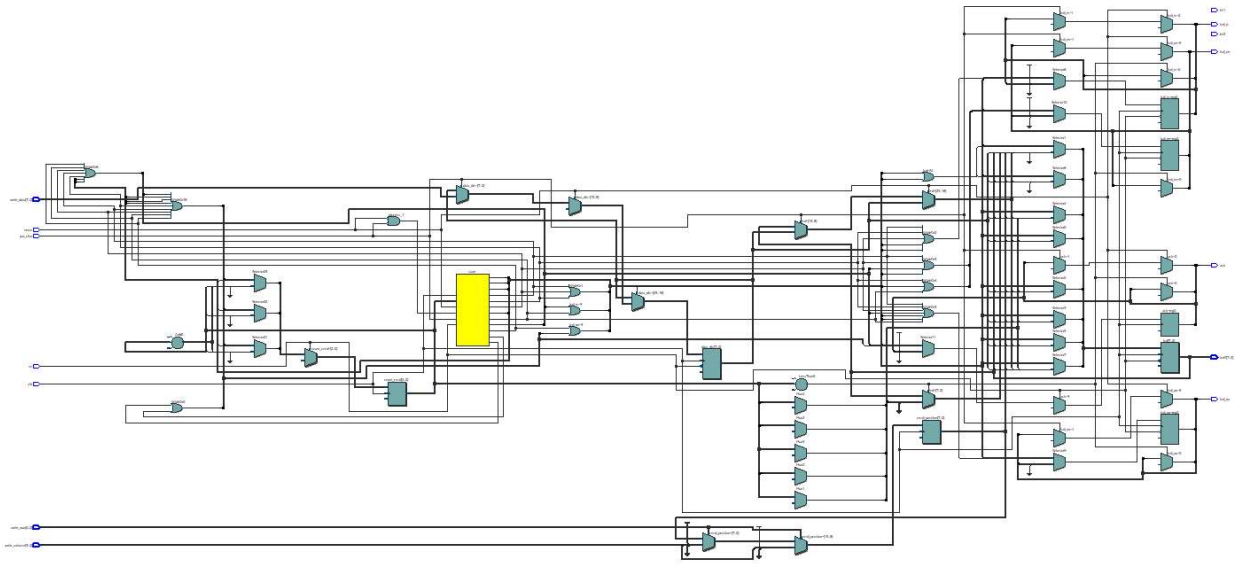
Master



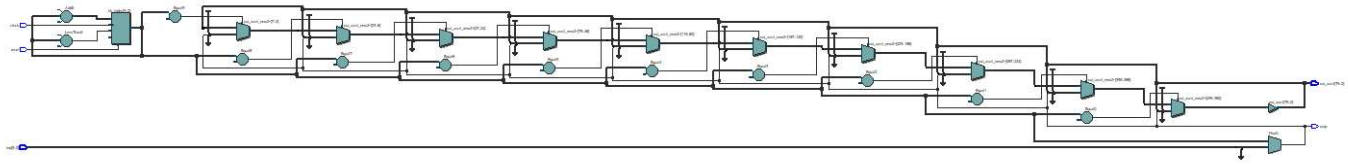
Test Module



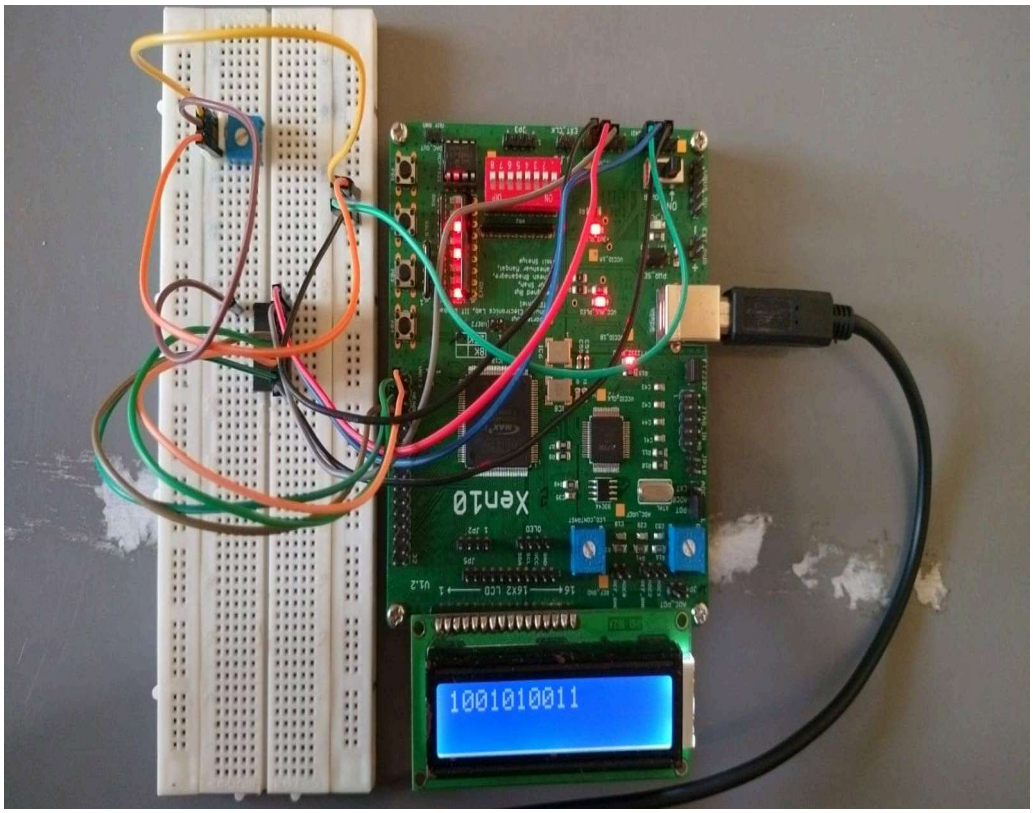
LCD Controller



INP Detect



Picture of LED and LCD Output with input voltage = 2V:



Calculations and Observations

- At Input voltage = 2V, and Vref = 3.3V, and since we have 10 bits => 2^10=1024,

  2V/3.3V * 1024 = 620.6

- The binary representation of 620.6 is around 1001101100.100
- The obtained value on LED and LCD outputs is 1001010011, which is very close to this value. The minor difference in the later bits is due to instrument errors and possible voltage fluctuations. Upto 4 MSBs, the value matches exactly, which is a fairly good result in the experimental limits.

Work Distribution

The codes were written together by both of us. The report work was divided - Foram wrote the theory, Saniya wrote the calculations and netlist viewers and drew the block diagrams. The circuit was implemented together and both did equal work.