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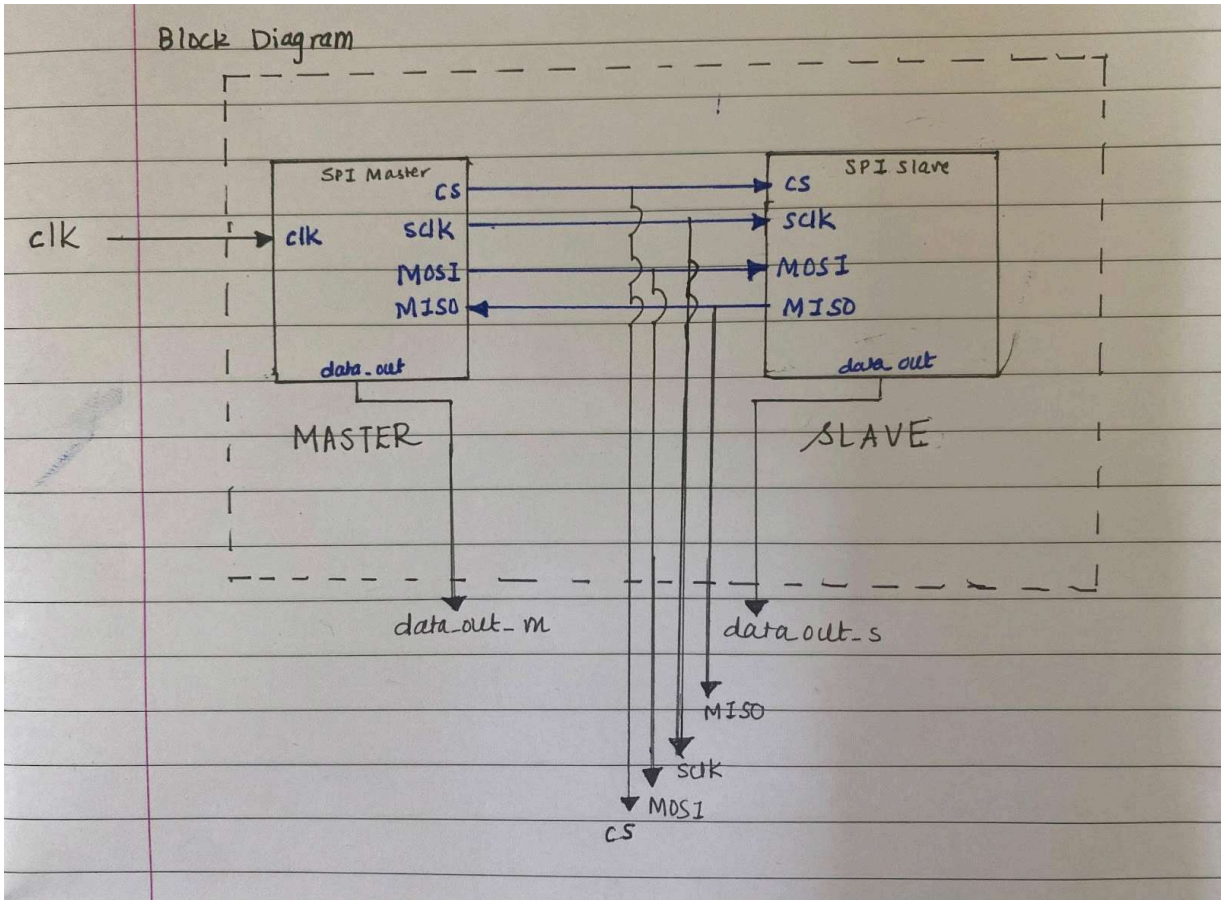
Implementation of SPI

VHDL Code Development for SPI Master and SPI Slave

Understanding SPI

Block Diagram



Detailed Explanation

Port:

Master

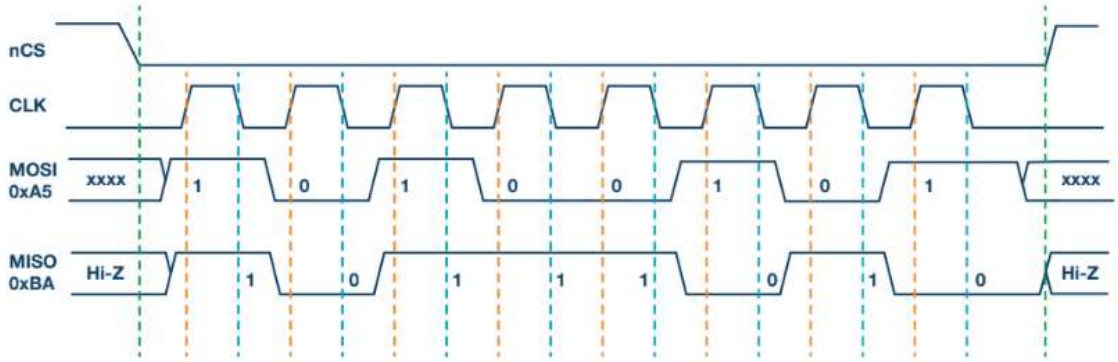
PORT	DIRECTION	DESCRIPTION
clk	Input	The clock signal generated by the master to synchronize data transmission.
miso	Input	Bit which stores the value to be shifted from slave to master.
cs	Output	Chip select signal to enable/disable communication with the slave.
mosi	Output	Bit which stores the value to be shifted from master to slave.
sclk	Output	Serial clock signal output to synchronize the slave device.
data_out	Output	3-bit vector to store the data received from the slave via miso.

Slave

PORT	DIRECTION	DESCRIPTION
sclk	Input	Serial clock input from the master, used to synchronize data transmission.
mosi	Input	Bit which stores the value to be shifted from master to slave.
cs	Input	Chip select signal to enable/disable communication with the slave.
miso	Output	Bit which stores the value to be shifted from slave to master.
data_out	Output	3-bit vector to store the data received from the master via mosi.

Mode:

Mode 0



Clock Polarity (CPOL) = 0: The clock signal (SCLK) is low when idle. This means that when the SPI communication is not happening, the clock remains in a low state.

Clock Phase (CPHA) = 0: Data is sampled on the rising edge of the clock signal and shifted out on the falling edge.

Timing Diagram for Mode 0

- Clock Idle State: Low
- Data Sampling: On the rising edge of the clock.
- Data Shifting: On the falling edge of the clock.

Data Transmission:

Master

- The master generates the clock (SCLK) and controls data transfer using the chip select (CS) signal.
- Data is transmitted through the MOSI line on the clock's falling edge, with counters controlling the transmission of a 3-bit data frame from a predefined data vector.
- Simultaneously, the master receives data from the slave via the MISO line, sampling on the rising edge of the clock and storing it in a 3-bit output vector.

Slave

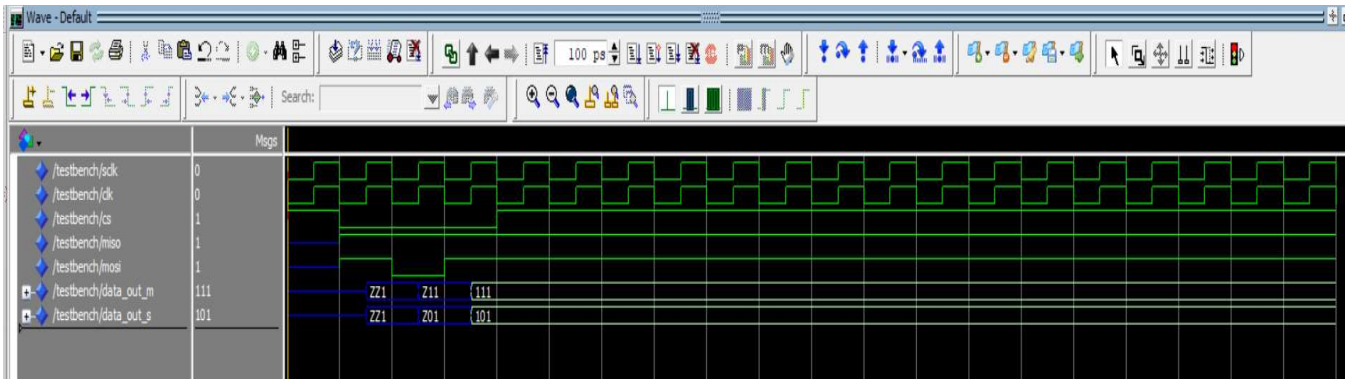
- Data is received from the MOSI line on the rising edge of the clock and stored in a 3-bit output vector, while data is transmitted through the MISO line on the falling edge of the clock.
- Counters control the shifting and sampling of data, ensuring synchronized transmission and reception of a 3-bit data frame.

Top Level

- The top-level module instantiates the master and slave components, connecting them through shared signals.

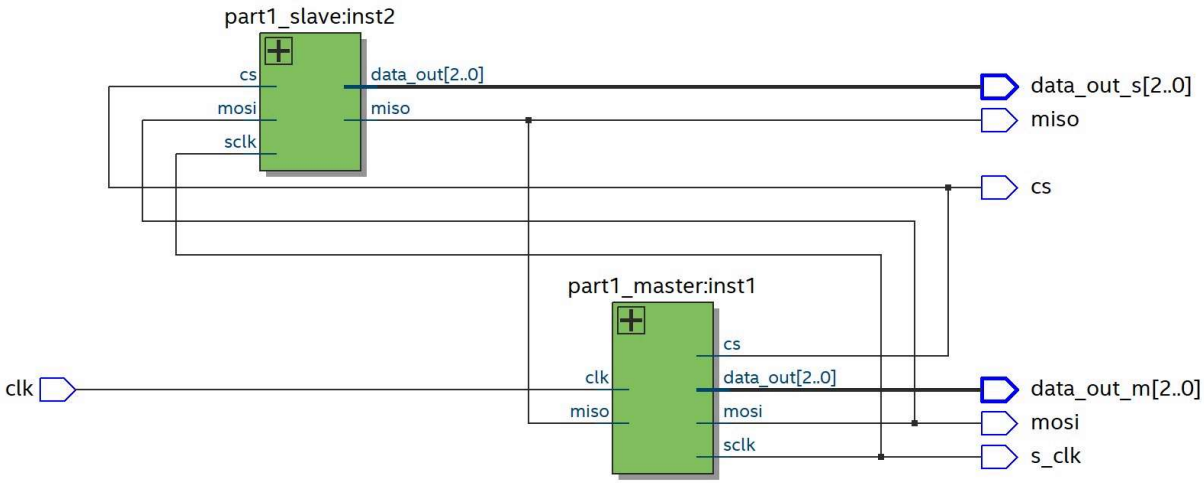
Results

Waveform:

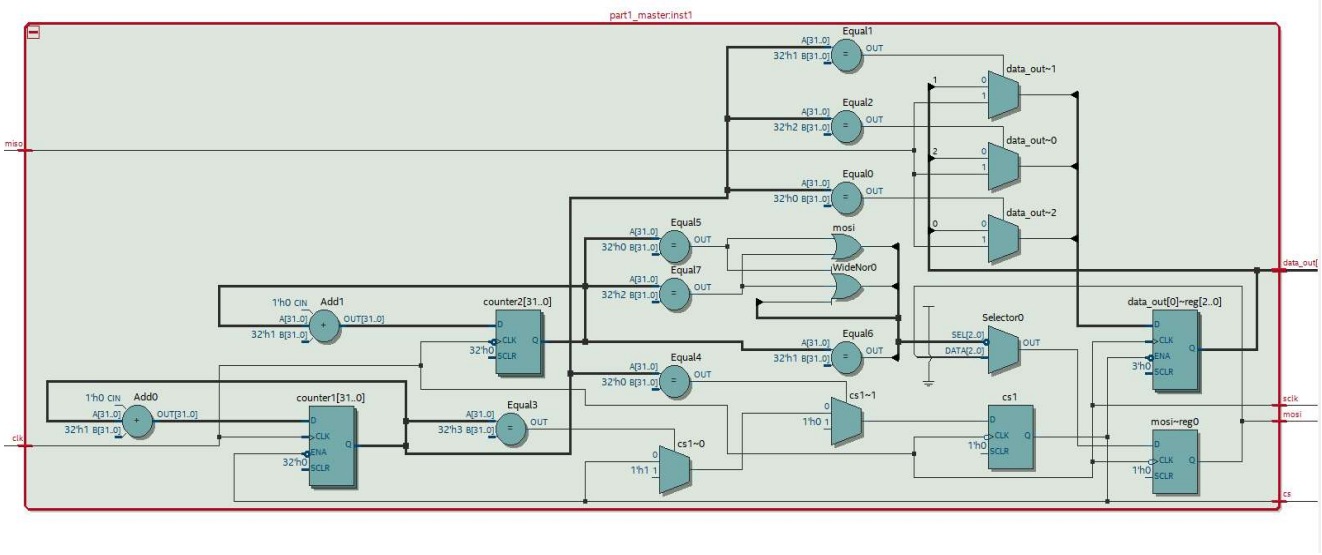


Netlist Viewer:

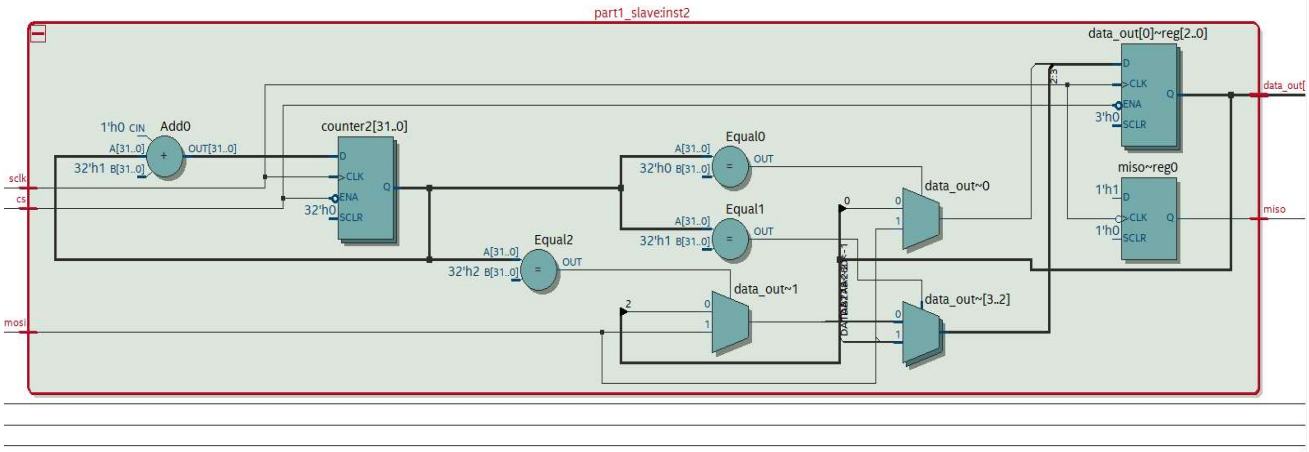
Toplevel



Master



Slave



Key Observations

- The **clk** and **sclk** signals are identical in this setup.
- The **cs** signal stays active low (set to '0') during the data transfer.
- **data_out_m** and **data_out_s** show the respective outputs for master and slave, indicating correct data exchange. The master is sending "101", while the slave is sending "111".

Work Distribution

- Saniya: Worked on the slave code.
- Foram: Worked on the master code.
- The testbench and top-level were made together and we both did debugging. The report was also made together.