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SPI to DAC and Multimeter

Digital-to-Analog Conversion and Verification via SPI Interface with DAC and Multimeter

Explanation:

1) **Retrieving the Digital Value**:

- The 10-bit digital value, stored in register reg_a on the FPGA, represents the sampled analog input voltage initially processed by the ADC (Analog-to-Digital Converter) in Task 2(a).
- This value serves as the input to the DAC, which will convert it back into an analog signal.

2) **Configuring the SPI Master for DAC Communication**:

- The SPI protocol is utilized to transfer the digital data from the FPGA to the DAC, ensuring precise and synchronized data transmission.
- The CS(Chip Select) signal is initially set low to begin the communication sequence. The SPI master then transmits the 10-bit digital value stored in reg a over the MOSI (Master Out Slave In) line, while the SCLK (Serial Clock) signal controls the timing of each bit sent to the DAC.
- The DAC operates in SPI Mode 0, as specified, ensuring compatibility with the SPI master setup and correct timing synchronization.

3) **Digital-to-Analog Conversion in the DAC**:

- The DAC receives the digital value from the FPGA and converts it into a proportional analog voltage output.
- A reference voltage (Vref) of 3.3V is applied to the DAC, allowing it to accurately scale the digital-to-analog conversion so that the output voltage corresponds to the original analog input.

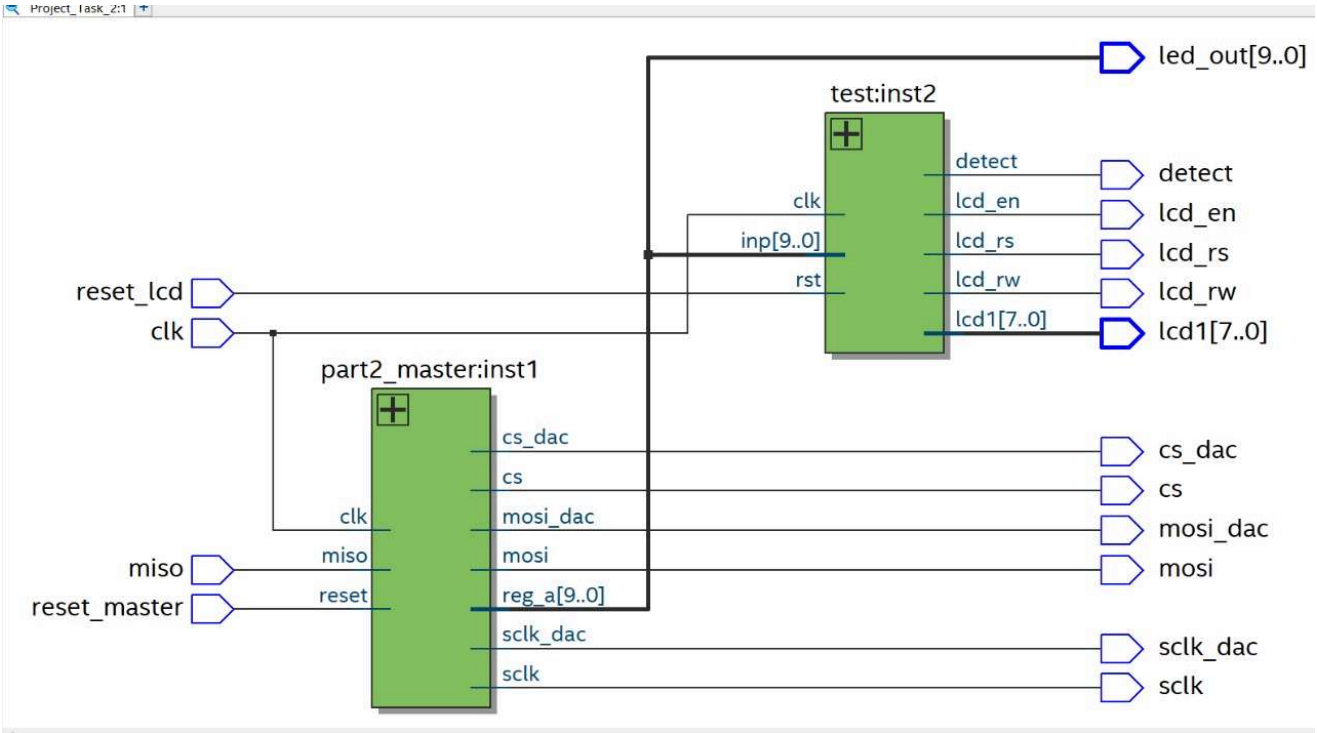
4) **Verification Using Multimeter**:

- The DAC's analog output is measured using a multimeter to verify that it matches the initial input voltage provided to the ADC.
- This measurement confirms that the entire SPI communication path—from ADC to FPGA to DAC—accurately retained the signal's integrity, converting it back to its original analog form.

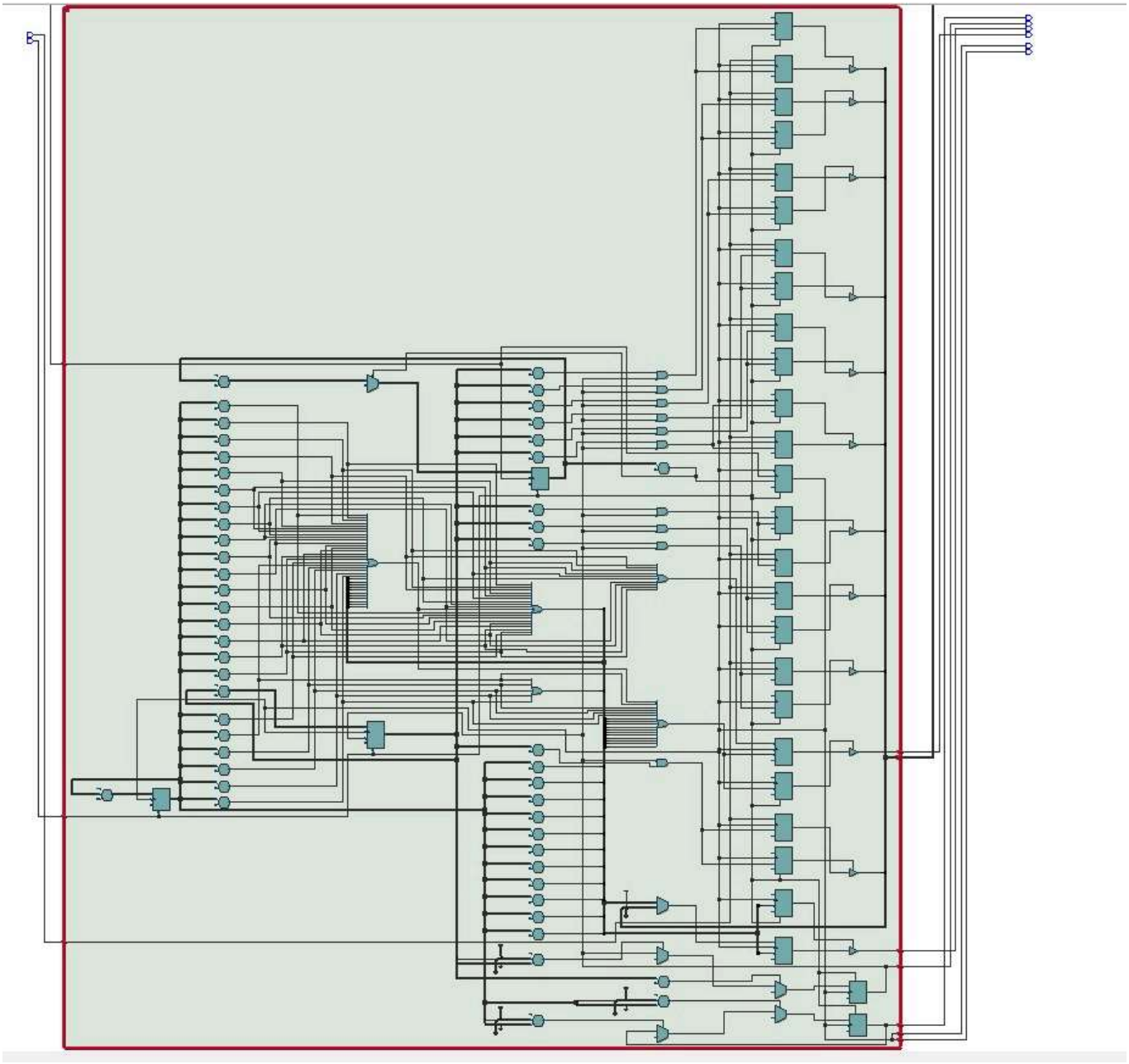
5) **Implementation in VHDL**:

- The SPI master code is modified to support data transmission specifically for the DAC interface, including setting up appropriate clock and CS signals for the DAC's requirements.
- Separate reset signals are configured for the DAC to ensure reliable operation without interference from other modules in the system.

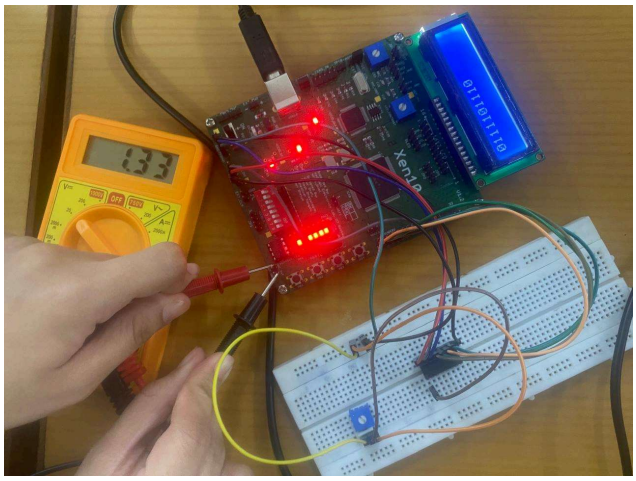
Overall Netlist:

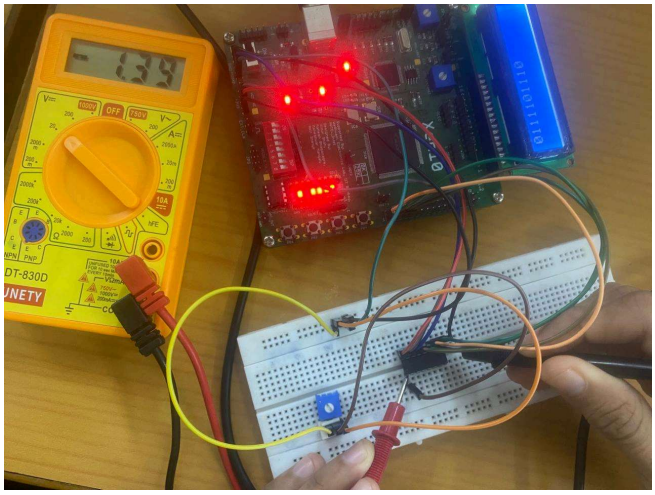


Master Netlist:



Pictures of the board showing the same voltage (measured using the DMM) across the DAC and ADC:





Work Distribution:

Both of us worked on the code together and made the report together.