1. What is pipelining in computer architecture? A) A technique to increase clock speed B) A technique to increase throughput C) A technique to reduce power consumption D) A technique to reduce latency **Answer: B**

2. Which of the following is not a stage in the classic five-stage RISC pipeline? A) Fetch B) Decode C) Execute D) Cache **Answer: D**

3. What is a hazard in pipelining? A) Bottleneck in the processor B) Situation that prevents the next instruction from executing during its designated clock cycle C) Increase in clock frequency D) All of the above **Answer: B**

4. What is data hazard? A) A situation where two instructions cannot execute simultaneously B) A situation where there is a conflict in accessing the cache C) A situation where an instruction depends on the result of a previous instruction D) A situation where there is a branch misprediction **Answer: C**

5. What technique is used to resolve data hazards by stalling the pipeline until the data is available? A) Forwarding B) Branch prediction C) Pipeline flushing D) Pipeline bubbling **Answer: D**

6. Which technique can be used to resolve data hazards by forwarding the required data directly from one pipeline stage to another? A) Branch prediction B) Pipeline bubbling C) Pipeline flushing D) Forwarding **Answer: D**

7. What is branch prediction used for in pipelining? A) To predict data hazards B) To predict control hazards C) To predict branch mispredictions D) To predict pipeline stalls **Answer: B**

8. What is meant by a pipeline stall? A) A bubble in the pipeline B) A situation where the pipeline cannot proceed due to a hazard C) A situation where there is a cache miss D) A situation where there is a branch misprediction **Answer: B**

9. Which technique allows multiple instructions to be executed simultaneously on different processing elements? A) Pipelining B) Superscalar processing C) Branch prediction D) Pipeline bubbling **Answer: B**

10. What is parallel processing? A) Executing multiple tasks simultaneously using multiple processors B) Increasing the clock speed of a single processor C) Decreasing the number of instructions executed per clock cycle D) None of the above **Answer: A**

11. What is the purpose of SIMD (Single Instruction, Multiple Data) architecture? A) To execute multiple instructions simultaneously B) To execute multiple data elements simultaneously using the same instruction C) To reduce clock speed D) To reduce power consumption **Answer: B**

12. What does MIMD (Multiple Instruction, Multiple Data) architecture involve? A) Executing multiple instructions on multiple processors B) Executing a single instruction on multiple processors C) Executing multiple instructions on a single processor D) None of the above **Answer: A**

13. Which of the following is an example of MIMD architecture? A) SIMD B) GPU (Graphics Processing Unit) C) FPGA (Field-Programmable Gate Array) D) All of the above **Answer: B**

14. What is the main advantage of pipelining in computer architecture? A) Reduced instruction set B) Increased clock speed C) Increased throughput D) Reduced power consumption **Answer: C**

15. In a pipelined processor, what is the term used for the time taken to complete a single instruction, considering all stages? A) Clock cycle B) Execution time C) Pipeline latency D) Throughput **Answer: B**

16. Which type of hazard occurs when an instruction depends on the outcome of a previous instruction that is still in the pipeline? A) Control hazard B) Data hazard C) Structural hazard D) Pipeline hazard **Answer: B**

17. Which technique is used to overcome structural hazards by allowing multiple instructions to use the same hardware concurrently? A) Loop unrolling B) Branch prediction C) Pipeline forwarding D) Hardware multithreading **Answer: D**

18. What is meant by in-order execution in pipelining? A) Executing instructions as they arrive B) Executing instructions out of sequence C) Executing instructions simultaneously D) Executing instructions in a parallel manner **Answer: A**

19. Which technique is used to predict the outcome of a conditional branch instruction before it is executed to avoid pipeline stalls? A) Data forwarding B) Loop unrolling C) Branch prediction D) Superscalar processing **Answer: C**

20. Which of the following is a hazard that cannot be resolved using forwarding or stalling techniques alone? A) Data hazard B) Control hazard C) Structural hazard D) Branch hazard **Answer: B**

21. Which of the following is NOT a phase of the classic RISC pipeline? A) Fetch B) Decode C) Execute D) Branch **Answer: D**

22. What is the purpose of pipelining in computer architecture? A) To reduce the number of clock cycles required to execute an instruction B) To increase the clock speed of the processor C) To decrease the number of instructions executed per clock cycle D) To reduce the size of the cache **Answer: A**

23. Which of the following is NOT a type of hazard in pipelining? A) Data hazard B) Control hazard C) Structural hazard D) Parallel hazard **Answer: D**

24. Which of the following is a technique used to handle data hazards by forwarding data directly from the execution stage to the instruction requiring it? A) Branch prediction B) Loop unrolling C) Data forwarding D) Superscalar processing **Answer: C**

25. Which technique is used to resolve hazards by introducing no-operation instructions (bubbles) into the pipeline? A) Branch prediction B) Loop unrolling C) Pipeline forwarding D) Pipeline bubbling **Answer: D**

26. Which of the following is a limitation of pipelining? A) Increased throughput B) Increased latency C) Reduced clock speed D) None of the above **Answer: B**

27. What is the primary advantage of parallel processing? A) Reduced power consumption B) Increased clock speed C) Increased throughput D) Reduced latency **Answer: C**

28. Which of the following is NOT a type of parallel processing architecture? A) SIMD B) SISD C) MIMD D) SPMD **Answer: B**

29. What is the goal of superscalar processing? A) To execute multiple instructions simultaneously on different processors B) To execute multiple instructions simultaneously on the same processor C) To reduce clock speed D) To reduce the number of instructions executed per clock cycle **Answer: B**

30. Which of the following is an example of SIMD architecture? A) CPU (Central Processing Unit) B) GPU (Graphics Processing Unit) C) FPGA (Field-Programmable Gate Array) D) None of the above **Answer: B**

31. Which of the following architectures supports multiple processors executing different instructions? A) SIMD B) MIMD C) SISD D) SPMD **Answer: B**

32. What does SPMD (Single Program, Multiple Data) architecture involve? A) Executing multiple programs on multiple processors B) Executing a single program on multiple processors C) Executing multiple data elements using the same program D) Executing a single program using the same data elements **Answer: B**

33. Which of the following is a challenge of parallel processing? A) Increased throughput B) Increased latency C) Reduced power consumption D) Increased clock speed **Answer: B**

34. Which of the following is a characteristic of pipelining? A) Reduced throughput B) Increased latency C) Reduced clock speed D) Reduced power consumption **Answer: B**

35. What is the main goal of hardware multithreading? A) To execute multiple threads on the same processor simultaneously B) To execute a single thread on multiple processors C) To execute a single instruction on multiple processors D) To execute multiple instructions simultaneously on different processors **Answer: A**

36. Which of the following is NOT an advantage of pipelining? A) Increased clock speed B) Increased throughput C) Reduced latency D) Reduced power consumption **Answer: A**

37. Which of the following techniques can help reduce pipeline stalls due to branch mispredictions? A) Data forwarding B) Loop unrolling C) Branch prediction D) Superscalar processing **Answer: C**

38. Which of the following is a limitation of superscalar processing? A) Reduced throughput B) Increased clock speed C) Increased power consumption D) Reduced latency **Answer: C**

39. What is loop unrolling? A) A technique to increase the clock speed of the processor B) A technique to execute loop iterations in parallel C) A technique to predict branch outcomes D) A technique to reduce the number of instructions executed per clock cycle **Answer: B**

40. Which of the following is an advantage of SIMD architecture? A) Increased clock speed B) Reduced power consumption C) Increased throughput D) Reduced latency **Answer: C**

41. What is the primary advantage of MIMD architecture? A) Increased clock speed B) Reduced power consumption C) Increased throughput D) Reduced latency **Answer: C**

42. What is the purpose of hardware multithreading in pipelining? A) To reduce clock speed B) To increase latency C) To reduce pipeline stalls D) To reduce power consumption **Answer: C**

43. Which of the following is NOT a type of hazard in pipelining? A) Data hazard B) Control hazard C) Pipeline hazard D) Loop hazard **Answer: D**

44. Which of the following is NOT a technique to handle hazards in pipelining? A) Data forwarding B) Branch prediction C) Pipeline flushing D) Clock throttling **Answer: D**

45. What is the purpose of instruction reordering in pipelining? A) To execute instructions out of sequence B) To reduce pipeline stalls C) To increase clock speed D) To increase latency **Answer: B**

46. Which of the following is an example of SISD architecture? A) SIMD B) MIMD C) Von Neumann architecture D) SPMD **Answer: C**

47. Which of the following architectures is used extensively in modern graphics processing? A) SIMD B) SISD C) MIMD D) SPMD **Answer: A**

48. What is the primary limitation of SISD architecture? A) Reduced throughput B) Increased power consumption C) Increased latency D) Limited parallelism **Answer: D**

49. Which of the following architectures is used in scientific computing and simulations? A) SIMD B) SISD C) MIMD D) SPMD **Answer: C**

50. Which of the following architectures is used in parallel programming paradigms like OpenMP? A) SIMD B) SISD C) MIMD D) SPMD **Answer: D**

1. What does I/O stand for in computer architecture? A) Input-Output B) Internal Organization C) Interconnected Operations D) Interrupted Operations **Answer: A**

2. Which of the following is NOT a component of I/O interface? A) Buffer B) Registers C) Control Unit D) CPU **Answer: D**

3. What is the purpose of the I/O interface in a computer system? A) To connect the CPU to the memory B) To connect the CPU to the I/O devices C) To connect the I/O devices to the memory D) To connect the memory to the cache **Answer: B**

4. Which of the following is NOT a mode of data transfer in I/O? A) Programmed I/O B) Interrupt-driven I/O C) Direct Memory Access (DMA) D) Interleaved I/O **Answer: D**

5. What is asynchronous data transfer in I/O? A) Data transfer that occurs simultaneously with CPU operations B) Data transfer that occurs without synchronization with CPU operations C) Data transfer that occurs only when CPU is idle D) Data transfer that occurs at fixed intervals **Answer: B**

6. Which of the following modes of transfer requires the CPU to continuously check the status of the I/O device? A) Programmed I/O B) Interrupt-driven I/O C) DMA transfer D) Synchronous I/O **Answer: A**

7. What is Direct Memory Access (DMA) in computer architecture? A) A technique to access the CPU registers directly B) A technique to access the memory without CPU intervention C) A technique to access the cache memory directly D) A technique to access I/O devices without interrupting the CPU **Answer: D**

8. Which of the following is NOT a benefit of using DMA for data transfer? A) Reduced CPU overhead B) Faster data transfer rates C) Simpler system design D) Reduced memory access latency **Answer: C**

9. What is a DMA controller in computer architecture? A) A device used to control the CPU operations B) A device used to control the memory operations C) A device used to control the I/O operations D) A device used to control the cache operations **Answer: C**

10. Which of the following is a function of a DMA controller? A) Managing CPU registers B) Managing cache memory C) Managing interrupts D) Managing data transfer between memory and I/O devices **Answer: D**

11. In DMA transfer, when does the DMA controller gain control of the system bus? A) After the CPU finishes its execution B) Before the CPU starts its execution C) During the CPU execution D) Only during system initialization **Answer: B**

12. What is the primary advantage of using DMA transfer over programmed I/O? A) Reduced CPU utilization B) Increased CPU speed C) Reduced memory latency D) Increased memory capacity **Answer: A**

13. What is the purpose of the Input-Output Processor (IOP) in a computer system? A) To manage CPU operations B) To manage memory operations C) To manage I/O operations D) To manage cache operations **Answer: C**

14. Which of the following is NOT a role of the IOP? A) Communication with I/O devices B) Buffering data C) Executing application programs D) Error handling **Answer: C**

15. What is the communication interface between the CPU and the IOP called? A) I/O channel B) Data bus C) Control bus D) Address bus **Answer: A**

16. Which of the following is NOT a method of CPU-IOP communication? A) Memory-mapped I/O B) Direct I/O C) Programmed I/O D) Interrupt-driven I/O **Answer: D**

17. What is memory-mapped I/O? A) A method of accessing I/O devices using dedicated I/O instructions B) A method of accessing I/O devices using memory addresses C) A method of accessing memory using I/O instructions D) A method of accessing memory using memory addresses **Answer: B**

18. Which of the following statements about memory-mapped I/O is true? A) It requires a separate address space for I/O devices. B) It uses dedicated I/O instructions to access I/O devices. C) It allows I/O devices to be treated as memory locations. D) It requires a separate memory bus for I/O operations. **Answer: C**

19. What is programmed I/O in computer architecture? A) A method of I/O transfer where the CPU continuously checks the status of the I/O device B) A method of I/O transfer where the CPU transfers data directly between memory and I/O devices C) A method of I/O transfer where the CPU uses interrupts to transfer data between memory and I/O devices D) A method of I/O transfer where the CPU uses dedicated I/O instructions to transfer data between memory and I/O devices **Answer: D**

20. Which of the following modes of transfer allows the CPU to transfer data between memory and I/O devices using special I/O instructions? A) Programmed I/O B) Interrupt-driven I/O C) DMA transfer D) Memory-mapped I/O **Answer: A**

21. What is the primary disadvantage of programmed I/O? A) Increased CPU utilization B) Reduced memory access latency C) Limited throughput D) Increased system complexity **Answer: A**

22. Which of the following methods of transfer is characterized by the use of interrupts to signal the CPU when data transfer is complete? A) Programmed I/O B) Interrupt-driven I/O C) DMA transfer D) Memory-mapped I/O **Answer: B**

23. In interrupt-driven I/O, what triggers the interrupt request from an I/O device? A) Data transfer completion B) Data transfer initiation C) CPU request D) I/O device request **Answer: A**

24. Which of the following is NOT a step involved in handling an interrupt in the CPU? A) Acknowledgment B) Response C) Data transfer D) Return from interrupt **Answer: C**

25. What is the purpose of the interrupt vector table in the CPU? A) To store data transferred between memory and I/O devices B) To manage interrupts generated by I/O devices C) To manage data transfer rates D) To execute application programs **Answer: B**

26. What is a disadvantage of interrupt-driven I/O compared to DMA transfer? A) Increased CPU utilization B) Slower data transfer rates C) Higher memory access latency D) Increased system complexity **Answer: A**

27. Which of the following is a role of the DMA controller in a computer system? A) Managing CPU operations B) Managing memory operations C) Managing I/O operations D) Managing cache operations **Answer: C**

28. In DMA transfer, what role does the DMA controller play during data transfer? A) It acts as an intermediary between the CPU and the I/O device. B) It manages the I/O device

operations independently of the CPU. C) It acts as a buffer between the memory and the CPU. D) It manages the CPU operations during data transfer. **Answer: B**

29. Which of the following statements is true about DMA transfer? A) DMA requires continuous CPU intervention during data transfer. B) DMA uses special I/O instructions for data transfer. C) DMA allows the CPU to initiate data transfer between memory and I/O devices. D) DMA reduces CPU overhead during data transfer. **Answer: D**

30. What is the purpose of the IOP in a computer system? A) To manage CPU operations B) To manage memory operations C) To manage I/O operations D) To manage cache operations **Answer: C**

31. Which of the following functions is typically performed by the IOP? A) Processing arithmetic operations B) Managing CPU registers C) Controlling data transfer between CPU and memory D) Managing data transfer between CPU and I/O devices **Answer: D**

32. What is the role of the I/O channel in CPU-IOP communication? A) To manage interrupts B) To provide a communication interface between CPU and IOP C) To manage memory operations D) To execute application programs **Answer: B**

33. What is the main purpose of the data bus in CPU-IOP communication? A) To transfer data between CPU and memory B) To transfer data between CPU and I/O devices C) To manage interrupts D) To execute application programs **Answer: B**

34. Which of the following methods of CPU-IOP communication allows the I/O devices to be accessed using memory-like commands? A) Memory-mapped I/O B) Programmed I/O C) Interrupt-driven I/O D) Direct I/O **Answer: A**

35. What is the role of the control bus in CPU-IOP communication? A) To transfer data between CPU and memory B) To transfer control signals between CPU and I/O devices C) To manage interrupts D) To execute application programs **Answer: B**

36. Which of the following statements is true about programmed I/O? A) Programmed I/O uses interrupts to transfer data between CPU and I/O devices. B) Programmed I/O requires continuous polling of the I/O device status by the CPU. C) Programmed I/O uses DMA for data transfer. D) Programmed I/O allows the CPU to directly access I/O device registers. **Answer: B**

37. What is a characteristic of DMA transfer compared to programmed I/O? A) DMA transfer requires continuous CPU intervention. B) DMA transfer uses interrupts for data transfer. C) DMA transfer reduces CPU overhead. D) DMA transfer is slower than programmed I/O. **Answer: C**

38. Which of the following is a function of the DMA controller during data transfer? A) Monitoring CPU operations B) Managing memory operations C) Managing I/O operations D) Managing cache operations **Answer: C**

39. Which method of transfer is more efficient in terms of CPU utilization: DMA or programmed I/O? A) DMA B) Programmed I/O C) Both have similar CPU utilization D) Neither affects CPU utilization **Answer: A**

40. What is the role of interrupts in CPU-IOP communication? A) To manage data transfer between CPU and memory B) To manage data transfer between CPU and I/O devices C) To manage control signals between CPU and I/O devices D) To execute application programs **Answer: C**

41. Which of the following methods allows the CPU to transfer data directly between memory and I/O devices without intermediate data buffering? A) Memory-mapped I/O B) Programmed I/O C) Interrupt-driven I/O D) Direct I/O **Answer: D**

42. What is the primary advantage of interrupt-driven I/O compared to programmed I/O? A) Reduced CPU utilization B) Faster data transfer rates C) Simpler system design D) Increased memory capacity **Answer: A**

43. Which of the following is a role of the DMA controller in CPU-IOP communication? A) To manage CPU operations B) To manage memory operations C) To manage I/O operations D) To manage cache operations **Answer: C**

44. Which of the following statements is true about DMA transfer? A) DMA requires continuous CPU intervention during data transfer. B) DMA uses interrupts for data transfer between memory and I/O devices. C) DMA reduces CPU overhead during data transfer. D) DMA requires special I/O instructions for data transfer. **Answer: C**

45. What is the primary disadvantage of programmed I/O? A) Increased CPU utilization B) Reduced memory access latency C) Limited throughput D) Increased system complexity **Answer: A**

46. Which of the following methods of data transfer allows the CPU to perform other tasks while data transfer is ongoing? A) Programmed I/O B) Interrupt-driven I/O C) Direct Memory Access (DMA) D) Memory-mapped I/O **Answer: C**

47. What is the primary role of the DMA controller in DMA transfer? A) To manage CPU operations B) To manage memory operations C) To manage I/O operations D) To manage cache operations **Answer: C**

48. Which of the following is a disadvantage of interrupt-driven I/O compared to DMA transfer? A) Slower data transfer rates B) Increased CPU utilization C) Higher memory access latency D) Reduced system complexity **Answer: B**

49. Which method of data transfer requires the CPU to continuously check the status of the I/O device? A) Programmed I/O B) Interrupt-driven I/O C) DMA transfer D) Memory-mapped I/O **Answer: A**

50. What is the primary benefit of using DMA transfer for data transfer between memory and I/O devices? A) Increased CPU utilization B) Reduced memory access latency C) Simpler system design D) Reduced CPU overhead **Answer: D**

1. What is the purpose of memory hierarchy in computer systems? A) To organize data in memory B) To improve memory access speed and cost efficiency C) To manage input-output operations D) To control CPU operations **Answer: B**

2. Which of the following is NOT a level of the memory hierarchy? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: D**

3. Which memory level in the hierarchy is the closest to the CPU and has the fastest access time? A) Secondary memory B) Cache memory C) Main memory D) Tertiary memory **Answer: B**

4. What is the purpose of cache memory in the memory hierarchy? A) To provide large storage capacity B) To store frequently accessed data for fast retrieval C) To store permanent data D) To manage virtual memory **Answer: B**

5. Which of the following is a characteristic of cache memory? A) It is volatile B) It is slower than secondary memory C) It is directly accessed by the CPU D) It has larger storage capacity than main memory **Answer: C**

6. What is the main disadvantage of using cache memory in the memory hierarchy? A) High cost per unit of storage B) Slower access time compared to main memory C) Limited storage capacity D) Volatility of data **Answer: A**

7. Which memory level in the hierarchy provides non-volatile storage for long-term data retention? A) Cache memory B) Main memory C) Secondary memory D) Register memory **Answer: C**

8. What is the purpose of main memory (RAM) in the memory hierarchy? A) To store instructions for the CPU B) To store frequently accessed data for fast retrieval C) To provide permanent storage for the operating system D) To hold data and instructions currently being processed by the CPU **Answer: D**

9. Which of the following is NOT a type of main memory technology? A) DRAM (Dynamic RAM) B) SRAM (Static RAM) C) ROM (Read-Only Memory) D) SSD (Solid State Drive) **Answer: D**

10. Which memory technology is commonly used for cache memory due to its faster access times? A) DRAM B) SRAM C) ROM D) SSD **Answer: B**

11. Which of the following is a characteristic of ROM (Read-Only Memory)? A) Volatile storage B) Can be written to multiple times C) Retains data even when powered off D) Typically used for temporary data storage **Answer: C**

12. Which memory level in the hierarchy has the largest storage capacity but the slowest access time? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: C**

13. Which of the following is an example of secondary memory? A) Cache memory B) RAM (Random Access Memory) C) HDD (Hard Disk Drive) D) CPU cache **Answer: C**

14. What is the purpose of virtual memory in memory organization? A) To increase the physical size of main memory B) To provide additional cache memory C) To manage input-output operations D) To extend the address space of main memory onto secondary storage **Answer: D**

15. Which memory technology is used for tertiary memory in the memory hierarchy? A) Magnetic tape B) SSD (Solid State Drive) C) Optical disk D) SRAM (Static RAM) **Answer: A**

16. Which of the following is NOT a characteristic of associative memory? A) Allows parallel comparison of multiple memory locations B) Provides fast access to data C) Requires linear search for data retrieval D) Used for cache memory **Answer: C**

17. What is associative memory in the context of memory organization? A) A type of main memory technology B) A memory hierarchy level C) A memory access method based on content rather than address D) A type of secondary memory **Answer: C**

18. Which memory technology is commonly used for storing firmware and system BIOS? A) DRAM B) SRAM C) ROM D) SSD **Answer: C**

19. Which of the following is NOT a benefit of using cache memory in the memory hierarchy? A) Faster access times B) Reduced CPU idle time C) Increased overall system performance D) Larger storage capacity **Answer: D**

20. Which memory level in the hierarchy is directly accessed by the CPU for data processing? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: B**

21. Which of the following is a characteristic of cache memory placement? A) It is managed by the operating system B) It is typically smaller in size than main memory C) It has slower access times compared to secondary memory D) It is used for long-term data storage **Answer: B**

22. Which memory technology is commonly used for persistent storage in mobile devices and laptops? A) DRAM B) SRAM C) ROM D) SSD **Answer: D**

23. What is the purpose of the memory management unit (MMU) in memory organization? A) To manage memory allocation to different processes B) To manage CPU cache operations C) To manage virtual memory mapping D) To manage I/O device access **Answer: C**

24. Which of the following is a characteristic of associative memory searching? A) Linear search based on address B) Parallel search based on content C) Sequential search based on cache hierarchy D) Hierarchical search based on cache size **Answer: B**

25. Which memory hierarchy level is often used for storing backup data and archives? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: C**

26. Which memory technology provides the fastest access times but is volatile? A) DRAM B) SRAM C) ROM D) SSD **Answer: B**

27. What is the purpose of the translation lookaside buffer (TLB) in memory organization? A) To store recently accessed cache lines B) To cache virtual-to-physical address translations C) To manage CPU cache coherence D) To control memory refresh cycles **Answer: B**

28. Which of the following memory technologies is NOT typically used in the memory hierarchy? A) Magnetic tape B) Optical disk C) SSD D) DRAM **Answer: A**

29. What is the primary function of secondary memory in memory organization? A) To provide high-speed storage for frequently accessed data B) To act as a buffer between cache memory and main memory C) To provide non-volatile storage for long-term data retention D) To manage CPU cache operations **Answer: C**

30. Which of the following is a benefit of using SSDs over traditional HDDs in secondary memory? A) Slower access times B) Higher storage capacity C) Lower power consumption D) Volatility of data **Answer: C**

31. What is the purpose of the memory hierarchy principle in computer architecture? A) To increase memory volatility B) To reduce memory access latency C) To eliminate the need for memory management D) To increase CPU speed **Answer: B**

32. Which memory technology is commonly used for storing the operating system kernel and device drivers? A) DRAM B) SRAM C) ROM D) SSD **Answer: C**

33. What is the purpose of block transfer in cache memory management? A) To improve cache hit rates B) To reduce cache access latency C) To manage cache replacement policies D) To synchronize cache coherence **Answer: B**

34. Which of the following is a characteristic of volatile memory? A) Retains data even when powered off B) Slower access times compared to non-volatile memory C) Typically used for long-term data storage D) Requires continuous power to retain data **Answer: D**

35. Which memory level in the hierarchy is directly accessible by the operating system for memory management? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: B**

36. Which memory technology is commonly used for storing BIOS settings and configurations? A) DRAM B) SRAM C) ROM D) SSD **Answer: C**

37. What is the purpose of prefetching in cache memory management? A) To load frequently accessed data into cache B) To flush cache contents to main memory C) To manage cache replacement policies D) To synchronize cache coherence **Answer: A**

38. Which of the following is NOT a characteristic of ROM (Read-Only Memory)? A) Volatile storage B) Non-volatile storage C) Retains data when powered off D) Used for firmware and system software **Answer: A**

39. Which memory level in the hierarchy has the smallest storage capacity but the fastest access time? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: A**

40. What is the purpose of wear leveling in SSDs? A) To improve access times B) To reduce power consumption C) To extend the lifespan of the SSD D) To synchronize memory operations **Answer: C**

41. Which memory technology is commonly used for storing video game consoles' firmware? A) DRAM B) SRAM C) ROM D) SSD **Answer: C**

42. What is the purpose of address mapping in memory organization? A) To manage CPU cache operations B) To control memory refresh cycles C) To translate virtual addresses to physical addresses D) To provide non-volatile storage **Answer: C**

43. Which memory level in the hierarchy is used for storing large datasets and user files? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: C**

44. What is the purpose of page tables in memory management? A) To manage cache replacement policies B) To map virtual addresses to physical addresses C) To synchronize memory operations D) To improve memory access latency **Answer: B**

45. Which of the following is a characteristic of SSDs compared to HDDs? A) Slower access times B) Mechanical moving parts C) Lower power consumption D) Larger storage capacity **Answer: C**

46. What is the purpose of memory interleaving in memory organization? A) To manage cache replacement policies B) To synchronize memory operations C) To improve memory access bandwidth D) To extend the lifespan of memory modules **Answer: C**

47. Which memory technology is commonly used for high-speed buffer storage in database systems? A) DRAM B) SRAM C) ROM D) SSD **Answer: B**

48. What is the purpose of dirty bit management in memory organization? A) To manage cache replacement policies B) To synchronize memory operations C) To track modified data in cache D) To extend the lifespan of memory modules **Answer: C**

49. Which memory level in the hierarchy is used for storing data backups and archives? A) Cache memory B) Main memory C) Secondary memory D) Tertiary memory **Answer: C**

50. What is the purpose of memory segmentation in memory management? A) To manage cache replacement policies B) To translate virtual addresses to physical addresses C) To synchronize memory operations D) To improve memory access bandwidth **Answer: B**