

## SCHOOL OF COMPUTING

CIA – III Exam: Nov 2024

**Course Code: CSE320** 

Course Name: Compiler Design
Duration: 90minutes Max. Marks: 50

#### PART A

#### **ANSWER ALL THE QUESTIONS**

10 MARKS

- 1. What do you understand from the code generated by a Cross Compiler. (2)
- 2. Give the structure of an activation record. (2)
- When does dangling reference occur? (2)
- 4. Discuss the properties of an optimizing compilers. (2)
- 5. For the given expression, write the TAC statements and build DAG for the sequence. d=(a-b) + (a-c) + (a-c). (2)

### **PART B**

### **ANSWER ALL THE QUESTIONS**

25 MARKS

6. (a) Construct CLR Parsing table for the following grammar and parse the input string "abde".

 $A \rightarrow aB \mid Ad$ 

 $B \rightarrow bBC \mid d$ 

$$C \rightarrow e$$
 (10)

OR

- (b) Show how the minimized DFA is obtained directly from an augmented regular expression  $r=(0|1) \ 0^* \ (0|1)$  (10)
- 7. (a) Write the Syntax directed translation scheme to generate the TAC statement for flow of control statements in C++. Illustrate your SDT with the following snippet of code

- (b) (i) Elaborate the issues in the design of code generator.
  - (ii) Write short notes on register allocation and register assignment during code generation phase. (5)
- 8.(a) Explain in detail the various transformations used in peephole optimization to improve the efficiency of target code. (5)

#### OR

(b) Describe the various Storage allocation strategies used to manage the Run-time memory allocated for the program. (5)

#### PART C

### **ANSWER ALL THE QUESTION**

15 MARKS

(3)

(5)

9. Examine the sequence of Three Address Code statements given below and perform the following tasks.

(1)	i	:= m-1	(16)	t <sub>7</sub> := 4*i
(2)	j	:= n	(17)	t <sub>8</sub> := 4*j
(3)	tı	:= 4*n	(18)	t <sub>9</sub> := a[t <sub>8</sub> ]
(4)	v	:= a[t <sub>1</sub> ]	(19)	a[t <sub>7</sub> ] := t <sub>9</sub>
(5)	i	:= i+1	(20)	t <sub>10</sub> := 4*j
(6)	t <sub>2</sub>	:= 4*i	(21)	$a[t_{10}] := x$
(7)	t <sub>3</sub>	= a[t <sub>2</sub> ]	(22)	goto (5)
(8)	if	t <sub>3</sub> < v goto (5)	(23)	t <sub>11</sub> := 4*i
(9)	j :	= j-1	(24)	$x := a[t_{11}]$
(10)	t4 :	= 4*j	(25)	t <sub>12</sub> := 4*i
(11)	t <sub>5</sub> :	= a[t <sub>4</sub> ]	(26)	t <sub>13</sub> := 4*n
(12)	if	t <sub>5</sub> > v goto (9)	(27)	$t_{14} := a[t_{13}]$
(13)	if	i >= j goto (23)	(28)	a[t <sub>12</sub> ] := t <sub>14</sub>
(14)		= 4*i	(29)	t <sub>15</sub> := 4*n
(15)	45	= a[t <sub>6</sub> ]	(30)	a[t <sub>15</sub> ] := x

- (a) The Basic blocks of Instructions.
- (b) Construct a flowgraph, specify the loops. (3)
- (c) For each variable, record its next-use and liveliness at the end of each basic block. (3)
- (d) Apply the code improving transformations wherever possible and generate the optimized TAC sequence. (6)



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CO – RBT

## **PART A**

## **ANSWER ALL THE QUESTIONS**

## **10 MARKS**

No	QUESTION	CO	RBT
1	What do you understand from the code generated by a	CO2	L2
	Cross Compiler.		
2	Give the structure of an activation record.	CO4	L1
3	When does dangling reference occur?	CO3	L2
4	Discuss the properties of an optimizing compilers.	CO5	L2
5	For the given expression, write the TAC statements and	CO4	L2
	build DAG for the sequence. $d=(a-b) + (a-c) + (a-c)$ .	CO5	

## **PART B**

## **ANSWER ALL THE QUESTIONS**

## 25 MARKS

No	QUESTION	CO	RBT
6.a	Construct CLR Parsing table for the following grammar		L3
	and parse the input string "abde".		
	A <del>-&gt;</del> aB   Ad		
	B → bBC   d		
	$C \rightarrow e$ (10)		
	OR		
6.b	Show how the minimized DFA is obtained directly from	CO1	L3
	an augmented regular expression $r=(0 1) 0* (0 1).(10)$		
7.a	Write the Syntax directed translation scheme to	CO4	L3
	generate the TAC statement for flow of control		
	statements in C++. Illustrate your SDT with the		
	following snippet of code		
	res[i][j] = mergeArrays (arr1, arr2);		
	for (int i = 0; i < n1 + n2; i++)		
	<pre>printArray (res[i][i+2]); (10)</pre>		

	OR		
7.b	(i) Elaborate the issues in the design of code generator.	<b>CO6</b>	L2
	(ii) Write short notes on register allocation and register	CO6	L2
	assignment during code generation phase.		
8.a	Explain in detail the various transformations used in	CO5	L2
	peephole optimization to improve the efficiency of		
	target code. (5)		
	OR		
8.b	Describe the various Storage allocation strategies used	CO3	L2
	to manage the Run-time memory allocated for the		
	program. (5)		

## PART C

## **ANSWER ALL THE QUESTION**

## 15 MARKS

No	QUESTION		CO	RBT
9	Examine the sequence of Thre	Address Code	CO5	L3
	statements given below and perfo	rm the following	&	
		iiii tiic iollowilig	CO6	
	tasks.			
	(a) The Basic blocks of Instructions.	(3)		
	(b) Construct a flowgraph, specify the	e loops.(3)		
	(c) For each variable, record its nex	-use and		
	, ,			
	liveliness at the end of each basi	C DIOCK. (3)		
	(d) Apply the code improving tra	nsformations and		
	generate the optimized code.	(6)		
	(1) i := m-1			
	(2) $j := n$ (1)			
		8) $t_9 := a[t_8]$		
		9) a[t <sub>7</sub> ] := t <sub>9</sub>		
		0) t <sub>10</sub> := 4*j 1) a[t <sub>10</sub> ] := x		
		1) a[t <sub>10</sub> ] := x 2) goto (5)		
		3) t <sub>11</sub> := 4*i		
		4) $x := a[t_{11}]$		
		5) $t_{12} := 4*i$		
		6) t <sub>13</sub> := 4*n		
		(7) $t_{14} := a[t_{13}]$		
		(8) $a[t_{12}] := t_{14}$		
	(14) $t_6 := 4*i$ (	(9) $t_{15} := 4*n$		
	(15) $x := a[t_6]$ (	0) a[t <sub>15</sub> ] := x	1	ı



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## **PART A**

### **ANSWER ALL THE QUESTIONS**

10 MARKS

- 1. What do you understand from the code generated by a Cross Compiler.
  - The Cross compiler is a type of compiler that generates executable code for a platform different from the one on which the compiler is running.
  - This code is not directly executable on the machine where the compiler is running but is intended to run on the target system, which may have a different instruction set architecture (ISA) or operating system.
- 2. Give the structure of an activation record.

(2)

Return Values
Actual Parameters
Control Link
Access Link
Saved Machine Status
Local variables
Temporaries

3. When does dangling reference occur?

(2)

- Activation records are data structures that are used in runtime memory management to support function calls and help manage the call / control stack.
- When a function returns a pointer to a local variable, the activation record for that function is popped off the stack once the function returns. The local variable's memory is reclaimed, leaving the pointer dangling.
- 4. Discuss the criteria for an optimizing compiler.

(2)

- **Correctness**: The compiler must preserve the semantics of the original program.
- Improve the Efficiency of target Code: The optimization must produce code that executes faster, uses less memory, or optimally utilizes system resources.
- 5. For the given expression, write the TAC statements and build DAG for the sequence. d=(a-b)+(a-c)+(a-c). (2)

$$t1 = a - b$$
;  $t2 = a - c$ ;  $t3 = a - c$ ;  $t4 = t1 + t2$ ;  $t5 = t4 + t3$ ;  $d = t5$  (1mark)

Correct DAG formation (1mark)

#### **PART B**

### **ANSWER ALL THE QUESTIONS**

25 MARKS

6. (a) Construct CLR Parsing table for the following grammar and parse the input string "abde".

 $A \rightarrow aB/Ad$ 

 $B \rightarrow bBC/d$ 

 $C \rightarrow e$  (10)

Augmented Grammar	1
CLOUSRE (A' $\rightarrow$ A) & Initial Set of LR items	1
Sets of LR Items using GOTO	4
CLR Parsing Table Construction	2
CLR Parsing	2
Total Marks	10

OR

(b) Show how the minimized DFA is obtained directly from an augmented regular expression r=(0/1) 0\* (0/1) (10)

Construction of Syntax Tree	1
Firstpos, Lastpos Computation	1+1=2
Followpos Computation	2
D_tran & D_states formation	3
Minimized DFA	2
Total Marks	10

7. (a) Write the Syntax directed translation scheme to generate the TAC statement for flow of control statements in C++. Illustrate your SDT with the following snippet of code

res[i][j] = mergeArrays (arr1, arr2);

for (int i = 0; i < n1 + n2; i++) printArray (res[i][i+2]);

(10)

SDT scheme for simple if statement	2
SDT scheme for if-else statement	2
SDT scheme for while statement	2
Three Address Code Representation	4
Total Marks	10

(b) (i) Elaborate the issues in the design of code generator.	(5)
5 Design Issues – Explanation of each carries 1 mark.	

(ii) Write short notes on register allocation and register assignment during code generation phase. (5)

 G	(-,
Register Allocation – Definition, 2 techniques	2
Register Assignment – Definition, 3 techniques	3
Total Marks	5

8.(a) Explain in detail the various transformations used in peephole optimization to improve the efficiency of target code. (5)

<u> </u>	, ,
Definition of Peephole, Peephole window operations	2
5 Transformations with suitable example	
Total Marks	5

OR

(b) Describe the various Storage allocation strategies used to manage the Run-time memory allocated for the program. (5)

• • •	, ,
Static allocation; Stack allocation; Heap allocation	
Definition, advantages & disadvantages of each	
Total Marks	5

## **PART C**

## **ANSWER ALL THE QUESTION**

15 MARKS

- 9. Examine the sequence of Three Address Code statements given below and perform the following tasks.
  - (a) The Basic blocks of Instructions.

(3)

Identifying the Leaders	1
Formation of Basic Blocks	2
Total Marks	3

(1)	i	;=	m-1	(16)	t <sub>7</sub>	:=	4*i
(2)	j	:=	n	(17)	t <sub>8</sub>	:=	4*j
(3)	tı	:=	4*n	(18)			a[tx]
(4)	v	:=	a[t <sub>1</sub> ]	(19)	a[t7]		
(5)	i	:=	i+1	(20)	t <sub>10</sub>	:=	4*j
(6)	$t_2$	:=	4*i	(21)	a[t10]	:=	x
(7)	t <sub>3</sub>	:=	a[t <sub>2</sub> ]	(22)	go	to	(5)
(8)	if	t <sub>3</sub>	< v goto (5)	(23)	tii	; =	4*i
(9)	j	:=	j-1	(24)	x	:=	a[t11]
(10)	t <sub>4</sub>	:=	4*j	(25)	t <sub>12</sub>	:=	4*i
(11)	t <sub>5</sub>	:=	a[t <sub>4</sub> ]	(26)	t <sub>13</sub>	:=	4*n
(12)	if	t <sub>5</sub>	> v goto (9)	(27)	t <sub>14</sub>	:=	a[t <sub>13</sub> ]
(13)	if	i	>= j goto (23)	(28)	a[t <sub>12</sub> ]	:=	t <sub>14</sub>
(14)			4*i	(29)			4*n
(15)	x	:=	a[t <sub>6</sub> ]	(30)	a[t <sub>15</sub> ]		

(b) Construct a flowgraph, specify the loops.

(3)

Flow graph nodes with predecessor node & link, loops flow	1
Representing each block with sequence of Instructions	2
Total Marks	3

(c) For each variable, record its next-use and liveliness at the end of each basic block. (3)

List of Next use information for each variable in every block	1.5
Marking of live on Entry & Live on exit at every block	1.5
Total Marks	3

(d) Apply the code improving transformations wherever possible and generate the optimized TAC sequence. (6)

Local – CSE, Copy Propagation & renaming of temp.	2
Global – CSE, Copy Propagation & renaming of temp.	4
Total Marks	15