Sanjay Deshpande

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Summary

I am a second-year Ph.D. student from Yale University, advised by Prof. Jakub Szefer. My research focuses on the efficient and secure hardware implementations of cryptographic algorithms and quantum computer security. I have 3+ years of experience in micro-architecture (RTL) design targeting FPGAs, designing Hardware IP cores for symmetric, asymmetric, and post-quantum cryptography algorithms. I have 1+ year of experience with quantum circuits and quantum computer security. In my previous roles, I have taken ownership of the hardware IPs and assisted in the integration process. I am actively looking for a Summer Internship (2023).

Education

Yale University — *New Haven, CT*
Doctor of Philosophy in Electrical Engineering (GPA: 4.0) — *Aug. 2021 – Present*

George Mason University — *Fairfax, VA*
Master of Science in Computer Engineering (GPA: 3.83) — *Aug. 2014 – Dec 2016*

Jawaharlal Nehru Technological University — *Hyderabad, India*
Bachelor of Technology in Electronics & Communication Engineering (GPA: 4.0) — *Sep. 2010 – May 2014*

Work Experience

Research Assistant — *Aug 2021 - Present*
Yale University — *New Haven, CT*

- Conducted research on primitives of Post Quantum Cryptosystems and designed and implemented secure and efficient hardware designs of Key Encapsulation Mechanism for multiple candidates from ongoing NIST PQC competition.
- Conducted research on Crosstalk based attacks on Quantum Computers and developed Antivirus to scan and detect malicious quantum circuits.
- Ongoing research on performing side channel analysis and attacks on candidates from ongoing Post Quantum and Lightweight Crypto competitions.
- Ongoing research on circuit splitting and circuit obfuscation techniques for quantum circuits.

Associate Researcher II — *Oct 2020 - Aug 2021*
Yale University — *New Haven, CT*

- Conducted research and developed hardware implementations of key components in Public Key Cryptography, and Post Quantum Cryptography targeting FPGAs
- Analyzed timing and optimized the design area of the RTL implementations.
- Conducted research on hardware accelerators compatible with RISC V CPU architecture.

Sr. Security Researcher (formerly Sr. Cryptography Hardware Engineer, DarkMatter LLC) — *Apr 2019 -Jul 2020*
Technology Innovation Institute — *Abu Dhabi, UAE*

- Research and implementation of hardware accelerators (RTL targeting FPGA) for Post Quantum Cryptography primitives.
- Platform independent RTL implementations of cryptographic algorithms and protocols targeting FPGAs and ASICs. Development process right from customer requirement to production-ready IP.
- Optimized RTL designs for performance in terms of Power, Timing, Frequency, and Area. Drew test plans for verification and validation of the IP.
- Took Ownership of the Hardware Accelerators for FPGA based design and assisted in the Integration process.
- Analyzed the RTL implementations for side-channel attacks and developed side-channel resistant RTL implementations of cryptographic algorithms.

Hardware Security Researcher — *Mar 2017 -Apr 2019*
DarkMatter LLC — *Abu Dhabi, UAE*

- Conducted research and implemented Hardware accelerators (RTL targeting FPGA) for Elliptic Curve Cryptography primitives.
- Reverse Engineering and hardware hacking of various devices.
- Tested and Provided mitigations for security threats related to hardware for various devices.

Research and Teaching Assistant *Aug 2014 – Dec 2016*

Cryptographic Engineering Research Group (CERG), George Mason University *Fairfax, VA*

- Hardware Implementations (VHDL and Verilog) of the Cryptographic Algorithms targeting FPGAs: Virtex 6, Virtex 7, and Zynq 7000 FPGA/SoC families.
- Analyzed performance bottlenecks of authenticated ciphers on hardware (Xilinx Virtex 7), and designed and implemented methods to overcome the bottlenecks.
- Conducted the Linear Electronics Lab for undergraduate students.
- Assisted students in Digital Systems Design using VHDL course and FPGA and ASIC Design with VHDL lab.

Junior Electrical Engineer *May 2015 – Aug 2015*

Rysc Corp. *Manassas, VA*

- Designed and Prototyped electronic hardware.
- Conducted PCB Design using Eagle CAD and Tested and Evaluated PCBs.
- Developed ARM Firmware in C.

Lab Assistant *Aug 2014 – Aug 2015*

George Mason University *Fairfax, VA*

- Assisted students in experiments based on Electrical and Computer Engineering.
- Verified the quality of the components used in Lab Experiments.

Publications

1. Sanjay Deshpande, Chuanqi Xu, Theodoros Trochatos, Hanrui Wang, Ferhat Erata, Song Han, Yongshan Ding, and Jakub Szefer, "Design of Quantum Computer Antivirus", in Proceedings of the International Symposium on Hardware Oriented Security and Trust (HOST), May 2023.

2. Sanjay Deshpande, Mamuri Nawan, Kashif Nawaz, Jakub Szefer, Chuanqi Xu, "Fast and Efficient Hardware Implementation of HQC," NIST - Fourth PQC Standardization Conference, Nov 2022.

3. Sanjay Deshpande, Mamuri Nawan, Kashif Nawaz, Jakub Szefer, Chuanqi Xu, "Don't Wait for SHAKE256: A Fast HQC Hardware Implementation," CANS, Abu Dhabi, UAE, Nov 2022.

4. Po-Jen Chen[1], Tung Chou, Sanjay Deshpande[1], Norman Lahr, Ruben Niederhagen, Jakub Szefer, Wen Wang, "Complete and Improved FPGA Implementation of Classic McEliece", CHES, Leuven, Belgium, Sept 2022. (also published at NIST - Fourth PQC Standardization Conference, Nov 2022.)

5. Sanjay Deshpande, Chuanqi Xu, Theodoros Trochatos, Yongshan Ding, Jakub Szefer, "Towards an Antivirus for Quantum Computers," HOST, Washington DC, USA, Mar 2022.

6. Sanjay Deshpande, Santos Merino del Pozo, Victor Mateu, Marc Manzano, Najwa Aaraj, Jakub Szefer, "Modular Inverse for Integers using Fast Constant Time GCD Algorithm and its Applications," FPL, Dresden Germany, Aug 2021.

7. Sanjay Deshpande, Kris Gaj, "Analysis and pipelined implementation of selected parallelizable CAESAR competition candidates," Euromicro DSD, Vienna Austria, Sept 2017.

8. Sanjay Deshpande, "High-Speed hardware implementations of cryptographic algorithms using FPGAs," Master of Science Thesis, Electrical and Computer Engineering Department, George Mason University, Dec 2016.

Projects

Optimized Decomposition of $U_{Heis3}(t)$ into Quantum Gates | *Qiskit, Python, IBMQ* *Mar 2022 – May 2022*

Participated in the IBM challenge and contributed in improving the fidelity of Heisenberg Hamiltonian H_{Heis3} circuit. Implemented a '`trotter`' function using optimal two-qubit transformations and demonstrated a fidelity of 52% on `ibmq_jakarta`.

Antivirus for Quantum Computers | *Qiskit, Python, Quantum Computing* *Sep 2021 – Dec 2021*

Proposed a method to detect malicious circuits in quantum programs. Explored the possibility of modifying Qiskit, and added multi-layered protection – an Antivirus system to detect the malicious attacker circuits, which would prevent malicious users from performing attacks, proposed to run Qiskit programs inside a trusted execution environment, protecting it from malicious users.

Survey on Inference Acceleration for various NN models on cloud processors *Oct 2021 – Dec 2021*

Benchmarked results for inference acceleration of pre-trained DNN models – ResNet50 and MobileNetV1 on cloud FPGAs, cloud GPUs, and cloud CPUs. Built a common framework to track different performance metrics - Time, Accuracy, Throughput, and Energy. Provided a fair performance comparison for DNN inference based on the different performance metrics on cloud CPU versus cloud GPU versus cloud FPGA.

[1] Equal Contributors

Complete ASIC Design Flow using Synopsys ASIC design tools | *ASIC, Verilog* *Aug 2015 – Dec 2015*

Implemented an ALU and carried out the complete ASIC design flow – used Design Compiler for floorplanning, place, and route, and PrimeTime for clock tree insertion and power estimation generated area, power, and timing reports and located the critical paths of the designs. Optimized false paths and maximum delay paths. Used IC Compiler to create back-end designs and generated the GDSII files.

High-Level Synthesis of an ALU | *FPGA, High Level Synthesis* *Jan 2015 – May 2015*

Designed an ALU using high-level synthesis, created an custom IP to Vivado and interfaced it with Zynq 7000 using AXI Lite and AXI Stream interfaces.

RTL implementation of an authenticated cipher | *FPGA, VHDL, Cryptography* *Aug 2014 – Dec 2014*

Designed an RTL implementation for CAESAR competition Round 2 authenticated block cipher candidate – Minalpher targeting FPGAs.

Motion Detection Camera | *Embedded Hardware* *Aug 2014 – Dec 2014*

Assembled hardware and designed a system that senses motion and captures images.

Technical Skills

Languages: VHDL, Verilog, TCL, C, Python, Qiskit, Assembly.
Operating Systems: Windows, Linux, OSX.
Programmable Hardware: Xilinx – Spartan 6, Artix 7, Spartan 3E, Zynq 7000, Virtex 7, Zynq UltraScale+
Tools: Xilinx Vivado, Xilinx ISE, Xilinx ISim, Mentor Graphics Modelsim, Aldec Active-HDL, Intel Quartus prime, GHDL, Xilinx SDK, GMU ATHENa, Code Composer Studio, Cadsoft Eagle, Matlab, Cryptool, GnuPG, Synopsys Tools: Design Compiler, PrimeTime, IC compiler.
Communication Interface: UART, SPI, I2C, AXI.
Word Processing Tools: LaTeX, Microsoft Word, PowerPoint, Excel.
Version Control Tools: Git, TortoiseSVN.
Graphic Design Tools: Omnigraffle, Microsoft Visio.
Microcontrollers worked on: 8051, MSP430, Arduino.
Experience with lab tools: Logic Analyzers, Oscilloscopes, Soldering.

Achievements

- *May 2017* – Won Outstanding Academic Achievement Award, Electrical and Computer Engineering Department at George Mason University.
- *Dec 2015* – Won third place in the Contest for the Best Project in the Cryptography and Computer Network Security course –at George Mason University.
- *July 2014* – Received Certificate of Excellence in Academics, Jawaharlal Nehru Technological University, India.
- *October 2013* – Won First Prize in Robocup 2k14, a zonal event, Jawaharlal Nehru Technological University, India.