Synopsys Synplify FAQ

Introduction to Synopsys Synplify (Ask a Question)

This document provides answers to frequently asked questions (FAQs) related to the Synopsys® Synplify® tool, and its integration with Microchip's Libero® SoC Design Suite. This document covers topics such as licensing, error messages and synthesis optimization. This document is intended to help users to effectively utilize Synplify for FPGA designs. It explains the supported HDL languages, licensing requirements and how to troubleshoot common issues. Additionally, the document addresses specific queries regarding RAM inference, attributes, directives and techniques to improve design area and quality of results.

What does Synplify do? (Ask a Question)

Synplify and Synplify Pro products are logic synthesis tools for Field Programmable Gate Array (FPGA) and Complex Programmable Logic Device (CPLD). The Synplify Pro tool is an advanced version of the Synplify tool, with many additional features for managing and optimizing complex FPGAs. Some additional features available in Synplify Pro are Finite State Machine (FSM) explorer, FSM viewer, Register re-timing and gated clock conversion.

These tools accept high-level input, written in industry-standard hardware description languages (Verilog and VHDL), and using the Synplicity Behavior Extracting Synthesis Technology (BEST) algorithms. They convert the designs into small and high-performance design netlists for popular technology vendors. The tools write VHDL and Verilog netlists after synthesis, which can be simulated to verify functionality.

Which HDL language does Synplify support? (Ask a Question)

Verilog 95, Verilog 2001, System Verilog IEEE® (P1800) standard, VHDL 2008, and VHDL 93 are supported in Synplify. For information on different language constructs, see Synplify Pro for Microchip Language Support Reference Manual.

Will Synplify accept manual instantiations of Microchip macros? (Ask a Question)

Yes, Synplify contains built-in macro libraries for all of Microchip's hard macros including logic gates, counters, flip-flops and I/Os. You can manually instantiate these macros in your Verilog and VHDL designs, and Synplify passes them through to the output netlist.

How does Synplify work with Microchip tools? (Ask a Question)

The Synopsys Synplify Pro® Microchip Edition (ME) synthesis tool is integrated into Libero, which enables you to target and fully optimize an HDL design for any Microchip device. As with all other Libero tools, you can launch Synplify Pro ME directly from the Libero Project Manager.

Synplify Pro ME is the standard offering in Libero editions. Synplify Pro ME is launched by invoking the executable specific in the Libero tool profile.

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1. Licensing Download Installation (Ask a Question)

This section answers the queries related to the license installing and download procedure of Synplify in Libero.

1.1 Where can I download the latest Synplify release? (Ask a Question)

Synplify is a part of Libero download and the standalone installation link is Microchip Direct.

1.2 Which version of Synplify is released with the latest Libero? (Ask a Question)

For the list of Synplify versions released with Libero, see Synplify Pro® ME.

1.3 How do I upgrade to the latest version of Synplify and use it in the Libero Project Manager? (Ask a Question)

Download and install the latest version of Synplify from the Microchip or Synopsys website, and change the synthesis settings in the Libero Project Manager tool profile from the **Libero Project > Profiles** menu.

1.4 Do I need a separate license to run Synplify in Libero? (Ask a Question)

No, all Libero licenses except for the Libero-Standalone license includes a license for the Synplify software.

1.5 Where and how do I get the license for Synplify? (Ask a Question)

To apply for a free license, see the Licensing Page and click the *Software Licenses and Registration System* link. Enter the required information, including the volume ID of your C drive. Make sure to apply with your C drive, even if that is not the drive you intend to install the software on. For paid licenses, contact the local Microchip Sales Office.

1.6 Why can I not run Synplify in batch mode? What license does it require? (Ask a Question)

From command prompt, go to the directory where the project files are located and type the following.

- For Libero IDE:

```
synplify_pro -batch -licensetype synplifypro_actel -log synpl.log TopCoreEDAC_syn.prj
```

- For Libero SoC:

```
synplify_pro -batch -licensetype synplifypro_actel -log synpl.log asdasd_syn.tcl
```

Note: You must have a silver license to run Synplify in batch mode. Generate your free silver license at Microchip portal.

1.7 Why is my Synplify license not working? (Ask a Question)

The steps to check the functioning of the license are as follows:

1. Check if the license has expired.
2. Check if the `LM_LICENSE_FILE` is set correctly as a windows user environment variable, which points to the location of the `Libero License.dat` file.
3. Check whether the Libero IDE tool profile is set to Synplify Pro and the Synplify license feature is enabled in your license file.
4. Look for the “synplifypro_actel” feature line in the `license.dat` file:

```
INCREMENT synplifypro_actel snpslmd 2016.09 21-nov-2017 uncounted \ 4E4905A56595B143FFF4
VENDOR_STRING=^1+S \
HOSTID=DISK_SERIAL_NUM=ec4e7c14 ISSUED=21-nov-2016 ck=232 \ SN=TK:4878-0:1009744:181759
START=21-nov-2016
```

5. After locating the feature line, make sure that the HostID is correct for the computer you are using.

1.8 Can I use the Synplify license obtained from Microchip (Ask a Question)

No, if you received a Synplify license from Microchip, you will only be able to run Synplify ME.

1.9 Is Synplify Pro Synthesis tool supported in all the Libero licenses? (Ask a Question)

Synplify Pro Synthesis tool is not supported in all the License types. For more information about licensing, see Licensing Page.

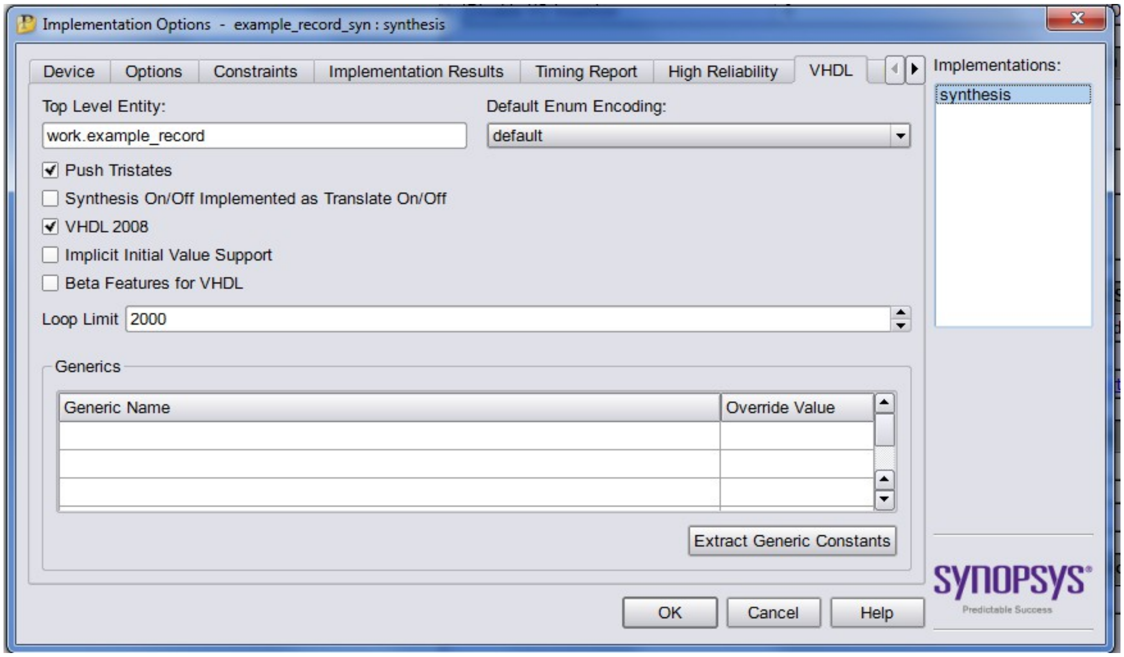
2. Warnings/Error Messages (Ask a Question)

This section provides information about various error messages that appear during the installation procedure.

2.1 Warning: Top entity isn't set yet! (Ask a Question)

This warning message means that Synplify could not identify the top entity in your design, due to design complexity. You need to manually specify the top entity name in Synplify implementation options. The following figure shows an example.

Figure 2-1. Example To Specify Top Entity Name



Implementation Options - example_record_syn : synthesis

Top Level Entity: work.example_record

Default Enum Encoding: default

☑ Push Tristates

□ Synthesis On/Off Implemented as Translate On/Off

☑ VHDL 2008

□ Implicit Initial Value Support

□ Beta Features for VHDL

Loop Limit 2000

Generics

Generic Name	Override Value

Implementations: synthesis

2.2 Warnings on Register Pruning (Ask a Question)

Synplify optimizes the design by pruning unused, duplicate registers, nets or blocks. You can manually control the amount of auto optimization by applying the following directives:

- `*syn_keep`—ensures that if a wire is kept during synthesis and hat there are no optimizations across the wire. This directive is usually used to break unwanted optimizations and to ensure manually created replications. It works only on nets and combinational logic.
- `*syn_preserve`—ensures that registers are not optimized away.
- `*syn_noprune`—ensures that a black box is not optimized away when its outputs are unused (that is, when its outputs do not drive any logic).

For more information about optimization control and Synplify documents, see Synplify Pro for Microchip User Guide.

2.3 @W: FP101 |The design has eight instantiated global buffers but allowed is only six (Ask a Question)

@W: FP103— User can use `syn_global_buffers` to increase the allowed global clock buffers to maximum of 18.

The warnings are created because Synplify identified more than six global macros instantiated in the design. The default maximum number of global nets allowed in Synplify is currently set to six.

So when the tool tries to use more than six for this design, it generates an error. You can manually increase the default limit to eight (up to 18 in IGLOO/e, ProASIC3/E and Fusion, and upto eight and 16 depending on the SmartFusion 2 and IGLOO 2 device) by adding a synthesis attribute called `syn_global_buffers`.

For example:

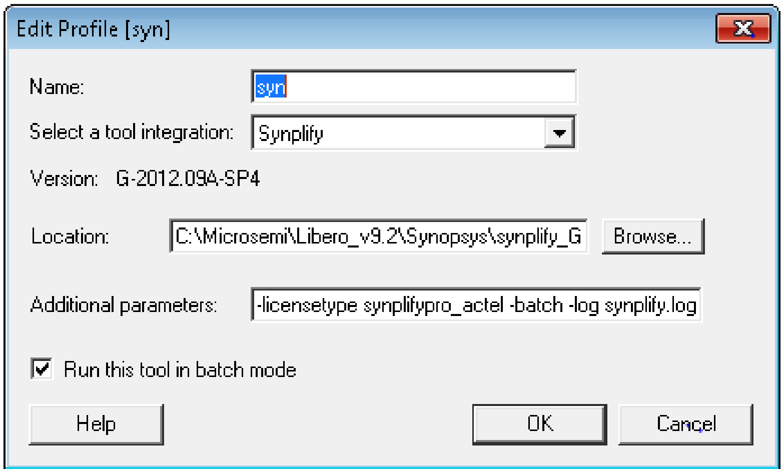
```
module top (clk1, clk2, d1, d2, q1, q2, reset) /* synthesis syn_global_buffers = 8 */;
……
or
architecture behave of top is attribute syn_global_buffers : integer;
attribute syn_global_buffers of behave : architecture is 8;
……
```

For more information, see Synplify Pro for Microchip User Guide.

2.4 Error: The profile for tool Synplify is interactive and you are running in batch mode: this tool cannot be invoked (Ask a Question)

You must have a silver license to run Synplify in batch mode. Contact the local Microchip sales representative to purchase a silver license. You must ensure that the Libero Synthesis tool profile is configured to launch Synplify in batch mode, if you are invoking Synplify from within Libero instead of directly from the command prompt. The following figure shows how to invoke Synplify from within Libero.

Figure 2-2. Example to Invoke Synplify from Within Libero



Edit Profile [syn]

Name: syn

Select a tool integration: Synplify

Version: G-2012.09A-SP4

Location: C:\Microsemi\Libero_v9.2\Synopsys\synplify_G

Additional parameters: -licensetype synplifypro_actel -batch -log synplify.log

☑ Run this tool in batch mode

2.5 @E: CG103: "C:\PATH\code.vhd":12:13:12:13|Expecting expression (Ask a Question)

```
@E: CD488: "C:\PATH\code.vhd":14:11:14:11—EOF in string literal
```

A comment following anything other than a semicolon or a new line is not allowed in VHDL. Two hyphens mark the start of a comment, which is ignored by the VHDL compiler. A comment can be on a separate line or at the end of the line. The error is due to comments in some other part of the VHDL code.

2.6 @E: Internal Error in m_proasic.exe (Ask a Question)

This is not an expected tool behavior. For more information, contact Synopsys Synplify support team, or Microchip Technical Support team if you do not have a Synopsys Support Account.

2.7 Why has my logic block disappeared after synthesis? (Ask a Question)

Synplify optimizes away any logic block that does not have any external output port.

3. Attributes/Directives (Ask a Question)

This section answers the queries related to attributes and directives.

3.1 How do I turn off automatic clock buffer usage in Synplify? (Ask a Question)

To turn off automatic clock buffering for nets or specific input ports, use the `syn_noclockbuf` attribute. Set the Boolean value to one or true to turn off automatic clock buffering.

You can attach this attribute to a hard architecture or module whose hierarchy will not be dissolved during optimization of a port, or net.

For more information about usage of the attribute, see the Synplify Pro for Microchip User Guide.

3.2 Which attribute is used for preserving registers? (Ask a Question)

`syn_preserve` directive is used for preserving registers. For more information about this attribute, see the Synplify Pro for Microchip User Guide.

3.3 Does syn_radhardlevel attribute support IGLOO and Fusion families? (Ask a Question)

No, `syn_radhardlevel` attribute is not supported in IGLOO® and Fusion families.

3.4 How do I disable serial optimization in Synplify? (Ask a Question)

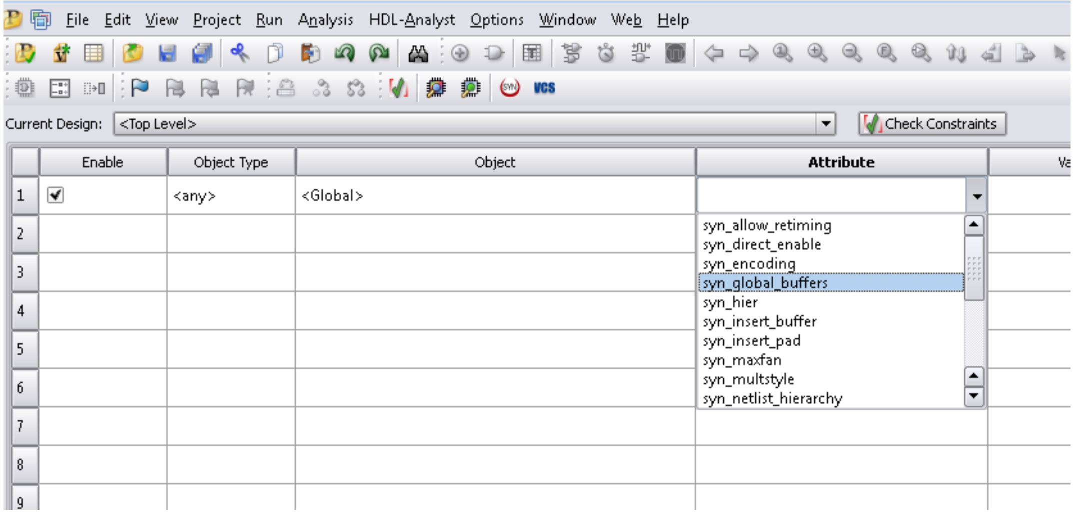
Use `syn_preserve` directive to disable serial optimization in Synplify.

3.5 How can I add an attribute in Synplify? (Ask a Question)

Perform the following steps to add an attribute in Synplify:

1. Launch Synplify from the Libero Project Manager.
2. Click on File > New > FPGA Design Constraints.
3. Click the Attributes tab at the bottom of the spreadsheet.
4. Double-click on any of the attribute cells in the spreadsheet. You should see a drop-down menu with many attributes listed. Select any of them, and fill in the required fields accordingly, as shown in the following figure.

Figure 3-1. Selecting Attributes from the Drop-down cell



Current Design: <Top Level>

	Enable	Object Type	Object	Attribute	Va
1	☑	<any>	<Global>		
2					
3					
4					
5					
6					
7					
8					
9					

5. Save the files and close the Scope Editor after completing the task.

3.6 How do I insert a clock buffer in my design? (Ask a Question)

Use `syn_insert_buffer` attribute to insert a clock buffer. The synthesis tool inserts a clock buffer according to the vendor-specific values you specify. The attribute can be applied on instances.

For more information about the usage of the attribute, see the Synplify Pro for Microchip User Guide.

3.7 How do I increase the number of global clock buffers used in my design? (Ask a Question)

Use `syn_global_buffers` attribute in the SCOPE to specify the number of global buffers to be used in a design. It is an integer between 0 and 18. For more information about this attribute, see the Synplify Pro for Microchip User Guide.

3.8 Is there any way to preserve my logic if the output ports are not used in my design? (Ask a Question)

Use `syn_noprune` attribute to preserve the logic if the output ports are not used in the design. For example: `module syn_noprune (a,b,c,d,x,y); /* synthesis syn_noprune=1 */;`

For more information about this attribute, see the Synplify Pro for Microchip User Guide.

3.9 Why is synthesis optimizing my high fanout net to buffered clock? (Ask a Question)

Use `syn_maxfan` to override the default (global) fanout guide for an individual input port, net, or register output. Set the default fanout guide for a design through the device panel on the Implementation Options dialog box, or with the `set_option -fanout_limit` command in the project file. Use the `syn_maxfan` attribute to specify a different (local) value for individual I/Os.

For more information about this attribute, see the Synplify Pro for Microchip User Guide.

3.10 How do I use the syn_encoding attribute for an FSM design? (Ask a Question)

The `syn_encoding` attribute overrides the default FSM compiler encoding for a state machine. This attribute takes effect only when FSM compiler is enabled. Use `syn_encoding` when you want to disable the FSM compiler globally, but there are a select number of state registers in your design that you want to be extracted. In this case, use this attribute with the `syn_state_machine` directive on for just those specific registers.

For more information about this attribute, see the Synplify Pro for Microchip User Guide.

3.11 Why Synplify generates a netlist that exceeds the maximum fanout of device, causing the netlist to fail compile? (Ask a Question)

A CC macro, available for Antifuse families, is a flip-flop element built using two C-cells. A net driving the CLK or CLR port of a CC macro is driving two cells. The hard fan-out limit on certain nets does not achieve the desired results because it fails to take this net doubling effect into account.

Include the `syn_maxfan` attribute in the RTL code to force Synplify to generate a valid netlist. Reduce the max fanout limit value by one for every CC macro driven by the net. For example, set the `syn_maxfan` limit to 12 for a net that is driving CC macros to keep the fanout at 24 or less.

4. RAM Inference (Ask a Question)

This section answers the queries related to the RAM inference Synplify support for Microchip product families.

4.1 Which Microchip families do Synplify support for RAM inference? (Ask a Question)

Synplify supports the Microchip ProASIC®, ProASIC PLUS®, ProASIC3®,SmartFusion® 2, IGLOO® 2 and RTG4™ families in generating both single and dual-port RAMs.

4.2 Is RAM inference ON by default? (Ask a Question)

Yes, the synthesis tool automatically infers RAM.

4.3 How can I turn off RAM inference in Synplify? (Ask a Question)

Use `syn_ramstyle` attribute and set its value to registers.

For more information, see the Synopsys Synplify Pro for Microchip Reference Manual.

4.4 How do I make Synplify infer embedded RAM/ROM? (Ask a Question)

Use `syn_ramstyle` attribute and set its value to block_ram or LSRAM and USRAM for SmartFusion 2 and IGLOO 2 devices.

For more information, see the Synopsys Synplify Pro for Microchip Reference Manual.

4.5 I cannot compile an existing design in a newer version of designer. (Ask a Question)

There could be possible RAM/PLL configuration change. Regenerate your RAM/PLL by opening the core configuration options from the Catalog in the Libero Project Manager, and resynthesize, compile, or layout.

5. Area or Quality of Results (Ask a Question)

This section answers the queries related to the area or quality usage for Synplify.

5.1 Why does area usage increase in the new version of Synplify? (Ask a Question)

Synplify is designed to achieve better timing results in every new version. Unfortunately, the trade-off is often an area increase.

If the timing requirement is achieved for the design, and the remaining task is to fit the design in a specific die, following are the methods:

1. Increase Fanout limit to reduce buffer replication.
2. Change global frequency settings to relax the timing requirement.
3. Turn on resource sharing (design specific) to optimize the design.

5.2 What kind of area improvement technique is available in Synplify? (Ask a Question)

Perform the following techniques to improve area in Synplify:

1. Increase the fanout limit when you set the implementation options. A higher limit means less replicated logic and fewer buffers inserted during synthesis, and a consequently smaller area. In addition, as place-and-route tools typically buffer high fanout nets, there is no need for excessive buffering during synthesis.
2. Check the **Resource Sharing** option when you set implementation options. With this option checked, the software shares hardware resources like adders, multipliers and counters wherever possible, and minimizes area.
3. For designs with large FSMs, use the gray or sequential encoding styles, because they typically use the smallest area.
4. If you are mapping into a CPLD and do not meet area requirements, set the default encoding style for FSMs to sequential instead of one hot.

5.3 How do I disable area optimization? (Ask a Question)

The optimization for timing is often under the expense of area. There is no specific way to disable area optimization. Perform the following to improve timing and thereby increase area utilization:

1. Enable re-timing option.
2. Enable Pipelining option.
3. Use realistic design constraints, about 10 to 15 percent of the real goal.
4. Select a balanced fanout constraint.

For more information about the optimization for timing, see Synplify Pro for Microchip User Guide.

5.4 How do I disable sequential optimization? (Ask a Question)

There is no explicit button or checkbox to disable sequential optimization. This is because there are different types of sequential optimizations that are performed by Synplify.

For more information about the options for disabling optimization, see Synplify Pro for Microchip Reference Manual .

For example, following are some options to disable optimization.

- Disable the FSM compiler.
- Use the `syn_preserve` directive to keep registers in certain cases.

Important: The Project Manager overwrites the Synthesis PRJ file every time you invoke synthesis when choosing this option.

5.5 Which family is TMR supported through Synplify? (Ask a Question)

It is supported on Microchip ProASIC3/E, SmartFusion 2, and IGLOO 2 devices as well as Microchip's Radiation Tolerant (RT) and Radiation Hardened (RH) devices. You can also get the Triple Module Redundancy (TMR) setting to work for Microchip's older Antifuse device families. However, it is not supported in the commercial AX device family.

Note: In Microchip's RTAX device family, better TMR support is available through hardware itself. For Axcelerator RT devices, the TMR is built into the silicon making soft TMR through the Synthesis tool unnecessary for sequential logic.

5.6 Why is TMR macro working in SX, but not in AX family? (Ask a Question)

There is no software TMR support in Synplify synthesis for the commercial Axcelerator family, but it is available for the SX family. If you are using RTAXS devices, the TMR is built into the the hardware/ device for the sequential flip- flops.

5.7 How can I enable TMR for a SX-A device? (Ask a Question)

For the SX-A device family, in the Synplify software, you need to manually import the file found in the Libero IDE Installation folder, such as:

```
C:\Microsemi\Libero_v9.2\Synopsys\synplify_G201209ASP4\lib\actel\tmr.vhd.
```

Note: The order of the files in the Synplify project is important and the top-level file must be at the bottom.

You can click and hold the top-level file in the Synplify project and drag it below the `tmr.vhd` file.

5.8 Which version of Synplify supports nano products? (Ask a Question)

All versions of Synplify after Synplify v9.6 A support nano products.

5.9 Which version of Synplify provides RTAX-DSP support? (Ask a Question)

All versions included with Libero IDE v8.6 and later provide RTAX-DSP support.

5.10 How do I create an IP core with the HDL files I have? (Ask a Question)

Create an EDIF netlist without I/O buffer insertion. This EDIF netlist is sent to the user as an IP. The user must treat this as a black box and include it in the design.

5.11 Nano devices have only four global clock networks. How do I set this constraint? (Ask a Question)

Use the attribute /`* synthesis syn_global_buffers` = 4*/ to set the constraint.

5.12 Why am I not seeing my new port list even after I updated the netlist? (Ask a Question)

Although the new port was added in the design, the netlist did not add a buffer to the port since there was no logic in the design which involves the port. Ports not associated with any logic in the design are not shown.

5.13 Why is Synplify not using Global for Set/Reset signals? (Ask a Question)

Synplify treats set/reset signals differently from clocks. Synplify global promotion always gives priority to the clock signals, even if some set/reset signals have higher fanout than clock nets. Manually instantiate a clkbuf to ensure that the set/reset signal is global, if you want to use the global network for these signals.

5.14 Why does Synplify write out SDC clock constraints even for auto-constraints? (Ask a Question)

This is the default behavior in Synplify and cannot be changed. However, you can control the SDC auto-constraints by manually modifying or removing the unwanted constraints.

5.15 Why is my internal tristate logic not synthesized correctly? (Ask a Question)

Microchip devices do not support internal tristate buffers. If Synplify does not correctly remap internal tristate signals, all internal tristates must be manually mapped to a MUX.

6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	12/2024	The following is a summary of the changes in revision A of this document. • Migrated the document to the Microchip template. • Updated the document number to DS60001871A from 55800015. • All Instances of Microsemi were updated to Microchip. • Updated sections Why can I not run Synplify in batch mode? What license does it require? and Error: The profile for tool Synplify is interactive and you are running in batch mode: this tool cannot be invoked to indicate that silver license is needed to run Synplify in batch mode. The platinium license was changed to silver license.
2.0		The following is a summary of the changes in revision 2.0 of this document. • All the Actel links were updated with the Microsemi links. • All instances of IDE are removed from the licensing section. For more information, see Licensing Download Installation. • FAQ 3.9 was added. For more information, see Is Synplify Pro Synthesis tool supported in all the Libero licenses? • FAQ 4.1 was updated. For more information, see Warning: Top entity isn't set yet. • FAQ 4.4 was updated. For more information, see Error: The profile for tool Synplify is interactive and you are running in batch mode: this tool cannot be invoked. • FAQ 5.5 was updated. For more information, see How can I add an attribute in Synplify?
1.0		This was the first publication of the document.

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