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Post-Lab Questions – Lab 01

1. What are the GPIO control registers that the lab mentions? Briefly describe each of their functions.

- GPIOx_MODER: Configures pin modes (input, output, alternate function, analog).
- GPIOx_OTYPER: Selects the output mode for each pin (open-drain or push-pull).
- GPIOx_OSPEEDR: Sets the speed mode for GPIO pins (low, medium, or high).
- GPIOx_PUPDR: Connects internal pull-up or pull- down resistors to a pin.
- GPIOx_IDR: Read-only register; reports the logical state of each pin.
- GPIOx_ODR: Sets the logical state of configured output pins.
- GPIOx_BSRR: Write-only register; quickly sets or clears bits in the output register.
- GPIOx_LCKR: Locks other configura[on registers for a pin to prevent accidental changes.
- GPIOx_AFRL/GPIOx_AFRH: Configures alternate func[ons for each pin.
- GPIOx_BRR: Similar to BSRR but dedicated to clearing bits.

2. What values would you want to write to the bits controlling a pin in the GPIOx_MODER register in order to set it to analog mode?
The values you want to write to the bits controlling a pin in the GPIOx_MODER register in order to set it to analog mode are 11. 11 is analog mode.

3. Examine the bit descriptions in GPIOx_BSRR register: which bit would you want to set to clear the fourth bit in the ODR?
Assuming counting starts with 0, you would want to set bit 20 to high state (1). If counting starts at 1, you would want to set bit 19 to high state (1).

4. Perform the following bitwise operations:
• 0xAD | 0xC7 = 0xEF
• 0xAD & 0xC7 = 0x85
• 0xAD & ~(0xC7) = 0x28
• 0xAD ^0xC7 = 0x6A

5. How would you clear the 5th and 6th bits in a register while leaving the others alone?
This is the proper C code:
GPIOC->MODER &= ~((1 << 5) | (1 << 6));

6. What is the maximum speed the STM32F072R8 GPIO pins can handle in the lowest speed setting?
The maximum speed these pins can handle in the lowest speed setting is 1000 kHz (table 38). From the I/O AC characteristics table, it says the maximum speed the pins can handle in lowest speed setting is 2 mHz if CL = 50 pF, VDDIOx >= 2V. If VDDIOx < 2 V, then maximum speed that the pins can handle in lowest speed is 1 MHz.

7. What RCC register would you manipulate to enable the following peripherals: (use the

comments next to the bit defines for better peripheral descriptions)

- TIM1 (TIMER1): RCC-> APB2ENR |= RCC_APB2ENR_TIM1EN
- DMA1: RCC-> AHBENR |= RCC_AHBENR_DMA1EN
- I2C1: RCC-> APB1ENR |= RCC_APB1ENR_I2C1EN;