1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time? **You can only use a single pin from each group, and there are limited EXTI inputs.**
2. What software priority level gives the highest priority? **0** What level gives the lowest? **3**
3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? **four 8-bit regions to set the priority of an interrupt.** Which bits in the group are implemented? **the uppermost two bits from these regions implemented giving four possible configurable priority levels**
4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission. **The latency between pushing the board button and LED change is about 1-2 seconds.**
5. Why do you need to clear status flag bits in peripherals when servicing their interrupts? **Typically you will need to clear the matching status bit manually for the interrupt condition that you are handling; otherwise, the interrupt will repeat continuously because the request never acknowledges as complete.**