SANJAY SESHAN

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Education

Massachusetts Institute of Technology (MIT) *Cambridge, MA*
Bachelor of Science, Course 6-2 Electrical Engineering and Computer Science *Sep. 2021 - May 2025*
GPA: 4.9/5.0

Relevant Coursework

6.175 Constructive Computer Architecture, *6.111* Digital System Laboratory (FPGA), *6.012* Nanoelectronics Systems, *6.2080* Semiconductor Electronics, *6.039* Operating Systems Engineering, *6.115* Microcomputer Systems, *6.823* Computer System Architecture (F24)

Work Experience & Research

EPFL – Verification and Computer Architecture Lab *Lausanne, Switzerland*
Research Intern *May 2024 - Aug. 2024*

- Contributed to development of SMT-based architecture that can scale to very large number of computation threads
- Extended RISC-V ISA to support thread creation, thread termination and inter-thread communication
- Implemented extensions to RISC-V design for "token"-based approach to managing inter-thread communication using Bluespec SystemVerilog HDL
- Verified design using a tandem verification system
- Expected to submit for publication in Fall 2024

MIT Computer Architecture 6.1920[6.175] Teaching Staff *Cambridge, MA*
Undergraduate Teaching Assistant *Feb. 2024 - May 2024*

- Supervised final projects for 30 students and developed course materials including lab assignments and course notes
- Hosted office hours and delivered multiple course lectures and recitations

Imperial College London - Adaptive Emergent Systems Engineering Group *London, United Kingdom*
Research Intern *Jun. 2023 - Aug. 2023*

- Evaluated numerous sensors (i.e. accelerometers, magnetometers) and embedded development boards for use in system to monitor freight shipments over the course of several months, without any maintenance
- Developed, implemented and programmed proof-of-concept design incorporating core sensing elements to demonstrate low-power capabilities
- Designed a custom PCB design containing of all the desired sensors, CPU, and interfacing chips, that was subsequently printed, assembled and tested with expectations to deploy sensor onto a freight ship in the near future

MIT CSAIL - Computation Structures Group *Cambridge, MA*
Undergraduate Research Assistant *Jan. 2023 - May 2024*

- Designed an application-specific accelerator for graph pattern mining and graph vector search
- Synthesized accelerator for Xilinx FPGA using Vivado and evaluated correctness and efficiency of implementation
- Evaluated performance of processing in memory (PIM) and parallelization techniques in the implementation

Emerald Innovations *Cambridge, MA*
Software Engineering Intern *May 2022 - Aug. 2022*

- Designed algorithm to extract common paths that a single person takes from raw position data (calculated from the RF signal feedback)
- Implemented algorithm as part of an in-house python package used to calculate a person's walking speed and detect changes that could indicate the progression of disease

Technical Skills

- C/C++, Bluespec, SystemVerilog, Python, Embedded Systems design and programming (e.g. Zephyr), Cadence simulation and layout, Xilinx FPGA toolchain (vivado)
- Photoshop & DSLR Photography, LaTeX, Machine Learning (pytorch), Signal Processing, PCB Circuit layout & Design (KiCad, Altium), Java, HTML/JS/CSS

Significant Projects

- **Silicon Differential Amplifier (MIT 6.2080):** Completed layout and tapeout preparation process for a CMOS-based differential amplifier in Cadence.
- **Embedded Oscilloscope (MIT 6.115):** Designed and implemented a PSoC (programmable system on chip) based oscilloscope, with two analog inputs and one analog output, including full frequency analysis and user customizability.
- **2D MoS_2-based Transistors (MIT 6.s059):** Fabricated a nano-scale 2D MOSFET-style transistor using MoS_2 channels for use in developing logic gates, working from design to physical tapeout. Work was accepted to Microsystems Annual Research Conferences (MARC), Jan. 2024.
- **Multicore RISC-V Implementation (MIT 6.175):** Designed and implemented a pipelined, dual-core RISC-V 32-bit processor with a shared cache hierarchy in Bluespec SystemVerilog. Synthesized design to work on AWS-based FPGA.

Leadership and Community Activities

- **MIT SPARK/SPLASH Instructor**:
  - Taught Graph Algorithms course to 30 high school students and Gravitation and Electrostatics to 30 middle school students.
- **Maseeh Hall Dorm Executive**:
  - Representative for Spring 2022. Managed a budget of $800 for 100 students.
  - Chair for Campus Preview Weekend (CPW) for incoming freshmen for the 2022-2023 and 2023-2024 school years. Organized dozens of events for several hundred incoming freshman, introducing them to MIT academics and culture.
  - Chair for REX (Freshman Orientation events) Fall 2023. Ran events to introduce the 1100 new Freshman to their new home at MIT, including 150+ to the dorm. Supported students during move-in.
  - Official photographer for several events, including Maseeh formal and boat cruise.
- **K-12 Youth Robotics Volunteer:**
  - Wrote introductory programming lessons for youth robotics students used by 100k+ per year.
  - Developed Web-based tournament management system for *FIRST* events with support to manage team submissions, judging, and scoring.
  - Alpha and beta-tested both hardware and software products under NDA for the LEGO Group in Billund, Denmark. Designed three robots for the official LEGO MINDSTORMS App released in 2021.