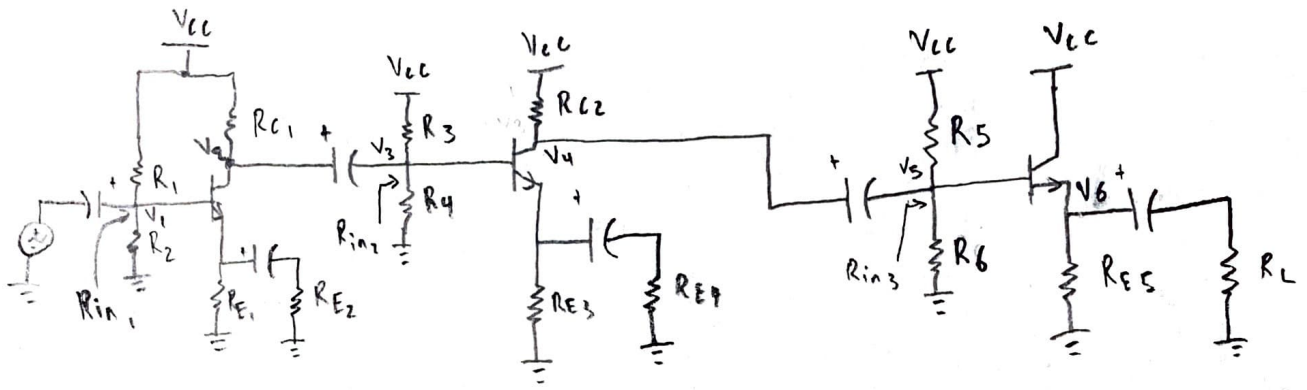
Design Project

Sonjay Sivapragasam
501045929 Section 14

Manual Calculations:

Proposed schematic idea → CE-CE-CC configuration



Known:

$V_{cc} = 10\ V$

$I_{DC} < 10\ mA$

$A_{V0} = 50$

$V_O \geq 8\ V_{pp}$

$V_L \geq 4\ V_{pp}$

$R_{in} \geq 20k\Omega$

all $R \leq 220K\Omega$

For a CC, the gain is close to unity so $A_{V3} = \frac{V_5}{V_4} \simeq 1$

Since the total A_V (gain) at the end should be close to 50, we have $A_{V_0} = A_{V_{01}} \times A_{V_{02}} \times A_{V_{03}}$

$50 = A_{V_1} \times A_{V_{02}} \times 1$

For simplicity sake, A_{V_1} and $A_{V_{02}}$ can have the same amplification.

$\sqrt{50} \doteq 7.1$

$7.1 \times 7.1 = 50.41$

$A_{V_{01}} = \frac{V_2}{V_1} = -7.1$

$A_{V_{02}} = \frac{V_4}{V_3} = -7.1$

Both are -7.1 because it is overall it should become non-inverting at the end.

Starting with stage 1 and 2:

Since $A_{V_{01}} = A_{V_{02}}$, I_C for both CE's can be 400 μA as seen from the load line.

$g_m = \frac{I_C}{V_T} = \frac{400\mu A}{26mV} \doteq 0.0154\ S$

$I_B = 3.5\ \mu A$

$\beta = \frac{400\mu}{3.5\mu} \doteq 114.3$

$I_{B,DC} = 2.\ \mu A$ (operating point / quiescent)

Stage 3: Assume $R_{E5} = 1k\Omega$ to be close to the R_L value

$I_C = 10\ mA$ (from load line).

$I_B = 65\ \mu A$ (from load line)

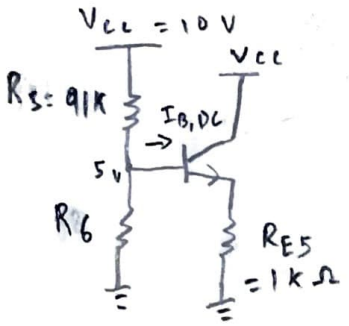
$\beta = \frac{I_C}{I_B} = \frac{10m}{65\mu} \doteq 153.8$

$I_{B,DC} = 30\ \mu A$ (operating point / quiescent)

To ensure that the voltage at the base is not changed too much, the divider current should be much larger than I_B. From the E24 series we can use $91K\Omega$ resistor for R5.

Also, $g_m = \frac{10mA}{26mV} \doteq 0.385\ S$

KCL at V_S:



$$\frac{5-10}{91K} + \frac{5}{R_6} + 30\mu A = 0 \quad (I_{B,DC} \text{ from graph})$$

$$-24.945\mu + \frac{5}{R_6} = 0$$

$$R_6 = \frac{5\ V}{24.945\ \mu A}$$

$$R_6 = 200440.5286$$

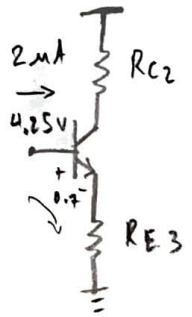
$$R_6 \doteq 200\ K\Omega$$

5 v is approximated as the voltage where Q, (operating point) is from the graph.

Assume $R_{E5} = 1K\Omega$ due to loading effect.

This process (going backwards) can continue to determine all the resistances.

Stage 2 (CE):



KVL:

$$-4.25 + 0.7 + I_E(R_{E3}) = 0$$

$$-4.25 + 0.7 + (1+\beta) I_B (R_{E3}) = 0$$

$$R_{E3} = \frac{3.55}{(1+114.3)(2mA)} = 15394.6\ 2272\ \Omega \doteq 15\ K\Omega$$

$$I_{C,DC} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_{E3} = \frac{10\ V}{400\mu A} = 25000 = 25\ K\Omega$$

$$R_C + R_{E3} = 25K\Omega$$

$$R_C = 25K - 15K = 10K\Omega$$

To find R_{C2} we need R_{in3}.

$$R_{in3} = R_5 // R_6 // \frac{\beta}{g_m} + (\beta+1) R_E$$

$$= 91K // 200K // \frac{153.8}{0.385} + (154.8)(1K)$$

$$\doteq 44.57\ K\Omega$$

} This is from stage 3

$$\frac{1}{10K} = \frac{1}{R_{C2}} + \frac{1}{44.57K}$$

$$R_{C2} \doteq 13\ K\Omega$$

Next we can find R_E by using the gain equation. Note, since stage 1 and 2 are both CE's and have the same amplifications they will have the same biasing resistors and the calculations will follow a similar procedure.

$$A_{V_{02}} = \frac{V_3}{V_2} = \frac{-g_{m_2}(R_{C_2} // R_{in_3})}{1 + g_{m_2} R_E}$$

$$-7.1 = \frac{-0.0154\,(13K // 44.57K)}{1 + 0.0154\,(R_E)}$$

$$-7.1 = \frac{-154.9924266}{1 + 0.0154\,(R_E)}$$

$$R_E = \left(\frac{-154.9924266}{-7.1} - 1\right) \div 0.0154$$

$$R_E = 1352.592159 \doteq 1353\ \Omega$$

From this the A_{V_2} (with load) can be found.

$R_{in_{L3}} = 91K // 200K // \frac{153.8}{0.385} + (154.8)(500)$
$\doteq 34.67\ K\Omega$

} From stage 3, the resistance changed from $1K\Omega$ to 500Ω when R_L is now used.

$$A_{V_2}\text{ (with load)} = \frac{-0.0154\,(13K // 34.67K)}{1 + 0.0154\,(1353)}$$

$$= \frac{-145.6038179}{23.8228} = -6.668001663 \doteq -6.7$$

Next is finding R_{E4} for stage 2:

$R_E = 1353\ \Omega \doteq 1.3K\ \Omega$

$$1.3K = \frac{1}{\frac{1}{R_{E3}} + \frac{1}{R_{E4}}}$$

$$\frac{1}{1.3K} = \frac{1}{15K} + \frac{1}{R_{E4}}$$

$$R_{E4} \doteq 1423.357664\ \Omega \doteq 1.3K\ \Omega$$

* 1.4K not apart of E24 series but 1.3K is.

Lowering emitter resistance yields more gain, so rounding down in intermediate calculations is acceptable to ensure gain is met.

Biasing resistors:

similar to stage 3, we need large enough resistors such that the divider current is much larger than I_B. This is especially critical for CE's because if the divider current is too small, it can affect V_b. Assume $R_3 = 91K\Omega$ (from E24 series for simplicity sake).

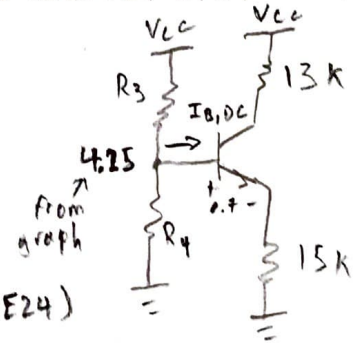
Applying KCL at V_3:

$$\frac{4.25 - 10}{91K} + \frac{4.25}{R_4} + 2\mu A = 0$$

$$R_4 = 4.25 // \left(-2\mu - \frac{4.25 - 10}{91K}\right)$$

$$= 69459.41092$$

$R_4 \doteq 68K\Omega$ (round down since 70K not apart of E24)

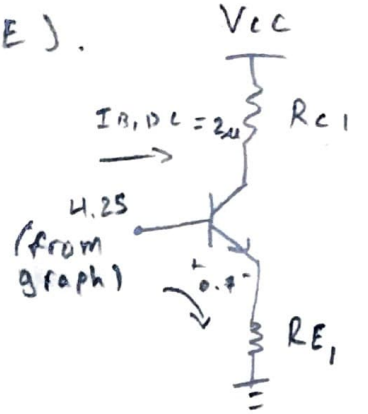


next, $R_{in_2} = R3 // R4 // \frac{\beta}{g_m} + (\beta + 1) R_E$

$= 91K // 68K // \frac{114.3}{0.0154} + (115.3)(1353)$

$\doteq 31432.72 \doteq 31.433K\Omega$

Lastly we have stage 1 (another CE).



$I_{C,DC} = \frac{V_{CC}}{R_C + R_{E_1}}$

$R_C + R_{E_1} = \frac{10\,V}{400\,\mu A}$

$= 25\,K\Omega$

Applying KVL:

$-4.25 + 0.7 + I_E \cdot R_{E_1} = 0$

$(1+\beta) I_B R_{E_1} = 3.55$

$(114.3 + 1)(2\mu) R_{E_1} = 3.55$

$R_{E_1} = 15394.62272$

$\doteq 15\,K\Omega$

$25\,K\Omega = R_{C_1} + R_{E_1}$

$\therefore R_C = 10\,K\Omega$

R_{C_1}: $R_C = R_{C_1} // R_{in_2}$

$10K = \frac{1}{\frac{1}{R_{C_1}} + \frac{1}{31.433K}}$

$R_{C_1} = 14665.70242$

$\doteq 15\,K\Omega$

→ we can use this and the same gain equation to find R_E.

$A_{V_1} = \frac{-g_m (R_{C_1} // R_{in_2})}{1 + g_m R_E}$

$-7.1 = \frac{-0.0154 (14K // 31.433K)}{1 + 0.0154 R_E}$

$R_E = \left(\frac{-150.5202242}{-7.1} - 1\right) \div 0.0154$

$\doteq 1299.3\,\Omega \doteq 1.3\,K\Omega$

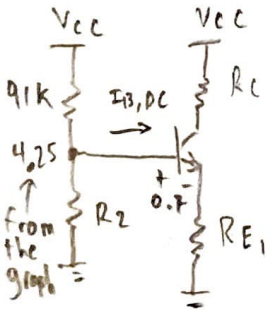
R_{E_2}: $R_E = R_{E_1} // R_{E_2}$

$1.3K = \frac{1}{\frac{1}{R_{E_2}} + \frac{1}{1.5K}}$

$R_{E_2} = 1423.357664$

$\doteq 1.5\,K\Omega$ (rounded to nearest E24 series)

Lastly, we can assume R_1 to be $91K\Omega$ (from the E24 series for simplicity sake) so the divider current is significantly larger than the base current.



KCL, solving for R_2:

$\frac{4.25 - 10}{91K} + \frac{4.25}{R_2} + 2\mu A = 0$

$\frac{4.25}{R_2} = 6.118681319 \times 10^{-5}$

$R_2 = 69459.41092$

$R_2 \doteq 68\,K\Omega$ (apart of E24 series)

$R_{in_1} = 91K // 68K // \frac{\beta}{g_m} + (\beta+1) R_E$

$= 91K // 68K // \frac{114.3}{0.0154} + (115.3)(1299)$

$= 31195.07046$

$R_{in_1} \doteq 31.195\,K\Omega$

Now that all the major calculations are done, capacitor values can be determined. Then the final quiescent current can be calculated as the final verification calculation for the circuit design, alongside the overall gain.

Values for $C_1 - C_6$: we can use the equation $Z = \frac{1}{j\omega C}$

It is important to note that emitter degeneration resistance is critical in order to maintain the gain of the CE stages. Larger capacitor values are expected for C_2, C_4, C_6. In contrast, R_{in_1}, R_{in_2}, R_{in_3} values were relatively high already so C_1, C_3, C_5 are not required to be as large (not as critical).

The frequency Range is from 20Hz - 50kHz, so we can examine the impedence over this range. The sample values to test this are 100μF and 10μF.

Worst case

$f = 20Hz$

C_2, C_4, C_6:

$$Z = \frac{1}{j2\pi fC}$$

$$= \frac{1}{j2\pi(20Hz)(100\mu F)}$$

$$= 79.6\Omega$$

C_1, C_3, C_5 :

$$Z = \frac{1}{j2\pi(20Hz)(10\mu F)}$$

$$= 796\Omega$$

Best case

$f = 50kHz$

C_2, C_4, C_6:

$$Z = \frac{1}{2\pi(50k)(100\mu)}$$

$$= 31.8m\Omega$$

C_1, C_3, C_5 :

$$Z = \frac{1}{2\pi(50k)(10\mu)}$$

$$= 0.32\Omega$$

An Average case (using 1kHz as it was apart of the requirements from the manual)

$f = 1kHz$

C_2, C_4, C_6:

$$Z = \frac{1}{2\pi(1k)(100\mu)} = 1.6\Omega$$

C_1, C_3, C_5 :

$$Z = \frac{1}{2\pi(1k)(10\mu)} = 15.9\Omega$$

As seen by the calculated impendances, the selected capacitors of 100μF and 10μF should allow the circuit to maintain the gains.

Final Gains:

$A_{V_0} = -7.1 \times -7.1 =$	50.41
$A_V = -6.7 \times -7.1 =$	47.57

For A_{V_0} and A_V we only multiply by 2 stages since stage 3 is a CC so gain is approximately unity at stage 3. For A_V (with load) it is assumed the first CE stage will not feel the loading effect of RL, so we multiply the -6.7 by the initially assumed -7.1.

Quiescent current: $I_{DC,Total} = I_{C_1} + I_{R_1} + I_{C_2} + I_{R_3} + I_{C_3} + I_{R_5}$

$$= \beta I_{B_1} + \frac{V_{cc}}{R_1+R_2} + \beta I_{B_2} + \frac{V_{cc}}{R_3+R_4} + \beta I_{B_3} + \frac{V_{cc}}{R_5+R_6}$$

$$= 114.3(2\mu) + \frac{10}{91k+68k} + 114.3(2\mu) + \frac{10}{91k+68k} + 153.8(30\mu) + \frac{10}{200k+91k}$$

$$\doteq 0.00523 \text{ A}$$

$I_{DC,Total} \doteq 5.23$ mA

5.23 mA < 10 mA ✓

Final Circuit schematic with calculated values: