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Introduction

The final report for the ELE 404 Amplifier Design Project is presented herein. This design project cultivates all of the course learning regarding Bipolar Junction Transistors (BJT), which tests a multi-stage amplifier that can adhere to a set of requirements. All manual calculations can be found in the appendix, and the circuit was simulated in Multisim for analysis.

Objectives

The main objective of this design project is to design and construct a BJT amplifier such that the specified requirements below are achieved.
The specifications that the circuit had to meet are summarized below:

- Power supply: +**10 V** relative to the ground;
- Quiescent current drawn from the power supply: no larger than 10 mA;
- No-load voltage gain (at 1 kHz): **|Avo| = 50 (± 10%)**;
- Maximum no-load output voltage swing (at 1 kHz): **no smaller than 8 V peak to peak**;
- Loaded voltage gain (at 1 kHz and with RL = 1 kΩ): **no smaller than 90% of the no-load voltage gain**;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 kΩ): **no smaller than 4 V peak to peak**;
- Input resistance (at 1 kHz): **no smaller than 20 kΩ**;
- Amplifier type: **inverting or non-inverting**;
- Frequency response: **20 Hz to 50 kHz (−3dB response)**;
- Type of transistors: **BJT**;
- Number of transistors (stages): **no more than 3**;
- Resistances permitted: **values smaller than 220 kΩ from the E24 series**;
- Capacitors permitted: **0. 1 µF, 1. 0 µF, 2. 2 µF, 4. 7 µF, 10 µF, 47 µF, 100 µF, 220 µF**;
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit**.

Graphs

Below are the 2 characteristic graphs that were used to create load lines and begin the design process. The graphs plot the collector current that passed through the BJT against the collector to emitter voltage drop.

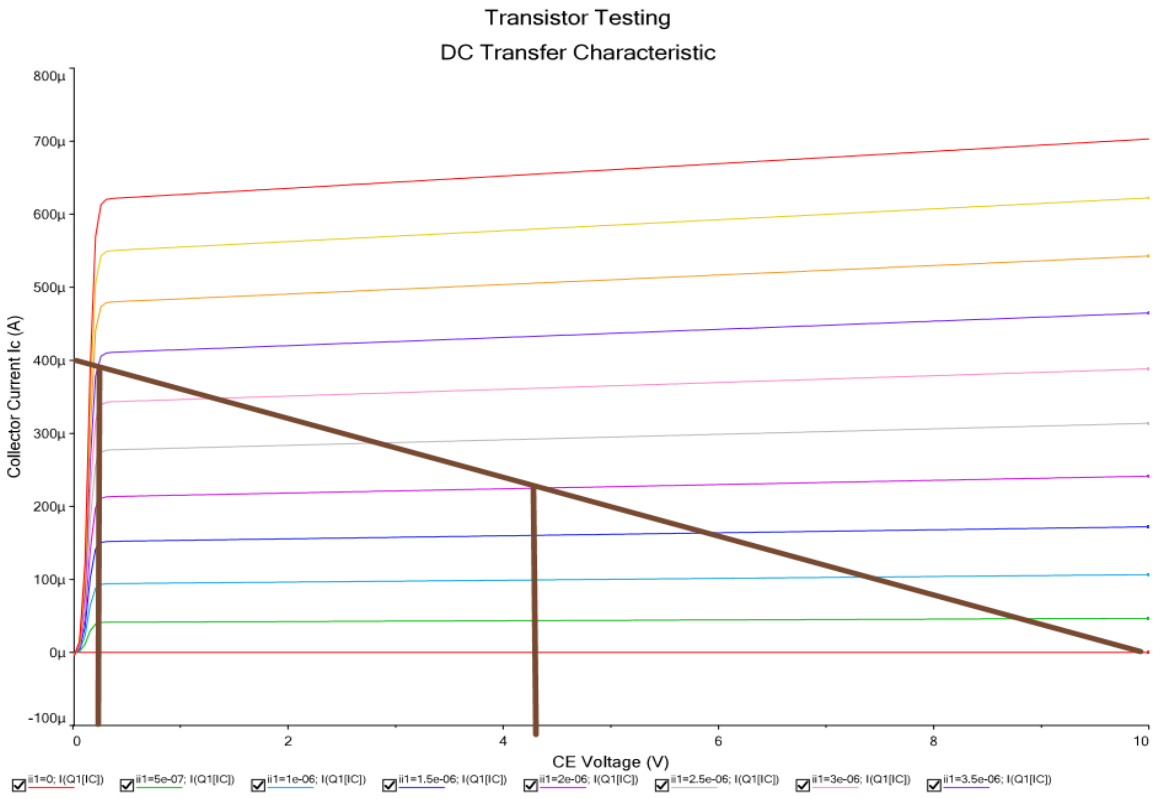

Figure 1. Characteristic graph of CE 2N3904 BJT with chosen load line.

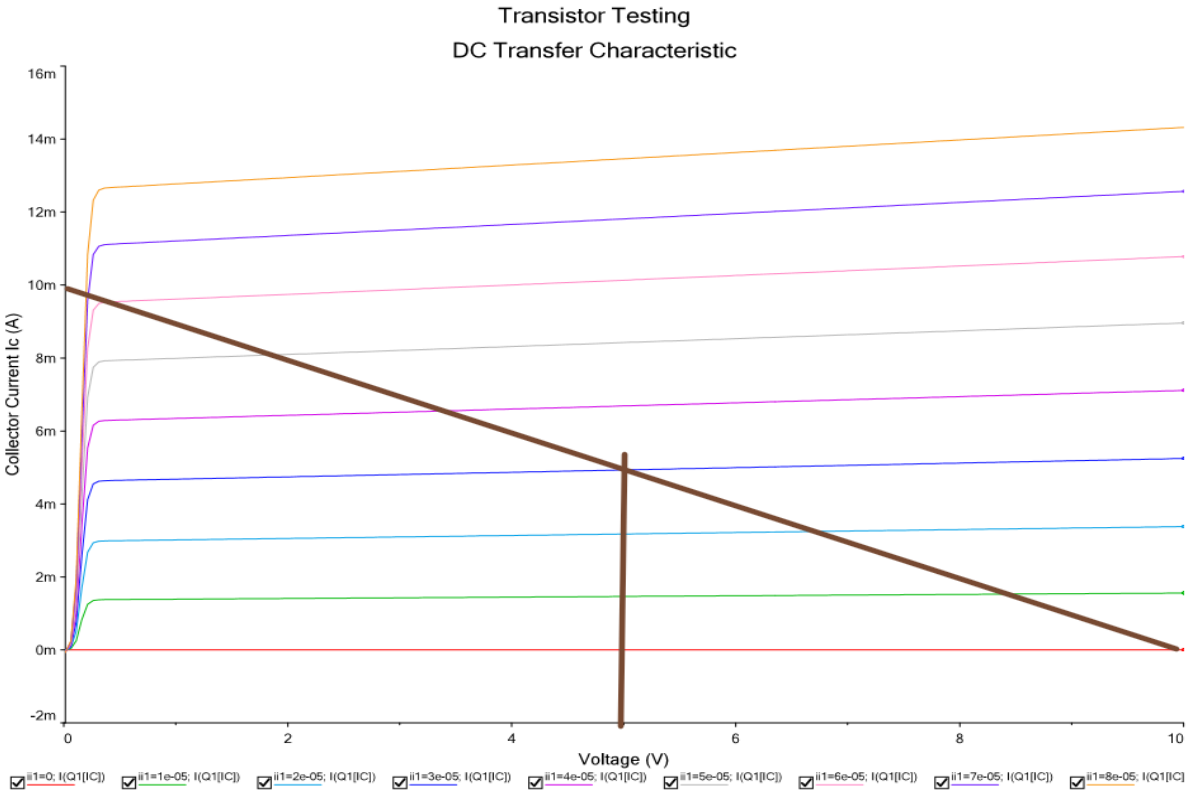

Figure 2. Characteristic graph of CC 2N3904 BJT with chosen load line.

These graphs were created from the DC sweep analysis option in Multisim. The testing circuit used to find the characteristic response of the 2N3904 transistor consists of a DC voltage source, and a current source connected to the base of the BJT.

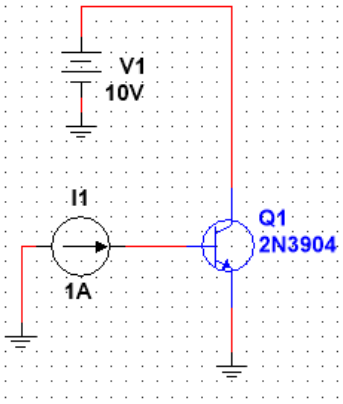

Figure 3. Testing circuit for BJT Characteristic graph.

Summary of Calculations

To summarise the calculations (all in the appendix), the tables below will display some of the final values of the circuit.

C_1	C_2	C_3	C_4	C_5	C_6
10 µF	100 µF	10 µF	100 µF	10 µF	100 µF

Table 1. Capacitor Values

R_1	R_2	R_3	R_4	R_5	R_6
91 kΩ	68 kΩ	91 kΩ	68 kΩ	91 kΩ	200 kΩ

Table 2. Biasing Resistor Values

R_{C1}	R_{C2}	R_{E1}	R_{E2}	R_{E3}	R_{E4}	R_{E5}	R_L (load)
15 kΩ	13 kΩ	15 kΩ	1.5 kΩ	15 kΩ	1.3 kΩ	1 kΩ	1 kΩ

Table 3. Collector and Emitter Resistor Values

I_B	$I_{B,\,DC}$	β	I_C	V	g_m
65 mA	30 µA	153.8	10 mA	5 V	0.385 S

Table 4. Some Critical Values of CC (Stage 3)

I_B	$I_{B,\,DC}$	β	I_C	V	g_m
3.5 µA	2 µA	114.3	400 µA	4.25 V	0.0154 S

Table 5. Some Critical Values of CE (Stages 1 and 2)

Process for Design and Justifications

Overall Process:

A 3-stage amplifier was chosen to achieve the gain of 50 while having $R_{in} \geq 20$ kΩ. The design involves 2 CE (common emitter) stages and 1 CC (common cathode/emitter follower) stage. To simplify the calculations, I found the square root of 50 (about 7.1) such that when I multiply the gains of stages 1 and 2 if I made them equal to each other and equal to -7.1 each, then the gain would be approximately 50. Since the last stage is a CC, the gain of the third stage will be close to unity and can be approximated to 1. This ensures that the voltage gain can be approximately 50 while both stages 1 and 2 will not impact each other's operating conditions since they have equivalent gains. To begin the rest of the calculations, the testing circuit was simulated in Multisim (**Figure 3**) via DC sweep to create the characteristic graph. A load line was manually created, and a low collector current of 400 μA was chosen for both CEs because of the small power supply current restriction. This was also performed for the CC stage as well. From the graphs, an operating point (quiescent) was selected and became the starting point for the manual calculations (see appendix). The calculations started from the last stage (CC) and went backwards to the first stage. Since the load (R_L) was required to be 1 kΩ, the CC emitter resistor was chosen so there is no significant change when R_L is either added or removed. From here the input resistance of the CC was calculated and used in the calculations of CE stage 2 (this is the backwards process of going from stage 3 towards stage 1). The biasing resistors for each step were found by assuming 1 of them to be large enough such that the divider current is significantly larger than the base current, and then applying KCL at the node to solve for the other resistor. The base current, voltage and DC operating point current from the graphs were used in this KCL calculation. Since the gain of stage 1 and stage 2 were made to be equivalent, the same calculation procedure was repeated in stage 1 using the input resistance of the second stage. As a result, the final circuit design was contracted with 2 cascading CEs, followed by a CC amplifier.

Resistors:

The resistors were selected for a variety of reasons depending on the location. Firstly, the emitter and collector resistors were calculated based on the current and the next stage input resistance. The assumed resistance of $R_{E5} = 1$ kΩ (emitter resistor of CC stage) was chosen to not significantly impact the loading effect on the circuit when the load is included or removed. Secondly, the emitter degeneration resistors were chosen based on the required gain for each stage. This was done by rearranging for R_E (total required emitter resistance) from the gain equation, as it was equal to the parallel combination of the emitter resistor and emitter degeneration resistor. Lastly, the remaining biasing resistors were chosen to be as large as possible while maintaining enough current. If the biasing resistors were too small, the input resistance decreases significantly, resulting in a large loading impact on the circuit.

Capacitors:

All of the capacitors were initially based on assumptions and then verified via calculations (view appendix for all manual calculations). Based on the operational frequency and

location, the values of the capacitors would change accordingly. C_1, C_3, and C_5 were all 10 µF because for coupling capacitors in between amplifier stages because the input resistances of the stages are relatively large so it would need a significant change in resistance to drastically change the overall circuit characteristic. Whereas, C_2, C_4, and C_6 were all 100 µF because they are connected to the emitter degeneration resistors. This helps ensure that resistance does not get changed drastically because small changes involving the emitter degeneration resistor can have a large effect on the gain, hence why a large capacitance is needed.

Circuit Under Test

Figure 4 below showcases the final design of the 3-stage BJT amplifier that will be simulated via Multisim. The circuit consists of 3, 2N3904 BJTs (Q_1, Q_2, Q_3), 14 resistors and 6 electrolytic capacitors. The V_{CC} power source is 10 V, which is driven by the sinusoidal signal source V_s. **Figure 5** is the schematic equivalent of Figure 4 constructed in Multisim for experimental testing.

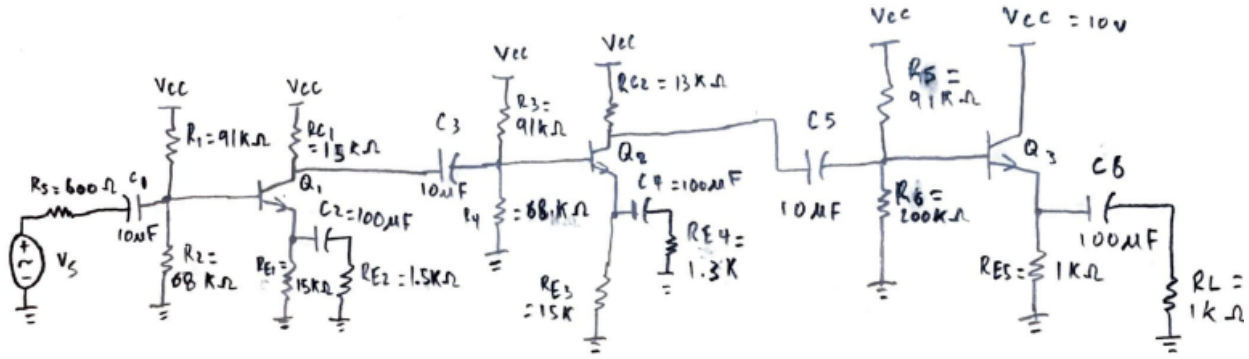

Figure 5. The constructed circuit in Multisim of **Figure 4**

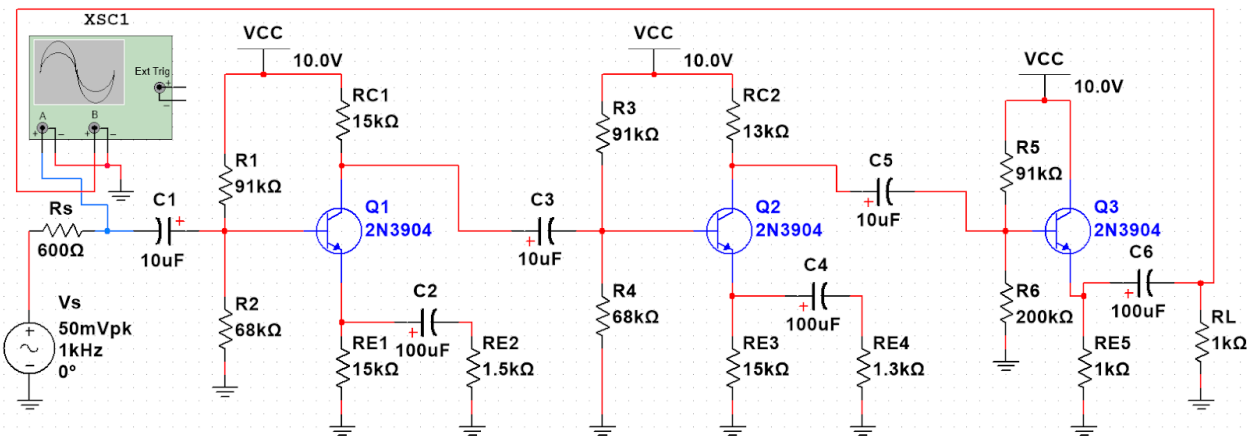

Figure 5. The constructed circuit in Multisim of **Figure 4**

Experimental Results

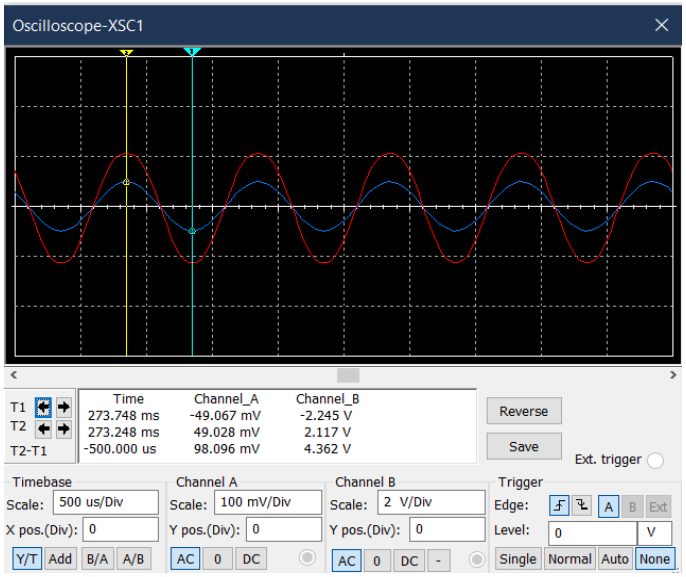

Figure E1. The waveform of input voltage and output voltage of **Figure 5** (R_L = 1 kΩ)

$V_{I,\,P\text{-}P}$ [mV]	$V_{O,\,P\text{-}P}$ [V]	A_{VO} [V/V]
98.096	4.362	44.467

Table E1. V_I, V_O, A_V (loaded voltage gain) → R_L = 1 kΩ, f = 1 kHz

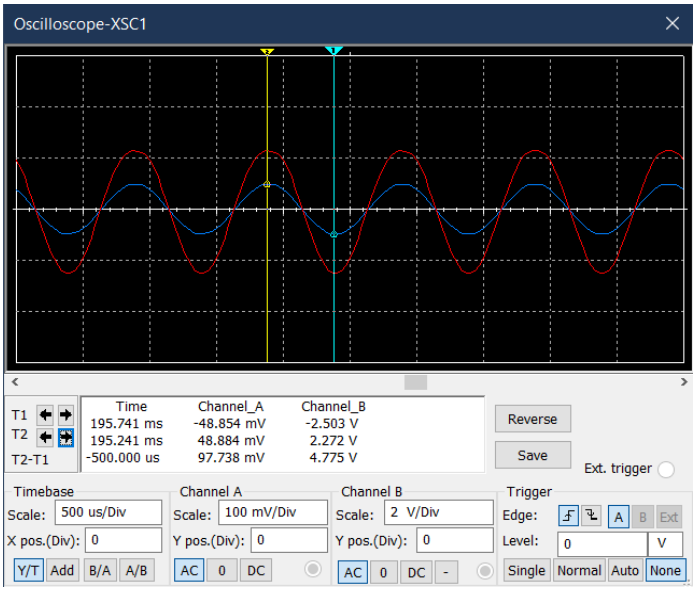

Figure E2. The waveform of input voltage and output voltage of **Figure 5** (R_L = ∞)

$V_{I,\,P\text{-}P}$ [mV]	$V_{O,\,P\text{-}P}$ [V]	A_{VO} [V/V]
97.738	4.775	48.855

Table E2. V_I, V_O, A_{VO} (no load voltage gain) → R_L = ∞, f = 1 kHz

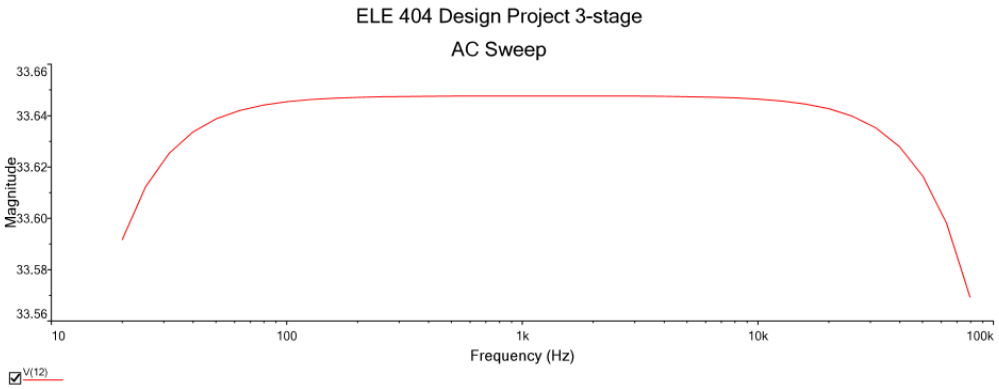

Figure E3. The frequency response graph of **Figure 5**

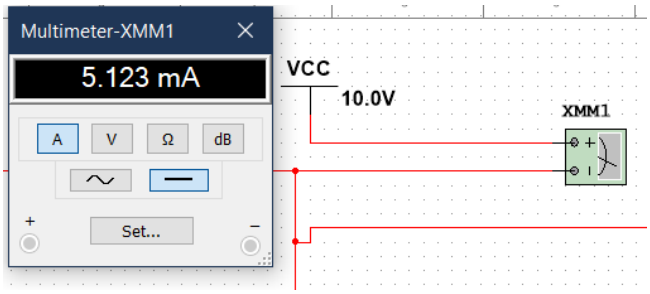

Figure E4. The quiescent current that is drawn from the power supply

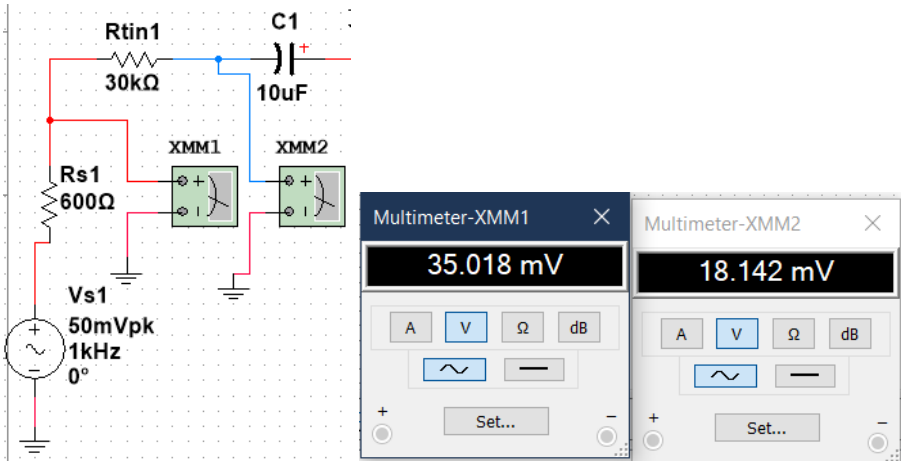

Figure E5. Finding V_t and V_i with new $R_{t,\,in}$

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

$R_{i,\,Calculated}$ [kΩ]	$R_{t,\,in}$ [kΩ]	V_t [Vrms]	V_i [Vrms]	R_i [kΩ]
31.195	30	35.018 mV	18.142 mV	32.251

Table E3. Parameters of the equation used to find input resistance (R_i)

Conclusion and Final Remarks

$$e\% = \frac{calculated\ value - measured\ value}{measured\ value} \times 100$$

Specification	Calculated Value	Tested Value	Achieved	% Error
Quiescent current: no larger than 10 mA;	5.23 mA	5.123 mA (this is < 10 mA)	**Yes**	2.09 %
|Avo| = 50 (± 10%);	50.41	48.855	**Yes**	3.18 %
Maximum no-load output voltage swing	8 V	4.775 V_{P-P}	**Not achieved**	59.69 %
Loaded voltage gain: **no smaller than 90% of Avo**	47.57	44.467 (91.018%> 90%)	**Yes**	6.98 %
Maximum loaded output voltage swing	4 V	4.362 V_{P-P}	**Yes**	8.30 %
Input resistance: **no smaller than 20 kΩ**;	31.195 kΩ	32.251 kΩ	**Yes**	3.27 %
Frequency response: **20 Hz to 50 kHz**;	N/A	(View **Figure E3.**)	**Yes**	N/A

Table C1. Assessing the design specifications

All of the required specifications for the design were met with small errors of less than 10%, except for the no-load voltage swing. Although the manual calculations indicated that this would be feasible, the Multisim simulation demonstrates this is not the case. This minor error is likely due to biasing or possibly the choice of the operating point from the load line graphs. Ultimately, even with this slight error, it did not negatively impact the characteristics of the circuit as all the other crucial specifications were met including the voltage gain, input resistance and frequency response (**Figure E3**). The minimal percent errors for the other measurements are likely due to rounding in manual calculations, and any assumptions made from the load line graphs. Therefore, the 3-stage (CE-CE-CC) was an effective design choice to achieve the objectives of this project, and everything including the manual calculations and the experimentation Multisim was a success.

Appendix: Manual Calculations

All manual calculations can be viewed on the pages below.