UNIT 3 Overview of 8086 microprocessor 5 Hrs]

3.1 Features of 8086 microprocessor
3.2 Functional diagram of 8086 microprocessor
3.3 Registers and Flags
3.4 ALP Development Tools: Editor, Assembler and linker

Features of 8086 Microprocessor

- 8086 Microprocessor is an **enhanced version of 8085 Microprocessor** that was designed by Intel in **1976.**

- It is a **16-bit Microprocessor having 20 address lines and 16 data lines** that provides up to **1MB storage**.
- It consists of a powerful **instruction set**, which provides operations like **multiplication and division easily**.
- It supports two **modes of operation, i.e. Maximum mode and Minimum mode**.
- Maximum mode is suitable for system having **multiple processors** and
- Minimum mode is suitable for system having a **single processor**.

- **16-bit Microprocessor**: Processes 16 bits of data simultaneously.
- **Clock Speed**: **Initially 5 MHz, with later models up to 10 MHz.**
- **Memory Addressing**: 20-bit address bus, capable of addressing up to 1 MB of memory.
- **Segmentation**: Divides memory into segments of 64 KB each, improving memory management.
- **Instruction Set**: Rich set of instructions with support for arithmetic, logic, control transfer, string manipulation, etc.

- **Operating Modes**: Operates exclusively in real mode.
- **Pipelining**: Pre-fetches instructions, allowing simultaneous fetching and execution.

- **Hardware Multiplication and Division**: Supports efficient execution of complex mathematical operations.
- **Interrupts**: Supports 256 vectored interrupts for handling various events and exceptions.
- **Compatibility**: Pin-compatible with the 8088 and software-compatible with later x86 processors.

- It has an **instruction queue, which is capable of storing six instruction bytes** from the memory resulting in faster processing.

- It was the **first 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, and 16-bit external data bus** resulting in faster processing.

- It is available in 3 versions based on the frequency of operation −
  - **8086 → 5MHz**
  - **8086-2 → 8MHz**
  - **(c)8086-1 → 10 MHz**

- It uses **two stages of pipelining, i.e. Fetch Stage and Execute Stage, which improves performance.**
- Fetch stage can prefetch up to 6 bytes of instructions and stores them in the queue.
- Execute stage executes these instructions.
- It consists of 29,000 transistors.

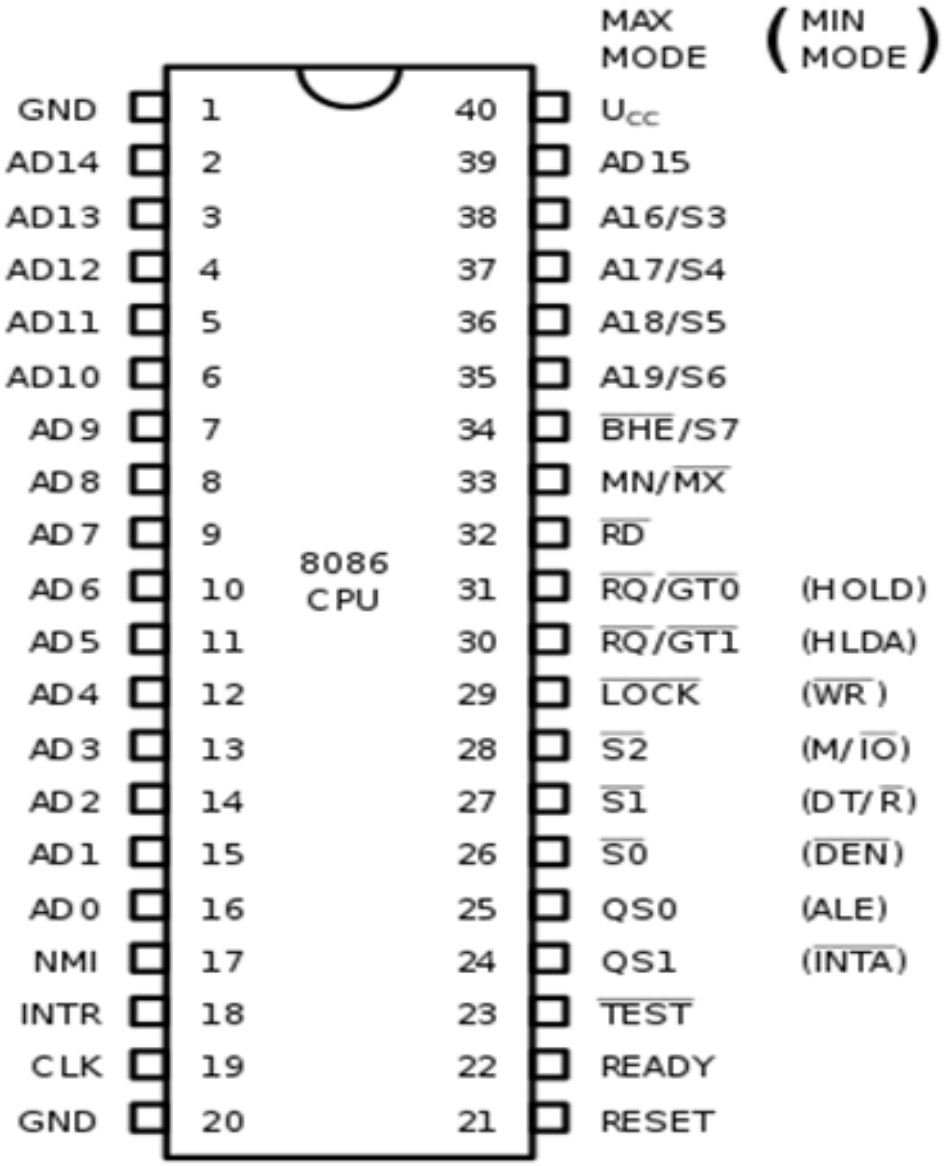
Comparison between 8085 & 8086

8085 Microprocessor	8086 Microprocessor
It is an 8-bit microprocessor.	It is a 16-bit microprocessor.
It has a 16-bit address line.	It has a 20-bit address line.
It has a 8-bit data bus.	It has a 16-bit data bus.
The memory capacity is 64 KB.	The memory capacity is 1 MB.
The Clock speed of this microprocessor is 3 MHz	The Clock speed of this microprocessor varies between 5, 8 and 10 MHz for different versions.
It has five flags.	It has nine flags.

8085 microprocessors do not support memory segmentation.	8086 microprocessor supports memory segmentation.
It does not support pipelining.	It supports pipelining.
It is accumulator-based processor.	It is general purpose register-based processor.
It has no minimum or maximum mode.	It has minimum and maximum modes.
In 8085, only one processor is used.	In 8086, more than one processor is used. An additional external processor can also be employed.
It contains less number of transistors compare to 8086 microprocessor. It contains about 6500 transistor.	It contains more number of transistors compare to 8085 microprocessor. It contains about 29000 in size.
The cost of 8085 is low.	The cost of 8086 is high.

8086 pins configuration

- **AD0-AD15 (Address Data Bus):** PIN 16 15 .. 7 .. 6 5 4 3 2 39 Bidirectional address/data lines. These are low order address bus. They are multiplexed with data.
    - When these lines are used to transmit memory address, the symbol A is used instead of AD, for example, A0- A15.
- **A16 - A19 (Output):** Pin 38 37 36 35 High order address lines. These are multiplexed with status signals.
    - **A16/S3, A17/S4:** A16 and A17 are multiplexed with segment identifier signals S3 and S4.
    - **A18/S5:** A18 is multiplexed with interrupt status S5.
    - **A19/S6:** A19 is multiplexed with status signal S6.



- **BHE/S7 (Output):** Bus High Enable/Status.
  - During T1, it is low.
  - It enables the data onto the most significant half of data bus, D8-D15.
  - 8-bit device connected to upper half of the data bus use BHE signal.
  - It is multiplexed with status signal S7. S7 signal is available during T3 and T4.

    - T1 State (Address State)
    - T2 State (Data Setup State)
    - T3 State (Data Transfer State)
    - T4 State (Idle State)

- **RD (Read):** 32 For read operation.
  - It is an output signal.
  - It is active when LOW.

- **Ready (Input):** 22 The addressed memory or I/O sends acknowledgment through this pin.
    - When HIGH, it denotes that the peripheral is ready to transfer data.

- **RESET (Input):** 21 System reset. The signal is active HIGH.
- **CLK (input):** 19 Clock 5, 8 or 10 MHz.
- **INTR:** 18 Interrupt Request.
- **NMI (Input):** 17 Non-maskable interrupt request.
- **TEST (Input):** 23 Wait for test control.
    - When LOW the microprocessor continues execution otherwise waits.

- **VCC:** 40 Power supply +5V dc.
- **GND:** 20 Ground.

Operating Modes of 8086

There are two operating modes of operation for Intel 8086, namely the

minimum mode

maximum mode.

- When only one 8086 CPU is to be used in a microprocessor system, the 8086 is used in the **Minimum mode** of operation.
- In a multiprocessor system 8086 operates in Maximum **mode**.

Pin Description for Minimum Mode

- In this minimum mode of operation, the pin MN/MX 33 is connected to 5V D.C. supply i.e. MN/MX = VCC.

- **The description about the pins from 24 to 31 for the minimum mode is as follows:**

- **INTA (Output):** Pin number 24 interrupts acknowledgement.
    - On receiving interrupt signal, the processor issues an interrupt acknowledgment signal.
    - It is active LOW.

- **ALE (Output):** Pin no. 25. Address latch enable.
    - It goes HIGH during T1.

- The microprocessor 8086 sends this signal to latch the address into the Intel 8282/8283 latch.

- **DEN (Output):** Pin no. 26. Data Enable.
  - When Intel 8287/8286 octal bus transceiver is used this signal.
  - It is active LOW.

- **DT/R (output):** Pin No. 27 data Transmit/Receives.
  - When Intel 8287/8286 octal bus transceiver is used this signal controls the direction of data flow through the transceiver.
  - When it is HIGH, data is sent out.
  - When it is LOW, data is received.

- **M/IO (Output):** Pin no. 28, Memory or I/O access.
  - When this signal is HIGH, the CPU wants to access memory.
  - When this signal is LOW, the CPU wants to access I/O device.

- **WR (Output):** Pin no. 29, Write.
  - When this signal is LOW, the CPU performs memory or I/O write operation.

- **HLDA (Output):** Pin no. 30, Hold Acknowledgment.
  - It is sent by the processor when it receives HOLD signal.
  - It is active HIGH signal.
  - When HOLD is removed HLDA goes LOW.

- **HOLD (Input):** Pin no. 31, Hold.
  - When another device in microcomputer system wants to use the address and data bus, it sends HOLD request to CPU through this pin.
  - It is an active HIGH signal.

Pin Description for Maximum Mode

- In the maximum mode of operation, the pin **MN/MX'** is made LOW.
- It is grounded.
- The description about the pins from 24 to 31 is as follows:

- **QS1, QS0 (Output):** Pin numbers 24, 25, Instruction Queue Status. Logics are given below:

QS1	QS0	Operation
0	0	No operation
0	1	1st byte of opcode from queue.
1	0	Empty the queue
1	1	Subsequent byte from queue

- **S0, S1, S2 (Output):** Pin numbers 26, 27, 28 Status Signals.
  - These signals are connected to the bus controller of Intel 8288.
  - This bus controller generates memory and I/O access control signals.
  - Logics for status signal are given below:

S2	S1	S0	Operation
0	0	0	Interrupt acknowledgement
0	0	1	Read data from I/O port
0	1	0	Write data from I/O port
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive state

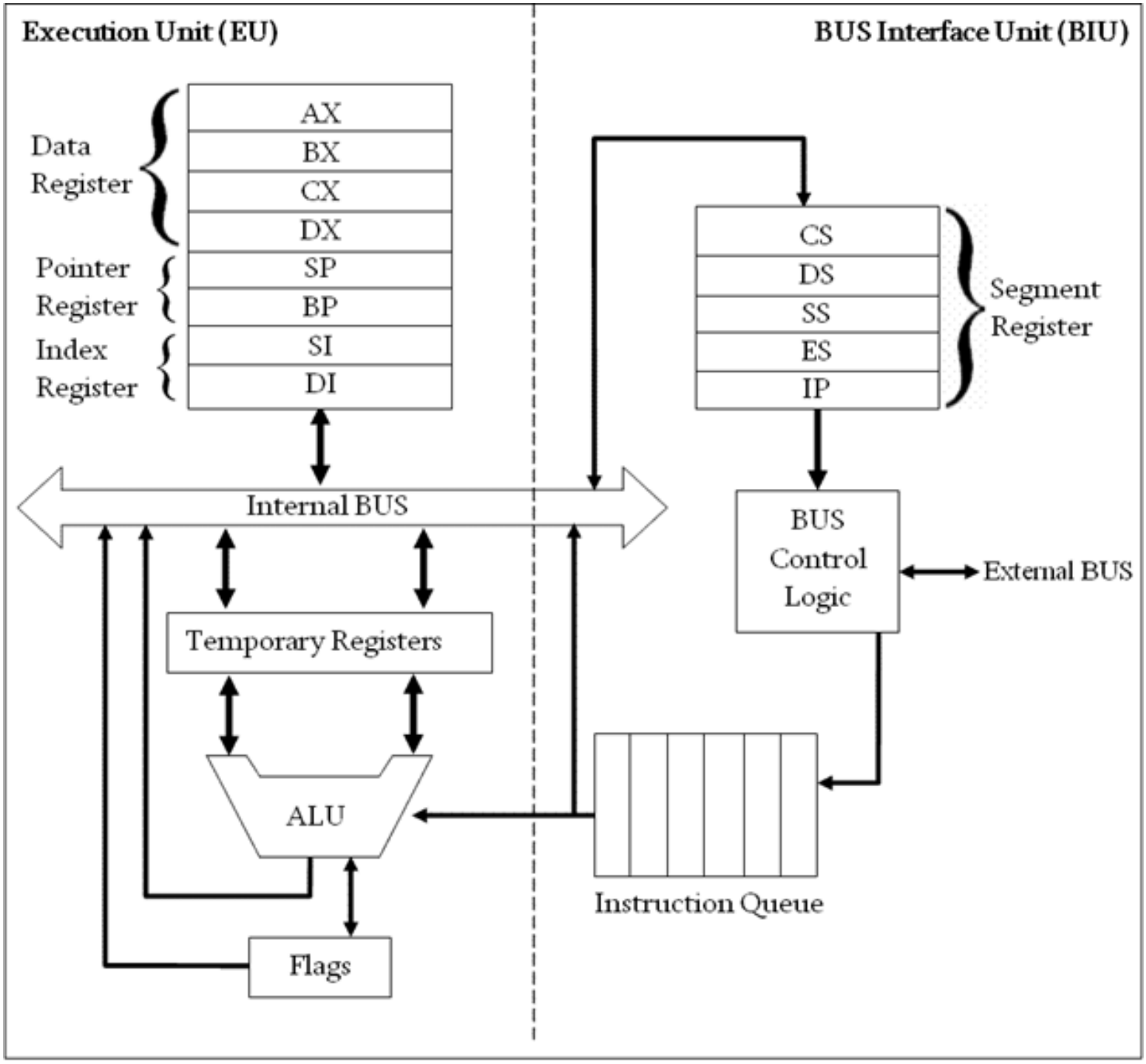
- **LOCK (Output):** Pin no. 29.
  - It is an active LOW signal.
  - When this signal is LOW, all interrupts are masked and no HOLD request is granted.
  - In a multiprocessor system all other processors are informed through this signal that they should not ask the CPU for relinquishing the bus control.

- **RG/GT1, RQ/GT0 (Bidirectional)**: Pin numbers 30, 31,
  - Local Bus Priority Control. Other processors ask the CPU by these lines to release the local bus.

In the maximum mode of operation signals WR, ALE, DEN, DT/R etc. are not available directly from the processor. These signals are available from the controller 8288.

Functional Diagram of 8086 Microprocessor

- **Bus Interface Unit (BIU)**:
  - **Segment Registers**: CS, DS, SS, ES
  - **Instruction Queue**: Pre-fetches instructions to improve performance.
  - **Instruction Pointer (IP)**: Holds the address of the next instruction to be executed.
  - **Address Generation**: Computes physical addresses from segment pairs.
- **Execution Unit (EU)**:
  - **Arithmetic Logic Unit (ALU)**: Performs arithmetic and logical operations.
  - **General Purpose Registers**: AX, BX, CX, DX
  - **Pointer and Index Registers**: SP, BP, SI, DI
  - **Flags Register**: Status and control flags.
  - **Control Unit**: Decodes and executes instructions.


Execution Unit (EU)
BUS Interface Unit (BIU)
Data Register
AX
BX
CX
DX
Pointer Register
SP
BP
Index Register
SI
DI
CS
DS
SS
ES
IP
Segment Register
Internal BUS
BUS Control Logic
External BUS
Temporary Registers
ALU
Instruction Queue
Flags