Course Title: **Computer Architecture and Organization Program: BICTE**
Course No. : ICT. Ed. 436 Nature of course: Theoretical + Practical
Level: Bachelor. Credit Hour: 3 hours (2T+1P)
Semester: Third Teaching Hour: 64 hours (32+32)

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1. Course Description

This course is an introduction to Computer Architecture and its Organization. It covers topics in physical design of the computer (i.e. computer organization). This course discusses the basic structure of a digital computer and deals with the detail study of data representation in computer system, Register transfer language and microoperations, and organization of the Control unit, the Arithmetic and Logic unit, the Memory unit and the I/O unit.

2. General Objectives

The general objectives of this course are as follows:

- To provide the students with the knowledge of data representation, register transfer language and microoperations
- To provide the organization and designing concept of computer system including processor, computer arithmetic, memory organization and I/O organization.
- To discuss in detail, the operation of the arithmetic unit including the algorithm to add, subtract and multiply signed magnitude data and signed 2's complement data.
- To study the multiprocessors and pipelining.
- To study the different ways of communicating with I/O devices and standard I/O interfaces

3. Course Outlines:

Specific Objectives	Contents	LH
• Explain different data types representation • Define the requirement of complement numbers	**Unit 1: Data Representation** 1.1 Data Types 1.2 Complements 1.3 Fixed Point Representation 1.4 Floating Point Representation **<u>Practical Works</u>** **1.1 Computer Program:** Write program to visualize the representation of complement numbers, integers, floating point numbers and character data, overflow detection while adding integers.	**4**
• Explain register transfer language • Apply different microoperations to perform specific task	**Unit 2: Register Transfer and Microoperations** 2.1 Register and Register Transfer Language 2.2 Bus and Memory Transfers 2.3 Arithmetic, Logic and Shift Micro-operations 2.4 Arithmetic Logic Shift Unit	**8**

• Explain instruction codes • Describe instruction format and instruction cycle • Design component organization in basic computer.	**Unit 3: Basic Computer Organization and Design** 3.1 Instruction Codes 3.2 Computer Registers 3.3 Computer Instructions 3.4 Timing and Control 3.5 Instruction Cycle 3.6 Input Output and Interrupt **Practical Works** **3.1 Circuit Design:** Design of Basic Computer 3.2 **Computer Program:** Write program to illustrate fetch, decode and execute instructions.	**8**
• Describe control memory and its usage • Apply address sequencing concept • Identify microinstruction format	**Unit 4: Microprogrammed Control** 4.1 Control Memory 4.2 Address Sequencing 4.3 Computer Configuration 4.4 Microinstruction Format	**6**
• Explain different CPU organizations • Describe the requirement of different instruction formats • Understand and apply addressing modes	**Unit 5: Central Processing Unit** 5.1 CPU Organizations 5.2 Instruction Formats 5.3 Addressing Modes **Practical Works** **5.1 Computer Program:** Write program to illustrate the use of different addressing modes.	**6**
• Define different types of computers • Explain pipelining • Utilizing different types of pipelining to improve performance • Understand pipeline hazards and suggest their solutions	**Unit 6: Pipelining** 6.1 Parallel Processing, Flynn's Classification of Computers 6.2 Pipelining 6.3 Arithmetic Pipeline 6.4 Instruction Pipeline 6.5 Pipeline Hazards and their Solutions 6.6 Array and Vector Processing **Practical Works** 6.1 **Case Study**: Available array and vector processors and their application domain 6.2 **Computer Program**: write program which simulates instruction pipeline and arithmetic pipeline.	**8**
• Demonstrate the addition and subtraction of signed magnitude	**Unit 7: Computer Arithmetic** 7.1 Addition and Subtraction of Signed Magnitude Data	**8**

data and signed 2's complement data • Trace Multiplication algorithms to multiply signed magnitude and signed 2's complement data.	7.2 Addition and Subtraction of Signed 2's Complement Data 7.3 Multiplication of Signed Magnitude Data 7.4 Multiplication of Signed 2's Complement Data **Practical Works** 7.1 **Computer Program:** Implement all algorithms learned in this chapter in high level language.	
• Explain I/O interface, async. data transfer, modes of transfer • Demonstrate interrupt handling and DMA transfer • Identify the need of IOP	**Unit 8: Input and Output Organization** 8.1 I/O Interface 8.2 Asynchronous Data Transfer 8.3 Modes of Transfer 8.4 Priority Interrupt 8.5 Direct Memory Access 8.6 I/O Processor **Practical Works** **8.1 Case Study:** USB (universal serial bus)	**6**
• Describe the concept of memory hierarchy • Explain associative memory organization and cache mapping techniques	**Unit 9: Memory Organization** 9.1 Memory Hierarchy 9.2 Main Memory 9.3 Associative Memory 9.4 Cache Memory **Practical Works** 9.1 **Computer Program**: write program to simulate associative memory (key value pair mapping) implementation.	**5**
• Specify the use of multiprocessor • Demonstrate interconnection structures of processors and IPC • Identify cache coherence problem with its solution	**Unit 10: Multiprocessors** 10.1 Characteristics of Multiprocessor 10.2 Interconnection Structures 10.3 Inter Processor Communication and Synchronization 10.4 Cache Coherence **Practical Works** 10.1 **Computer Program**: write program to simulate cache coherence problem and its solution.	**5**

6 Instructional Techniques

The instructional techniques for this course are divided into two groups. First group consists of general instructional techniques applicable to most of the units. The second group consists of specific instructional techniques applicable to particular units.

4.1 General Techniques

Reading materials will be provided to students in each unit. Lecture, Discussion, use of multi-media projector, brain storming are used in all units.

4.2 Specific Instructional Techniques

Demonstration is an essential instructional technique for all units in this course during teaching learning process. Specifically, demonstration with practical works will be specific instructional technique in this course. The details of suggested instructional techniques are presented below:

Unit 2 and 4: Lecture, Discussion

Unit 1, 3, 5, 6, 7, 8, 9 and 10 : Lecture, Discussion, Practical

7 Evaluation

Evaluation of students' performance is divided into parts: Internal assessment (theory and practical and internal external examinations (theory and practical). The distribution of points is given below:

Internal Assessment Theory	Internal Assessment Practical	Semester Examination (Theoretical exam)	External Practical Exam/Viva	Total Points
25 Points	15 Points	40 Points	20 Points	100 Points

***Note**: Students must pass separately in internal assessment, external practical exam and semester examination.*

7.1 Internal Assessment (25 Points) of Theoretical Part

Internal assessment will be conducted by subject teacher based on following criteria:

Attendance and learning Activities	5 points
First assignment (Written assignment)	5 points
Second assignment (Project work with presentation)	10 points
Third assignment/written examination	5 point
Total	25 points

7.2 Internal Assessment (15 Points) of practical part

Internal practical assessment will be conducted by subject teacher based on following criteria:

Attendance and learning Activities	5 points
Practical work/project work/lab work	10 points
Total	15 points

7.3 Semester Final Examination (40 Points) theoretical part

Examination Division, Dean office will conduct final examination at the end of semester.

Objective question (Multiple choice questions 10 x 1 point)	10 Points
Subjective questions (6 questions x 5 marks with ‘OR” two questions)	30 Points
Total	40 points

7.4 **Practical Exam/Viva (20 Points)**

Examination Division, Office of the Dean will appoint an external examiner (ICT teachers working another campus) for conducting practical examination

Items	Points
Evaluation of Record Book	4
Project work/practical work presentation/skill test	10
Viva	6
Total	20

8 Recommended books and References materials (including relevant published articles in national and international journals)

Recommended books:

1. Mano, M. M. (2003), *Computer System Architecture*, (3rd Ed.), Prentice Hall of India.
2. Stalling, W. (2016), *Computer Organization and Architecture: designing for performance* (10th Ed.), Pearson Education.
3. Tanenbaum, A.S. (2013), *Structured Computer Organization*, (6th Ed.), Pearson Education.