Contents

[Day 1: Basics of NMOS (drain current Ids vs drain to source voltage Vds) 2](#_Toc93963308)

[Why do we need SPICE simulation? 2](#_Toc93963309)

[SPICE simulation of std cell. 3](#_Toc93963310)

[Study of Nmos transistor: 4](#_Toc93963311)

[Surface inversion and VT 5](#_Toc93963312)

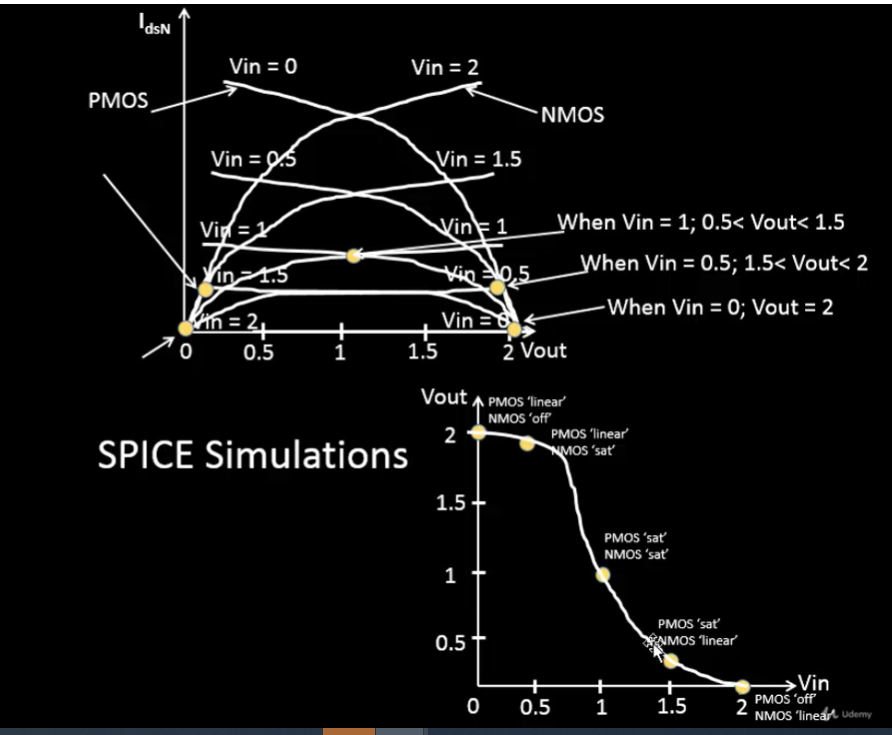
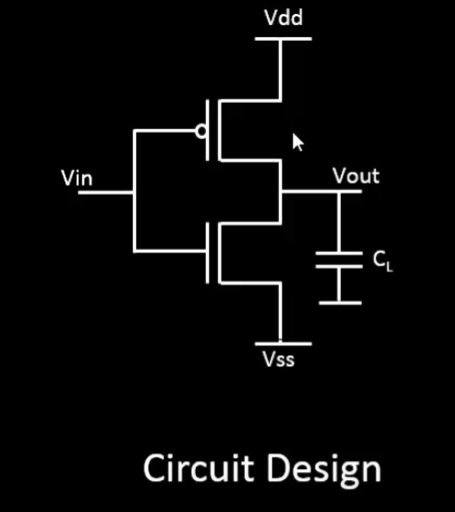
[Impact of Vsb on VT 6](#_Toc93963313)

# Day 1: Basics of NMOS (drain current Ids vs drain to source voltage Vds)

## Why do we need SPICE simulation?

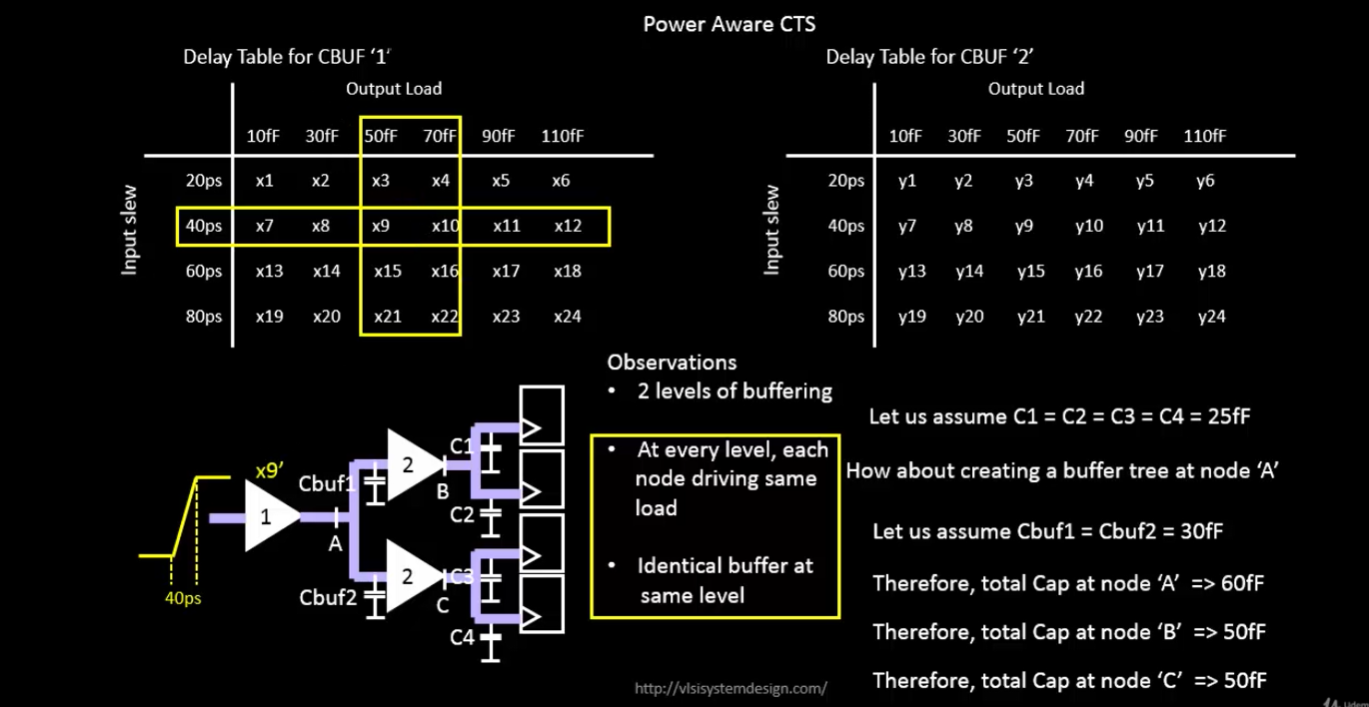
Study of P mos and-n mos transistor characteristic

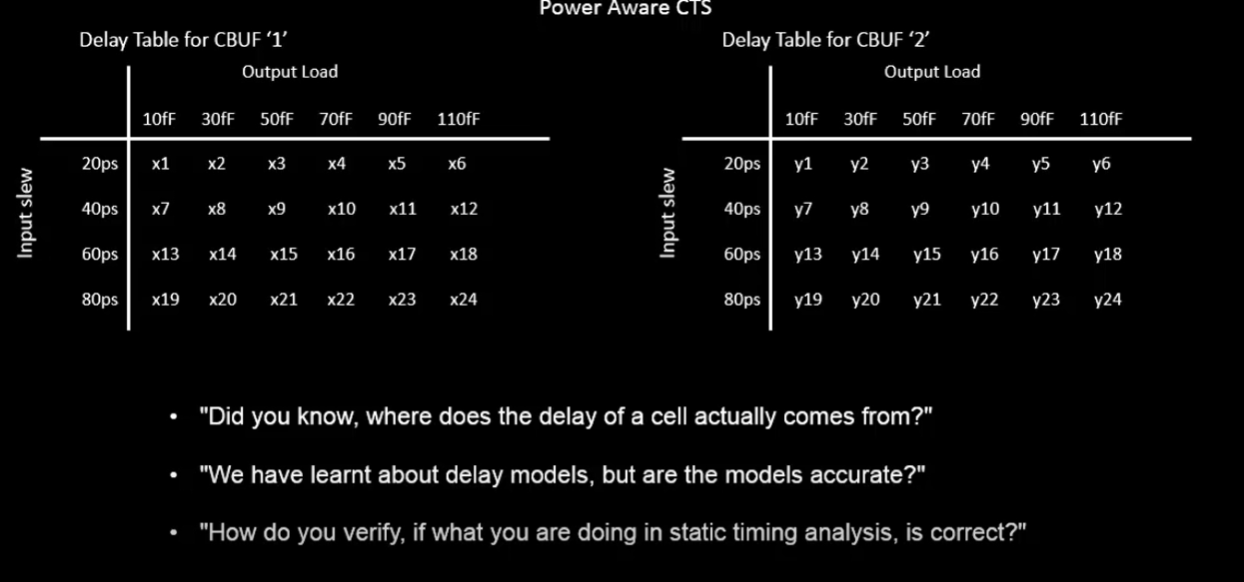
* Voltage to Idsat graph.
* How leakage peaks during switching



## SPICE simulation of std cell.

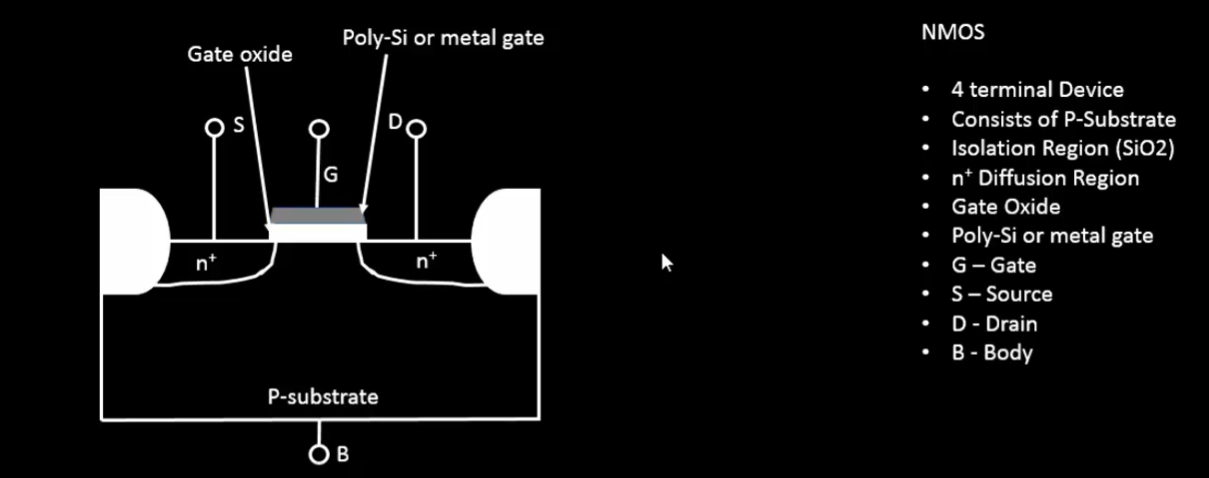
* Why do we need it?
* All STA is built on SPICE simulation of fundamental devices in the std cell circuit.
  + Simulation helps to come up with the delay table calculation
  + The table contains Slew (rate of input change) vs output load
  + Depending upon different situation of the cell placement, the delays can be ‘looked-up’ on the table
  + If the table element doesn’t exists, then the value is extrapolated.
  + The source of these tables comes from spice simulation.



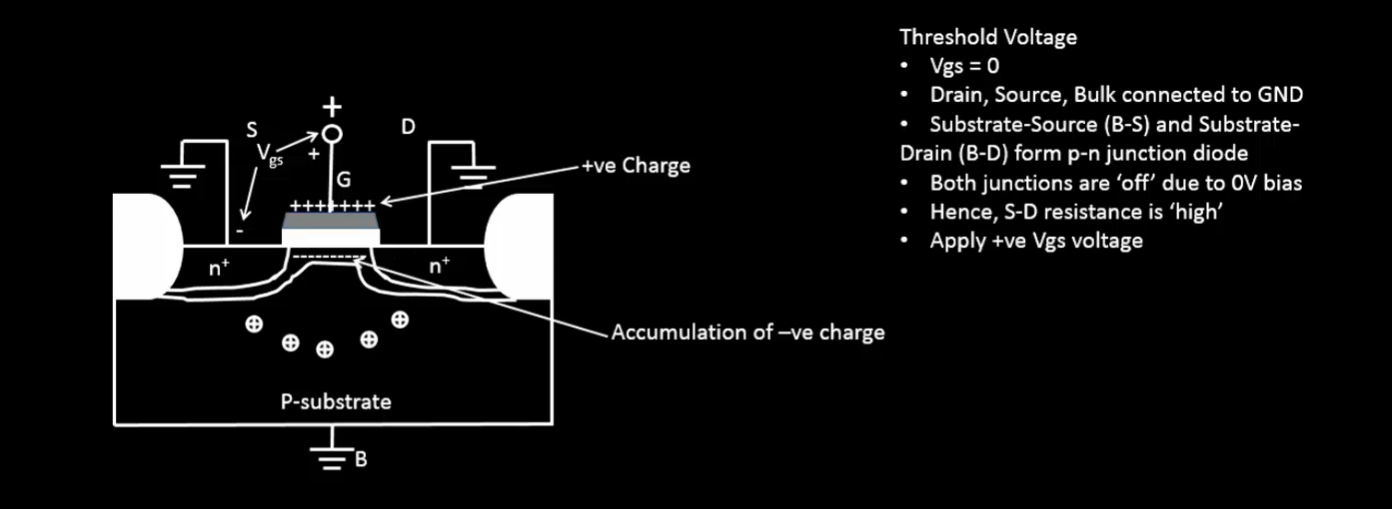


## Study of Nmos transistor:

* Nmos are isolated at the edge
* Bulk (psub) is tied to ground
* Gate is the most important control

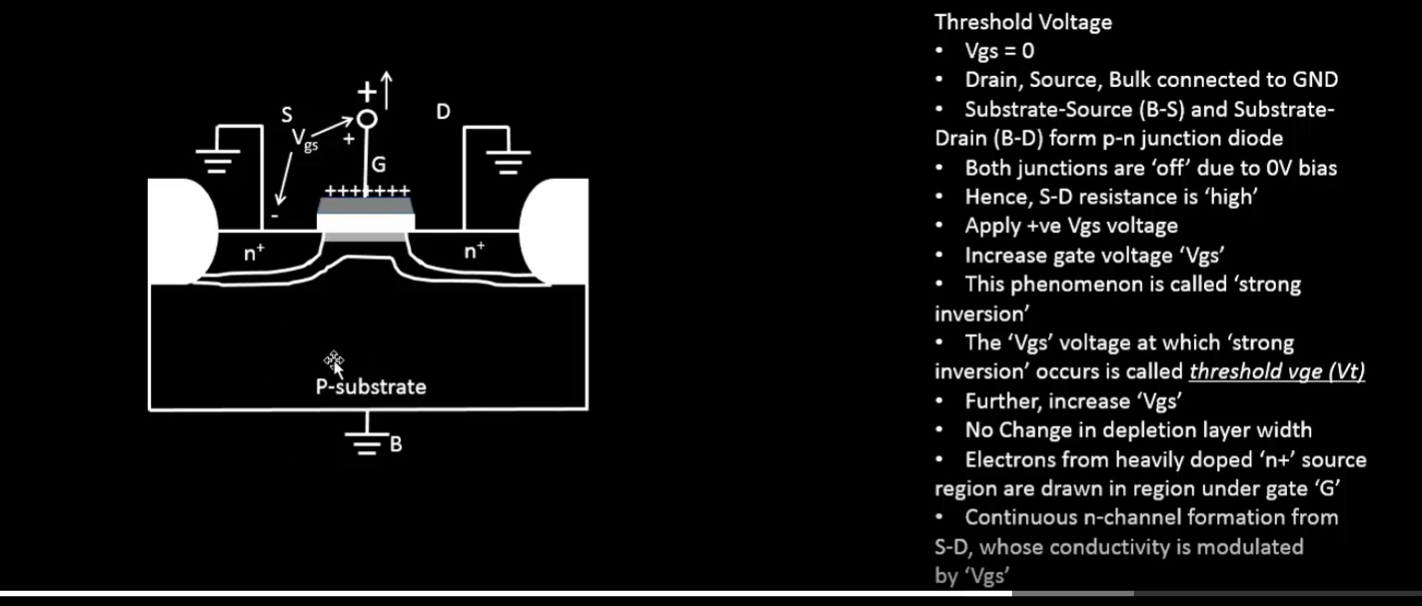


* Applying voltage to Gate (Vgs)
* It builds a positive charge over the oxide cap plate.
* Which builds negative charge in the channel region

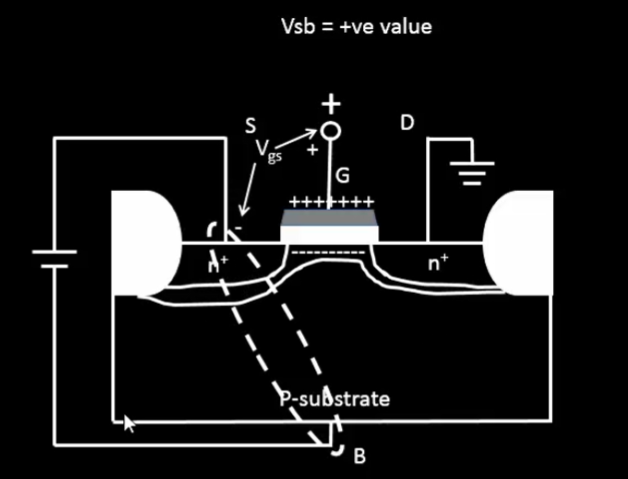


## Surface inversion and VT

* When the voltage applied is steadily increased, it leads to greater accumulation of negative dchange in the channel,
* In a P-substrate, there is a region created of negative change, and thus called inversion region.
* When inversion is at its highest, it’s called threshold voltage.



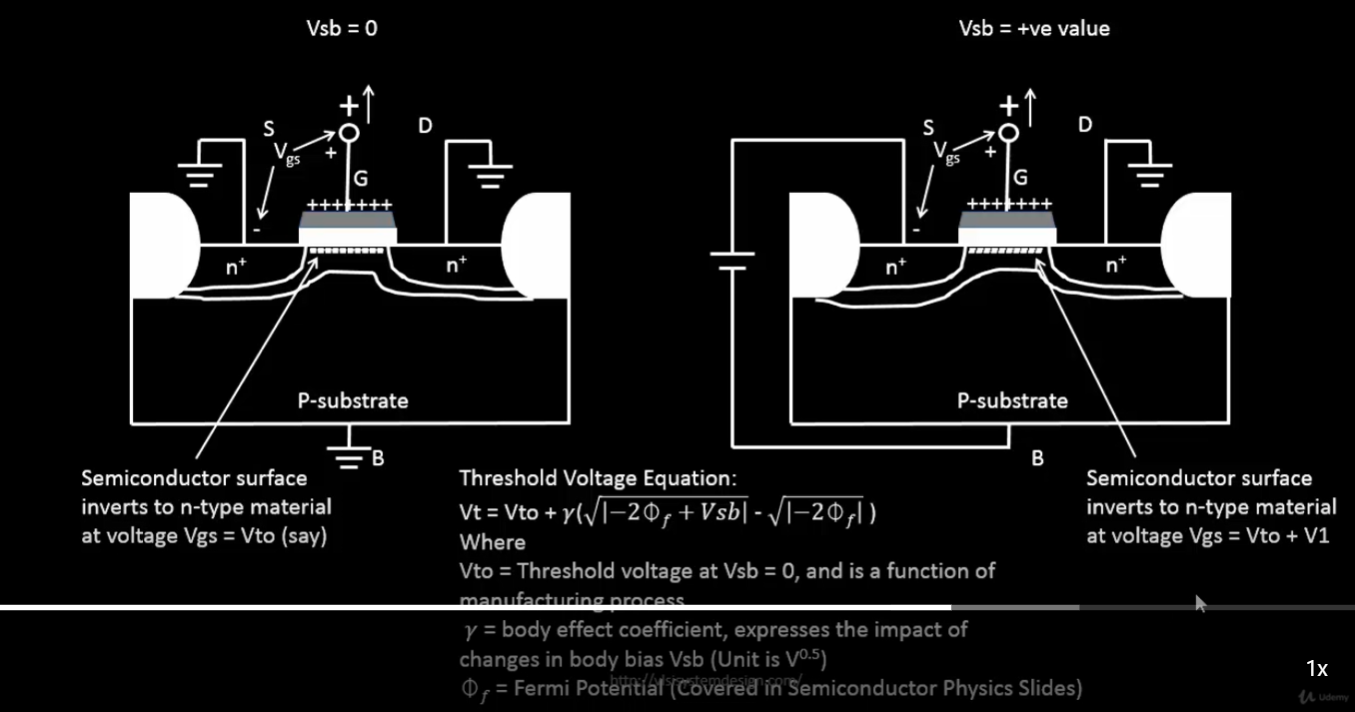
* Once the majority positive charge is repelled from the channel at VT, further negative charges are absorbed from the N+ region
* This forms the continus channel

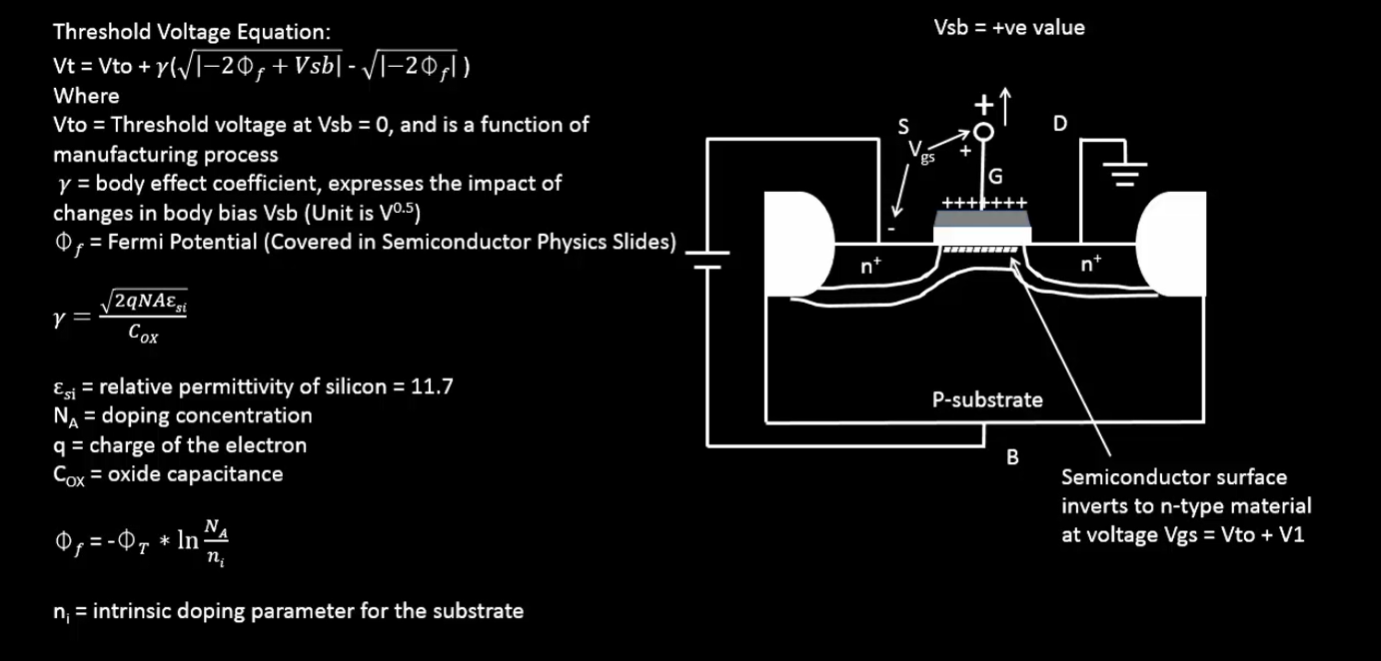


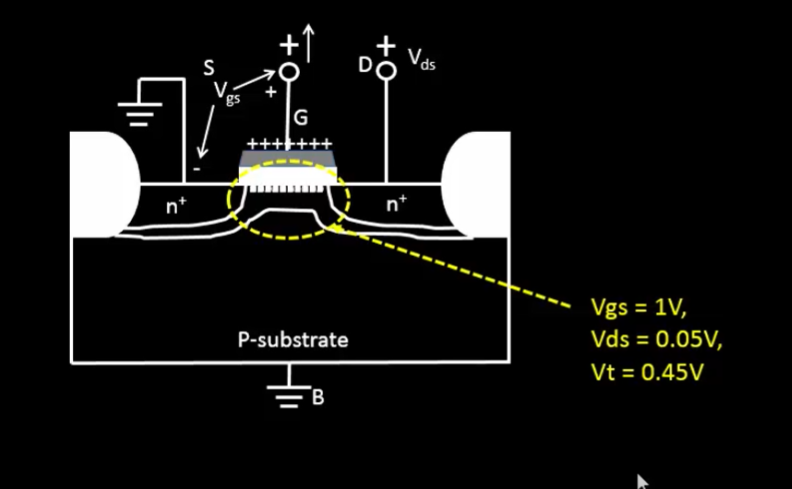
* Applying potential between Source and Substrate makes the diode more reverse biased
* This increases the channel width near source and substrate

## Impact of Vsb on VT

* In the presence of Vsb, additional voltage V1 is required to create the inversion region Vto+V1
* When Vds < Vgs -Vt device behave differently







* Voltage is not constant across the channel. There is a gradient
* From 0 to Vds

