Hybrid integrators for analog computers

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***Abstract*—Integrators have a wide range of applications in analog signal processing, e. g. in filters, $\Delta\Sigma$-modulators and analog computers. With decreasing supply voltage, integrators reach saturation earlier, which reduces the dynamic range. Better noise characteristics and logarithmic signal compression can help preserve small signals. When integrators are concatenated in analog computers, for example when differential equation systems are calculated or in $\Delta\Sigma$-modulators, scaling is a critical issue. Therefore, methods are sought that allow an extension of the dynamic range while maintaining high linearity.**

With hybrid integrators, the dynamic range can be extended by a multiple of the supply voltage range. The basic principle of hybrid integrators is the digital counting of an analog range overflow. This overflow is detected with comparators before the integrator goes into saturation. There are now various ways in which the analog signal level can be reduced after the analog overflow has been digitally detected.

In this paper, a new concept for a hybrid integrator is presented, which uses a continuous-time reset and still provides an exact analog and digital representation of the hybrid integral at all times. This method makes the new concept universally applicable in analog computer systems.

***Index Terms*—hybrid, integrator, analog, scaling, computer**

I. Introduction

Analog integrators are a fundamental component in numerous electronic circuits and systems. Electronic integrators are operated not only in the small-signal range, such as in filters and RF circuits, but also in the large-signal range. Applications for integrators in the large signal range are analog computers [1] and integrators in time-continuous $\Delta\Sigma$-ADCs [2], meanwhile also in robust analog control systems [3]. The topology of continuous-time $\Delta\Sigma$-ADCs is influenced not only by the desired noise shaping, but also significantly by the scaling [2]. When using the integrators in analog computers, analog control systems or CT-$\Delta\Sigma$-modulators overdriving of the integrators must be avoided. This is generally achieved by scaling the integrators appropriately by adjusting the time constant of the integrators to the signal amplitudes. If this is not done the dynamic range cannot be used optimally for small signal amplitudes, and the integrator is overdriven for large signal amplitudes.

Fig. 1 shows the output signals of a hybrid integrator. The curve is shown in red if the voltage over time exceeds a reference level in the analog computer, the so-called machine unit (MU), and in blue the desired curve for a hybrid integrator.

In a hybrid integrator, when a defined threshold is reached that is well below the supply voltage, the integrator is fully or partially reset and a parallel digital register is incremented by the value 1, as shown in Fig. 1. The voltage at which the reset is performed can be at the maximum voltage to be processed, the so-called machine unit (MU), or smaller, e.g. at 0.5 MU, for an analog computer. Due to the periodic reset and parallel digital integration, the dynamic range of the integrator is increased to a multiple of the supply voltage.

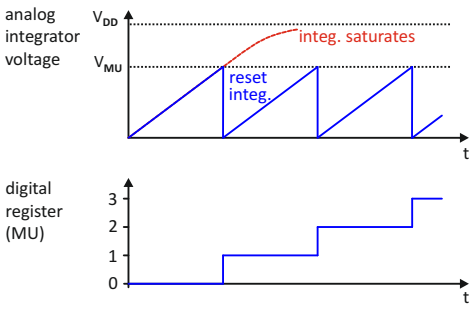

Fig. 1. Analog and digital signals in the hybrid integrator

The resetting of the integrator does not have to be a complete reset, but can also be done partially, by connecting a capacitor with a charge of the correct sign to the input node of the integrator [4]. The comparator level does not have to be at the machine unit (MU), but can also be smaller and have a hysteresis.

The errors that result from the time course of the voltage of the capacitive reset proposed in [4] are certainly problematic.

While in CT-$\Delta\Sigma$-modulators the time response of the DAC feedback pulse can be systematically taken into account [2], the non-ideal voltage response during reset will cause a systematic error, since the step-like digital transition of the digital register of the hybrid integrator is not exactly complementary to the voltage response during capacitive reset of the analog part of the integrator. For this reason, continuous-time compensation of the analog integration process in combination with digital integrator registers was proposed early on.

II. First proposals for hybrid integrators

Early proposals for hybrid integrators assume the use case of an analog computational circuit solving a differential equation, which means that the integrators are arranged in a feedback loop. The feedback makes it possible to consider the overflow of an integrator only in the subsequent integrator stage [5]–[7]. This does not avoid the overflow of the single integrator, but

in the configuration of a loop the overflow of each subsequent integrator is reduced.

A. Hybrid integration basics

The integrator integrates the input variable X over time t with initial value Y_0. T is the time constant of the integrator:

$$Y = Y_0 + \frac{1}{T}\int_0^t X dt \tag{1}$$

In the hybrid integrator, the integration variable X and the integral Y are decomposed into an analog and a digital component:

$$X = X_D + X_A \tag{2}$$

$$Y = Y_D + Y_A \tag{3}$$

Thus, the analog and digital components of X are integrated. The initial values are also divided into analog Y_{0A} and digital Y_{0D} components:

$$Y = Y_{0D} + Y_{0A} + \frac{1}{T}\int_0^t (X_D + X_A) dt \tag{4}$$

The integral over the analog X_A and digital component X_D of X can be decomposed into a sum, an instantaneous term and an integral over time t. The digital component is integrated in multiples of the time interval Δt. The instantaneous value of the integral in the n-th time interval is here:

$$Y = Y_{0D} + Y_{0A} + \frac{1}{T}\left[\sum_{i=1}^{n-1} X_{D,i}\Delta t + X_{D,n-1}\tau + \int_0^t X_A dt\right] \tag{5}$$

Here $X_{D,i}$ is the value of X_D in the i-th time interval [5]. Assuming that the initial values Y_{0D} and Y_{0A} are both 0, Fig. 2 shows the integral of the equation 5. The summand with index $i = 0$ to $n-1$ is the Integral 1 in Fig. 2. The second term $X_{D,n-1}\tau$ is the instantaneous value of the digital integral in the time interval $(n-1)\Delta t$ and $(n-1)\Delta t + \tau$ and denoted Integral 2 in Fig. 2. The third term, the analogous integral, is Integral 3.

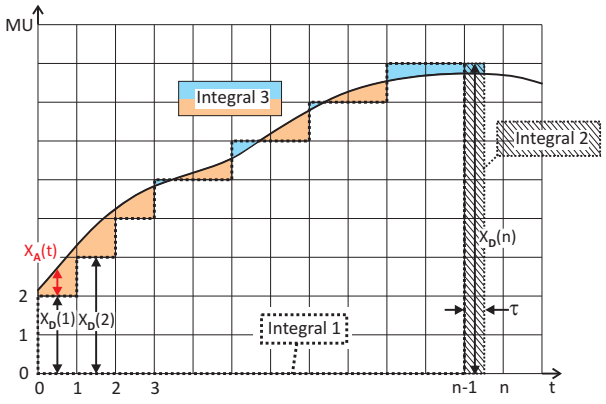

Fig. 2. Hybride integration for analog computer [5]

Fig. 3 shows the block diagram of the hybrid integrator according to [5]. The digital part consists of two registers R1 and R2. The register R1 represents the integral 1. It sums up with each clock, i. e. at each time $n\Delta t$, the value $X_{D,n-1}$ from the register R2 and the change $\Delta X_D = X_{D,n} - X_{D,n-1}$. ΔX_D is generated by a window comparator whose thresholds are $\pm 1/2$ MU (MU, machine unit). The digital value of the integral 1 is DA-converted by DAC1 and then fed to the analog output Y_A of the integrator. Since $Y_A(t)$ is supposed to represent the analog part of the integral without the digital part, the DAC1 gets negative MU as reference for Integral 1.

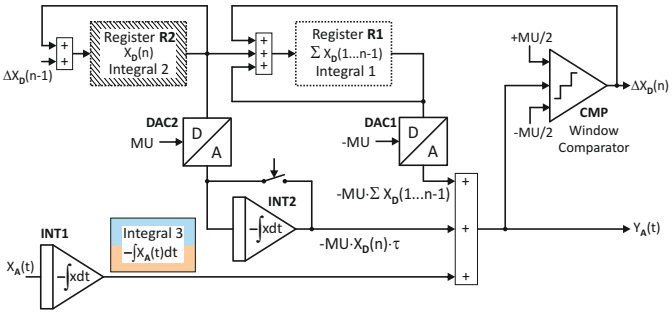

Fig. 3. Hybrid integrator block diagram [5]

The value $X_{D,n-1}$ of the register R2 is given via the DAC1 with MU as reference to an integrator INT2 which is periodically reset at the instants $n\Delta t$. This generates a saw-tooth voltage representing the instantaneous value of the integral 2, that is added to the output Y_A with the summer.

The analog portion of the Integral 3 with input $X_A(t)$ is integrated and added directly to Y_A. Assuming that $X_A(t)$ corresponds to $Y_A(t)$ of the previous integrator stage, and that $Y_A(t)$ is obtained subtracting the digital part of Integral 2, Integral 3 is the color-coded area in Fig. 2. Integral 3 may become positive or negative. If several hybrid integrators are concatenated and fed back, as is the case when solving differential equations in analog computers, the Integral 3 is indirectly minimized in the individual hybrid integrators by keeping $Y_A(t)$ small in amount by subtracting the digital parts of the total integral.

B. Disadvantages of the previous hybrid integrator

From Fig. 3 it can be seen that the hybrid integrator has no local feedback, i. e. if $Y_A(t)$ exceeds $\pm 1/2$ MU, this is added to Integral 1 and the analog output $Y_A(t)$ is reduced in amount accordingly, but the integrator for Integral 3, i. e. the actual analog integrator, is not reduced in amount. The reduction occurs indirectly when the chain of integrators is fed back.

Therefore, the operation and efficiency of the hybrid integrator presented so far is readily demonstrated in [5]–[7] on examples with feedback, i. e., by means of using differential equations such as $\dot{y} = -y$ or $-\ddot{y} = y$. For general applications in analog computing or instrumentation, the previous hybrid integrator does not allow to constrain the actual analog part of the hybrid integrator, because a local feedback on the analog integrator component is missing.

The issue of a hybrid integrator requiring local feedback is addressed in [4]. Here, a partial capacitive reset of the

integrator is performed when a window comparator exceeds its thresholds. The problem here is that the reset does not have an ideal voltage waveform, i. e., the digital portion of the hybrid integrator does not match the complementary analog portion just after the reset signal. While this can be systematically taken into account in CT-$\Delta\Sigma$-modulators by the Laplace transforms of the feedback DAC, and only influences the noise shaping, the non-ideal voltage curve in the switched-capacitor-based reset of the hybrid integrator leads to errors in the result of analog computing circuit.

III. Hybrid Integrator with Local Continuous-Time Reset

Based on [4], a partial reset of the analog integrator is to be realized when the range of the window comparator is exceeded. The reset shall not be realized by a switched capacitance, but by a continuous square wave signal. This reset realized by a rectangular signal shaped negative feedback needs a further compensation later to represent the correct time characteristics of the integrator when the digital part of the hybrid integrator switches.

A. Operating principle of new hybrid integrator

The improved hybrid integrator with local feedback is shown in Fig. 4. The corresponding integrals of the analog and digital parts of the total integral are depicted in Fig. 5. The digital portion of the total integral, Integral 1, is held in register R1. This register sums the digital input X_D and the ΔX_D and represents the digital portion Y_D of the current hybrid value of the integrator.

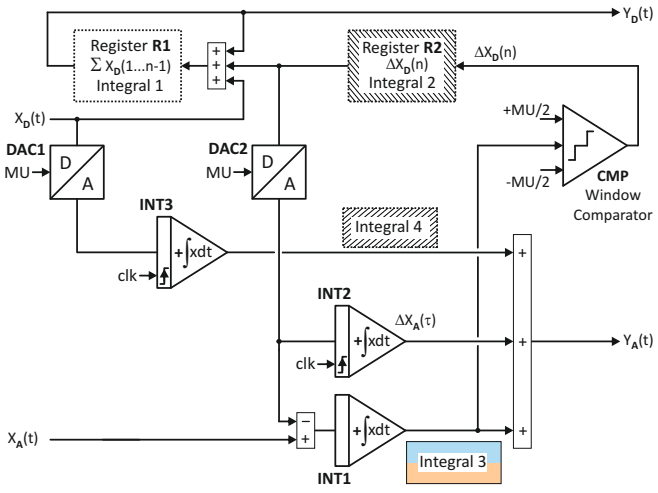

Fig. 4. New hybrid integrator with local feed back

The improved hybrid integrator requires three analog integrators INT1 to INT3, two of which are periodically reset with the clock. The integrator INT1 forms the analog Integral 3. Its output is given to a window comparator, which generates the digital overflow ΔX_D when the thresholds are exceeded, which is then DA-converted with MU as a reference in DAC2 and then negatively fed back to the analog input of the integrator INT1 for Integral 3. Because the window comparator directly measures Integral 3 and there is negative feedback in the case of digital overflow, the improved hybrid integrator achieves a constraint on the analog Integral 3 even without arranging the hybrid integrator in a loop, unlike the solutions in [5]–[7].

The digital overflow leads to a linear characteristic of the reset of the Integral 3. However, because the overflow is not yet stored in the digital output register R1 with the value Integral 1, the linear reset must be compensated with an opposite ramp $\Delta X_A(\tau)$ provided by the analog integrator INT2. This ensures that at each time $Y = Y_A + Y_D$ represents the correct value of the hybrid integral.

If a digital overflow X_D is present at the input of the hybrid integrator, it will only be taken over in the following clocking of the register for Integral 1, and must therefore be DA-converted with DAC1 and then fed to the sum Y_A with the integrator INT3 to obtain the correct total integral Y at any time.

Fig. 5 shows the composition of the integral. Integral 1 is identical to the previously known hybrid integrator. The integral 2 in the improved hybrid integrator no longer has the current analog represented value of $X_D(n) \cdot \tau$, but only the value $\Delta X_D(n) \cdot \tau$, which of course simplifies the scaling of the summation. To obtain the correct instantaneous value for a digital input quantity, the digital input X_D must be integrated analogously and fed to the analog output component $Y_A(t)$. This component corresponds to the integral 4.

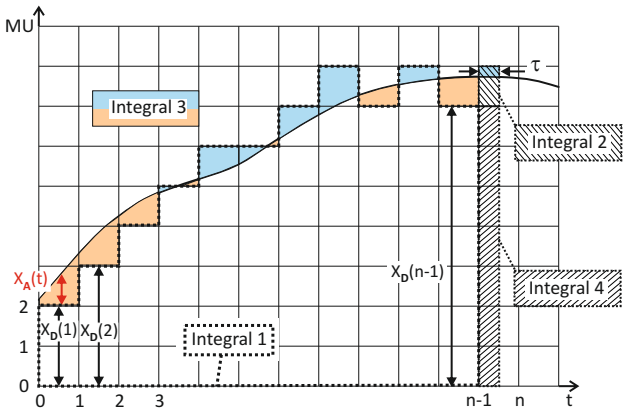

Fig. 5. Composition of integral of new hybrid integrator

B. Application examples and simulation

In the following, we will demonstrate the functionality of the new hybrid integrator using two Matlab Simulink simulations. In the first test case, we apply a constant signal to the analog input and show the internal signal characteristics of the hybrid integrator. In the second test case, we demonstrate the function on the differential equation $-\omega^2 \ddot{y} = y$.

Fig. 6 shows the basic signal characteristics at the integrators and registers. The quantities are normalized to machine units (MU). The analog input $X_A(t)$ (blue signal in the 1st diagram of Fig. 6) has a value of 0.5 for 3.5 time units. In the 2nd diagram of Fig. 6 the output of the window comparator is

shown in green. The comparator switches when integral 3 (green signal in the 3rd diagram of Fig. 6) reaches the value 0.5 MU.

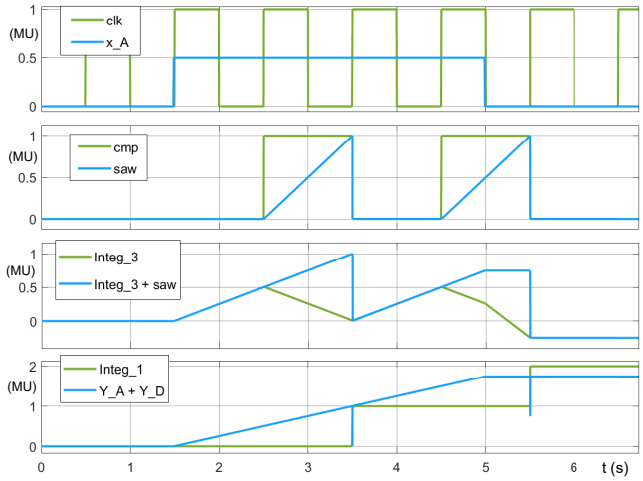

Fig. 6. Simulation of new hybrid integrator

When the window comparator has exceeded the threshold of 0.5 MU, integral 3 is reduced in magnitude in the time intervals $t = 2.5 \ldots 3.5$ and $t = 4.5 \ldots 5.5$. In these two time intervals, the digital part Y_D of the total integral has not yet been increased, so that the saw-tooth signal saw (blue signal in the 2nd diagram of Fig. 6) must be added to Integral 3 to always obtain the correct analog part Y_A of the total integral Y.

Since Integral 3 exceeds the threshold 0.5 MU twice, at the end of the integration phase $Y_D = 2$ (green signal in the 4th diagram of Fig. 6 from $t = 5.5$). Since the total integral must yield 1.75, the analog part of the total integral turns out to be $X_A = -0.25$ at the end.

In another example the harmonic oscillator with the differential equation $-\omega^2 \ddot{y} = y$ is calculated. The analog computational circuit consists of integrators configured in a loop with coefficient elements $\omega = 0.1$ in between. A selection of the simulated signals is shown in Fig. 7. The first three diagrams in Fig. 7 represent signals at the inputs and outputs of the first integrator only. The 4th diagram shows the total integrals of the first integrator as a blue colored curve $(Y_A + Y_D)$, the total integral of the second integrator as an orange colored curve $(Y_{2,A} + Y_{2,D})$. This first integrator gets an initial value $y_{D0} = 10$ in the digital register (blue curve in the 4th diagram in Fig. 7).

In the 3rd diagram of Fig. 7 it can be seen that the analog integrator for Integral 3 reaches at most 0.5 MU, and also together with the sawtooth from Integral 2 and Integral 4 (Fig. 5) does not significantly exceed the value of a MU. Crucial for this is that the digital slew rate of the Integral 1 is of the order of the slew rate of the total integral of the hybrid integrator.

IV. Summary

The new hybrid integrator is suitable for applications without negative feedback and can therefore be used universally

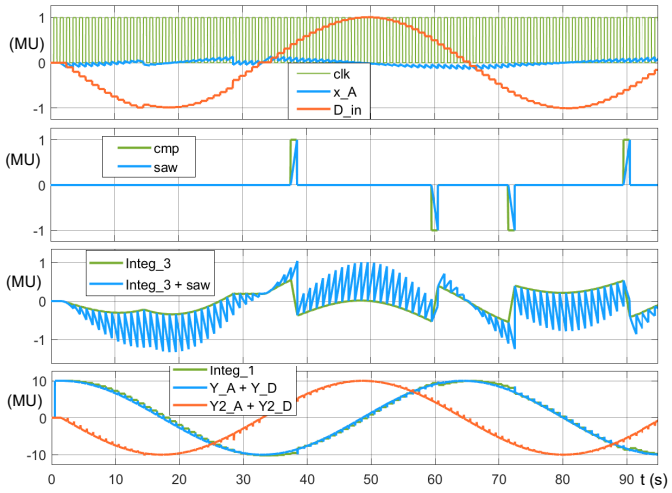

Fig. 7. Harmonic oscillator from two hybrid integrators

in analog computers and analog controls. A key feature is that the digital part of the integral does not have to be converted into an analog voltage. Only the overflow of a bit in the hybrid integrator corresponding to a machine unit (MU) must be considered during a clock phase in the analog section, as well as the digital input and the digital integrand. This helps to scale the digital components represented as analog signals. The reset of the analog component of the hybrid integrator is done continuously in time. During the reset process, an additive ramp signal is used to achieve a continuously correct value for the analog part of the hybrid integral. After the reset process, the ramp signal is switched off and the digital component is incremented. Disadvantages due to capacitive reset are avoided.

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