SANJIT KAUR

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OBJECTIVE

I am an Electronics and Communications Engineer specializing in VLSI with a strong foundation in SystemVerilog, Verilog, and digital design principles. Seeking a challenging role in a dynamic organization where I can leverage my skills to contribute to the development of semiconductor technologies and further my knowledge in the field of VLSI design and verification.

EDUCATION

Course Name	Institution/University	Year of Passing	Marks Obtained
Electronics and Communication Engineering(Bachelor of Technology)	GGSIPU, Bharati Vidyapeeth's College of Engineering, Delhi	2021-2025	8.6 CGPA
Class XII (Science-PCM)	S.S Mota Singh Sr. Sec. School, New Delhi	2021	92%
Class X	S.S Mota Singh Sr. Sec. School, New Delhi	2019	90.5%

SKILLS

- **Technical Skills:** OOPS, Machine Learning, MYSQL
- **Programming Languages**: C, C++, Python
- **Hardware Description Languages**: Verilog, System Verilog, UVM
- **Scripting Languages**: Shell Scripting
- **Technologies and Frameworks**: Design & Verification, UVM, Functional Coverage, Assertions, PCIe, LTI, APB, AXI, UNR Flow, Static Timing Analysis (STA), Clock Domain Crossing (CDC), Debugging, Tcl scripting
- **EDA Tools**: Mentor Graphics Questa Sim, Xilinx ISE, Cadence Xcelium, Vmanager, Simvision

INDUSTRIAL EXPERIENCE

- DESIGN VERIFICATION TRAINEE (CADENCE) *Jan 2025 - June 2025*

  Thoroughly studied the APB protocol and developed its UVM testbench in compliance with the AMBA ARM specification. Contributed to the verification of PCIe at the top level and the LTI submodule, with a strong focus on writing and sampling functional coverage, debugging failing tests, implementing assertions, and regression analysis. Designed covergroups for multiple LTI interfaces and enabled the UNR flow. Also worked with tools such as Xcelium, VManager, and Simvision. Additionally, gained hands-on experience in AXI register and helped enhance RTL and vplan understanding through close collaboration with designers.

- VLSI SIEMENS EMPOWER EDUCATION TRAINING (3ST TECHNOLOGIES) *March 2023 – December 2024*

  System Verilog training material has been developed by North Carolina State University (NCSU), Carolina USA and Siemens EDA funded NCSU with technical inputs for the course. The training course content includes subjects like Linux, Digital Design, STA, CDC, Verilog HDL, UVM, C++, C and data structures, CMOS along with System Verilog.

PROJECTS

- **PCIe Top-Level Verification** *SystemVerilog, Verilog, UVM, Xcelium, Vmanager*

  Contributed to Top-Level PCIe Verification by actively debugging failing coverage bins, reviewing and updating the vPlan, and proposing corrections to improve verification completeness. Created new coverpoints, mapped missing logical instances, and worked to enhance overall functional coverage. Gained a strong conceptual understanding of PCIe architecture, including its layered structure (Transaction, Data Link, and Physical), Transaction Layer Packets (TLPs), Credit-based flow control, and both Flit and Non-Flit modes of data transfer.

- **LTI Verification** *SystemVerilog, Verilog, UVM, Xcelium, Vmanager, SimVision*

  Implemented functional coverage for all major LTI interfaces and core requirements by writing and sampling covergroups, enhancing Vplan and actively participated in debugging LTI module behavior. Developed the Timeout Manager test framework, gaining hands-on experience with the UVM RAL model, and deepened understanding of LTI registers and IP-XACT-based register modeling. Additionally, enabled and executed the UNR flow for the LTI module, enhancing coverage quality and contributing to verification.

- **FIFO Buffer** Verilog, Mentor Graphics QuestaSim, Xilinx Vivado

  Simulated FIFO Buffer (First In First Out) in Synchronous, Asynchronous and Circular design mechanism to transfer data packets between different modules.

- **LC3 Microcontroller** SystemVerilog, Verilog, Mentor Graphics Questa Sim, Putty

  Designed and implemented an LC3 microcontroller using SystemVerilog, focusing on developing the control and datapath units. Utilized hardware description language to model the instruction set architecture, execute instructions, and manage memory. Including simulation and verification of the microcontroller's functionality.

- **Lowest Cost Smart Board Using CIS Sensor** Hardware components

  Frame + projector design instead of typical smart boards. Photoelectric sensors to be placed on the edges of the target region, in the form of CMOS technology found in CIS of scanners. Microcontroller to be used with the sensors-installed frame to convert the finger location input by the sensors into digital.

- **Machine Learning based Power Estimation for CMOS VLSI Circuits** ML, Cadence Virtuoso

  Machine Learning techniques using Monte Carlo simulation and random forest algorithm, for the prediction of power consumption by different CMOS VLSI circuits.

Extra-curricular activities

- Won Inter-Academy Lawn Tennis Tournament Under Mahesh Bhupathi Team Tennis Academy
- Head Position At College Gaming and Debating Society