**Design and Layout of Voltage Control Oscillator (VCO)**

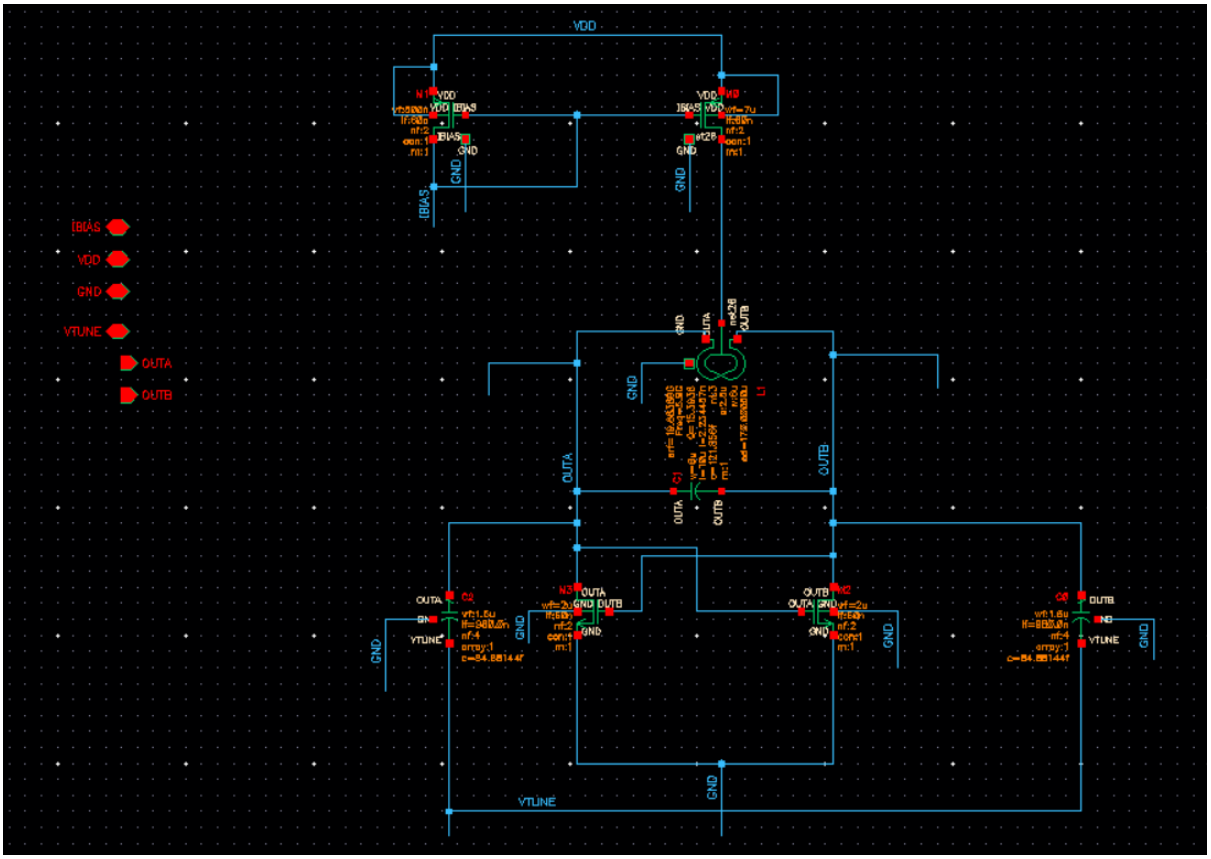
# ROLL NO-22M1180

# SANJOY KUMAR BASU

**Provide the VCO architecture along with the component values. Explain your choice of architecture. Briefly describe the design procedure.**

**Solutions:**

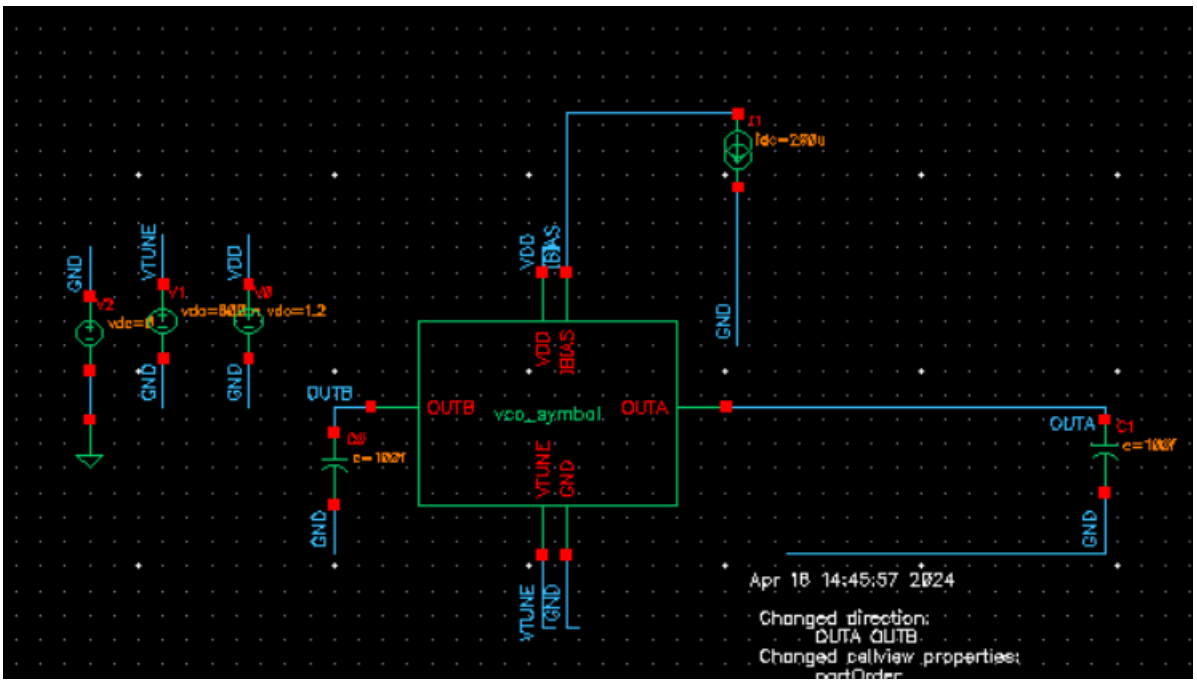
**VCO Schematic Diagram:**



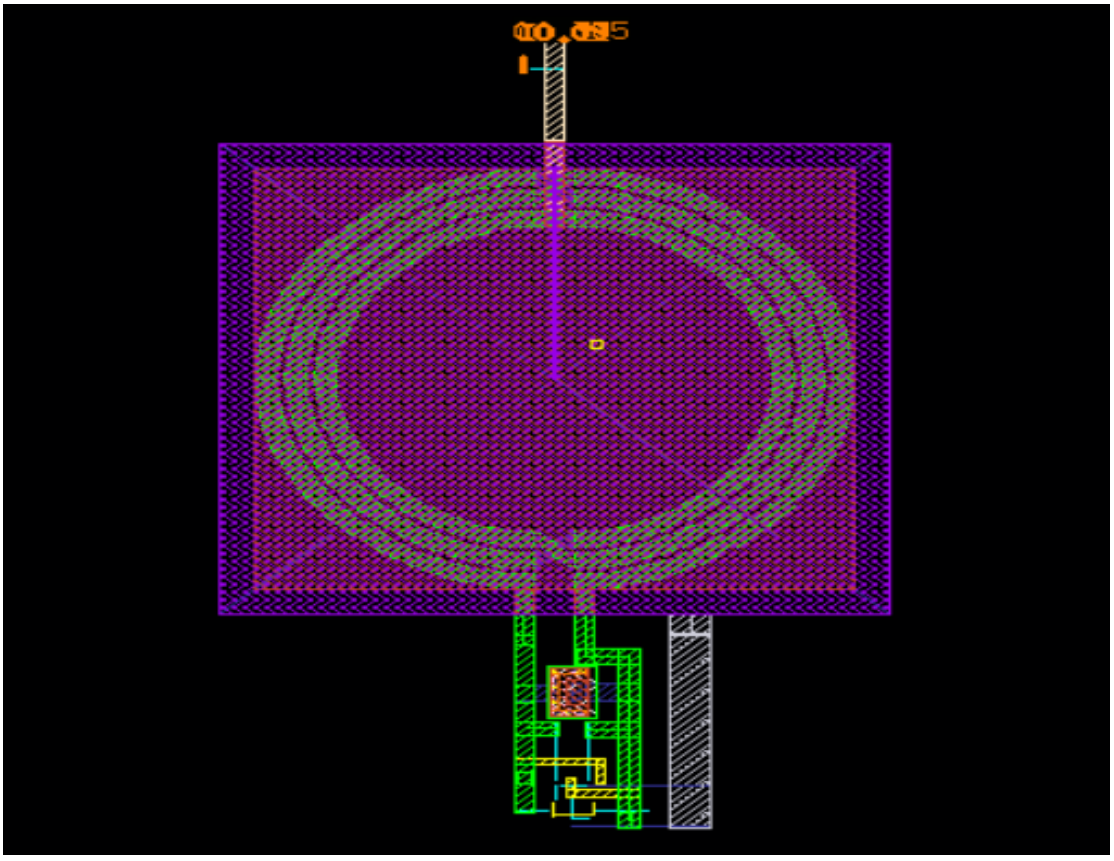
| Components | Value |
|---|---|
| VDD | 1.2V |
| VTUNE | 0.6V |
| NMOS-N_12_LLLVTRF | W=2U,L=60n |
| MIMCAPS_20F_MM | 121.856fF |
| L_SYCT30K_RFVIL | 2.2344nH |
| VARMIS_12_LLRF | 84.88144f F |
| | |

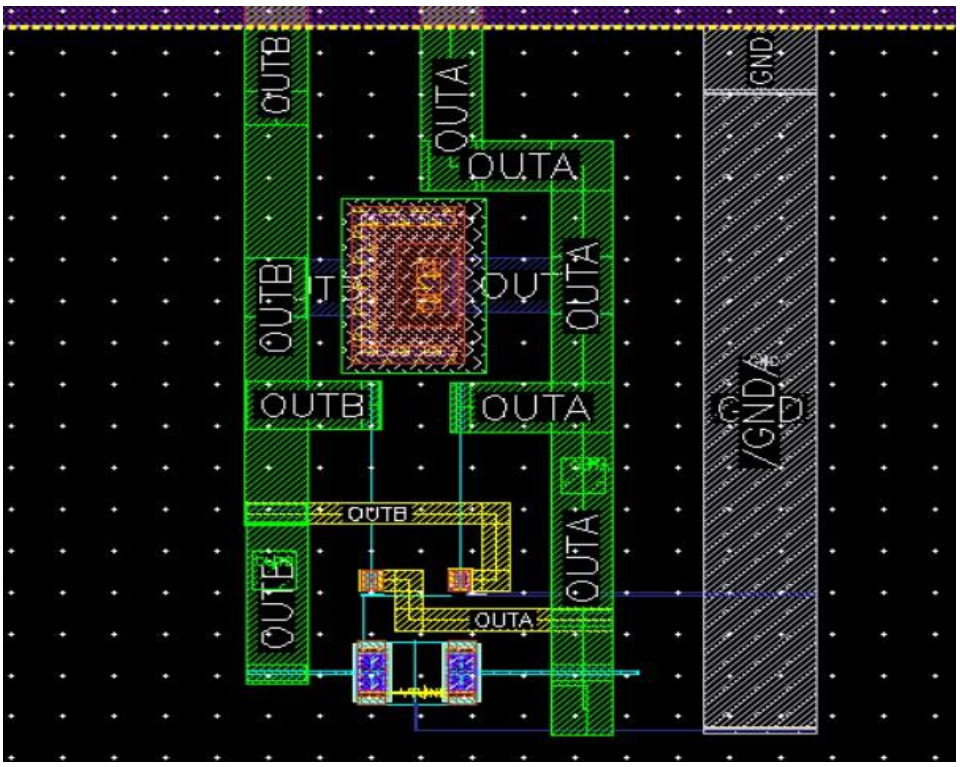
**So in this VCO design I have taken the current mirror circuit as a PMOS circuit. From Vdd to through PMOS the current is going to Centre tap inductor and then it is oscillating at a certain frequency with the given criteria based. We have used the VTUNE at varactor diode to tune the exact frequency as given in project. It is showing oscillation at two outputs. We know that frequency is inversely proportional to the square root of product of inductor and capacitor so keeping in that mind I have design in given frequency.**

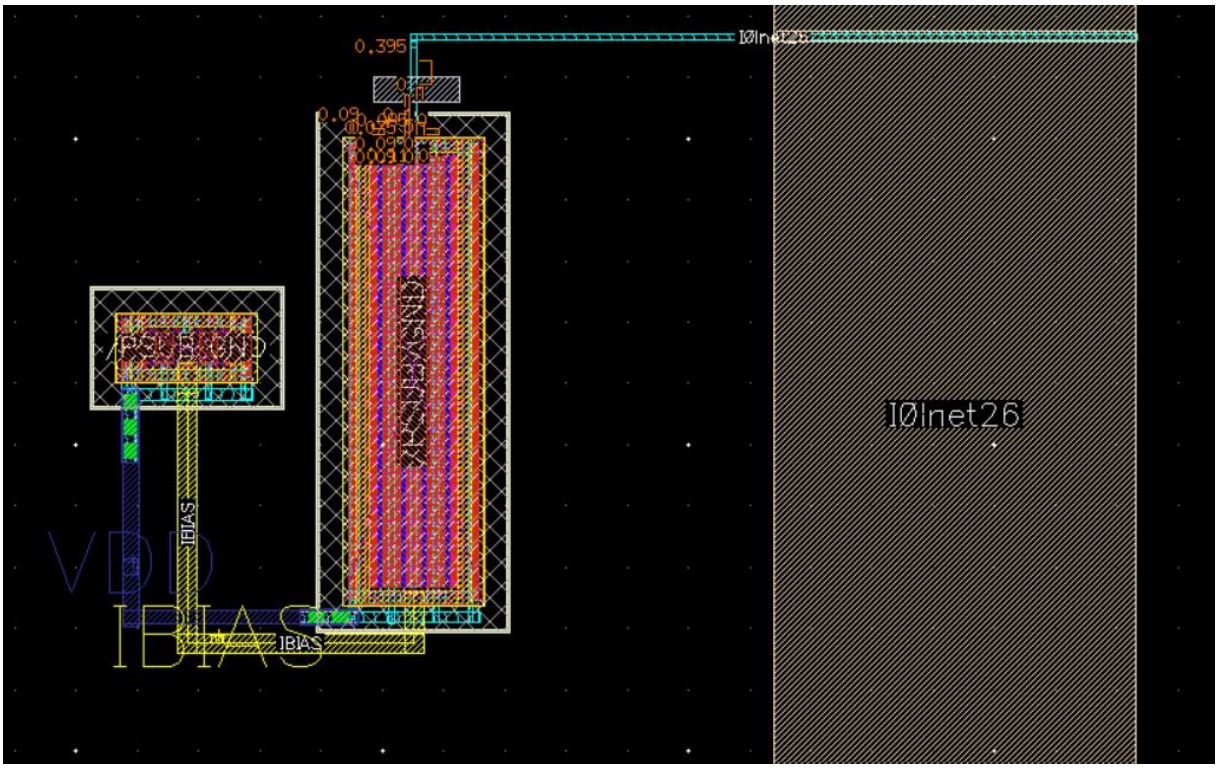
**TEST BENCH**



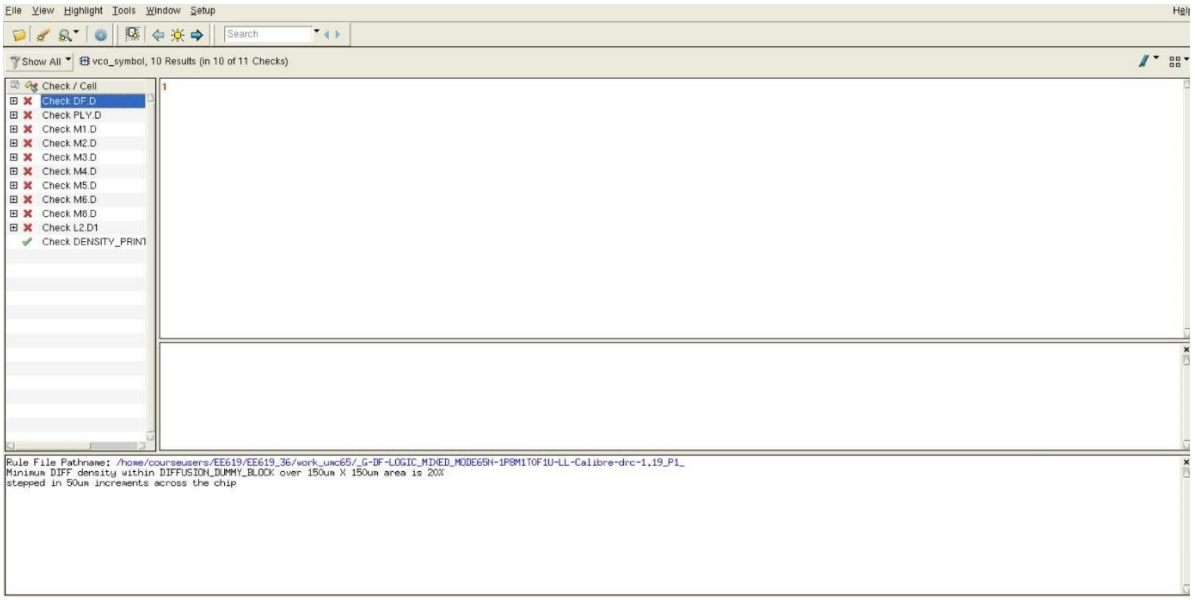
**Provide a high-resolution image of your layout. Provide DRC and LVS summary screenshots. (Points will be awarded based on quality of the layout)**



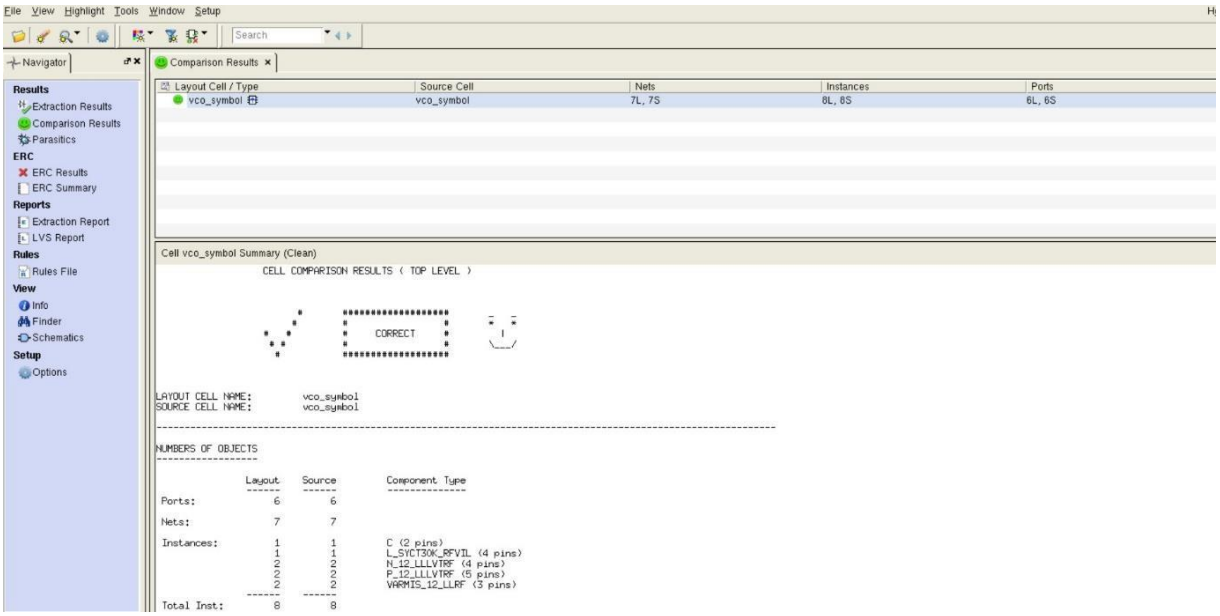




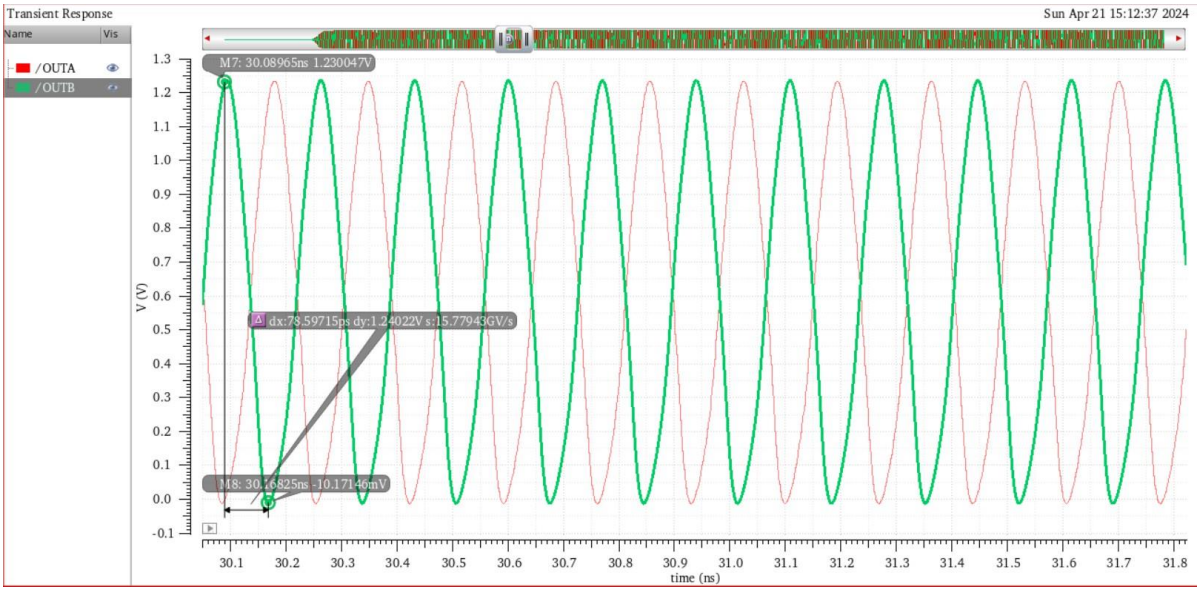

## DRC SUMMARY SCREENSHOT



## LVS SUMMARY SCREENSHOT

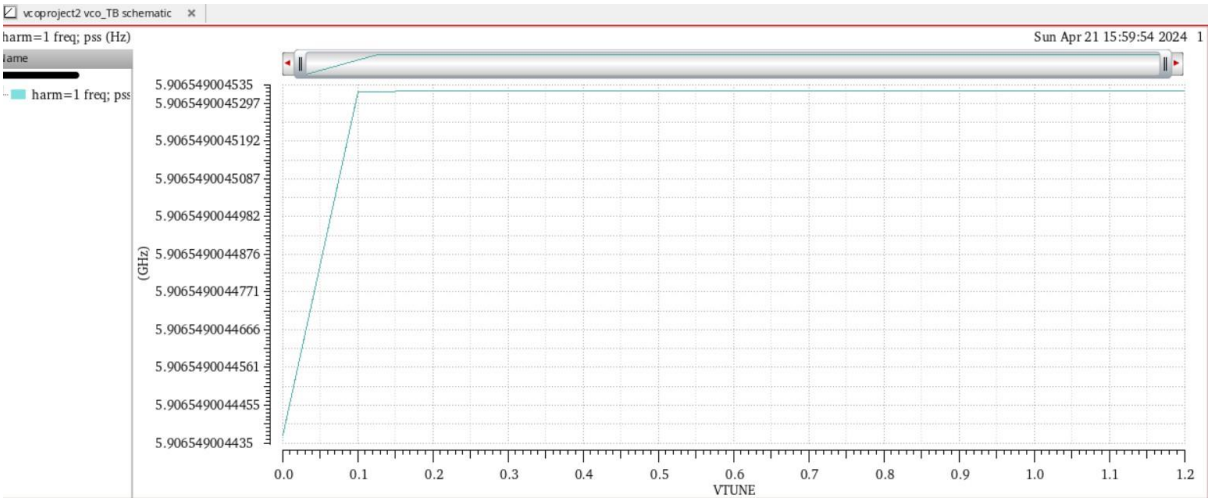



## Show the transient signals at output nodes for the $f_{OSC}$ assigned to you.



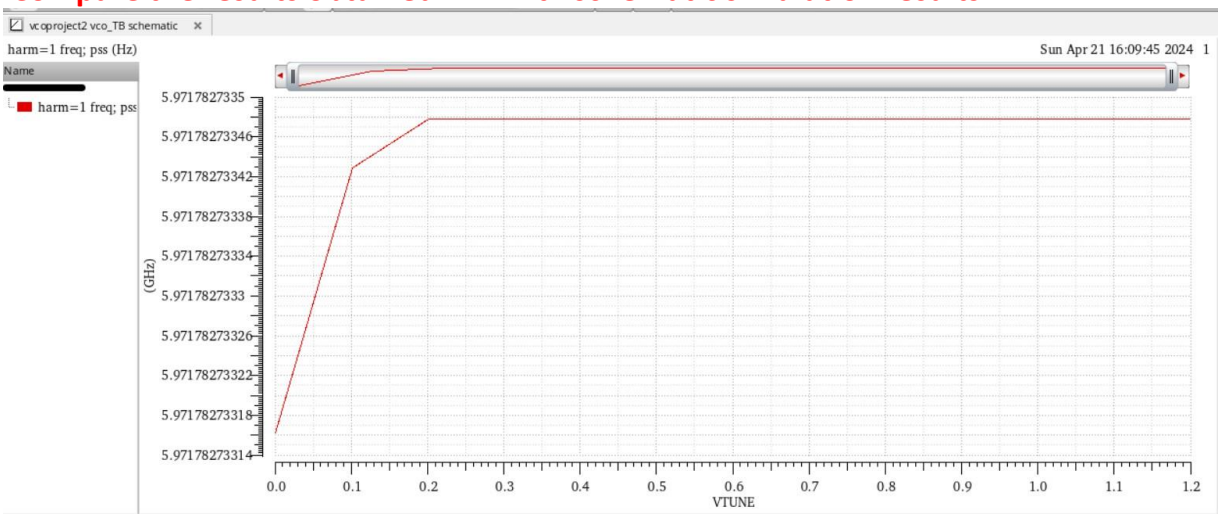

**This is the two output results from calibre view.The value of Vp-p is 1.24volt which is greater than 0.8 volt.**

**Plot the frequency vs $V_{TUNE}$ for $V_{TUNE}$ ranging from 0 to 1.2 V. Report frequency tuning range.**




**Changing the VTUNE we are observing a change in frequency.As it is Coming from Varactor diode it is showing that kind of nature.**

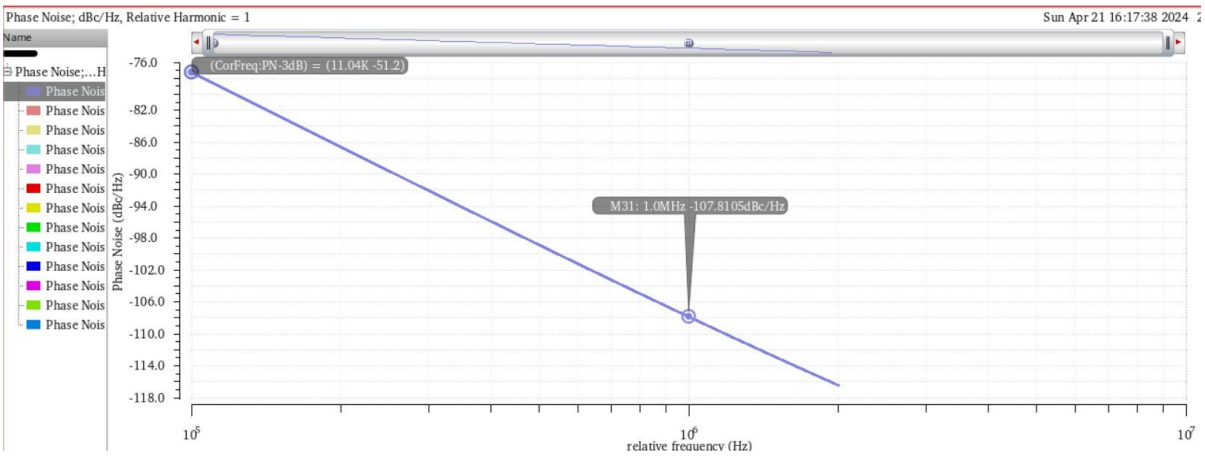
**Compare the results obtained in 4 with schematic simulation results.**




**This is from schematics. I have overdesigned it because of parasitic capacitance effect.**

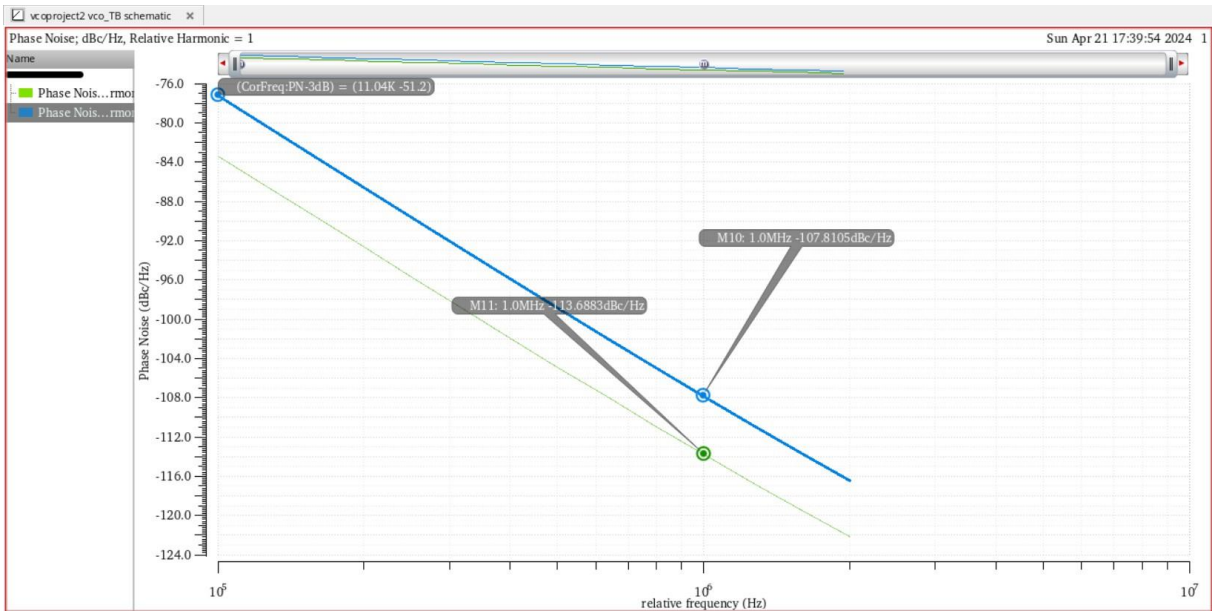
**This is showing same type of result compared to calibre view extraction.**

**Plot the phase noise (100 KHz to 2 MHz offset) plot of the VCO at $f_{osc}$.**



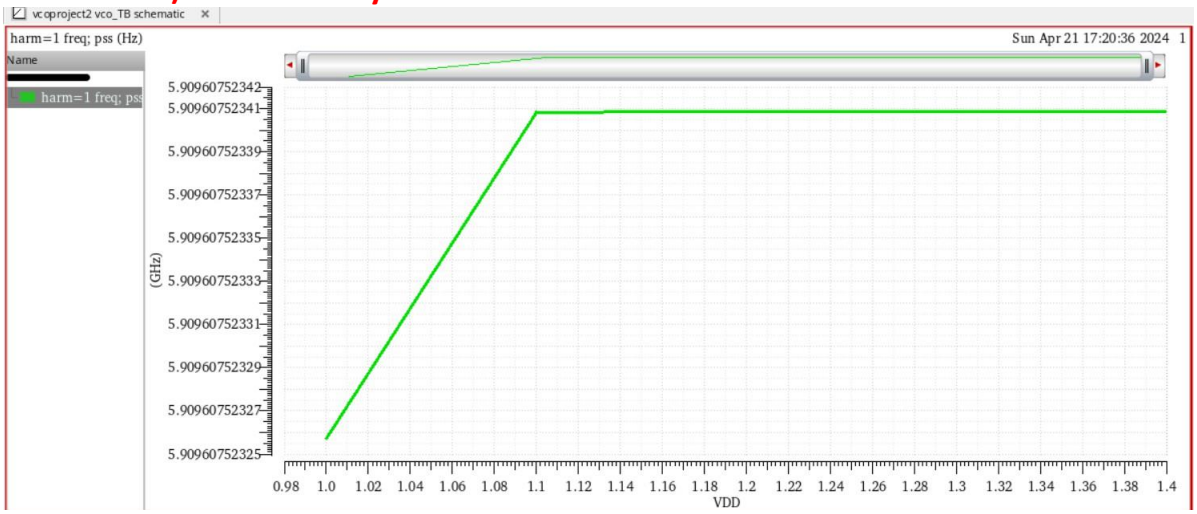

**Phase noise is coming -107.81dBc/Hz which is less than -100dBc/Hz.**

**Superimpose the phase noise plot (100 KHz to 2 MHz offset) at $f_{osc}$ from the PEX simulations by running it in C+CC Mode and R+C+CC Mode.**




**The green is for C+CC extraction result and the blue line for R+C+CC extraction and for that the phase noise is showing -113.688 dBc/Hz**

**Observe the frequency variation of the VCO by varying the $V_{DD}$ from 1-1.4V. (Keep $V_{TUNE}$= 0.6 V). Reason out your observations.**




**Change of frequency with respect to the value of VDD**