University of Rajshahi

Dept. of Computer Sc. & Engg.

B.Sc. (Engg) Part-2, Odd Semester Examination 2020

Course: CSE2112 (Digital System Design Lab)

1. Design and implement the 4-bit Adder-Subtractor Circuit using Digital IC Trainer and simulate the circuit using HDL.
2. Design and implement the BCD to Excess-3 code converter Circuit using Digital IC Trainer and simulate the circuit using HDL.
3. Design and implement the Excess-3 code to BCD code converter Circuit using Digital IC Trainer and simulate the circuit using HDL.
4. Design and implement the 4 bit Asynchronous Mod 10 counter using Digital IC Trainer and simulate the circuit using HDL.
5. Design and Implement the 3 bit synchronous up/down counter using Digital IC Trainer and simulate the circuit using HDL.
6. Design and implement the 4 bit synchronous counter for counting the following binary sequence using Digital IC Trainer or simulate the circuit using HDL.

0000→1101→1011→1001→0110→1100→0011→1111→0000

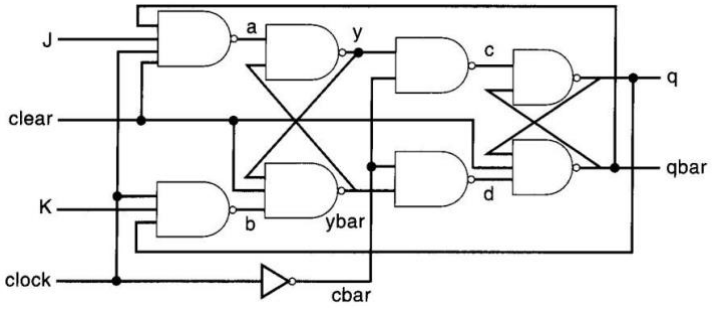

Fig: Circuit diagram of JK flip-flop