CO224 - Lab 6 - Part 2 - Report

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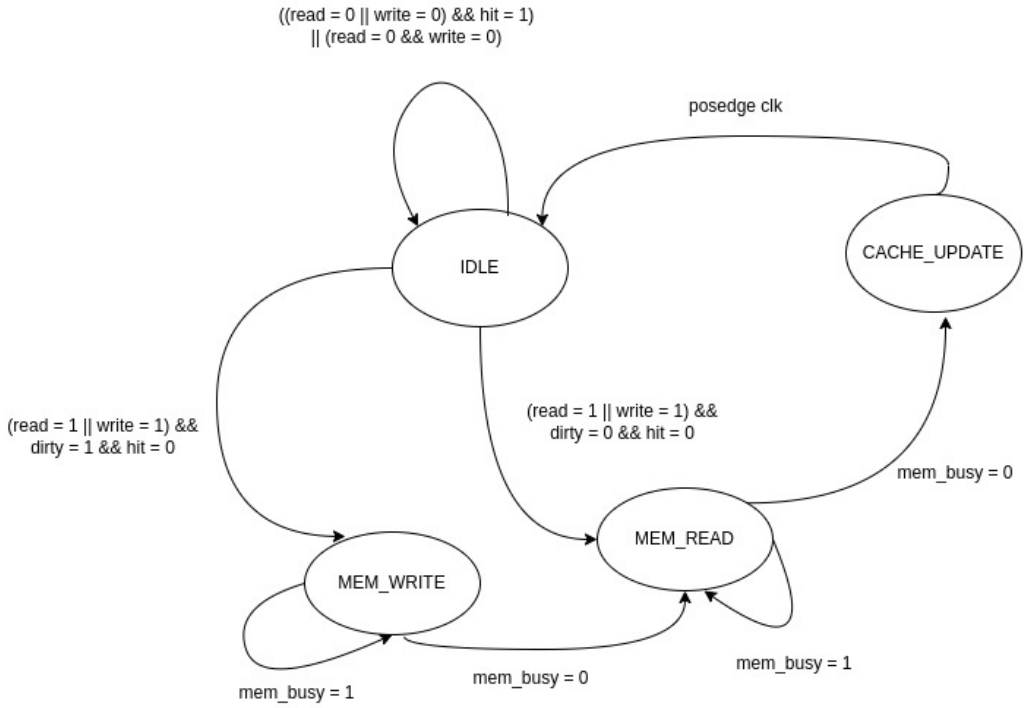
FSM of Cache Module



Performance Comparison

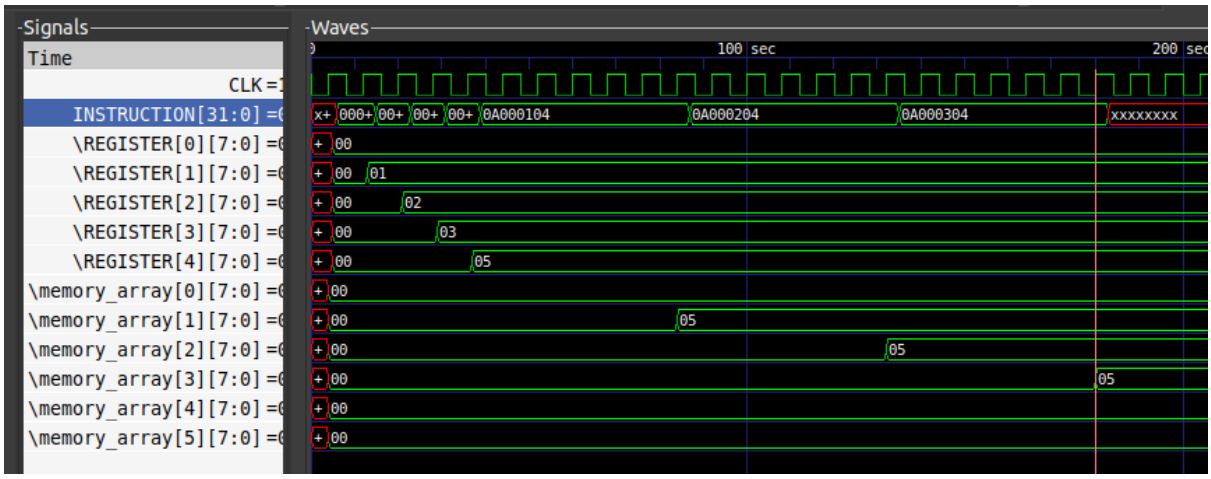
2 assembly programs were used to evaluate the performance of the systems from part 1 and part 2

Program 1

```
loadi 1 0x01    // r1 = 1
loadi 2 0x02    // r2 = 2
```

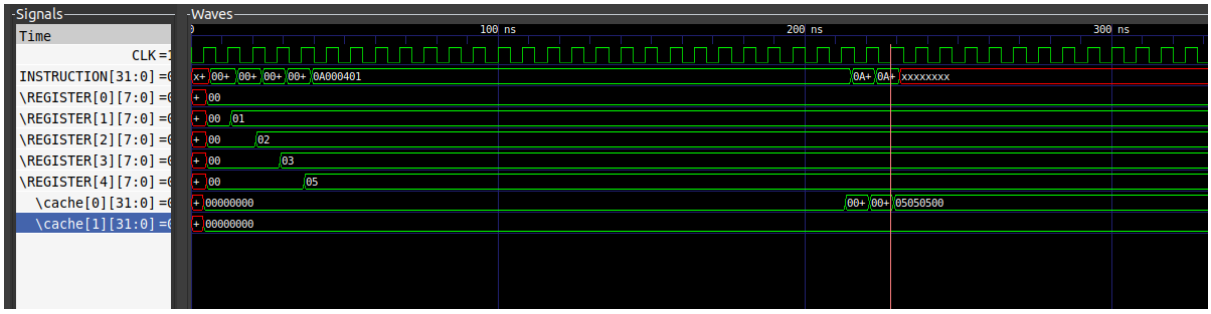
```
loadi 3 0x03    // r3 = 3
loadi 4 0x05    // r4 = 5
swd 4 1 // store 5 in memory[1] => expect a cold miss (21 clock cycles)
swd 4 2 // store 5 in memory[2] => expect a cold miss (21 clock cycles)
swd 4 3 // store 5 in memory[3] => expect a cold miss (21 clock cycles)
```

Timing Diagram of Part 1 System



The program finished in 22 clock cycles

Timing Diagram of Part 2 System



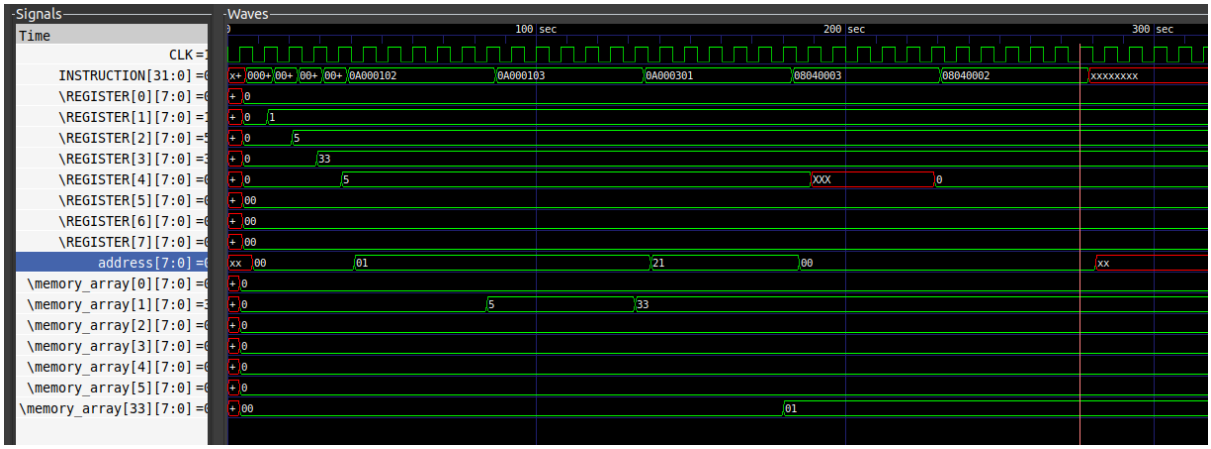
The program finished in 28 clock cycles

Program 2

```
loadi 1 0x01    // r1 = 1
loadi 2 0x05    // r2 = 5
loadi 3 0x21    // r3 = 33
loadi 4 0x05    // r4 = 4
swd 1 2 // store 5 in memory[1] => expect a cold miss (21 clock cycles)
swd 1 3 // store 33 in memory[1] => expect a write hit
swd 3 1 // store 1 in memory[33] => expect a dirty write miss (42 clock cycles)
```

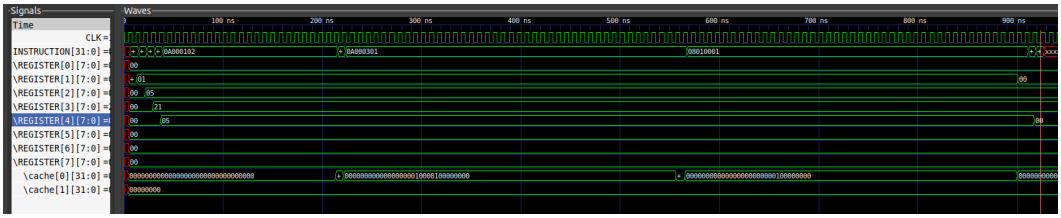
```
lwd 4 3 // r4 = memory[33] = 1 => read hit
lwd 4 1 // r4 = memory[33] = 1 => read hit
```

Timing Diagram of Part 1 System



The program finished in 34 clock cycles

Timing Diagram of Part 2 System



The program finished in 115 clock cycles

Conclusion

- Cold misses cannot be avoided by using a cache
- Once cold misses are all retrieved, cache can be faster than accessing data memory if there is a high hit rate. But, the hit rate is heavily affected by the direct mapping block placement and the size of the cache.