

General Bus Operation:

- 8086 has combined address and data bus referred to as time multiplexed address and data bus.
- The reason behind multiplexing address and data over same pins is maximum utilization of processor pins.
- This bus can be demultiplexed using a few latches and transreceivers whenever required.
- Here we discuss the general bus operation cycle.
- Basically all processor bus cycles consist of atleast four clock cycles. These are referred to as T_1 , T_2 , T_3 and T_4 .

→ The address is transmitted by the processor during T_1 .

It is present on the bus only for one cycle.

→ During T_2 , the bus is tri-stated for changing the direction of bus for the following data read cycle.

→ The data transfer takes place during T_3 and T_4 .

→ In case, an addressed device is slow and shows 'NOT READY' status, the wait states T_w are inserted between T_3 and T_4 .

These clock states during wait period are called idle states (T_i), wait states (T_w) or inactive states.

The processor uses these cycles for internal house keeping.

→ ALE is emitted during T_1 by the processor (minimum mode) or the bus controller (maximum mode) depending on the status of MN/\overline{mX} input.

- The negative edge of this ALE pulse is used to separate the address and the data or status information.
- In maximum mode the status lines $\overline{S_0}, \overline{S_1}, \overline{S_2}$ indicate the type of operation.
- Status bits $\overline{S_3}$ to $\overline{S_7}$ are multiplexed with higher order address bits and $\overline{\text{BHE}}$ signal.
- Address is valid during T_1 , while the status bits S_3 to S_7 are valid during T_2 to T_4 .

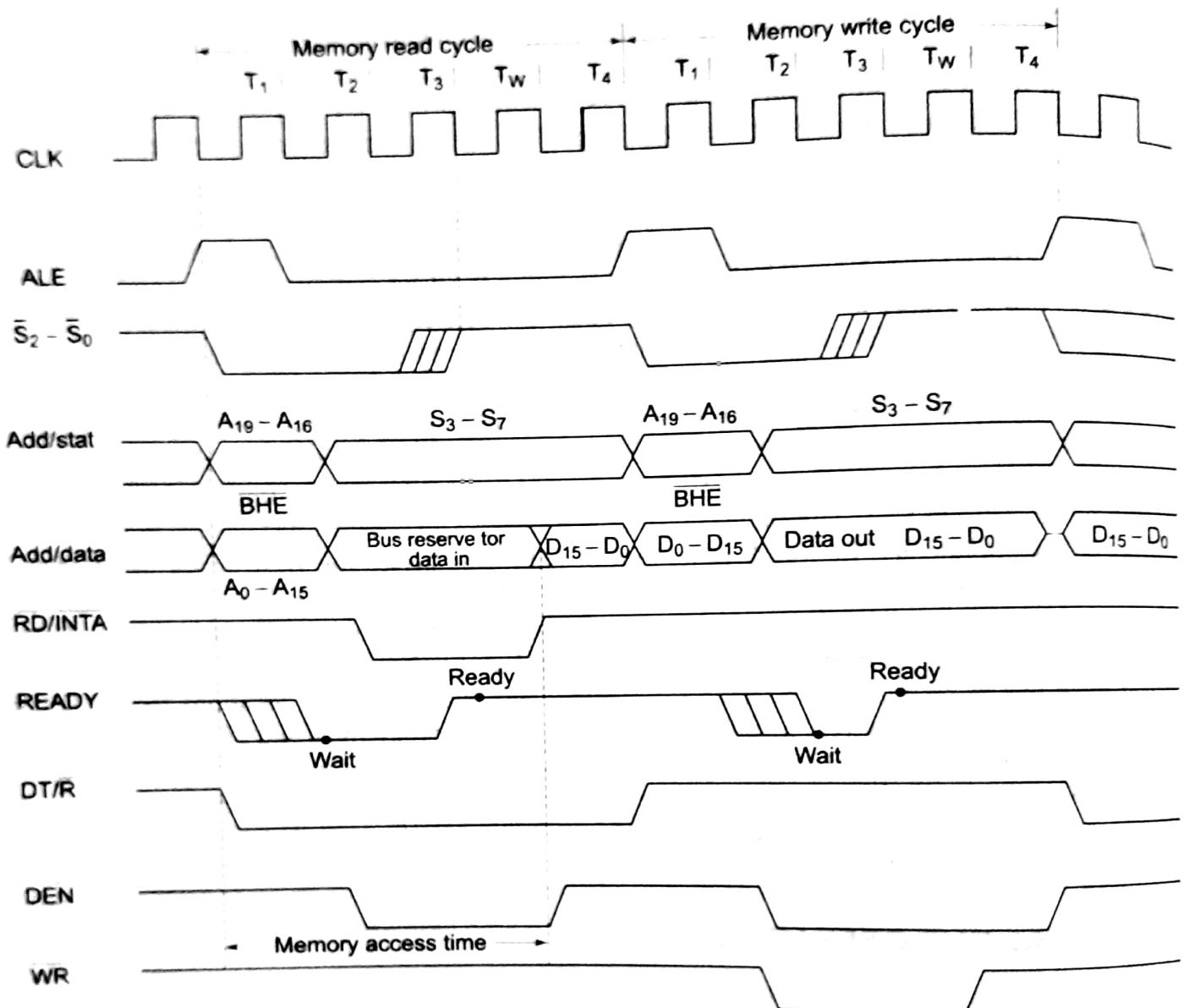


Fig. 1.8 General Bus Operation Cycle of 8086

2/0 Addressing capability

- The 8086/8088 processor can address up to 64 k 2/0 bytes registers or 32k word register.
 - The limitation is that the address of an 2/0 device cannot be greater than 16 bits in size, which means a maximum of 64 k byte 2/0 device can be accessed by CPU.
 - The 2/0 address appears on the address lines A₀ to A₁₅ for one clock cycle (T₁). It may then be latched using the ALE signal. The upper address lines A₁₆-A₁₉ are at logic 0 level during 2/0 operations.
 - The 16 bit register DX is used as a 16 bit 2/0 address pointer, with full capability to address upto 64 k devices.
 - In memory mapped I/O interfacing, the 2/0 device addresses are treated as memory locations in page 0 ie. segment address 0000H. Even addressed bytes are transferred on D₀-D₇ lines odd addressed bytes are transferred on D₈-D₁₅ lines

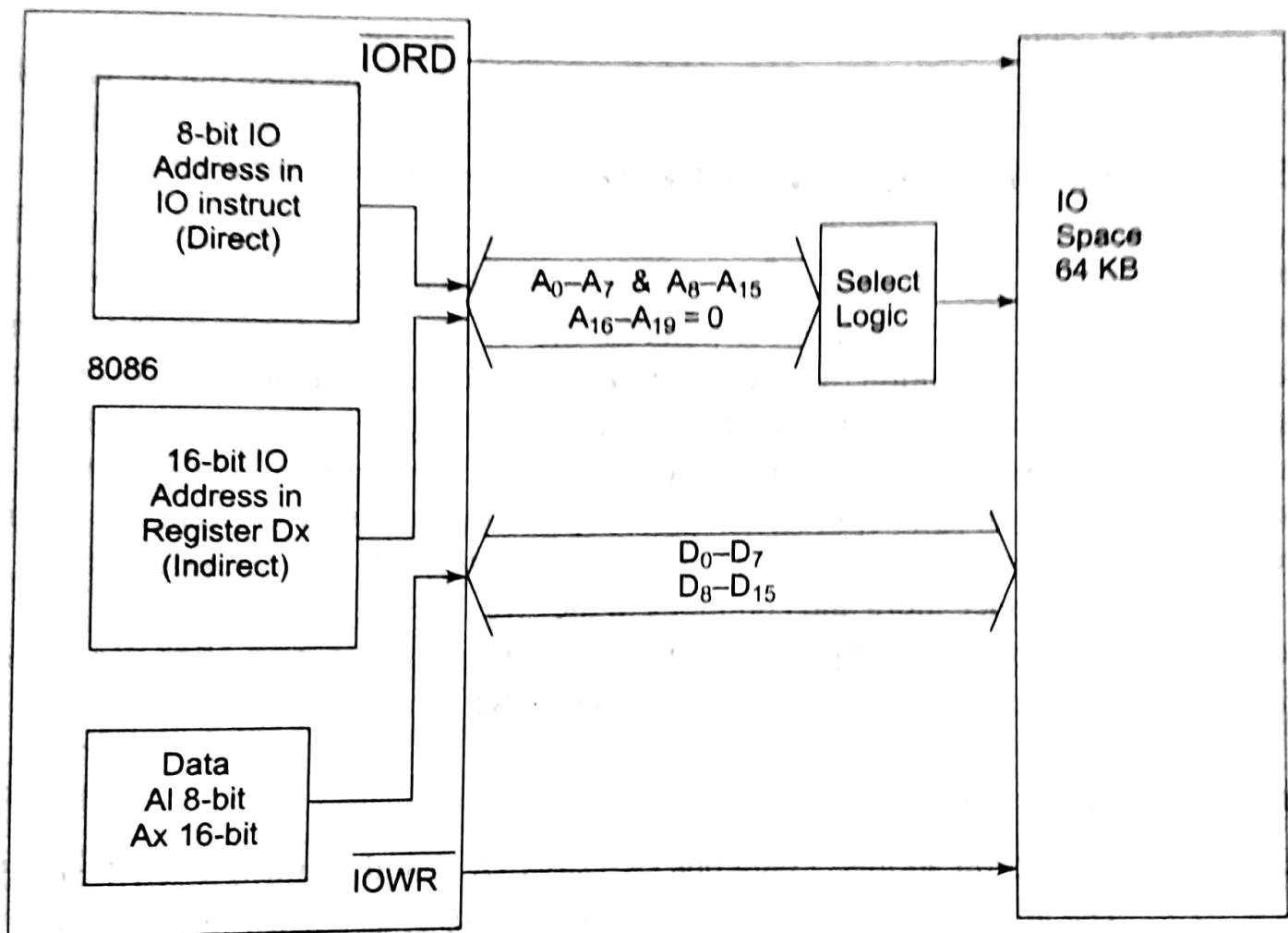


Fig. 1.9 8086 IO Addressing

→ While designing an 8bit I/O system around 8086 , care must be taken that all the byte registers in the system should be even addressed.

Special processor activities

① Processor Reset and Initialization:

- When logic 1 is applied to the RESET pin of the microprocessor, it is reset. It remains in this state till logic 0 is again applied to the RESET pin.
- The 8086 terminates the on going operation on the positive edge of the reset signal. When the negative edge is detected, the reset sequence starts and continues for 10 clock cycles.
- During this period, all internal register contents are set to 0000H except CS which is set to value FFFFH.
- Then execution starts again from the physical address FFFF0H. Due to this reason, the EPROM in 8086 system is interfaced to have physical mem. locations FFFF0H to FFFFFH.

- For the reset signal to be accepted by 8086, it must be high for atleast 4 clock cycles.
- From the instant the power is on, the reset pulse is not applied ~~left~~ to 8086 before $50\ \mu s$ to allow proper initialization of 8086.
- In the reset state, all 3-state outputs are triated.
- Status signals are active in the idle state for the first clock cycle after Reset becomes active and then floats to tristate.
- The ALE and HZDA lines are driven low during reset operation.
- NM2 request, which appears before the second clock after the end of reset operation will not be served.
for NM2 to be served, it must appear after the second clock cycle during reset initialization or later.
- If HOLD request appears after RESET, it will be immediately served after initialization.

② HALT

- When the processor executes a HLT instruction, it enters the 'halt' state.
- However, before going into halt state, it indicates that it is going into halt state in two ways depending on whether it is in the minimum or maximum mode.
 - ① When the processor is in minimum mode and wants to enter HALT state, it issues an ALE pulse but does not issue any control signal.
 - ② When the processor is in maximum mode and wants to enter HALT state, it puts the HALT status (011) on $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ pins and then the bus controller issues an ALE pulse but no qualifying signal i.e. no appropriate address or control signals are issued to the bus.
- Only an interrupt request or reset will force the 8086 to come out of the 'halt' state. Even the HOLD request cannot force the 8086 to come out of 'halt' state.

③ TEST and Synchronization with External Signals.

- Besides interrupt, hold and general I/O capabilities 8086 has an extra facility of TEST signal.
- When the CPU executes a WAIT instruction, the processor preserves the content of registers before execution of the WAIT, and CPU waits for the TEST signal to go low.
- If TEST signal goes low, it goes on executing further otherwise it keeps on waiting for the TEST signal to go low.
- For TEST signal to be accepted, it must be low for atleast 5 clock cycles.
- While waiting any HOLD request from external device may be served.
- When an interrupt occurs when processor is waiting, it fetches the WAIT instruction once more, executes it and then serves the interrupt. After returning from the interrupt, it fetches wait instruction once more and then continues in 'wait' state.

Minimum mode 8086 System and Timings

- 8086 is operated in minimum mode when MN/M_X pin is logic 1.
- All control signals are given out by the microprocessor itself.
- There is a single microprocessor in the minimum mode system.
The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.
- Some type of chip selection logic is required for selecting memory or I/O devices, depending upon the address map of the system.
- The latches are generally buffered output D type flip flops like 74LS373, or 8282. They are used for separating valid address from multiplexed address/data signals and are controlled by the ALE signal.

Table 1.5

M/IO	RD	DEN	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

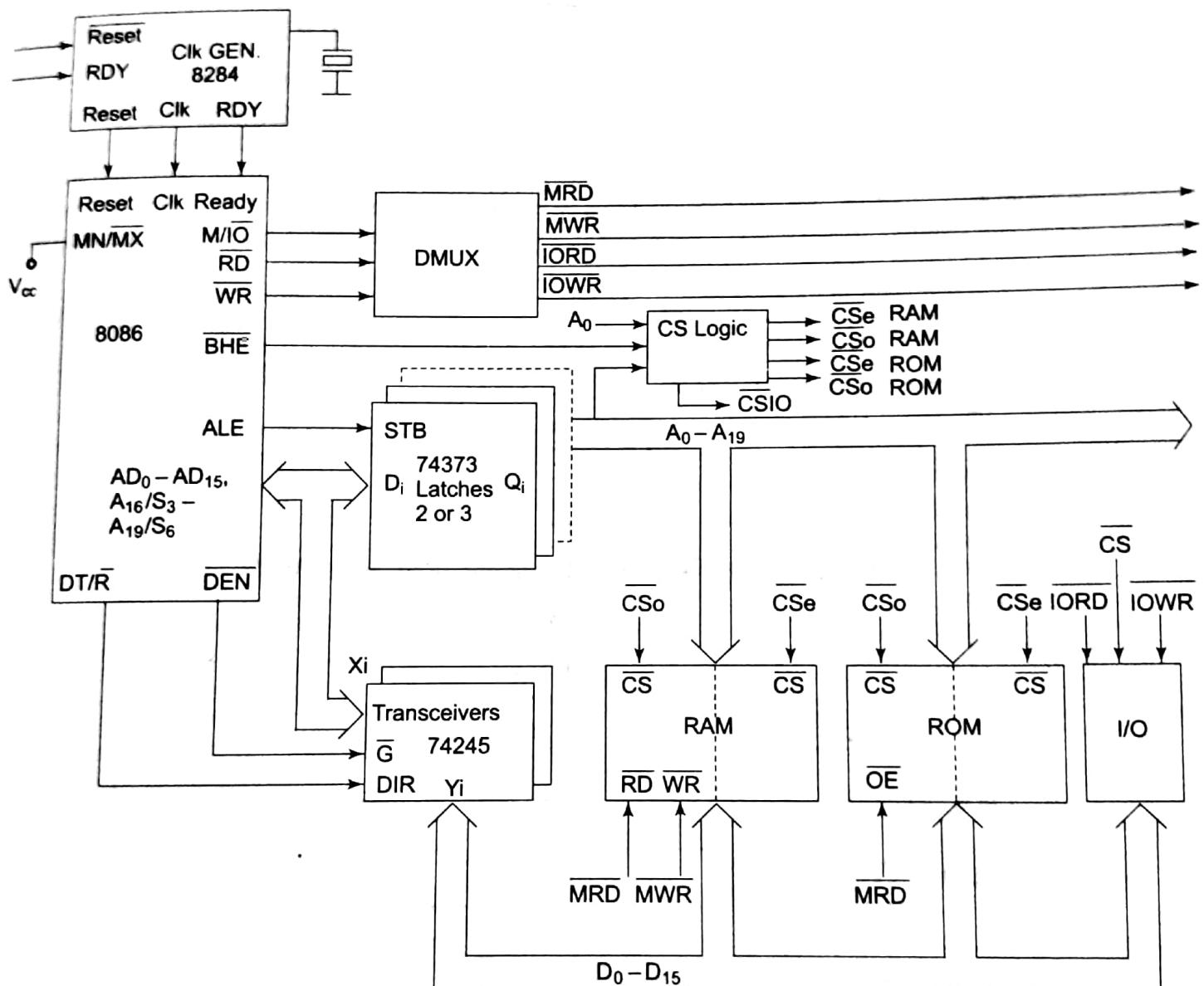


Fig. 1.13 Minimum Mode 8086 System

→ Transceivers are bidirectional buffers and some time , they are called data amplifiers.

They are required to separate the valid data from multiplexed address / data signal.

They are controlled by two signals , namely \overline{DEN} and DT/R .

\overline{DEN} signal indicates that valid data is available on the data bus .

DT/R signal indicates the direction of data i.e. from / to the processor .

→ Memory is provided for monitor and user program storage.

EPROMs are used for monitor storage

RAMs are used for user's program storage.

- I/O devices are used for communication with the processor as well as some special purpose I/O devices.
- The clock generator (IC 8284) generates the clock from crystal oscillator and then shapes it to make more precise so that it can be used as an accurate timing reference. It also synchronizes some external signals with system clocks.

- The working of minimum mode configuration can be described in terms of timing diagrams
- The opcode fetch and read cycles are similar.
- The timing diagram can be categorized into two parts:
 - ① first is the timing diagram for the read cycle
 - ② second is the timing diagram for write cycle

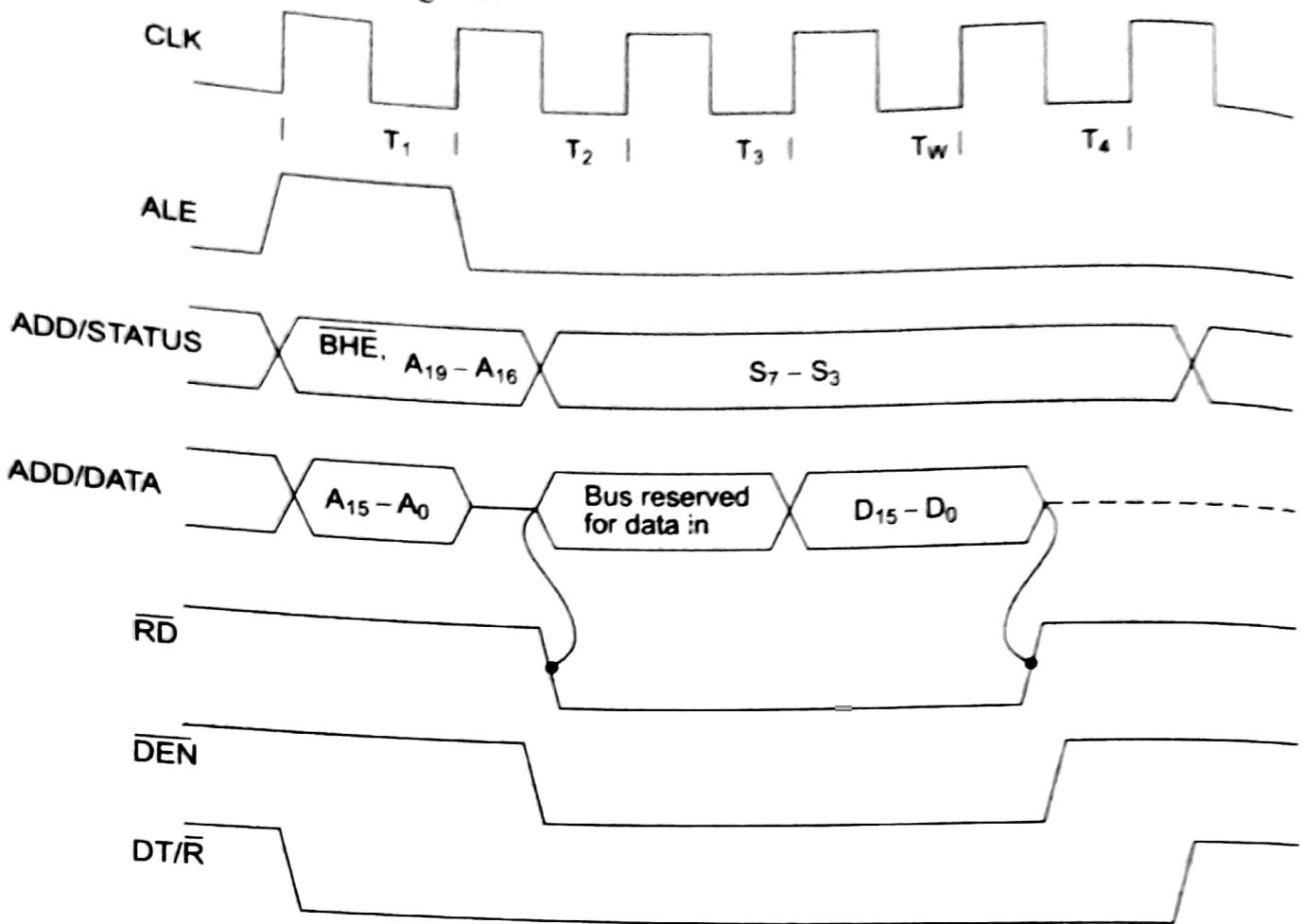


Fig. 1.14(a) Read Cycle Timing Diagram for Minimum Mode

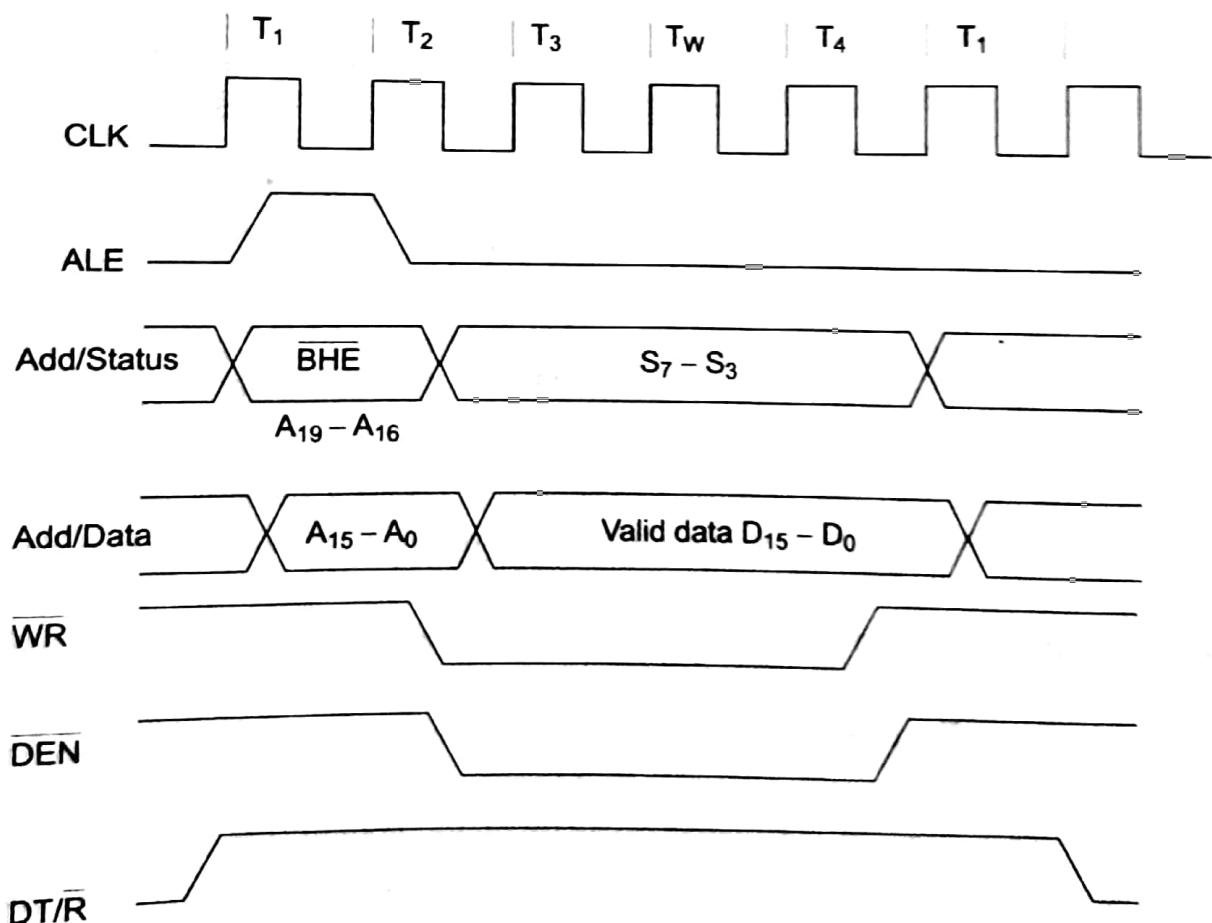


Fig. 1.14(b) Write Cycle Timing Diagram for Minimum Mode Operation

- The read cycle begins in T_1 , with enabling of ALE and $m/20$ signals.
- During negative going edge of ALE, valid address is latched on local bus.
- The \overline{BTE} , A_0 signals address low, high or both bytes.
- From T_1 to T_4 , the $m/20$ signals indicate a memory or I/O operation.
- At T_2 , the address is removed from the local bus and sent to output. The bus is then triated.

The \overline{RD} control signal is also activated in T_2 .

This causes the addressed device to enable its data bus drivers.

After \overline{RD} signal goes low, valid data is available on the data bus.

At the same time \overline{DEN} , DT/R signals are enable for ~~the~~ read operation.

→ The CS logic enables the even and odd address memory banks.

- Write cycle also begins with enabling of ALE and extension of the address
- The m/\bar{r}_0 signal is enabled to indicate a memory or \bar{r}_0 operation.
- In T_2 , after sending the address in, the processor sends the data to be written to the addressed location.
- The data remains on the bus until the middle of T_4 .

The \bar{w}_R is enabled at the beginning of T_2

- The m/\bar{r}_0 , \bar{r}_D and \bar{w}_R signals indicate the type of data transfer

m/\bar{r}_0	\bar{r}_D	\bar{w}_R	Transfer type
0	0	1	\bar{r}_0 Read
0	1	0	\bar{r}_0 write
1	0	1	Memory Read
1	1	0	Memory write

HOLD Response Sequence:

- The HOLD pin is checked at the end of each bus cycle.
- If it is received active by the processor before T_4 of previous cycle or during T_1 of the current cycle, the CPU activates the HLDA in the next clock cycle and the bus is given to another requesting master for the succeeding bus cycles.
- The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low.

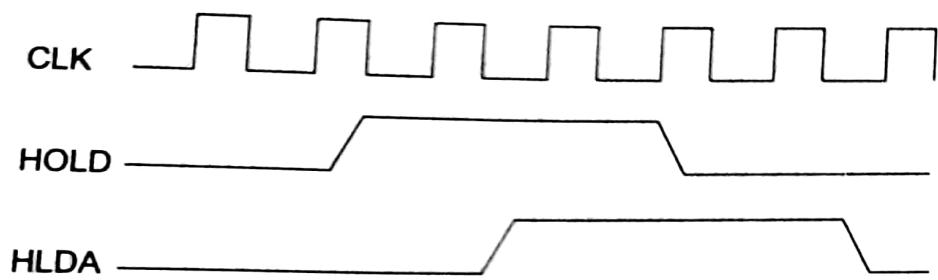


Fig. 1.14(c) Bus Request and Bus Grant Timings in Minimum Mode System

Maximum mode 8086 System and Timings

- In maximum mode, $M_N / \bar{M}_X = 0$.
- In this mode, the processor derives the status signals $\bar{S}_2, \bar{S}_1, \bar{S}_0$. Another chip called bus controller derives control signals using this information.
- In maximum mode, there may be more than one microprocessor in the system configuration.
- The other components can include latches, transceivers, clock generator, memory and I/O devices as in the case of minimum mode of configuration.
- The functions of all the pins having special function in maximum mode have already been discussed.
- We study here bus controller chip and its functions in brief.

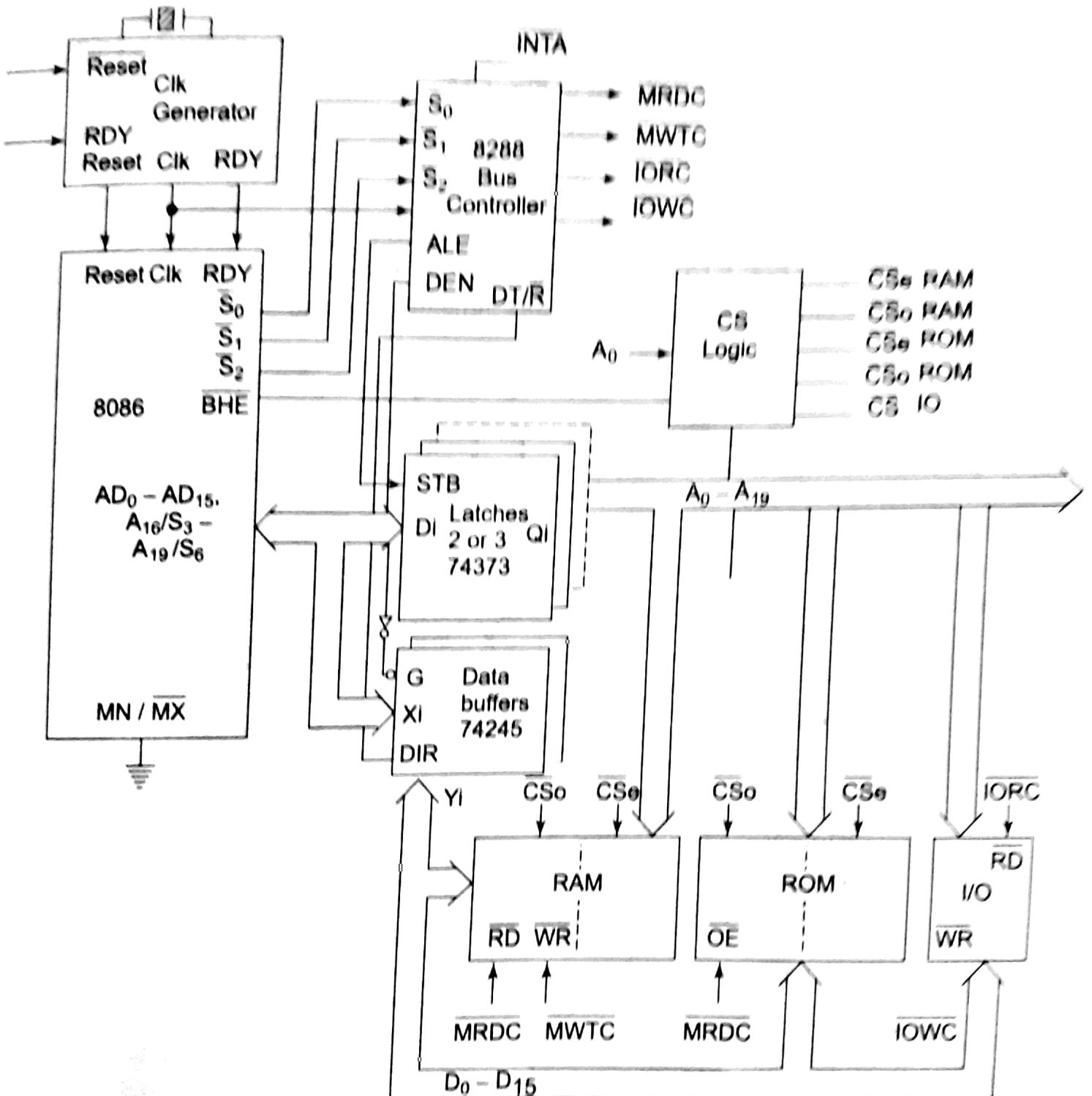


Fig. 1.15 Maximum Mode 8086 System

→ The basic functions of the bus controller chip 2C8288 is to derive control signals like \overline{RD} , \overline{WR} (for memory & I/O device), \overline{DEN} , $\overline{DT/R}$, ALE etc, using the information made available by the processor on the status lines.

→ The bus controller chip has input lines S_2 , S_1 , S_0 and CLK, which are provided by the CPU.

→ It provides the outputs ALE, DEN, $\overline{DT/R}$, \overline{MRDC} , \overline{MWTC} , \overline{IORC} , $\overline{20WC}$, $\overline{A20WC}$, \overline{AMWC} .

→ \overline{AEW} , $20B$ and CEN pins are specially useful for multi processor system.

\overline{AEW} , $20B$ are generally grounded.
CEN pin is normally tied to +5V.

→ The significance of MCE) \overline{PDEN} output depends on the status of $20B$ pin.

If $20B$ pin is grounded, it acts as master cascade enable to control cascaded 8259A else it acts as peripheral data enable used in multiple bus configuration.

- $\overline{\text{INTA}}$ pin is used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.
- $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$ are I/O read and I/O write commands which enable the I/O interface to read or write data from or to the addressed port.
- $\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$ are memory read command and memory write command signals for memory read and memory write respectively.
- $\overline{\text{AIOWC}}$, $\overline{\text{AMWTC}}$ are advanced write command signals, which also serve the same purpose, but are activated one clock cycle earlier than $\overline{\text{IOWC}}$ and $\overline{\text{MWTC}}$ signals respectively.

- The maximum mode system timing diagram are also divided into two portions as read (input) and write (output) timing diagrams.
- The address/data and address /enable timings are similar to minimum mode.

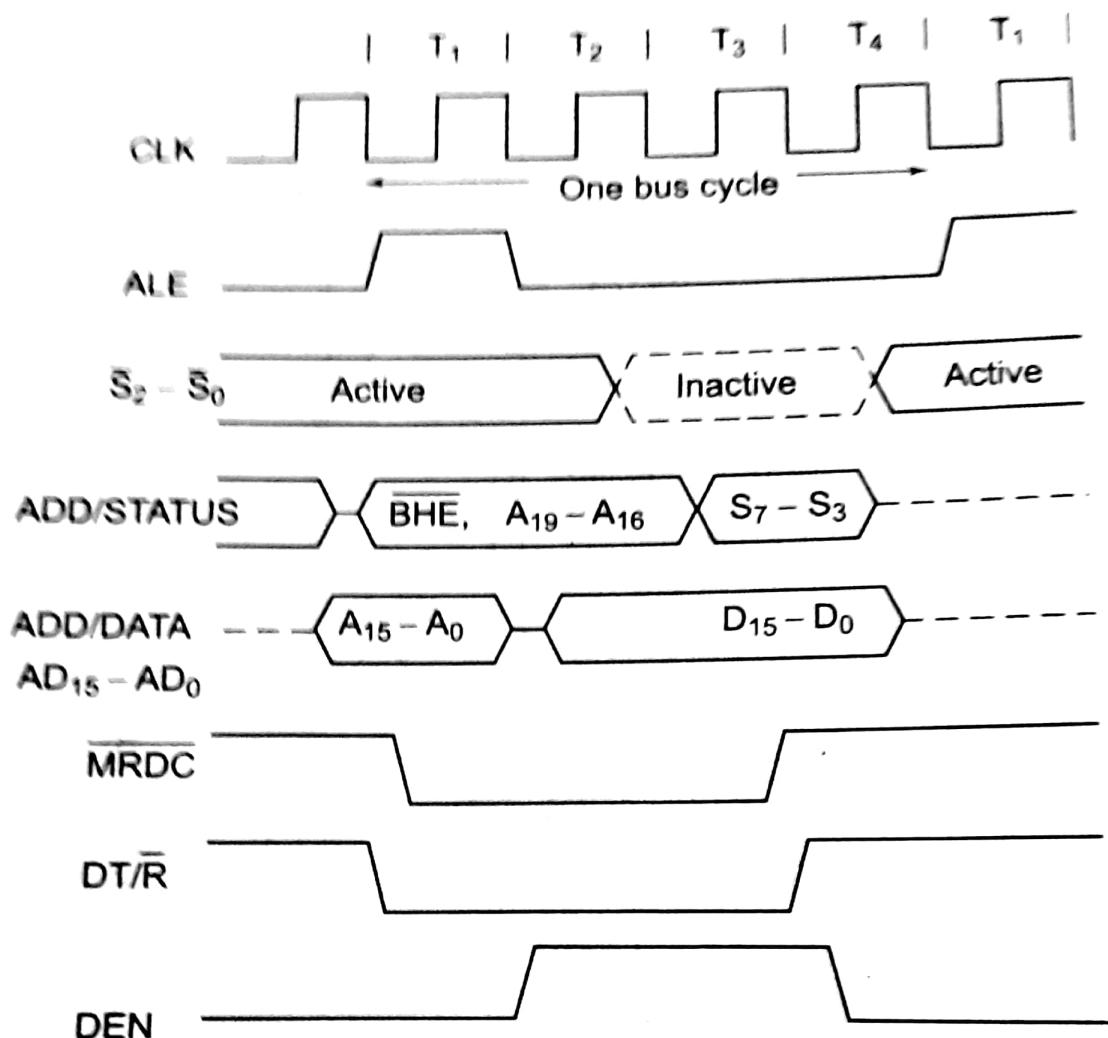


Fig. 1.16 (a) Memory Read Timing in Maximum Mode

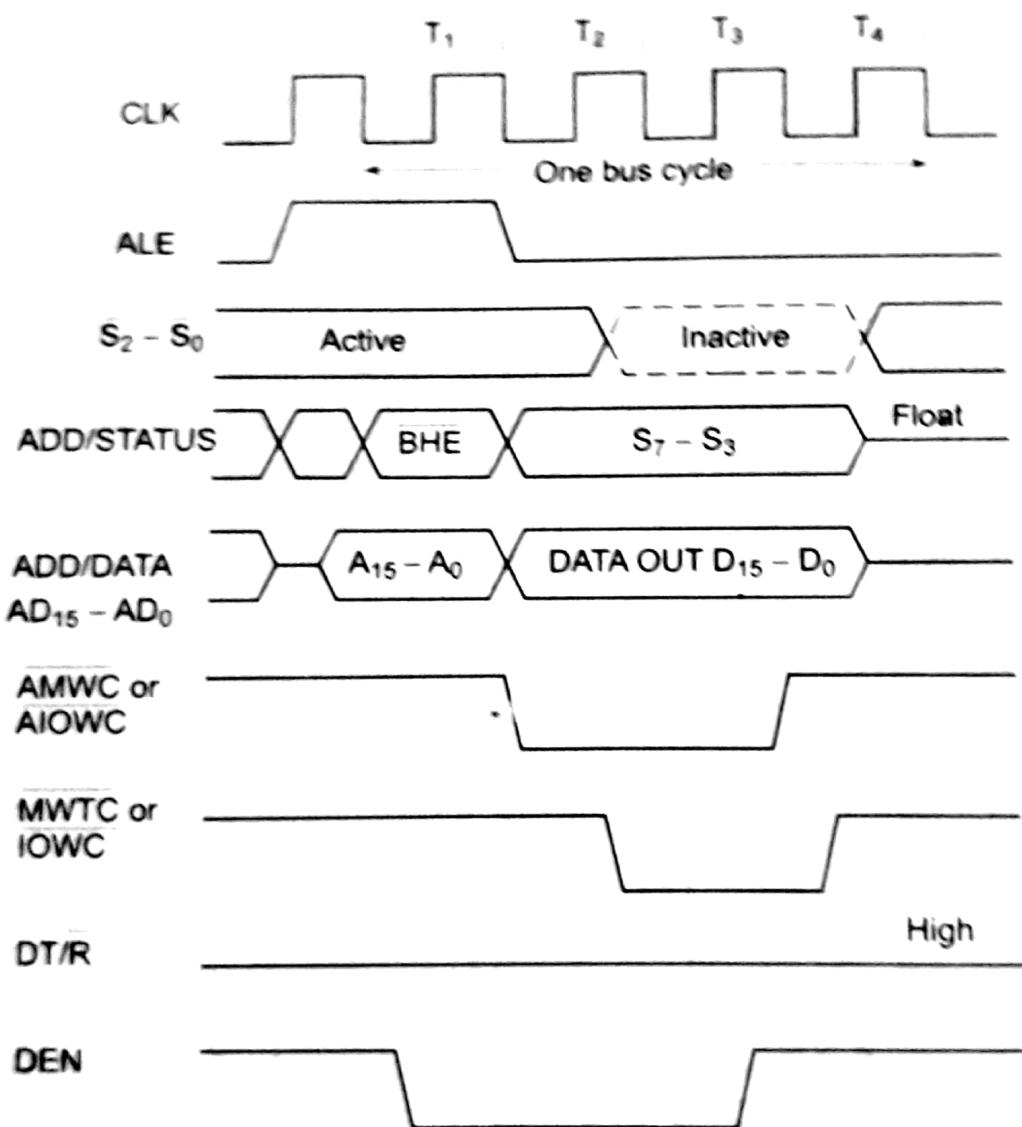


Fig. 1.16(b) Memory Write Timing in Maximum Mode

Timings for \overline{RQ} / \overline{GT} signals:

- The request / grant response sequence contains a series of three pulses as shown in timing diagram.
- The request / grant pins are checked at each rising pulse of clock input.
- When a request is detected and if the conditions for valid HOLD request are satisfied, the processor issues a grant pulse over \overline{RQ} / $\overline{GT_0}$ pin immediately during T_4 (current) or T_1 (next) state.

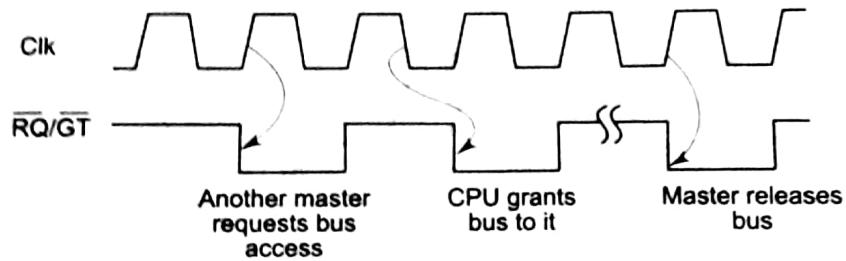


Fig. 1.16 (c) $\overline{RQ}/\overline{GT}$ Timings in Maximum Mode

- when the requesting master receives this pulse, it accepts the control of the bus.
- The requesting master uses the bus till it requires.
- When it is ready to relinquish the bus, it sends a release pulse to the processor using the $\overline{RQ}/\overline{GT}$ pin.