

Special purpose Programmable Peripheral Device and their Interfacing

- In the last few classes, we discussed few general purpose peripheral devices along with their interfacing techniques.
- All the peripheral device provide the interface between the CPU and slow electro-mechanical processes or devices.
All these peripherals (interfaces) were taken care by the CPU using interrupt mechanism or polling techniques.
However, due to the low speed of the processes, a considerable amount of time of CPU gets consumed in the interface and communication activities, resulting in reduced overall efficiency and low processing speed.
- To minimize the slow speed I/O communication overhead, a set of dedicated programmable peripheral devices have been introduced.

→ Once initiated by the CPU, these programmable peripheral devices take care of all the interface activities for which they have been designed.

Thus, the CPU becomes free from the interface activities and can execute its main task more efficiently.

→ Some of the general purpose programmable peripheral devices include

- ① Programmable Interval Timer 8254
- ② programmable Interrupt controller 8259A
- ③ The Keyboard /Display controller 8279
- ④ Programmable communication interface 8251 USART
- ⑤ DMA controller 8257

Programmable Interval Timer 8254 :

- It is not possible to generate an arbitrary time delay precisely using delay routines.
- Intel's 8254 programmable counter/timer device facilitates the generation of accurate time delays
- When 8254 is used as timing and delay generation peripheral, the micro processor becomes free from the tasks related to counting process and can execute the programs in memory, while the timer device can perform the counting tasks. This minimizes the software overhead on the micro processor.

Architecture and Signal descriptions :

- The programmable timer device 8254 contains three independent 16 bit counters, each with a maximum count rate of 10MHz. Thus, it is possible to generate three totally independent delay or maintain three independent counters simultaneously.
- All the three counters can be independent controlled by programming the three internal command word registers.
- The 8 bit, bidirectional data buffer interfaces the internal circuit of 8254 to microprocessor system bus.
- Data is transmitted or received by the buffer upon the execution of IN or OUT instruction.
- The read/write logic controls the direction of data buffer depending on whether it is read operation or write operation.
(IN reads data while OUT writes data to a peripheral)

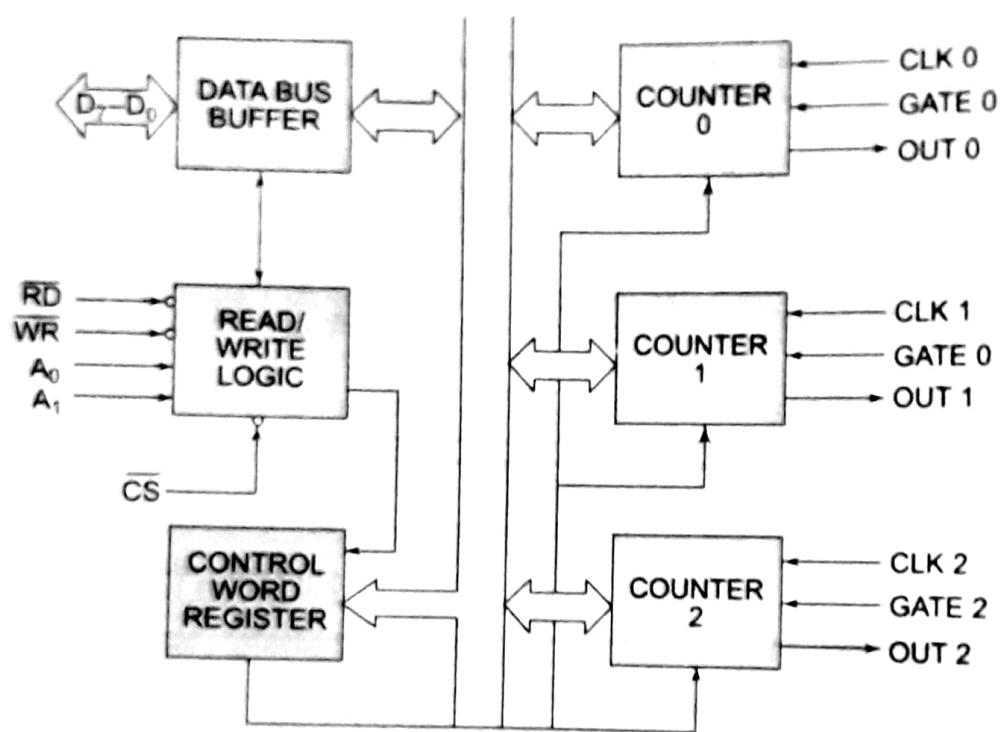


Fig. 6.1(a) Internal Block Diagram of 8254

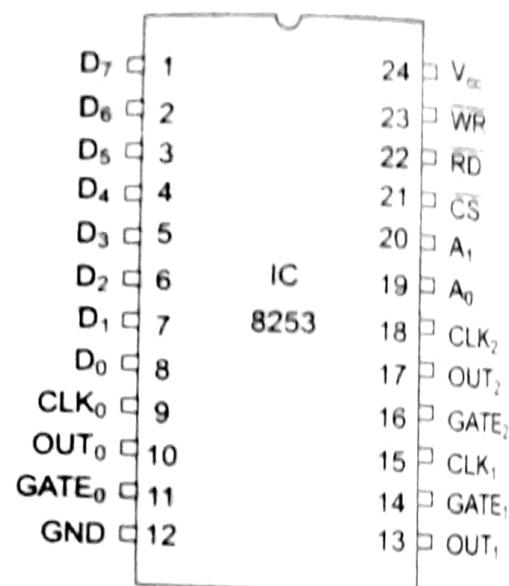


Fig. 6.1(b) Pin Configuration of 8254

- The three counters are independent of each other in operation, but they are identical to each other in organization.
- There are all 16 bit presettable, down counters, able to operate either in BCD or in hexadecimal mode.
- The mode control word register can be used for writing or reading the count value into or from the respective count register using OUT and IN instruction.
- The peculiarity of 8254 counters is that they can be easily read on line without disturbing the clock input to the counter.

This facility is called as "on the fly" reading of counters and is invoked using 9 mode control word.

- A₀, A₁, P₀ are the address input pins and are required internally for addressing the mode control word registers and the three counter registers. A low on \bar{CS} enables the 8254.

→ A control word register accepts the 8 bit control word written by the microprocessor and stores it for controlling the complete operation of the specific counter.

Note : The control word register can only be written and cannot be read.

→ The CLK, GATE and OUT pins are available for each of the three timer channels.

Their functions will be clear when we try to understand the various modes of operation of 8254.

Table 6.1 Selected Operations for Various Control Inputs of 8254

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A_1	A_0	<i>Selected Operation</i>
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation (tristated)
0	1	1	x	x	No Operation (tristated)
1	x	x	x	x	Disabled (tristated)

control word Register :

- 8254 can operate in any one of the six different modes.
- A control word must be written to the respective control word register by the microprocessor to initialize each of the counters of 8254 to decide its operating mode.
- Each of the counter works independently depending on the control word decided by the programmer as per the needs.
In other words, all the counters can operate in any one of the modes or they may be even in different modes of operation at a time.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Control Word Format

SC ₁	SC ₀	OPERATION
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

SC-Select Counter Bit Definitions

RL ₁	RL ₀	OPERATION
0	0	Latch Counter for 'ON THE FLY' reading
0	1	Read/Load Least Significant Byte only
1	0	Read/Load MSB only
1	1	Read/Load LSB first then MSB

RL-Read/Load Bit Definitions

M ₂	M ₁	M ₀	Selected Mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

M₂M₁M₀ Mode Select Bit Definitions

BCD	Operation
0	Hexadecimal Count
1	BCD Count

HEX/BCD Bit Definition

Fig. 6.2 Control Word Format and Bit Definitions

6.1.3 Operating Modes of 8254

Each of the three counters of 8254 can be operated in one of the following six modes of operation:

1. Mode 0 (Interrupt on terminal count)
2. Mode 1 (Programmable monoshot)
3. Mode 2 (Rate generator)
4. Mode 3 (Square wave generator)
5. Mode 4 (Software triggered strobe)
6. Mode 5 (Hardware triggered strobe)

MODE 0:

- This mode of operation is known as interrupt on terminal count.
- In this mode, the output is initially low after the mode is set. The output remains low even after the count value (5) is loaded in the counter.
- The counter starts decrementing the count value after the falling edge of the clock, if the GATE input is high.
- When the terminal count is reached, the output goes high until the counter register is loaded with new value.

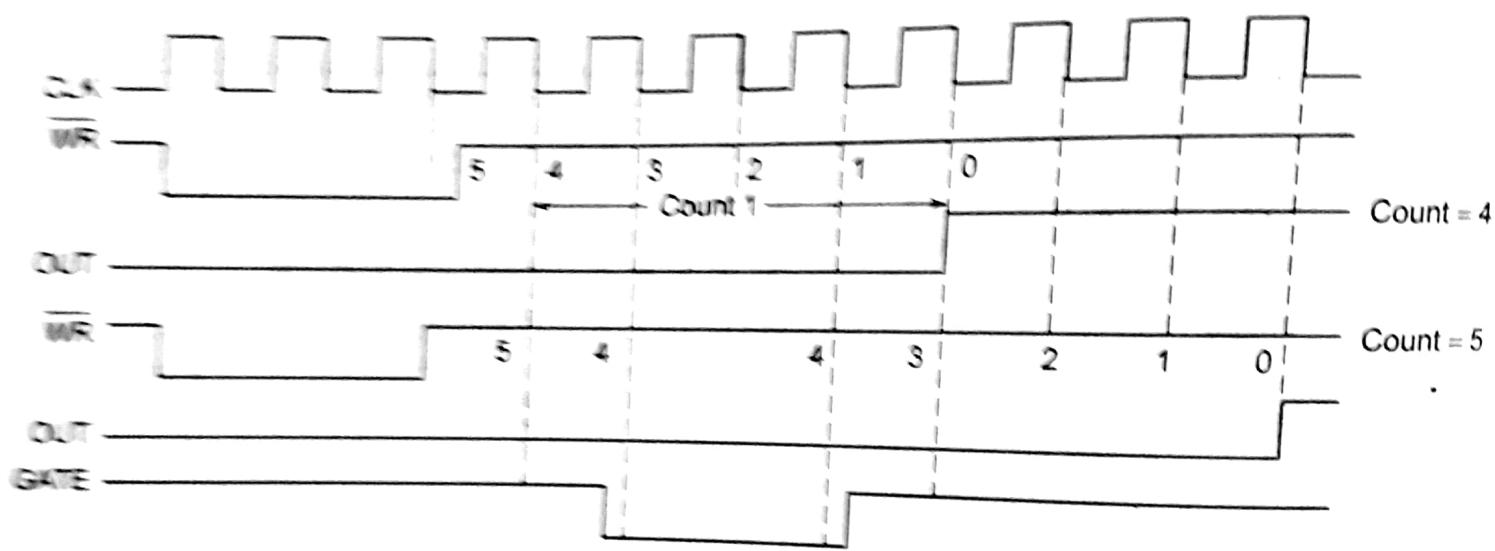


Fig. 6.3 Waveforms of \overline{WR} , OUT and GATE in Mode 0

MODE 1 :

- This mode of operation is called programmable one-shot mode.
- In this mode, 8254 is used as a mono stable multivibrator.
- The duration of the quasi-stable state of the mono stable multivibrator is decided by the count value loaded in count register.
- The gate input is used as trigger input in this mode of operation.
- Normally the output remains high till suitable count is loaded in count register and a trigger is applied.
- After the trigger is applied, the output goes low and remains low till the ~~trigger~~ - count becomes zero.
- If another count is loaded when the output is already low , it does not disturb the previous count, till a new trigger is applied at Gate input .

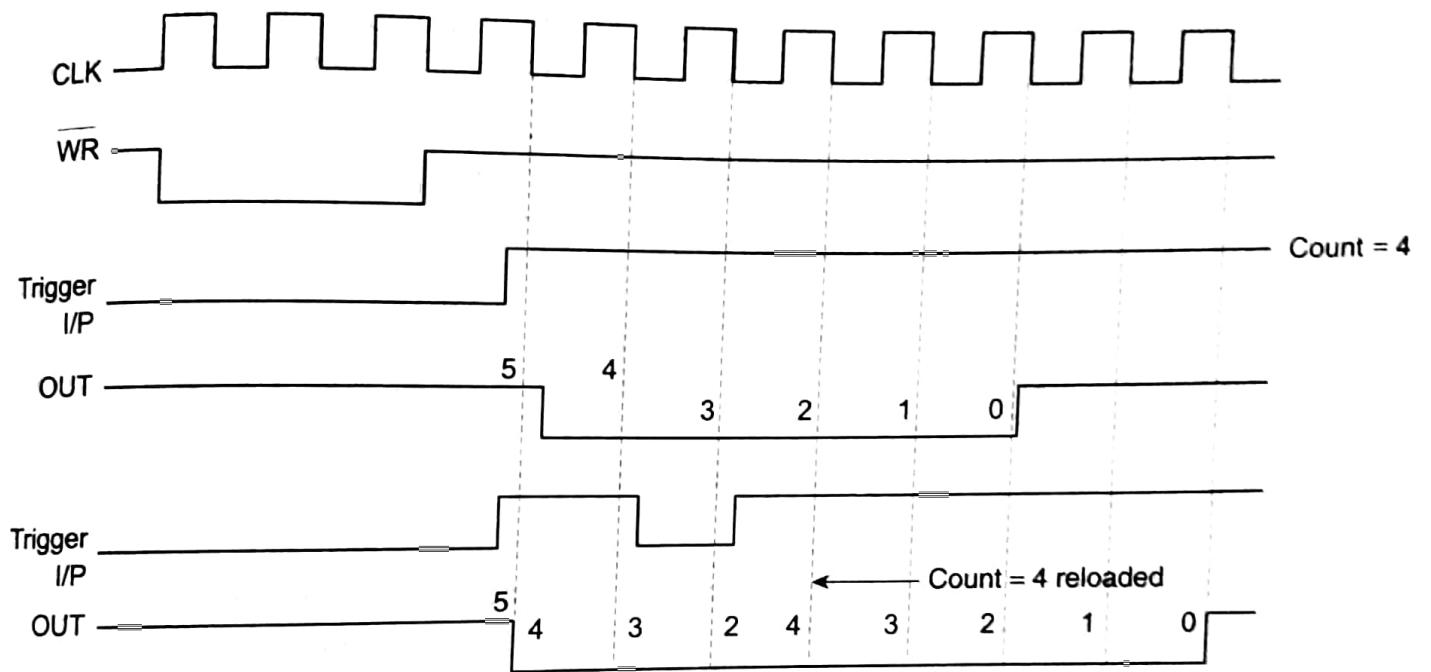


Fig. 6.4 \overline{WR} , GATE and OUT Waveforms for Mode 1

MODE 2:

- This mode is called either rate generator or divide by N counter.
- In this mode, if N is loaded as the count value, then after $(N-1)$ cycles, the output becomes low only for one clock cycle.
- The count N is reloaded and again the output becomes high and remains so for $(N-1)$ clock pulses.
- The output is normally high after initialization or even a low signal on Gate input can force the output to go high.
- If the Gate is high, the counter starts counting down from the initial value.
- The counter generates an active low pulse at the output initially, after the counter is loaded with a count value. Then count down starts and whenever the count becomes zero another active low pulse is generated at the output.

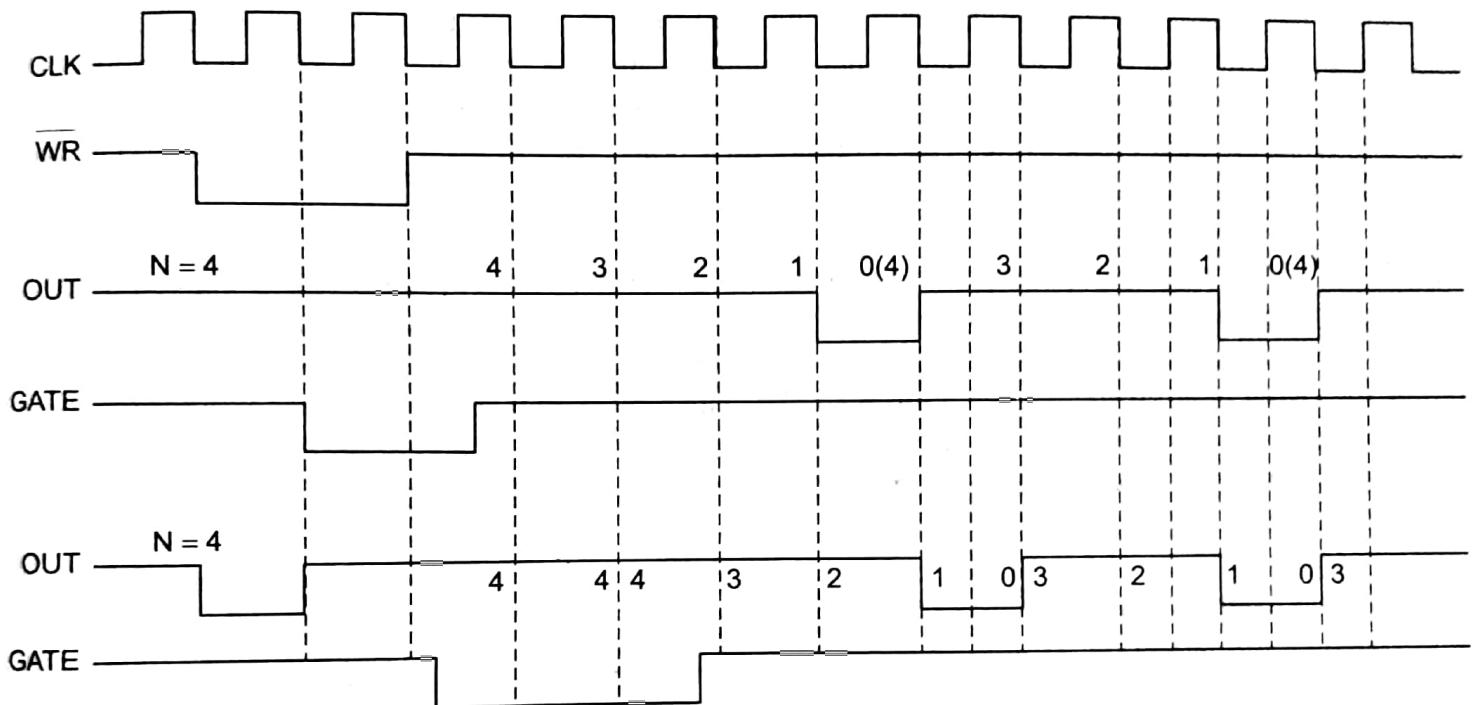


Fig. 6.5 Waveforms at Pin WR and OUT In Mode 2

MODE 3 :

- In this mode, 8254 is used as a square wave generator.
 - The operation of this mode is similar to mode 2.
 - When, count N loaded is even, then for half of the count, the output remains high and for the remaining half it remains low.
 - If the count loaded is odd, the first clock pulse decrements it by 1, resulting in an even count value. Then the output remains high for half of the new count and goes low for the remaining half.
 - The above procedure is repeated continuously, resulting in generation of a square wave.
- Note : In case of odd count, the output is high for longer duration and low for shorter duration.

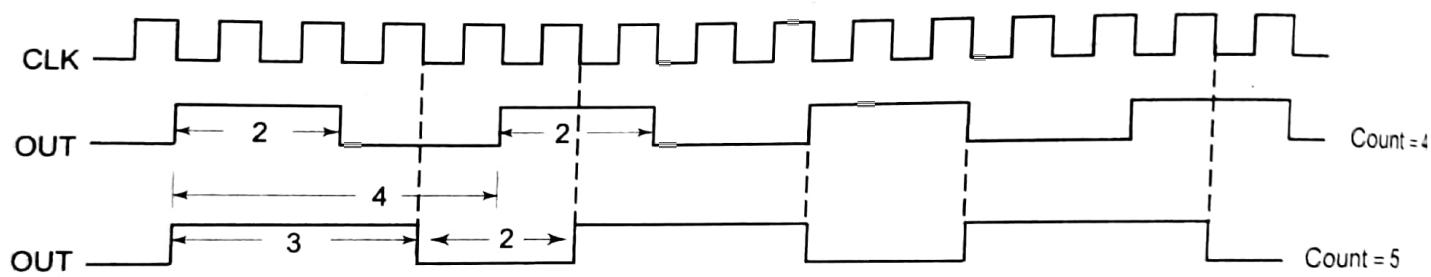


Fig. 6.6 Waveforms for Mode 3

- MODE 4 : operation is known as
- This mode of software triggered mode.
 - After the mode is set, the output goes high.
 - When a count is loaded, counting down starts.
 - On terminal count, the output goes low for one clock cycle and then it goes high.
 - This low pulse can be used as a strobe, while interfacing the microcontroller with other peripherals.
 - The count is inhibited and the count value is latched, when the GATE signal goes low.
 - If a new count is loaded into the count register, while the previous counting is in progress, it is accepted from next clock cycle. The counting then proceeds from new count value.

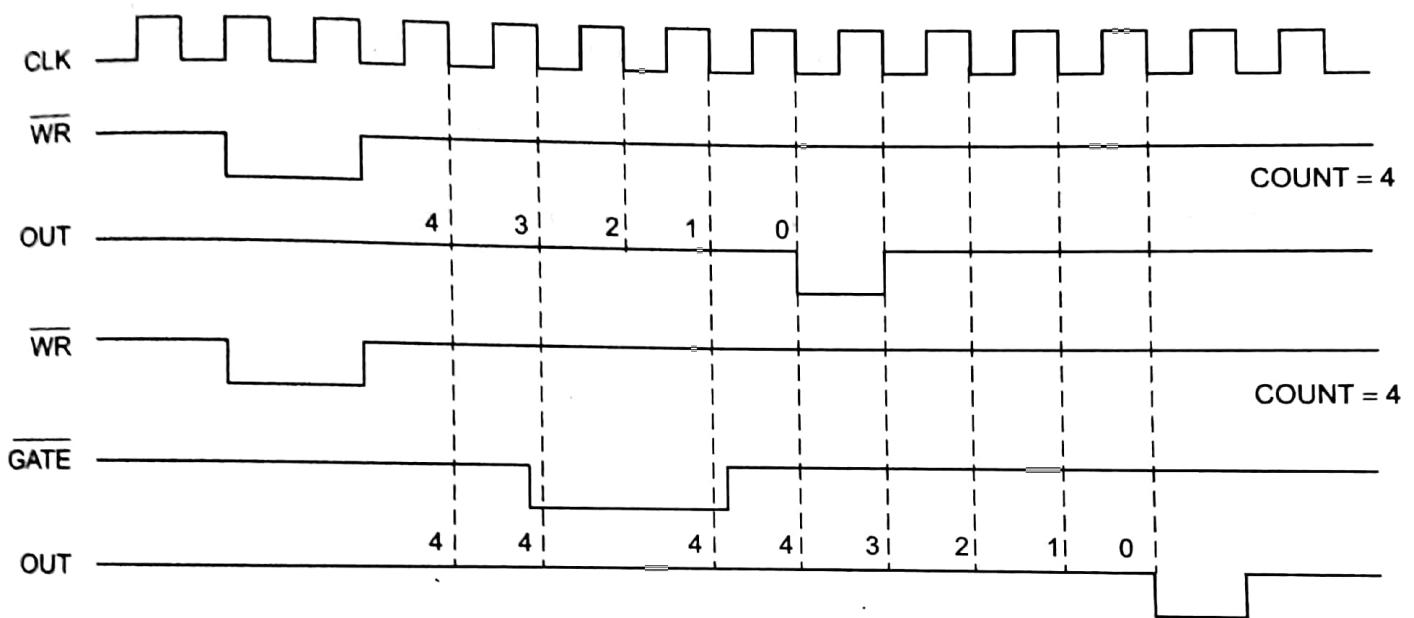


Fig. 6.7 WR, GATE and OUT Waveforms for Mode 4

MODE 5:

- This mode of operation also generates a strobe in response to the rising edge at the trigger input.
- This mode may be used to generate a delayed strobe in response to an externally generated signal.
- Once this mode is programmed and the counter is loaded, the output goes high.
- The counter starts counting after the rising edge of trigger input (GATE).
- The output goes low for one clock period, when the terminal count is reached.
- The output will not go low until the counter content becomes zero after the rising edge of any trigger.
- The GATE input in this mode is used as trigger input.

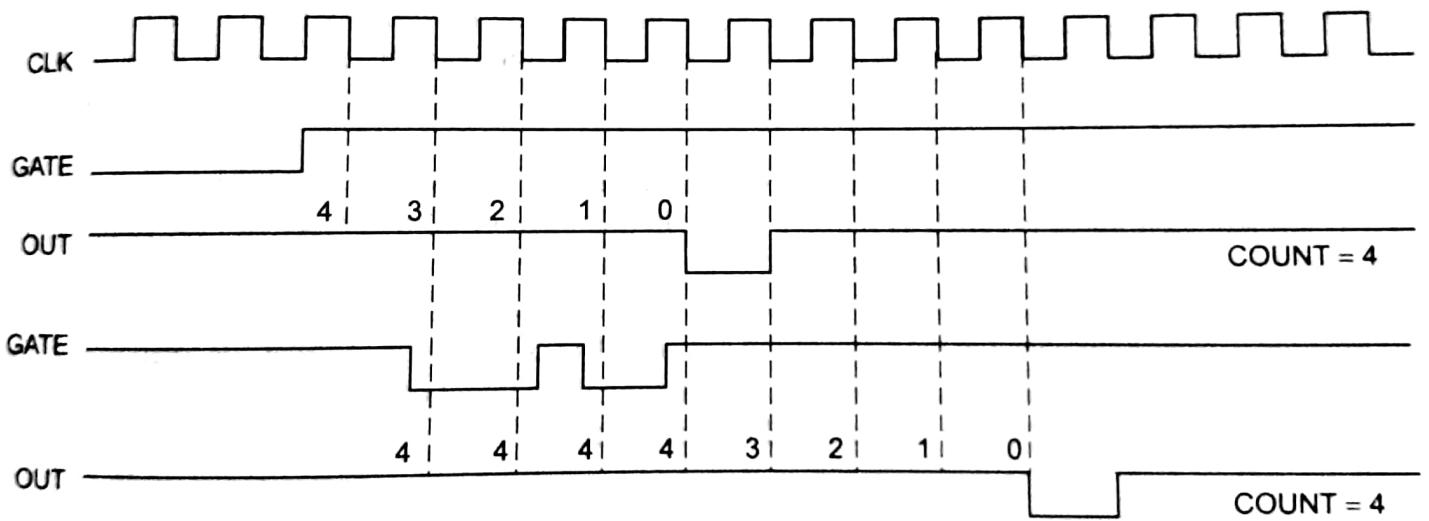


Fig. 6.8 Waveforms in Mode 5

Table 6.2 shows the selection of different mode control words and counter register bytes depending upon address lines A_1 and A_0 .

Table 6.2 Selection of Count Registers and Control Word Register with A_1 and A_0

<i>Selected Register</i>	A_1	A_0
Mode Control Word Counter 0	1	1
Mode Control Word Counter 1	1	1
Mode Control Word Counter 2	1	1
Counter Register Byte Counter 2 LSB	1	0
Counter Register Byte Counter 2 MSB	1	0
Counter Register Byte Counter 1 LSB	0	1
Counter Register Byte Counter 1 MSB	0	1
Counter Register Byte Counter 0 LSB	0	0
Counter Register Byte Counter 0 MSB	0	0

Programming and Interfacing 8254

→ There are two types of write operation

in 8254, viz

(i) Writing a control word into control word register

(ii) writing a count value into a count register

→ The control word register, accepts data from the data buffer and initializes the counters as required.

→ The control word register contents are used for

(a) initializing operating mode (mode 0 - mode 4)

(b) selection of counters (counter 0 - counter 2)

(c) choosing binary | BCD counters

(d) loading of the counter registers

Note: The mode control register is a write only register and the CPU cannot read its contents.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	0	0	X	X	X	X

D₇-D₆ = SC1, SC0—Specify the counter to be selected
as in Fig. 6.2

D₅-D₄ = 00—Designate counter latching operation

X = Don't Care—All other bits are neglected

Fig. 6.9 Mode Control Word for Latching Count

- One can directly write the mode control word for counter 2 or counter 1, prior to writing the control word for counter 0.
- Mode control word register has a separate address so that it can be written independently.
- A count register ^{must be} loaded with the count value in the same byte sequence that was programmed in the mode control word of that counter, using the bits RL₀, RL₁.
- The loading of count registers for different counters is again sequence independent.
- One can directly write the 16 bit count register for counter 2 before writing counter 0 and 1, but the two bytes in a count must be written in the byte sequence programmed using RL₀ and RL₁ bits of the mode control word of counter.

- All the counter in 8254 are down counter, hence their count values go on decrementing if the CLK input pin is applied with a valid clock signal.
- A max. count is obtained by loading all zeros into a count register, ie. 2^{16} for binary counting and 10^4 for BCD counting.
- The 8254 responds to the negative clock edge of the clock input.
- The maximum operating clock frequency of 8254 is 2.6 MHz . (2.6 mHz)
For higher frequencies, one can use timer 8254, which operates upto 10 MHz maintaining compatibility with 8254.

→ In most of the practical applications, the counter is to be read and depending on the contents of the counter a decision is to be taken.

→ In 8254, the 16 bit contents of counter can simply be read using successive 8 bit IN instructions.

→ The mode control register cannot be read for any of the counters.

There are two methods for reading 8254 counter registers.

① In this method, either the clock or the ~~counter~~ counting procedure (using GATE) is inhibited to ensure a stable count.

Then the contents are read by selecting the suitable counter way A₀, A₁ and executing the IN instruction.

The first IN instruction reads the LCB byte.

The second IN instruction reads the MCB byte.

② In this method, the counter can be read while counting is in progress.

This method is also known as reading on the fly.

The content of a counter can be read 'on fly' using a newly defined control word register format for on line reading of count register.

Writing a suitable control word, in the mode control register, internally latches the contents of counter.

Sol

Design a programmable timer using 8254 and 8086, interface an 8254 at an address 0040H for counter 0 and write the following ALPs.

The 8086 and 8254 run at 6MHz and 1.5MHz respectively

- (i) To generate a square wave of period 1ms
- (ii) To interrupt the processor after 10ms
- (iii) To derive a monostable pulse with programmable state duration 5ms.

Sol

Based on the address 0040H for counter 0 we can use the LCB 1~~6~~ address lines for the CS logic and the counter selection

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	0	0	0	= 40H for counter 0
0	0	0	0	0	0	1	0	= 42H for counter 1
0	0	0	0	0	1	0	0	= 44H for counter 2
0	0	0	0	0	1	1	0	= 46H for CWR.

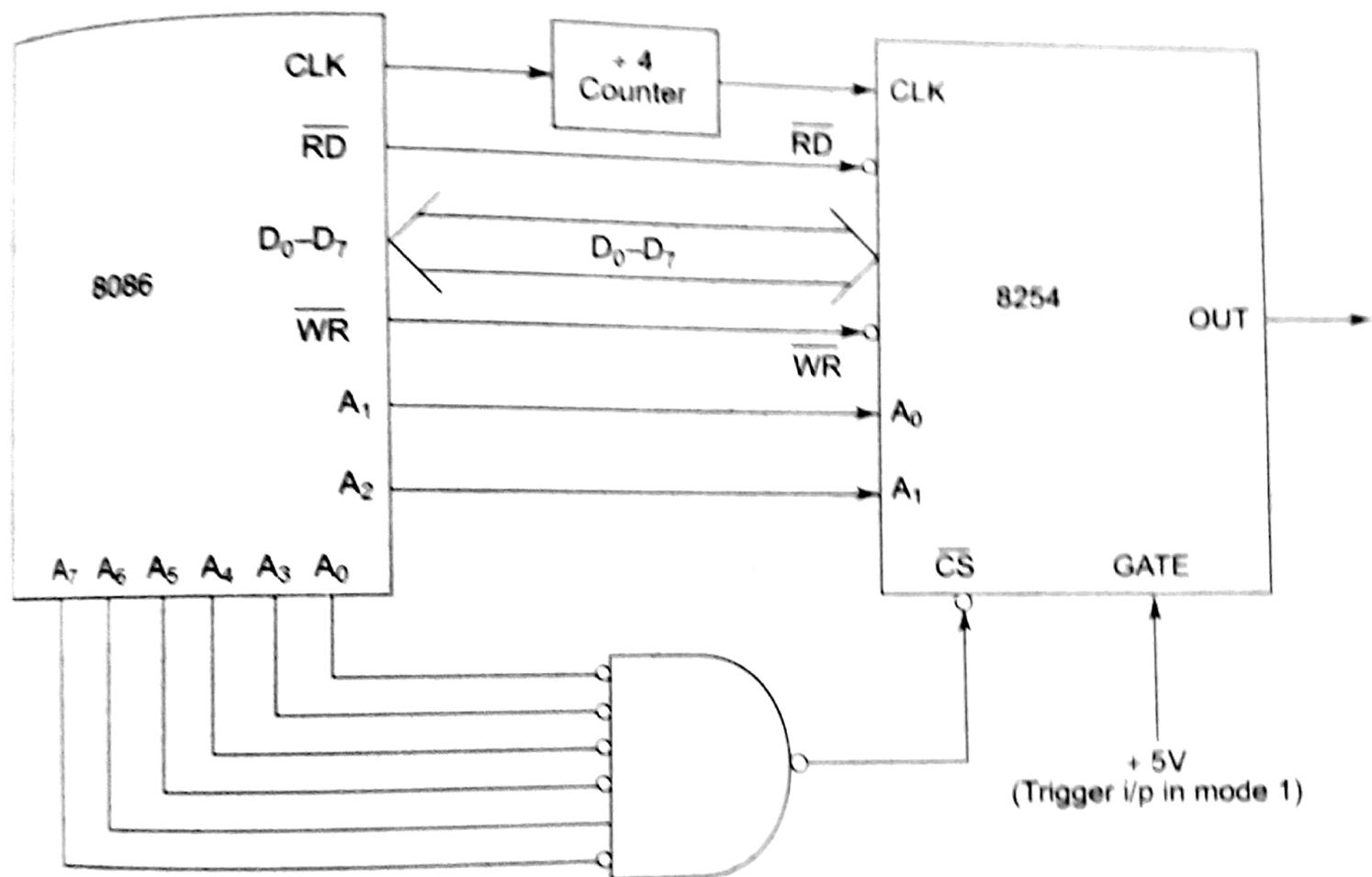


Fig. 6.10 Interfacing 8254 with 8086 for Problem 6.1

(i) Generation of square wave of period 1ms

- For generating a square wave, 8254 should be operated in mode 3.
- Select counter 0
- Select the counter operating in C_{A} mode.
- We need to calculate the count value for generating a 1ms time period.

$$f = 1.5 \text{ MHz} \text{ for } 8254$$

$$\therefore T = \frac{1}{1.5 \times 10^6} = 0.66 \mu\text{s}$$

If N is the no. of states for 1ms

$$N = \frac{1 \times 10^{-3}}{0.66 \times 10^{-6}} = 1.5 \times 10^3 \\ = 1500 \text{ state}$$

∴ count value N should be initialized to 1500.

→ The control word is decided as

SC1	SC0	RL1	RL0	M2	M1	M0	BC1
0	0	1	1	0	1	1	1

= 3FH

The ALP is as follows:

```
CODE SEGMENT
ASSUME CS: CODE
START:    MOV AL, 37H
          OUT 46H, AL
          MOV AL, 00 ; write 00 decimal
                     ; in count reg
          OUT 40H, AL ;
          MOV AL, 15 ; word MCB is in
                     ; count reg.
          OUT 40H, AL ;
          MOV AH, 4CH
          INT 21H
CODE ENDS
END START.
```

(ii) Generating interrupt to the processor after 10ms.

- To generate interrupt to the processor after 10ms, the 8254 has to be operated in mode 0 (Interrupt on terminal count)
- OUT1 pin of 8254 connected to the interrupt input of processor
- count value (N)

$$N = \frac{10 \text{ ms}}{0.66 \mu\text{s}}$$
$$= \frac{10 \times 10^{-3}}{0.66 \times 10^{-6}} = 15000$$
$$= 3A98H.$$

$$N =$$

- Control word

SCI	SCO	RLI	RLO	M2	M1	M0	BCD
0	1	1	1	0	0	0	0

= 70H

∴ The ALP can be written as

```
CODE SEGMENT
ASSUME CS: CODE
START:    MOV AL, 70H
          OUT 46H, AL
          MOV AL, 98H ; Load 98H as LSB
                      ; of count
          OUT 40H, AL
          MOV AL, 3AH ;
          OUT 42H, AL ;
          MOV AH, 4CH
          INT 21H
CODE ENDS
END START.
```

(iii) Derive a monoshot pulse with quantifiable state duration 5ms.

T

- To generate a monoshot pulse, we have to operate 8254 in mode 1 (programmable monoshot).
- we use counter 2.
- The OUT2 signal normally remains high after the counter is loaded, till the trigger is applied. After the application of trigger signal, the output goes low in the next cycle, countdown starts, and whenever count becomes zero, the output goes high.

→ ~~Set~~ Count value (N)

$$N = \frac{5 \times 10^3}{0.66 \times 10^{-6}} = 2500.$$
$$= 1D4CH.$$

→ Control word.

SC1	SC0	RL1	RL0	m2	m1	m0	BCD
1	0	1	1	0	0	1	0

The ALP is as follows:

```
CODE SEGMENT  
ASSUME CS: CODE  
START:  
    MOV AL, B2H  
    OUT 46H, AL  
    MOV AL, 4CH  
    OUT 44H, AL  
    MOV AL, 1D  
    OUT 44H, AL  
    MOV AH, 4CH ; Return to DS  
    INT 21H  
CODE ENDS  
END START.
```

Prob:

Interface 8254 with 8086 at counter 0 address 7430H and write a program to call subroutine after 100ms. Assume that the system clock available is 2MHz.

Sol

→ Based on the address given to counter 0 we can see the least significant 16 lines for CS of 8254 and the connection.

Port	Hex Addr.	Primary Address	Address
counter 0	7430H	0111 0100	0011 0000
counter 1	7432H	0111 0100	0011 0010
counter 2	7434H	0111 0100	0011 0100
CWR	7436H	0111 0100	0011 0110

∴ A₁ A₂ address lines are used for selecting of timer
remaining address lines are used for CS enabling of 8254.

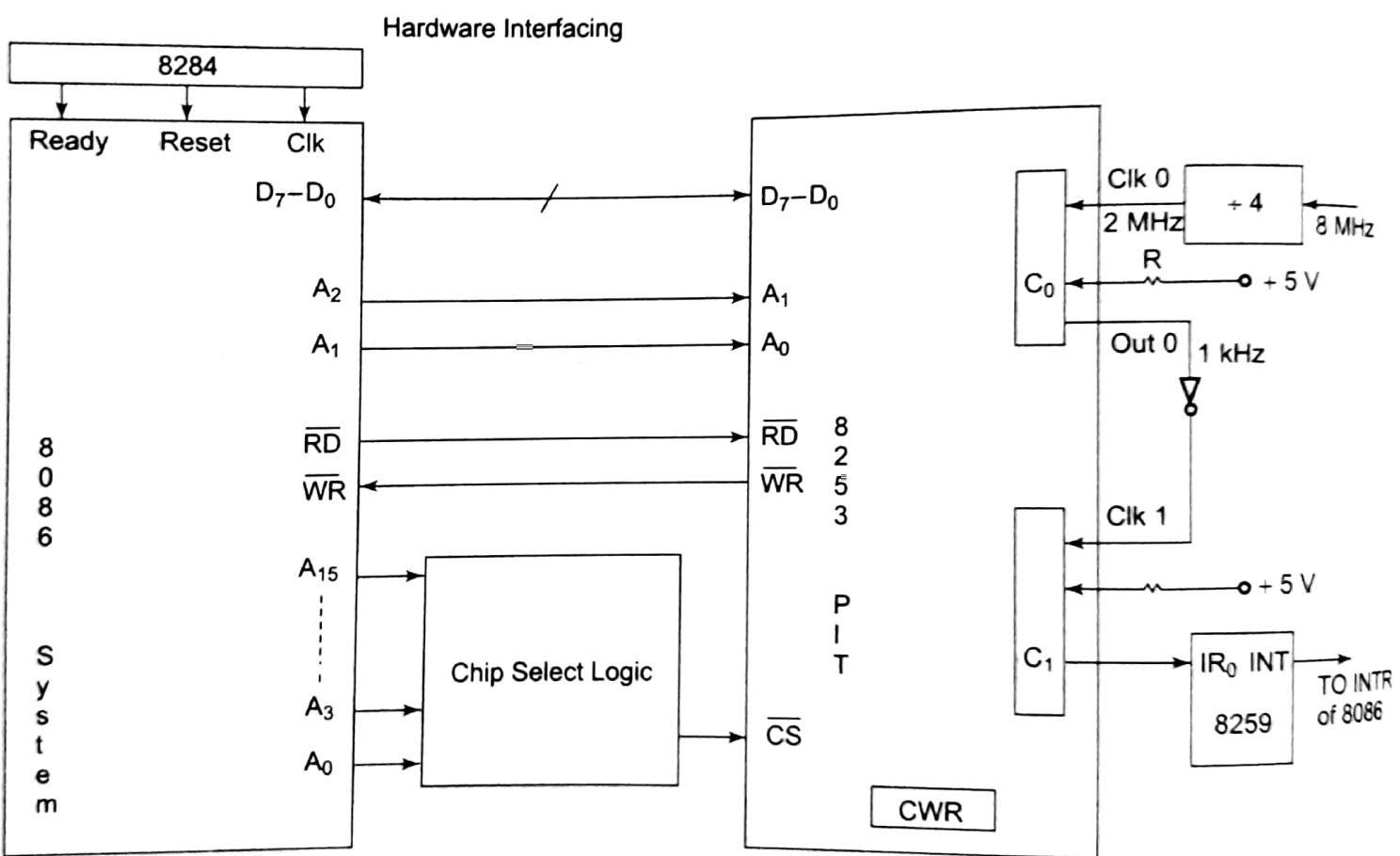


Fig. 6.11 Interfacing 8254 with 8086 for Problem 6.2

- Input circuit signal to counter 0 is 2MHz.
 counter 0 is utilized in mode 3 to generate
 a square wave of frequency 1kHz.
- output square wave of counter 0 is given
 as circuit signal to counter 1.

counter 1 is used in mode 0 (interrupt on
 terminal count)

- Count value of ~~first~~ counter 0

$$N_0 = \frac{\text{input freq}}{\text{output freq}} = \frac{2\text{MHz}}{1\text{kHz}} = 2000$$

we have to load only mSB ie (20)_D. LSB is initialized automatically to (00)_D

- count value of counter 1

$$N_1 = \frac{100\text{ms}}{1\text{ms}} = 100$$

we have to load only mSB (10)_D

- CWR for counter 0

SCI	SCE	RLI	RLO	m ₂	m ₁	m ₀	BCD
0	0	1	0	0	1	1	→ 27H

- CWR for counter 1

SCI	SCE	RLI	RLO	m ₂	m ₁	m ₀	BCD
0	1	1	0	0	0	0	→ 61H

~~... to load address~~

```

ASSUME CS : CODE, SS : STACK
STACK SEGMENT
TOP DW 100 DUP (?)
STACK ENDS
CODE SEGMENT
START : MOV AX, STACK
        MOV      SS, AX
        LEA      SP, TOP + 200
MOV    DX, 7436 H      ; CWR address is transferred to DX
register.
MOV    AL, 27H          ; Initialization of counter 0.
OUT   DX, AL.
MOV    AL, 61H          ; Initialization of counter 1
OUT   DX, AL
MOV    AL, 20H
MOV    DX, 7430H         ; Count 20 loaded in BCD counter 0 MSBs.
OUT   DX, AL
MOV    AL, 01H
MOV    DX, 7432 H         ; Count 01 is loaded in MSBs of counter 1
OUT   DX, AL
STI
MOV    AH, 4 CH          ; Set IF Flag.
INT   21H
CODE ENDS
END   START

```

Program 6.4 ALP for Problem 6.2