

Till now, we studied some common interfacing methods for I/O ports and have also solved some problems based on I/O ports.

In all the above problems, the ports were either input or output, but using programmable peripheral interface (PPI) chip 8255, the same port may be programmed to work as input or as output port.

Hence the above chip is also known as

Programmable input output (PIO) device.

Programmable
input output

Programmable I/O port output (P20) 8255

Programmable peripheral interface (PPI)

- The Intel's 8255 is designed for use with Intel's 8 bit, 16 bit and higher capability microprocessors.
- It has 24 input / output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines.
- The two groups of 24 pins are named as Group A and Group B.
- Each of these two groups contain a subgroup of 8 8 bit lines called as 8 bit port and another subgroup of four 8 bit lines or a 4 bit port.
- Group A contains 8 bit port A and 4 bit port C upper.
- Group B contains 8 bit port B and 4 bit port C lower.

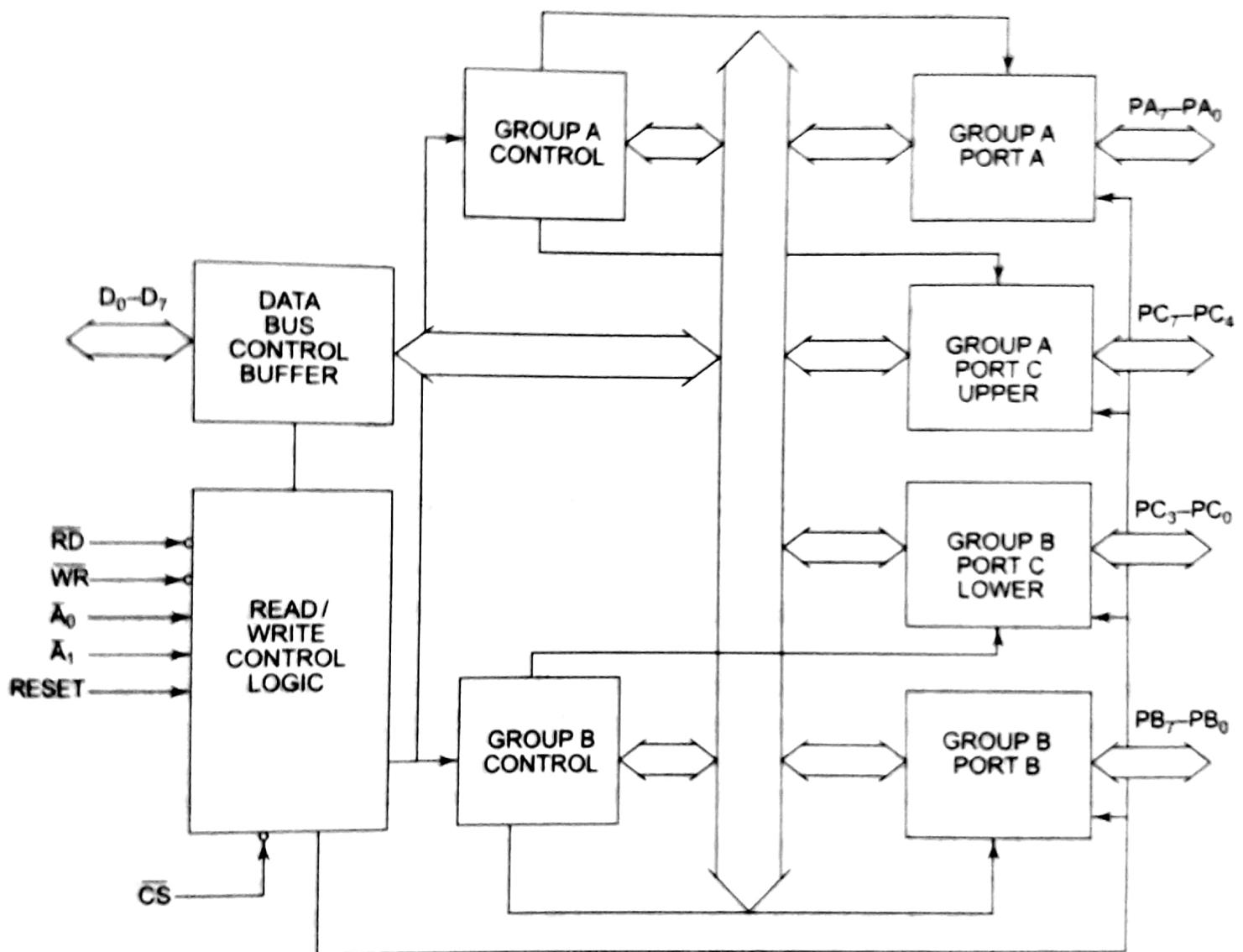


Fig. 5.17(a) 8255 Internal Architecture

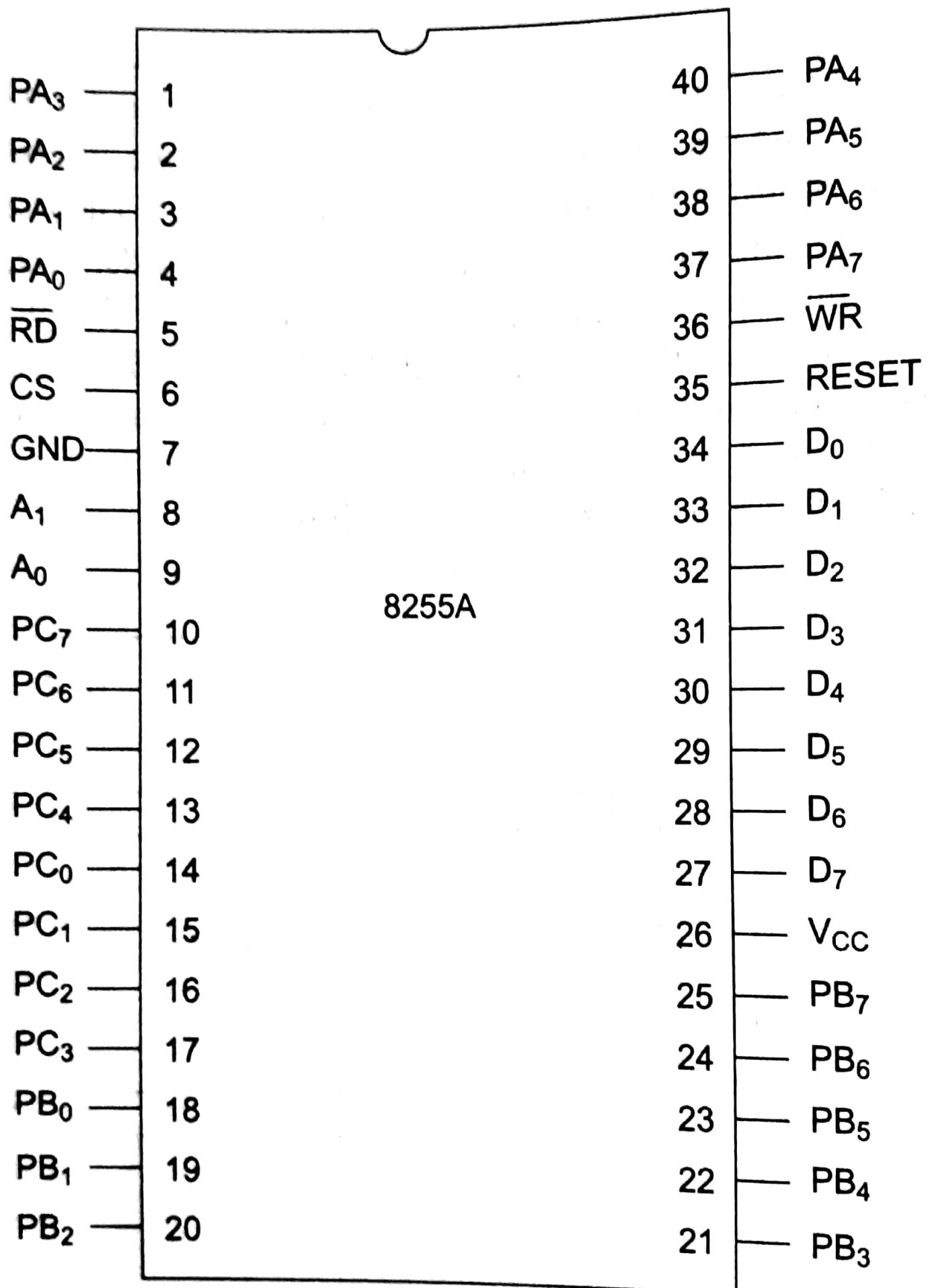


Fig. 5.17(b) 8255A Pin Configuration

→ Port C upper and Port C lower can also be used in combination as an 8bit port C.

Both the port C's are assigned same address

→ Thus we have three 8 bit I/O ports, or two 8 bit and two 4 bit I/O ports from 8255.

→ All the ports can function independently as input or output ports.

→ This can be achieved by programming the bits of an internal register of 8255 known as the ~~control~~ control word register (CWR).

PA₇-PA₀ These are eight port A lines that act as either latched output or buffered input lines depending upon the control word loaded into the control word register.

PC₇-PC₄ Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode1 or mode 2.

PC₃-PC₀ These are the lower port C lines, other details are the same as PC₇-PC₄ lines.

PB₀-PB₇ These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

RD This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.

WR This is an input line driven by the microprocessor. A low on this line indicates write operation.

CS This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signals are neglected.

A₁-A₀ These are the address input lines and are driven by the microprocessor. These lines ($A_1 - A_0$) with RD, WR and CS form the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e. three ports and a control word register as given in Tables 5.9 (a), (b) and (c).

In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A_0 and A_1 pins of 8255 are connected with A_1 and A_2 respectively.

Table 5.9(a)

\overline{RD}	\overline{WR}	\overline{CS}	A_1	A_0	<i>Input (Read) cycle</i>
0	1	0	0	0	Port A to data bus
0	1	0	0	1	Port B to data bus
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus

Table 5.9 (b)

\overline{RD}	\overline{WR}	\overline{CS}	A_1	A_0	<i>Output (Write) cycle</i>
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

Table 5.9 (c)

\overline{RD}	\overline{WR}	\overline{CS}	A_1	A_0	<i>Function</i>
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

modes of operation of 8255:

Two basic modes of operation possible

- ① 8 Z/Io mode.
- ② Bit-Set Reset mode (BSR).

In Z/Io mode, the 8255 ports work as programmable Z/Io ports.

In BSR mode only port C ($PC_0 - PC_7$) can be used to set or reset its individual port bits.

Under Z/Io mode of operation, there are three modes of operation of 8255 to support different applications known as mode 0, mode 1 and mode 2.

BSR Mode :

- In this mode , any of the 8 bits of Port C can be set or reset depending on the B₀ bit of the control word.
- The bit to be set or reset is selected by the bit select flags B₃, B₂, B₁ of CWR .

Table 5.10

B_3	B_2	B_1	<i>Selected Bits of port C</i>
0	0	0	B_0
0	0	1	B_1
0	1	0	B_2
0	1	1	B_3
1	0	0	B_4
1	0	1	B_5
1	1	0	B_6
1	1	1	B_7

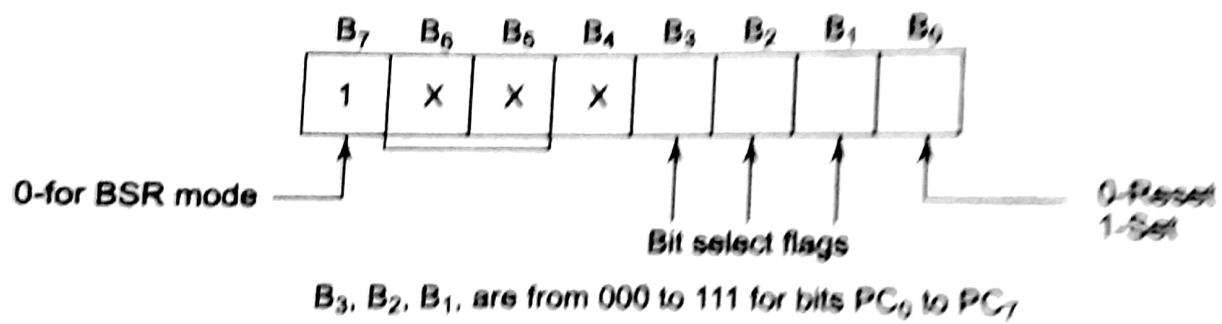


Fig. 5.18(a) BSR Mode Control Word Register Format

I/O modes:

① Mode 0 (Basic I/O mode):

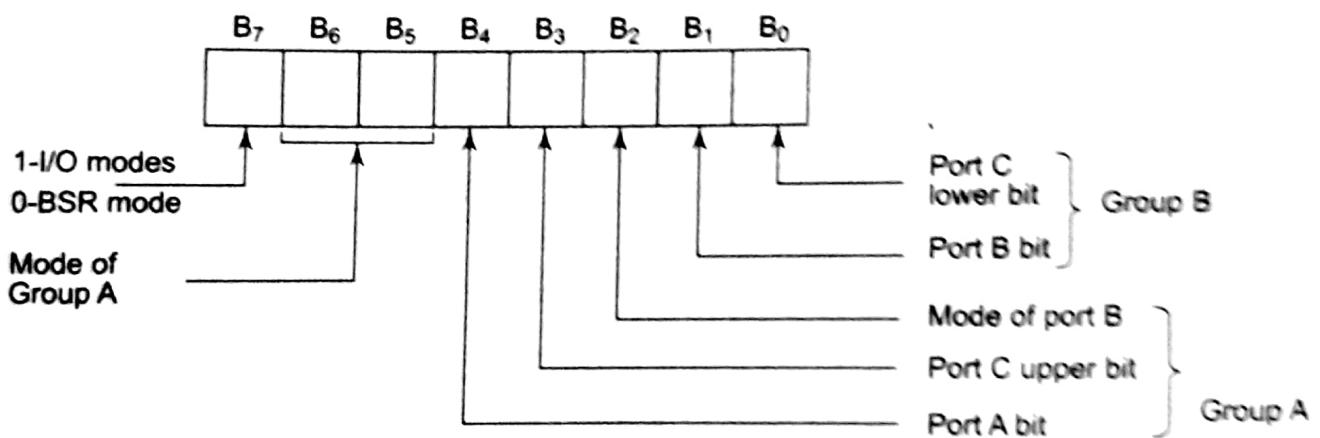
This mode is also known as basic input/output mode. This mode provides a simple input and output capability using each of the three ports.

Data can be read from and written to the input and output ports respectively after appropriate initialization.

The salient features of this mode are as listed below:

- (i) Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combinedly used as a third 8-bit port.
- (ii) Any port can be used as an input or output port.
- (iii) Output ports are latched. Input ports are not latched.
- (iv) A maximum of four ports are available so that overall 16 I/O configurations are possible.

All these modes can be selected by programming a register internal to 8255, known as Control Word Register (CWR) which has two formats. The first format is valid for I/O modes of operation, i.e. modes 1, mode 1 and mode 2 while the second format is valid for bit set/reset (BSR) mode of operation. This format is shown in Fig. 5.18(b).



Group A modes

B ₆	B ₅	Mode
0	0	mode 0
0	1	mode 1
1	0	mode 2
1	1	x

- (i) Port B mode is either 0 or 1 depending upon B₂ bit.
- (ii) A port is an output port if the port bit is 0 else it is input port

Fig. 5.18(b) I/O Mode Control Word Register Format

Problem based on mode 0 of 210 modes

① Interface an 8255 with 8086 to work as an 210 port. Initialize port A as output port, port B as input port and port C as output port.

Port A address should be 0740H.

Write a program to sense switch positions SW₀-SW₇ connected at port B. The sensed pattern is to be displayed on port A, to which 8 LED are connected, while port C lower displays the number of on switches out of the total eight switches.

----- WORD IS ASSIGNED UPON AS -----								Control word = 82H
B7	B6	B5	B4	B3	B2	B1	B0	
1	0	0	0	0	0	1	0	
I/O mode	Port A	Port	Port	Port	Port	Port	Port	
in mode 0	A,o/p	C,o/p		B,mode 0		B,i/p	C,o/p	

8255

I/O Address lines

Hex. Port
Addresses

Ports	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}	
PortA	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0740H
Port B	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0742H
Port C	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0	0744H
CWR	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0746H

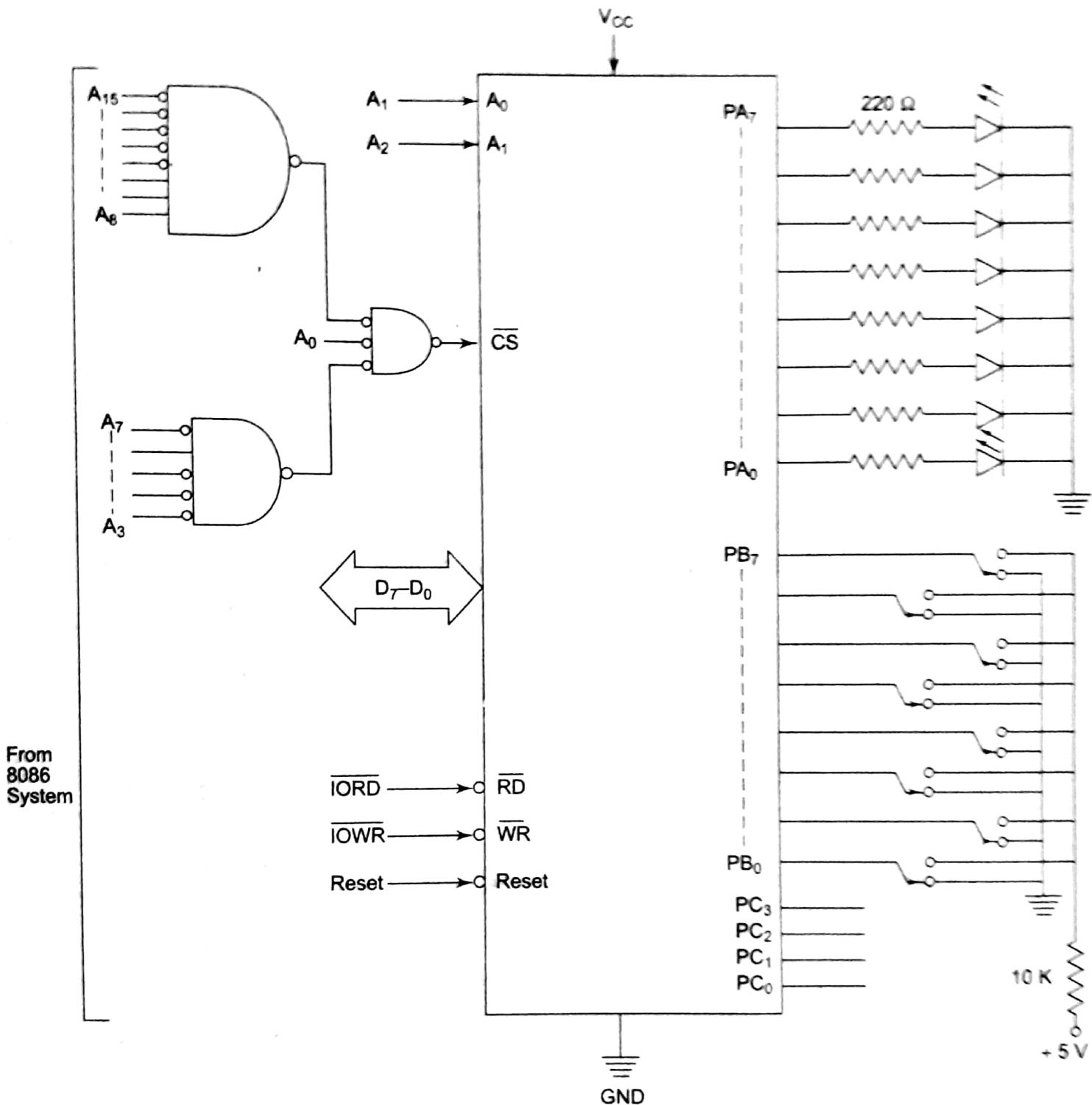


Fig. 5.19 8255 Interfacing with 8086 for Problem 5.10

The ALP for the problem is developed as follows:

```
MOV DX, 0746 H          ; Initialise CWR with
MOV AL, 82 H            ; control word 82H
OUT DX, AL              ;
SUB DX,04               ; Get address of port B in DX
IN AL, DX               ; Read port B for switch
SUB DX,02               ; positions in to AL and get port A address
                        ; in DX.
OUT DX, AL              ; Display switch positions on port A
MOV BL, 00 H            ; Initialise BL for switch count
MOV CH, 08H              ; Initialise CH for total switch number
YY: ROL AL              ; Rotate AL through carry to check,
JNC XX                 ; whether the switches are on or
INC BL                 ; off, i.e. either 1 or 0
XX :DEC CH              ; Check for next switch. If
JNZ YY                 ; all switch are checked, the
MOV AL, BL              ; number of on switches are
ADD DX, 04              ; in BL. Display it on port C
OUT DX,AL              ; lower.
HLT                   ; Stop
```

Program 5.5 ALP for Problem 5.10

Mode 1 (strobed I/O mode):

- This mode is also known as strobed I/O mode.
- In this mode, the hand shaking signals control the input and output action of the specified port.
- Port C lines $PC_0 - PC_2$ provide the strobe or hand shaking signals for port B. This group which includes port B and $PC_0 - PC_2$ is called group B for strobed data input /output
- Port C lines $PC_3 - PC_5$ provide strobe lines for ~~not~~ port A. This group including port A and $PC_3 - PC_5$ forms Group A.
- Thus Port C is used for generating hand shaking signals.

The salient features of mode 1 are

- (i) Two groups - group A and group B are available for strobed data transfer
- (ii) Each group contains one 8 bit data I/O port and one 4 bit control/data port
- (iii) The 8 bit data port can be used as either an input or output port.
Both the inputs and outputs are latched.
- (iv) Out of the 8 bits of port C,
 $PC_0 - PC_2$ are used to generate control signals
for port B
 $PC_3 - PC_5$ are used to generate control signals
for port A
 PC_6, PC_7 lines may be used as independent
data lines.

Input control signal definitions in Mode 1

1	0	1	1	I/O	X	X	X
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

1 - Input
0 - output } for PC₆-PC₇

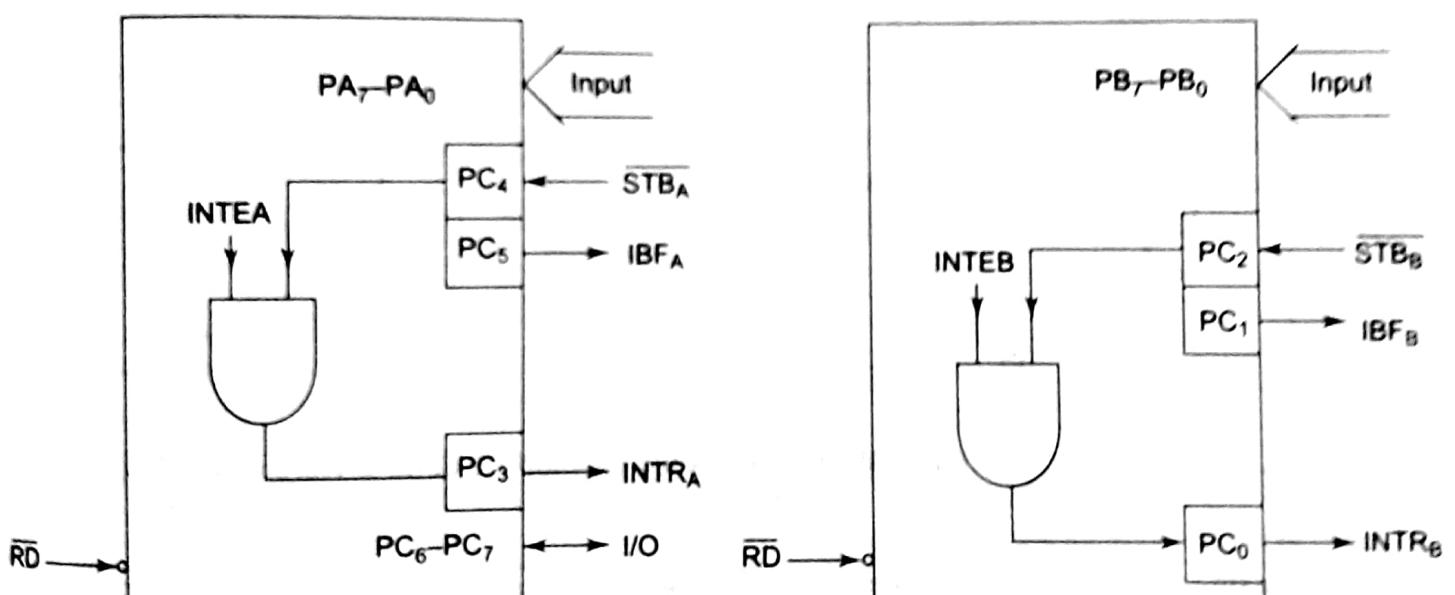


Fig. 5.27 (a) Mode 1 Control Word Group A I/P (b) Mode 1 Control Word Group B I/P

Input control signal definitions (mode 1):

\overline{STB} (Strobe input): If this line falls to low logic level, the data available at 8 bit input port is loaded into input latches.

IBF (Input Buffer full):

If this signal rises to logical 1, it indicates that data has been loaded into latches i.e. it works as an acknowledgement. IBF is set by a low on \overline{STB} and is reset by rising edge of \overline{RD} input.

INTR (Interrupt Request):

This active high output signal can be used to interrupt the CPU whenever an input device requests the service.

INTR is set ^{by a} high at \overline{STB} pin and a high at IBF pin.

INTE is an internal flag that can be controlled by the bit set/reset mode & either

PC₄ (INTEA) or PC₂ (INTEB).

INTR is reset by falling edge of \overline{RD} input

Output control signal definitions Mode 1

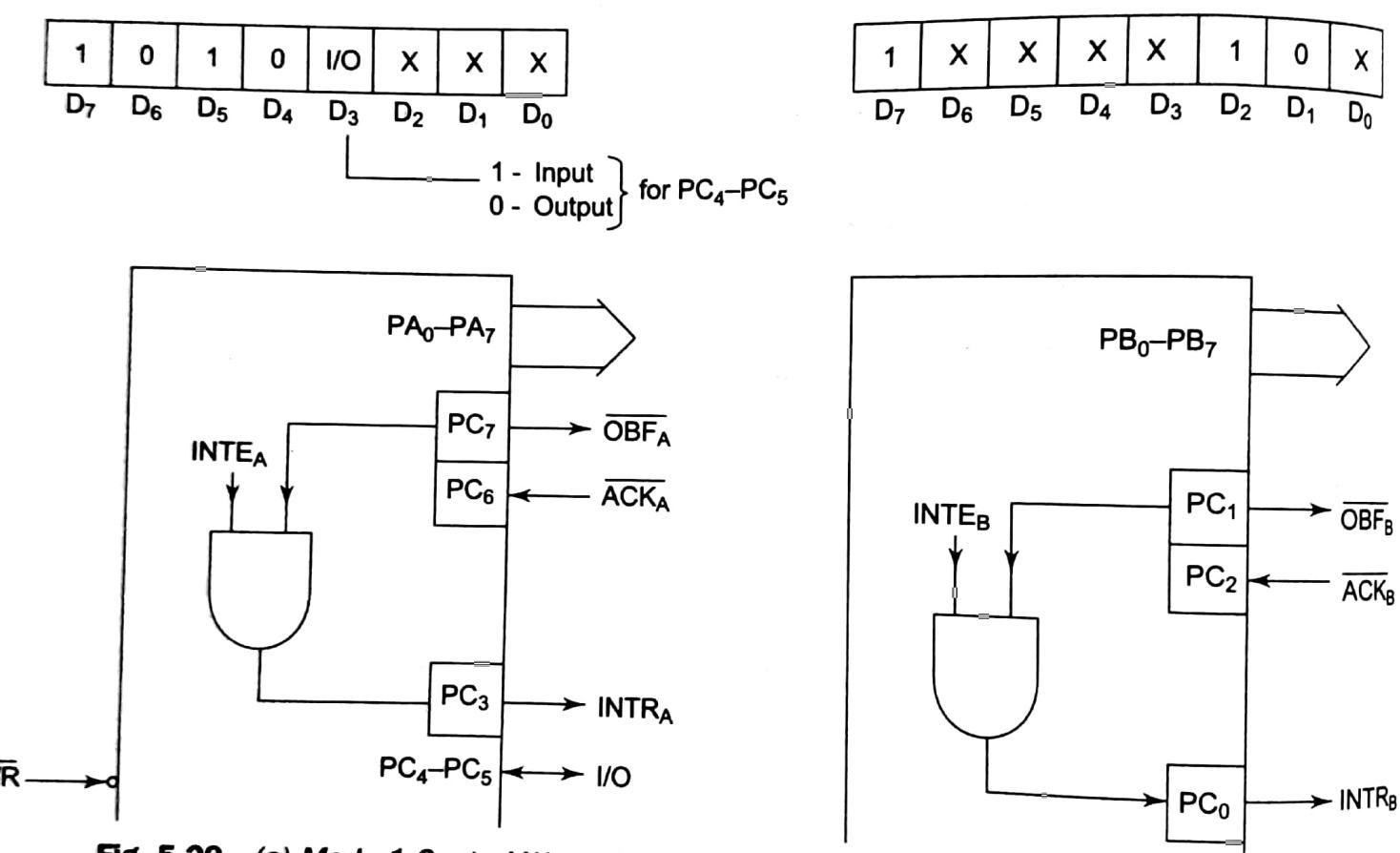


Fig. 5.29 (a) Mode 1 Control Word Group A o/p (b) Mode 1 Control Word Group B o/p

Output control signal definition (mode 1)

OBF (output buffer full):

This status signal, whenever goes low, indicates that CPU has written data to the specified output port.

The OBF flop flop will be set by a rising edge of WR signal and reset by a low going edge at the $\overline{\text{ACK}}$ input.

$\overline{\text{ACK}}$ (Acknowledge input) - $\overline{\text{ACK}}$ signal acts as an acknowledgement to be given by an output device.

$\overline{\text{ACK}}$ signal, whenever low, informs the CPU that the data transferred by the CPU to the output device through the port is received by the output device.

INTR (Interrupt request):

This is an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from CPU.

INTR is set when $\overline{\text{ACK}}$, $\overline{\text{OBF}}$ and INTE are '1'.

It is reset by a falling edge on WR input.

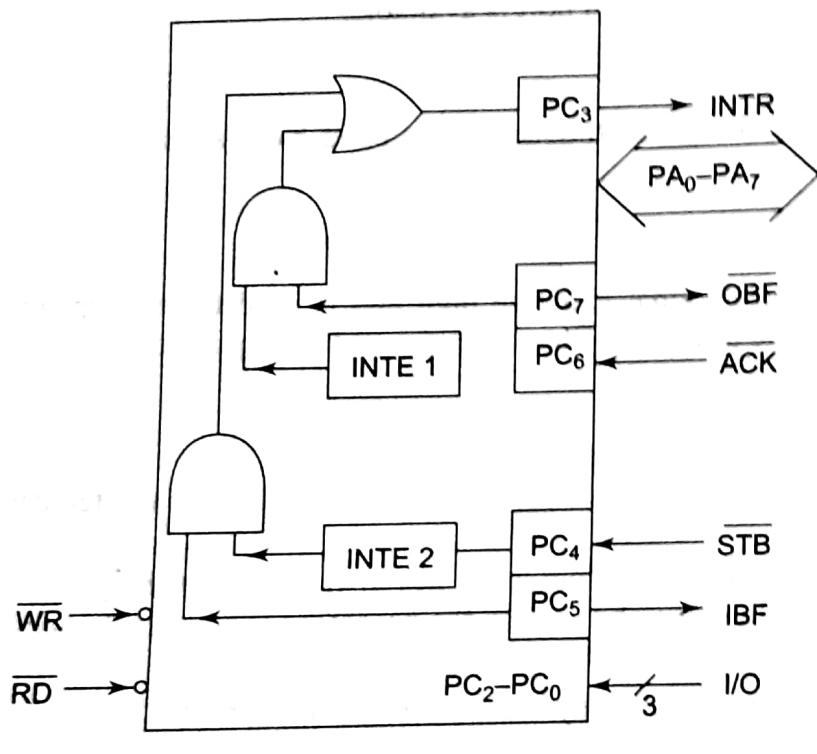
INTEA, INTEB are controlled by BSR mode of PC₆ to PC₂ register.

Mode 2 (strobed bidirectional 2/0):

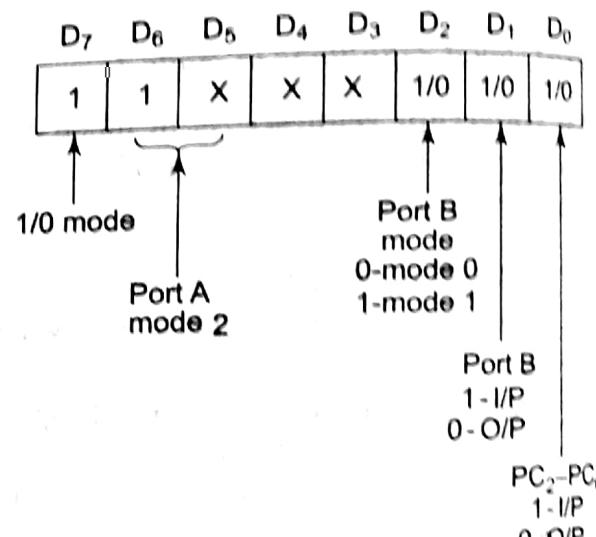
- This mode of operation of 8255 is also known as strobed bidirectional 2/0.
- This mode provides 8255 with an additional feature for communicating with a peripheral device on an 8 bit data bus.
- Hand shaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver.
- The interrupt generation and other functions are similar to mode 1.
- Thus in this mode 8255 is a bidirectional 8 bit port with hand shake signals. The \overline{RD} and \overline{WR} signals decide whether 8255 is acting as an input port or output port.

The important features of mode 2 of 8255 are listed as follows:

1. The single 8 bit port in group A is available.
2. The 8 bit port is bidirectional and additionally a 5 bit control port is available.
3. Three 210 lines are available at port C viz $PC_2 - PC_0$.
4. Inputs and outputs are both latched.
5. The 5 bit control port C ($PC_3 - PC_0$) is used for generating / accepting hand shake signals for the 8 bit data transfer on port A.



(a)



(b)

Fig. 5.35 (a) Mode 2 pins (b) Mode 2 control word

Control Signal definitions in mode 2:

INTR (Interrupt Request):

As in mode 1, this control signal is active high and is used to interrupt the microprocessor to ask for transfer of next byte to / from it.

This signal is used for input (read) as well as output (write) operations.

control signals for output operations :

\overline{OBF} (output buffer full):

This signal, when level, indicates that the data to port A.

\overline{ACK} (Acknowledge)

This control input falls to logic 0 that the previous data byte is received by the destination and the next byte may be sent by the processor. This signal enables the internal tri-state buffers to send out the next byte to port A.

INTE1 (A flag associated with \bar{OBF}) :

This can be controlled by bit ~~get/reest~~
mode with PC_6 .

control signals for input operations:

\overline{STB} (strobe input):

A low on this line is used to strobe in the data into the input latches of 8255.

IBF (Input buffer full):

When the data is loaded into the input buffer, this signal rises to logic '1'. This can be used as an acknowledgement that the data has been received by the receiver.

Some observations:

Mode 2 contains 8 bit bidirectional port, 5 bit control port and relation of INTR with the control pins.

PORT B can be set to mode 0 or mode 1. PORT A is in mode 2. Mode 2 is not available for port B.
The INTR goes high if either IBF, INT_{E2}, \overline{STB} and RD goes high or OBF, INT_{E1}, ACIC, WR goes high. PORT can be read to know the status of the peripheral device.

Ex:-

Interface 16 bit 8255 ports with
8086. The address of port A is F0H.

Sol

To implement a 16 bit port, two
8255's are required.

One will act as a lower 8 bit port,
i.e. D₀ - D₇, while the other will act as
the upper 8 bit port D₈ - D₁₅.

While initializing AL and AH
(AX), both should be loaded with a
suitable (common) control word.

Ports A, B, C all may work as
16 bit ports.

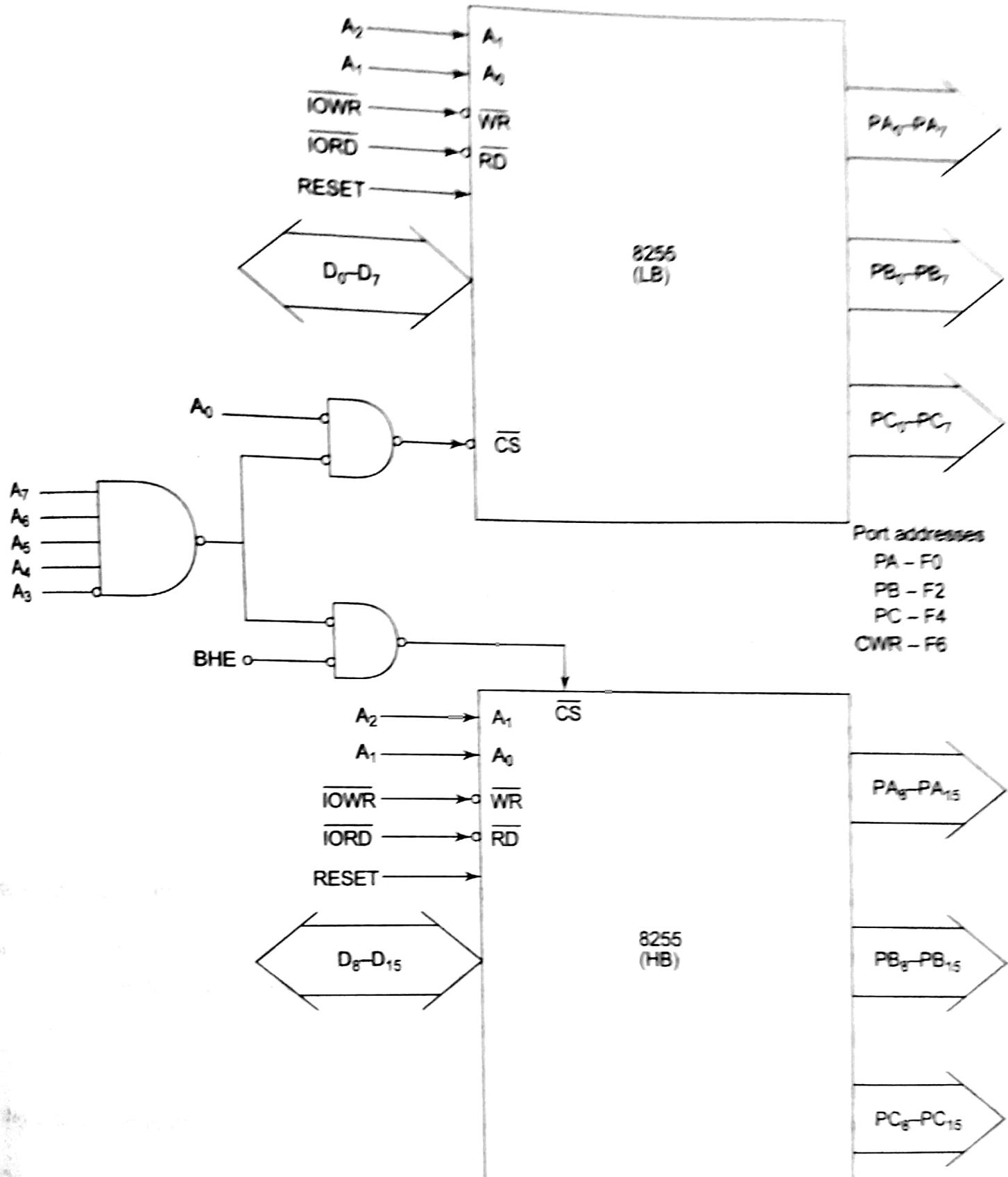


Fig. 5.25 Interfacing 16-bit 8255 ports with 8086