

Programmable Interrupt Controller 8259A

- The 8085 had five hardware interrupt pins.
- Out of these five interrupt pins, four pins were allotted fixed vector addresses, but the pin INTR was not allotted any vector address, rather an external device was supposed to hand over the type of interrupt (i.e. Type 0 to 7 for RST0, to RST7).
- Consider an application, where a no. of I/O devices connected with CPU desire to transfer data using interrupt driven data transfer mode.
In these type of applications, more no. of interrupt pins are required than available in a typical microprocessor.
- Also, in multiple interrupt systems, the processor has to take care of the priorities of the interrupts.
- To overcome these difficulties, we need a programmable interrupt controller that can handle simultaneous multiple interrupt requests along with their types and priorities.

Architecture and signal descriptions of 8259A

- The programmable interrupt controller 8259A from INTEL is one such device.
- 8259, its predecessor was designed to operate only with 8 bit processors like 8085.
- A modified version 8259A that was compatible with 8 bit as well as 16 bit processor was later introduced.

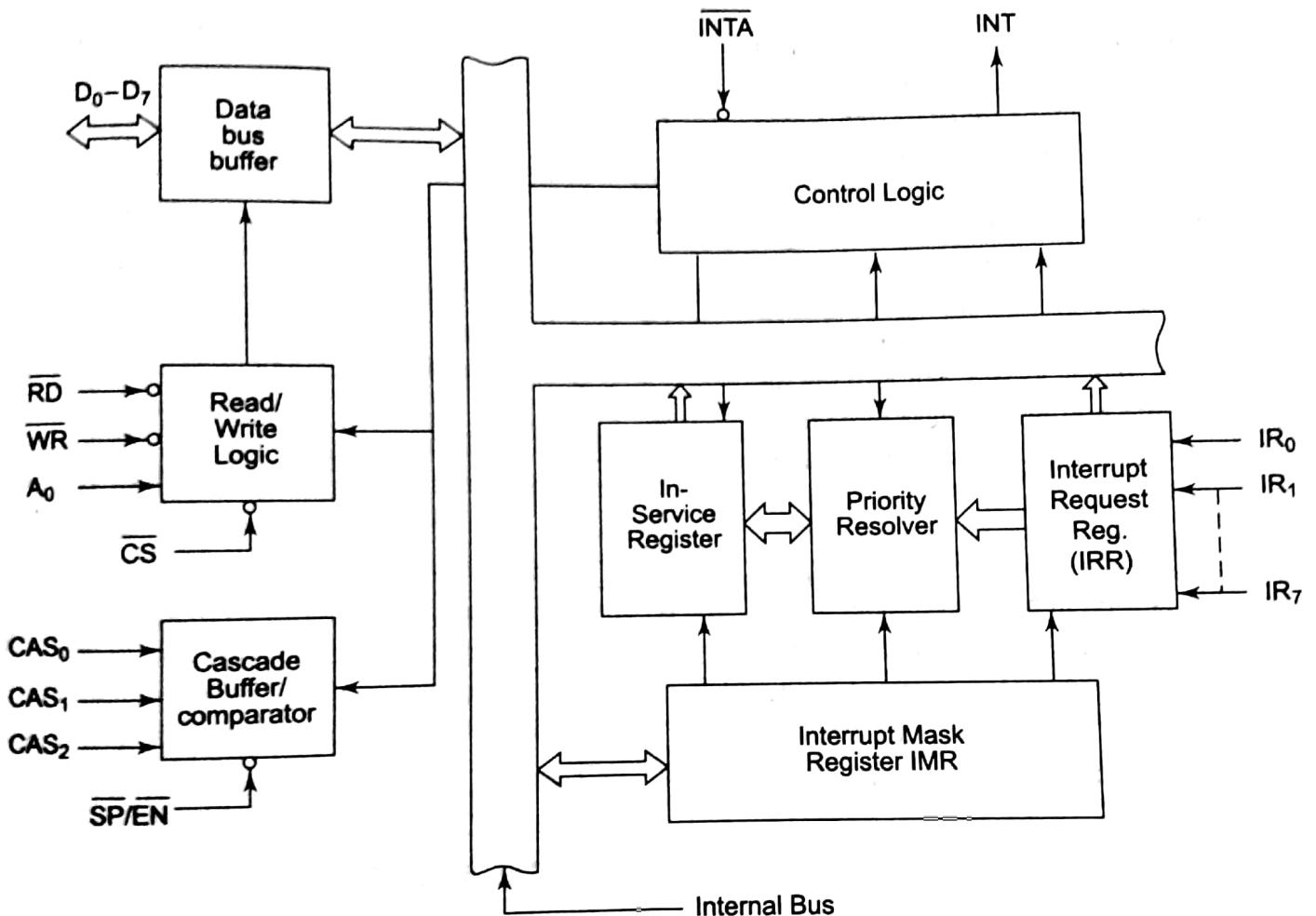


Fig. 6.12 8259A Block Diagram

→ Interrupt Request Register (IRR):

The interrupts at 2R₀ lines are handled by IRR internally. IRR stores all the interrupt requests in it in order to serve them one by one on priority basis.

→ In Service Register (ISR):

This stores all the interrupt requests that are ~~being~~ being serviced, it keeps a track of requests being served.

→ Priority Resolver:

This unit determines the priorities of interrupts appearing simultaneously.

The highest priority is selected and stored in the corresponding bit of ISR during INTA pulse.

The 2R₀ has the highest priority, while 2R₇ has the least priority in fixed priority mode.

The priorities however may be altered by programming the 8259A in rotating priority mode.

→ Interrupt Mask Register (IMR)

This register stores the bits required to mask the interrupt inputs. IMR operate on ZRR at the direction of Priority Resolver.

→ Interrupt Control Logic:

This block manages the interrupt and interrupt acknowledge signals to be sent to CPU for serving one of the eight interrupt requests.

This also accepts INTA signal from CPU that causes 8259A to release vector address bn to the data bus.

→ Data Bus Buffer:

The tri state bidirectional buffer interface internal 8259A bus to the microprocessor system data bus.

control words, status and vector information pass through data buffer during read or write operations.

→ Read/Write control logic :

This circuit accepts and decodes commands from CPU. This block also allows the status of 8259A to be transferred on to the data bus.

→ Cascade Buffer/comparator

This block stores and compares the ID's of all 8259's used in the system. The three 2/0 pins CAS0-2 are outputs when 8259A is used as a master. The same pins act as inputs when 8259A is in slave mode. The 8259A in master mode, sends the 2D of the interrupting slave device on these lines. The slave thus selected, will send its preprogrammed vector address on the data bus during the next $\overline{\text{INTO}}$ pulse.

Minimum mode

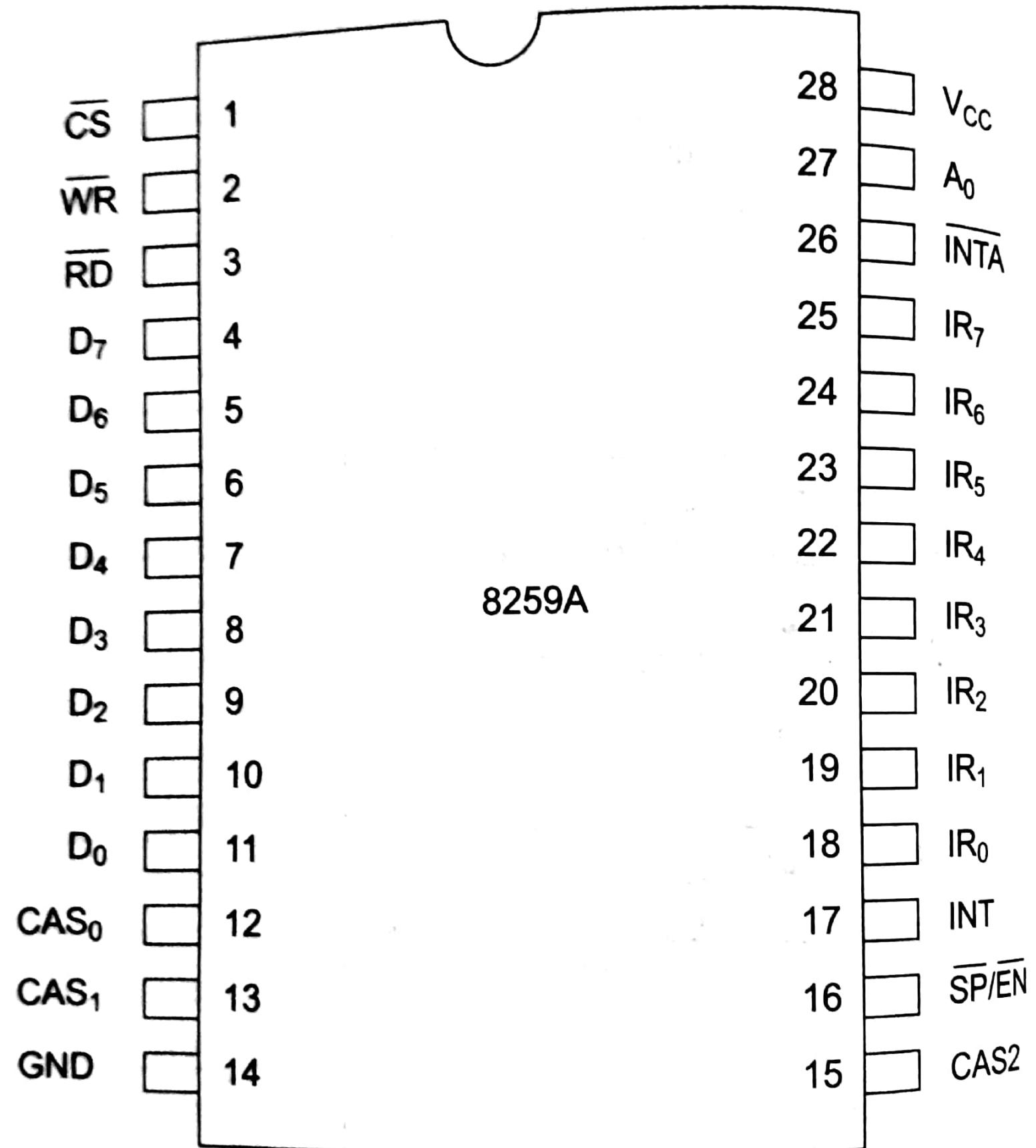


Fig. 6.13 8259 Pin Diagram

Functional description of pins of 8259A:

→ \overline{CS} active low chip select signal for RD and WR operation of 8259A.

\overline{INTA} function is independent of \overline{CS} .

→ \overline{WR} : Active low write enable input to 8259A. This enables it to accept command word from CPU.

→ \overline{RD} : Active low read enable input to 8259A. A low on this line enables 8259A to release status onto data bus of CPU.

→ $D_7 - D_0$: These pins form a bidirectional data bus that carries 8 bit data either to control word or from status word registers. This also carries interrupt vector information.

→ $CAS_0 - CAS_2$ cascade line:

A single 8259A provides eight vectored interrupts. If more interrupts are required the 8259A is used in the cascade mode in which a master 8259A along with eight slaves 8259A can provide upto 64 vectored interrupt lines. Three three lines act as select lines for addressing slave 8259A.

$\rightarrow \overline{SP}/\overline{EN}$:

This pin is a dual purpose pin. When the chip is used in buffered mode, it can be used as a buffer enable to control buffer transceivers.

If this is not used in buffered mode, then the pin is used as input to designate whether the chip is used as a master ($\overline{SP} = 1$) or a slave ($\overline{EN} = 0$).

$\rightarrow INT$:

This pin goes high whenever a valid interrupt request is asserted. This is used to interrupt the CPU and is connected to the interrupt input of CPU.

$\rightarrow 2R0-IR7$ (Interrupt Requests):

These pins act as inputs to accept interrupt requests to the CPU. In the edge triggered mode, an interrupt service is requested by raising an $2R$ pin from a low to a high state. It is held high until it is acknowledged, and just by latching it to high level, if used in the level triggered mode.

→ $\overline{\text{INTA}}$ (Interrupt Acknowledge) :

This pin is an input need to store 8259A interrupt vector data on to the data bus.

In conjunction with $\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins, this pin selects the different operations like writing command words, reading status word etc.

8259A interfacing methods with CPU:

① Polling method:

In this method, the CPU keeps on checking each peripheral device in sequence to ascertain if it requires any service from the CPU. If any such service request is noticed, CPU serves the request and then goes on to the next device in sequence. After all the peripherals are scanned, CPU again starts from the first device.

This type of operation results in the reduction of processing speed because most of the CPU time is consumed in polling the peripheral devices.

② Interrupt driven method:

In this method, CPU performs the main processing task till it is interrupted by a service requesting peripheral.

The net processing speed of these type of systems is high because the CPU serves the peripheral only if it receives the interrupt request.

If more than one interrupt requests are received at a time, all the requesting peripherals are serviced one by one on priority basis.

This method of interfacing requires more additional hardware if the no. of peripherals to be interfaced is more than the interrupt pins available with the CPU.

Interrupt Sequence in an 8086 System

→ The interrupt sequence in an 8086-8259A system is described as follows:

- ① One or more IR lines are raised high that set corresponding IRR bits.
- ② 8259A resolves priority and sends an INT signal to CPU.
- ③ The CPU acknowledges with $\overline{\text{INTA}}$ pulse.
- ④ Upon receiving an $\overline{\text{INTA}}$ signal from CPU, the highest priority ISR bit is set and corresponding IRR bit is reset.
- ⑤ The 8086 will initiate a second $\overline{\text{INTA}}$ pulse. During this period 8259A releases an 8-bit pointer to the data bus where it's read by the CPU.
- ⑥ This completes the interrupt cycle.

The ISR bit is reset at the end of second $\overline{\text{INTA}}$ pulse if automatic end of interrupt (AE0I) mode is programmed. Otherwise ISR bit remains set until an appropriate EOJ command is issued.

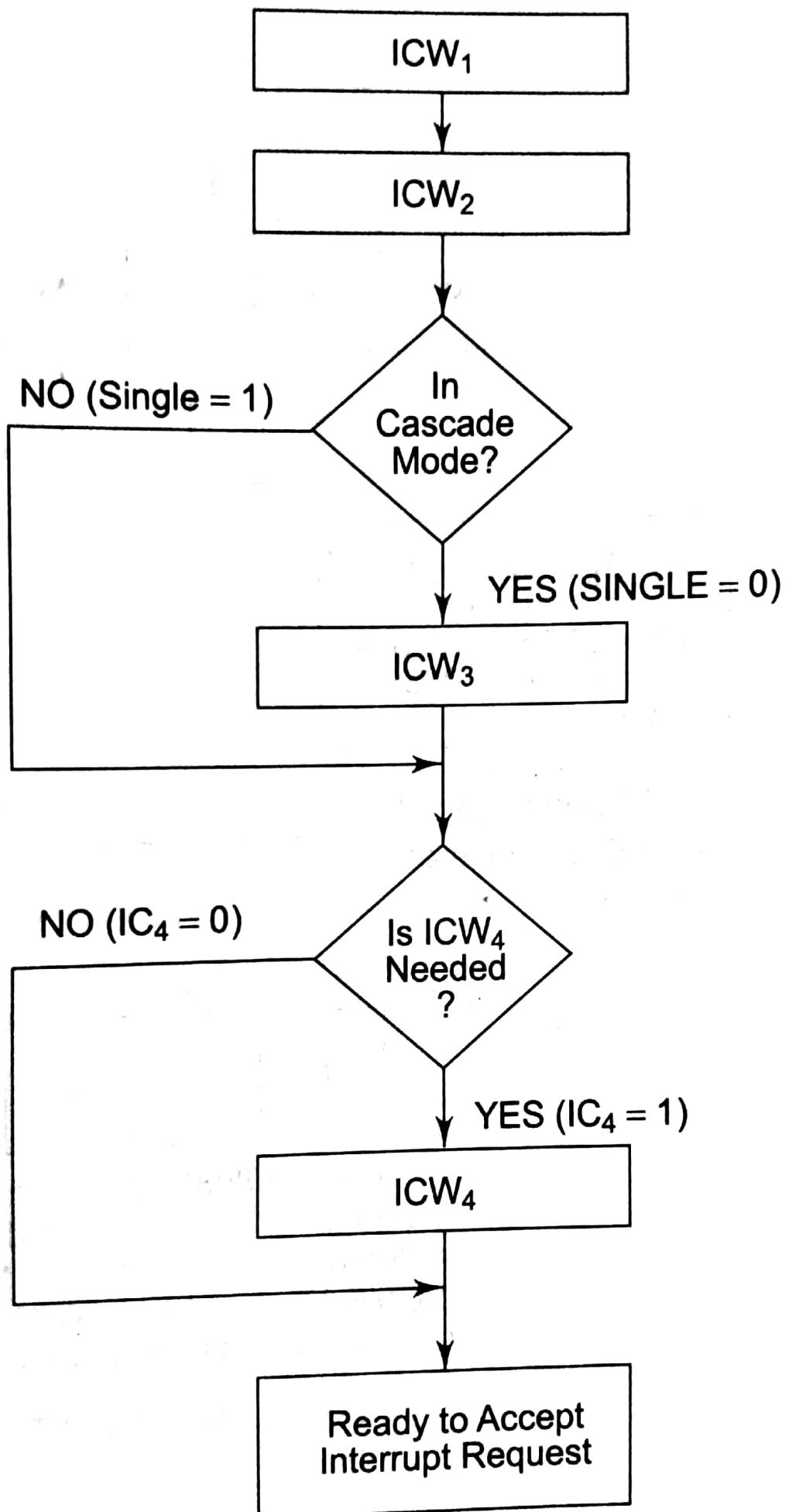


Fig. 6.14 Initialization Sequence of 8259A

Command Words of 8259A

The command words of 8259A are classified in two groups:

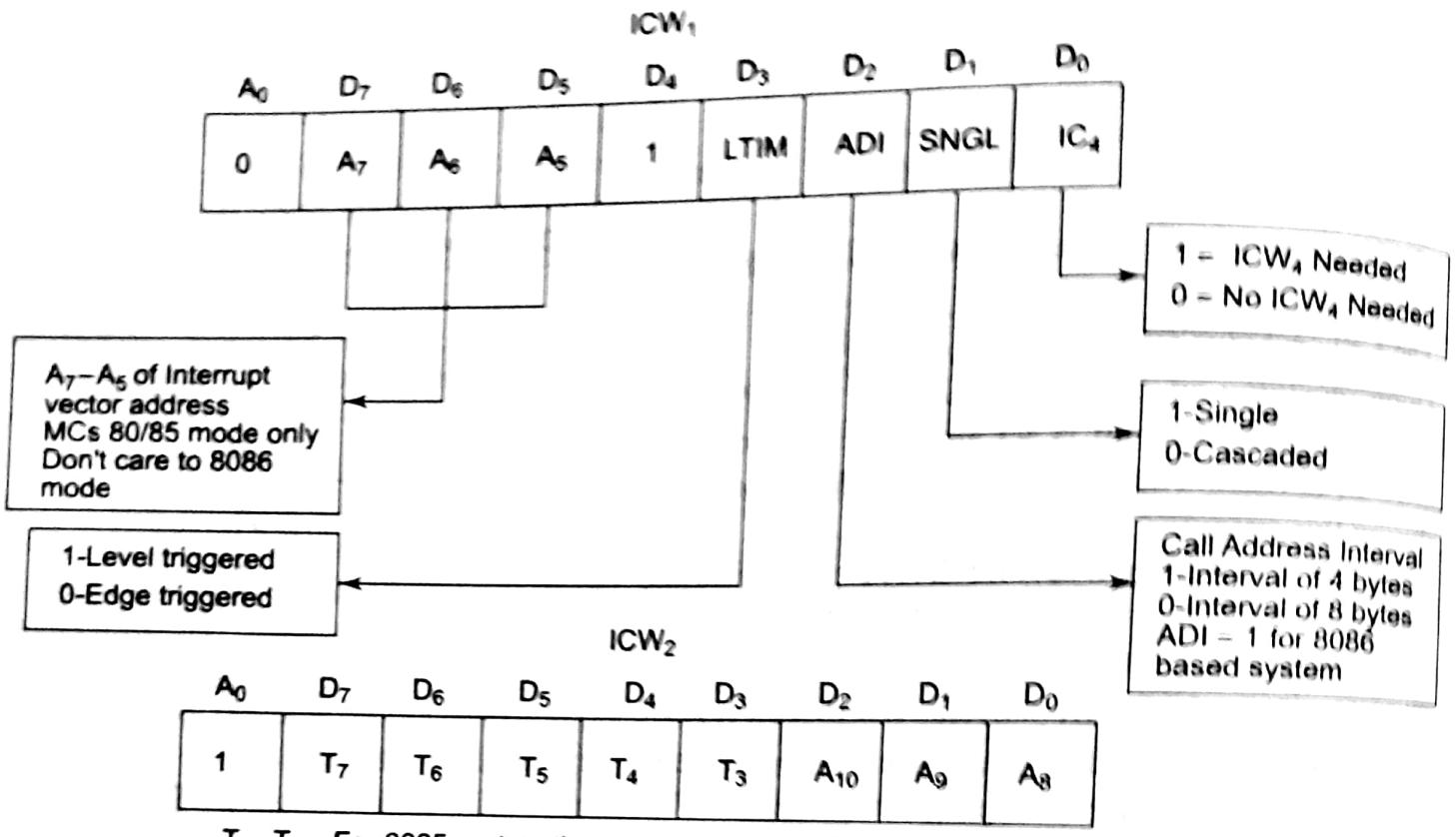
- (1) Initialization command words (ICWs)
- (2) Operation command words (OCWs).

ICWs:

Before it starts functioning, 8259A must be initialized by writing two to four command words into respective command word registers. These are called Initialization command words (ICWs).

If $A_0 = 0$ and $D_4 = 1$, the control word is recognized as ICW1. It contains the control bits for edge/level triggered mode, single/cascade mode, all address interval, and whether ICW_4 is required or not etc.

If $A_0 = 1$, the control word is recognized as ICW2. The ICW2 stores details regarding interrupt vector addresses.



T₇-T₃ – For 8085 system they are filled by A₁₅-A₁₁ of the interrupt vector address and the least significant 3 bits are same as the respective bits of vector address. For 8086 system they are filled by most significant 5 bits of interrupt type and the least significant 3 bits are 0, pointing to Ir₀

Fig. 6.15 Initialization Command Words ICW₁ and ICW₂

Once ICW_1 is loaded, the following initialization procedure is carried out internally.

- (a) The edge sense circuit is reset, i.e. by default 8259A interrupts are edge sensitive
- (b) IMR is cleared
- (c) IR7 input is assigned the lowest priority
- (d) Slave mode address is set to 7
- (e) Special mask mode is cleared and the status read is set to IRR
- (f) If $IC_4 = 0$, all the functions of ICW_4 are set to zero. Master/slave bit in ICW_4 is used in the buffered mode only.

→ In 8085 based systems, A₁₅-A₈ of the interrupt vector address are the respective bits of ICW₂.

In 8086/88 based systems, five most significant bits of the interrupt byte are inserted in place of T₇-T₃ respectively and the remaining three bits (A₈, A₉, A₁₀) are inserted internally as 000 (as if they are pointing to ZR₀).

Other seven interrupt levels vector addresses are internally generated automatically by 8259 using ZR₀ vector.

Address interval is always four in 8086 based systems.

→ ICW₁ and ICW₂ are compulsory command words while ICW₃ and ICW₄ are optional.

ICW₃ is read only when there are more than one 8259A's in the system i.e cascading is used ($SNGL = 0$).

ICW₃ loads an 8 bit slave register.

Master mode ICW₃

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀

S_n = 1-IR_n Input has a slave
 = 0-IR_n Input does not have a slave

Slave mode ICW₃

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	ID ₂	ID ₁	ID ₀

D₂D₁D₀ - 000 to 111 for IR₀ to IR₇ or slave 1 to slave 8

Fig. 6.16 ICW₃ in Master and Slave Mode

ICW ₄									
A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
1	0	0	0	SFNM	BUF	M/S	AEOI	mPM	

Fig. 6.17 ICW₄ Bit Functions

ICW_4 :

The use of this command word depends on
 IC_4 bit of ICW_1 . If $IC_4 = 1$, ICW_4 is used,
otherwise it is neglected.

The bit functions of ICW_4 are as follows:

SFNN: Special fully Nested mode if SFNM=1

BUF: If BUF=1, buffered mode is selected.

In buffered mode SPEN acts as enable
output and the master/slave is determined
using the M/S bit of ICW_4 .

M/S: If M/S=1, 8259A is a master.

If M/S=0, 8259A is a slave.

If BUF=0, M/S is to be neglected.

AEOI: If AEOI=1, the automatic end of
interrupt mode is selected.

mPM: If mPM bit is 0, the MCS-85
system operation is selected

and if mPM=1, 8086/88 operation
is selected.

Operation Command Words:

- Once 8259 is initialized using the previously discussed command words for initialization, it is ready for its normal function i.e. for accepting the interrupts, but 8259A has its own ways of handling the received interrupts called as modes of operation.
- These modes of operation can be selected by programming i.e. writing three internal registers called as operation command word registers.
- In the three operation command word registers every bit corresponds to some operational features of the mode selected, except for a few bits those are either 1 or 0.

→ OCW₁ is used to mask the unwanted interrupt requests.

If the mask bit is '1', the corresponding interrupt ~~is~~ request is masked and if it is '0', the request is enabled.

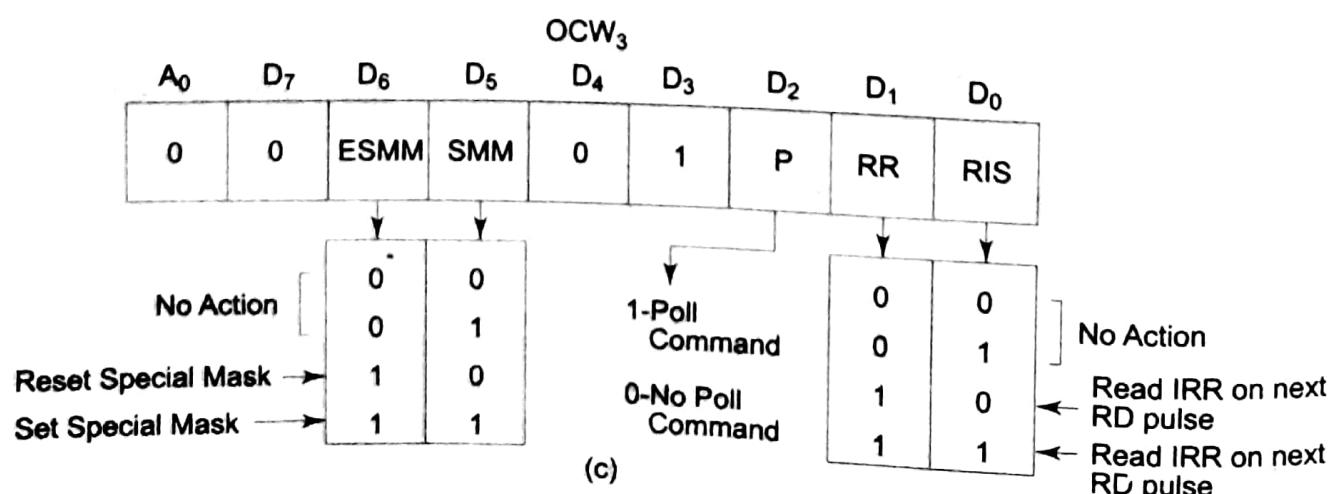
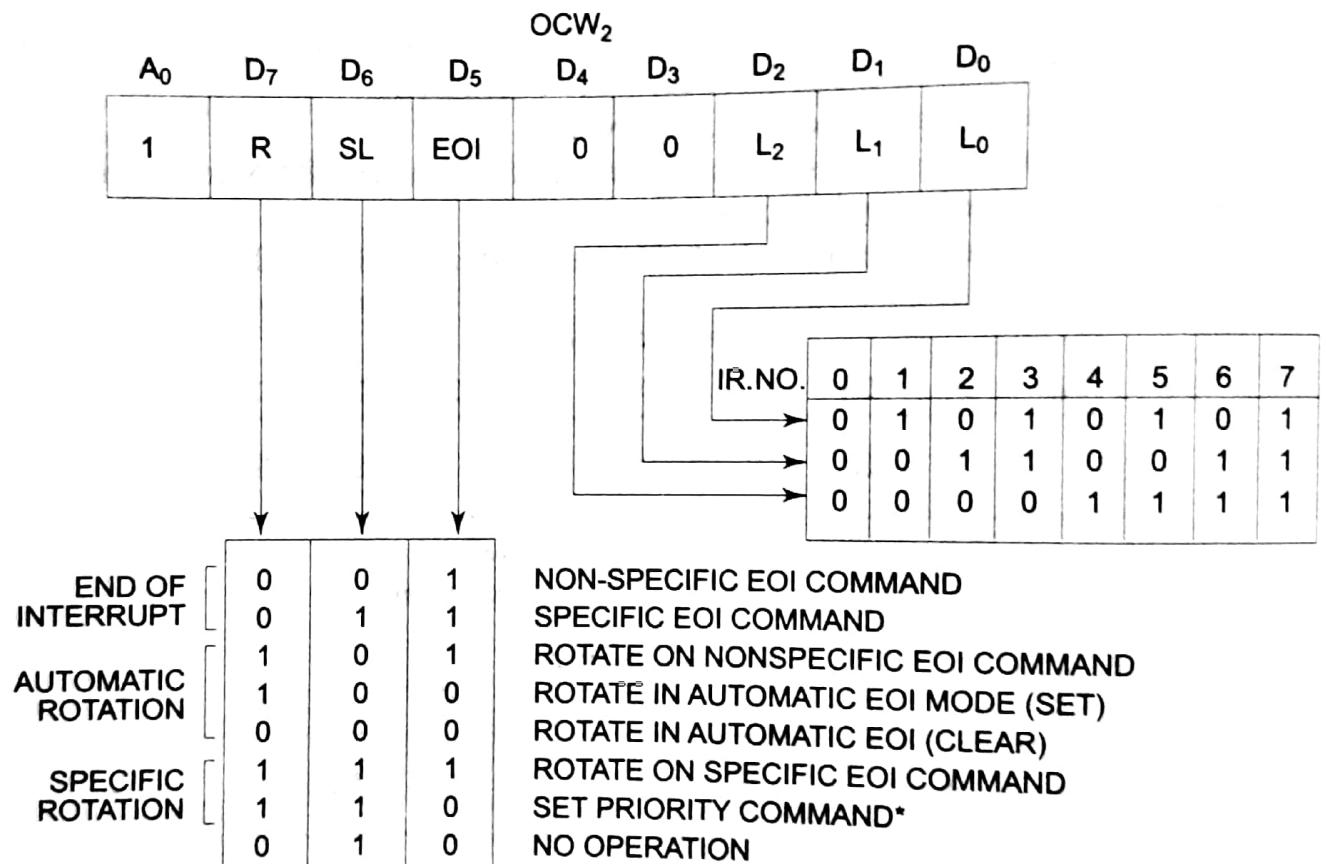
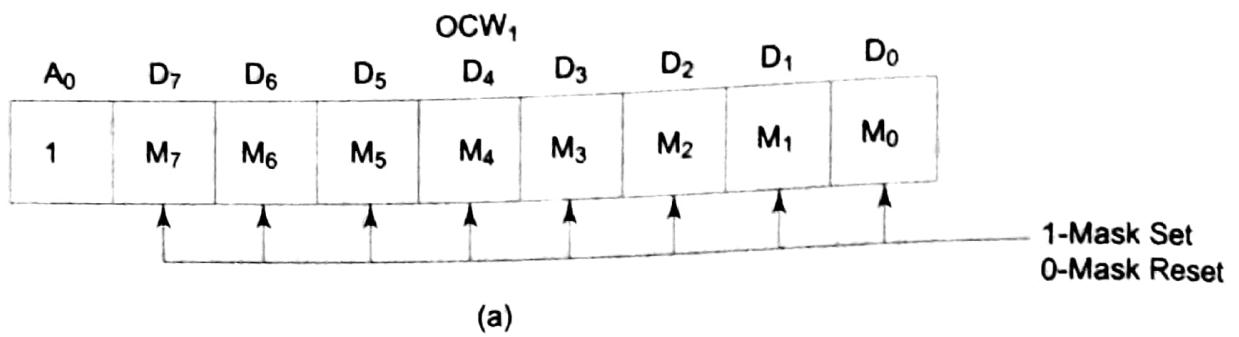


Fig. 6.18 Operation Command Words

→ In OCW₂, the three bits R, SL, E_{O2} control the end of interrupt, rotate mode.

The three bits L₂, L₁, L₀ of OCW₂ determine the interrupt level to be selected for operation, if the SL bit is 1.

→ In OCW₃, if the ESMM bit ie.
Enable Special mask mode bit is set to '1'
the SMM bit is enabled to select or
mask the Special mask mode.
When ESMM bit is '0', the SMM bit is
neglected.
If SMM bit is = 1, 8259A will enter
special mask mode if ESMM = 1.
If ESMM = 1, and SMM = 0, 8259A will
operate in normal mask mode.

6.2.4 Operating Modes of 8259

The different modes of operation of 8259A can be programmed by setting or resting the appropriate bits of the ICWs or OCWs as discussed previously. The different modes of operation of 8259A are explained in the following text:

Fully Nested Mode This is the default mode of operation of 8259A. IR₀ has the highest priority and IR₇ has the lowest one. When interrupt requests are noticed, the highest priority request amongst them is determined and the vector is placed on the data bus. The corresponding bit of ISR is set and remains set till the microprocessor issues an EOI command just before returning from the service routine or the AEOI bit is set. If the ISR (In Service) bit is set, all the same or lower priority interrupts are inhibited but higher levels will generate an interrupt, that will be acknowledged only if the microprocessor's Interrupt enable Flag (IF) is set. The priorities can afterwards be changed by programming the rotating priority modes.

End of Interrupt (EOI) The ISR bit can be reset either with AEOI bit of ICW₁ or by EOI command, issued before returning from the interrupt service routine. There are two types of EOI commands specific and non-specific. When 8259A is operated in the modes that preserve fully nested structure, it can determine which ISR bit is to be reset on EOI. When non-specific EOI command is issued to 8259A it will automatically reset the highest ISR bit out of those already set.

When a mode that may disturb the fully nested structure is used, the 8259A is no longer able to determine the last level acknowledged. In this case a specific EOI command is issued to reset a particular ISR bit. An ISR bit that is masked by the corresponding IMR bit, will not be cleared by a non-specific EOI of 8259A, if it is in special mask mode.

Automatic Rotation This is used in the applications where all the interrupting devices are of equal priority. In this mode, an Interrupt Request (IR) level receives lowest priority after it is served while the next device to be served gets the highest priority in sequence. Once all the devices are served like this, the first device again receives highest priority.

Automatic EOI Mode Till AEOI = 1 in ICW₄, the 8259A operates in AEOI mode. In this mode, the 8259A performs a non-specific EOI operation at the trailing edge of the last INTA pulse automatically. This mode should be used only when a nested multilevel interrupt structure is not required with a single 8259A.

Specific Rotation In this mode a bottom priority level can be selected, using L_2 , L_1 and L_0 in OCW₁ and R = 1, SL = 1, EOI = 0. The selected bottom priority fixes other priorities. If IR₅ is selected as a bottom priority, then IR₅ will have least priority and IR₄ will have a next higher priority. Thus IR₆ will have the highest priority. These priorities can be changed during an EOI command by programming the rotate on specific EOI command in OCW₂.

Special Mask Mode In the special mask mode, when a mask bit is set in OCW₁, it inhibits further interrupts at that level and enables interrupt from other levels, which are not masked.

Edge and Level Triggered Mode This mode decides whether the interrupt should be edge triggered or level triggered. If bit LTIM of ICW₁ = 0, they are edge triggered, otherwise the interrupts are level triggered.

Reading 8259 Status The status of the internal registers of 8259A can be read using this mode. The OCW₃ is used to read IRR and ISR while OCW₁ is used to read IMR. Reading is possible only in no polled mode.

Poll Command In the polled mode of operation, the INT output of 8259A is neglected, though it functions normally, by not connecting INT output or by masking INT input of the microprocessor. The poll mode is entered by setting P = 1 in OCW₃. The 8259A is polled by using software execution by microprocessor instead of the requests on INT input. The 8259A treats the next RD pulse to the 8259A as an interrupt acknowledge. An appropriate ISR bit is set, if there is a request. The priority level is read and a data word is placed on to data bus, after RD is activated. The data word is shown in Fig. 6.19.

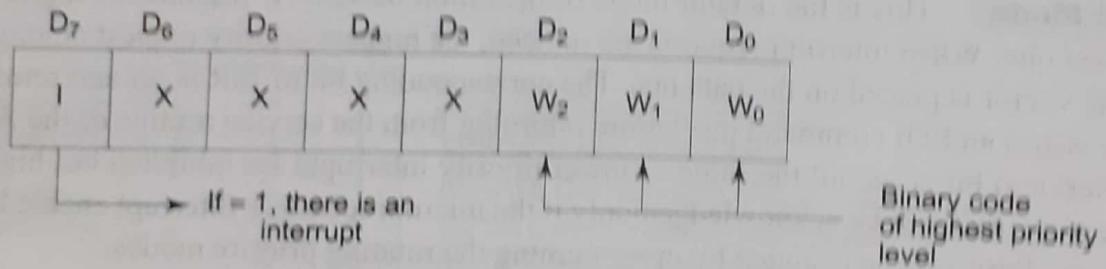


Fig. 6.19 Data Word of 8259

A poll command may give you more than 64 priority levels. Note that this has nothing to do with the 8086 interrupt structure and the interrupt priorities.

⑩ Special Fully Nested Mode:

- This mode is used in more complicated systems, where cascading is used and the priority has to be programmed in the master using PCW4.
- This mode of operation is similar to normal nested mode.
- In this mode, when an interrupt request from a certain slave is in service, this slave can further send requests to the master, if the requesting device connected to the slave has higher priority than the one being served.
- In this mode, master interrupts the CPU only, when interrupting device has higher or same priority than the one currently being served.
- In normal mode, other requests than one being served are masked out.

→ When entering the interrupt service routine, the software has to check whether this is the only request from the slave. This is done by sending a non specific EOI command to the slave and then reading its ISR and checking for zero.

If its zero, a non specific EOI can be sent to master, otherwise no EOI should be sent.

This mode is important, since in the absence of this mode, the slave would interrupt the master only once and hence priorities of slave inputs would have been disturbed.

⑪ Buffered mode:

- When 8259A is used in systems in which bus driving buffers are used on data buses (e.g. cascade systems), the problem of enabling buffers arises.
- The 8259A sends a buffer enable signal on $\overline{SP}/\overline{EN}$ pin, whenever data is placed on the bus.

(12) Cascade Mode

- The 8259A can be connected in a system containing one master and eight slaves (maximum) to handle upto 64 priority levels.
- The master controls the slaves using CAS₀-CAS₂, which act as chip select inputs (encoded) for slaves.
- In this mode, the slave INT outputs are connected with master IR inputs.
- When a slave request line is activated and acknowledged, the master will enable the slave to release the vector address during the second pulse of INTA sequence.
- The cascade lines are normally low and contain the slave address code from the trailing edge of first INTA pulse to the trailing edge of second INTA pulse.
- Each 8259A in the system must be separately initialized and programmed to work in different modes.
- The EOI command must be issued twice, one for the master and other for slave.
- A separate address decoder is used for each 8259A.

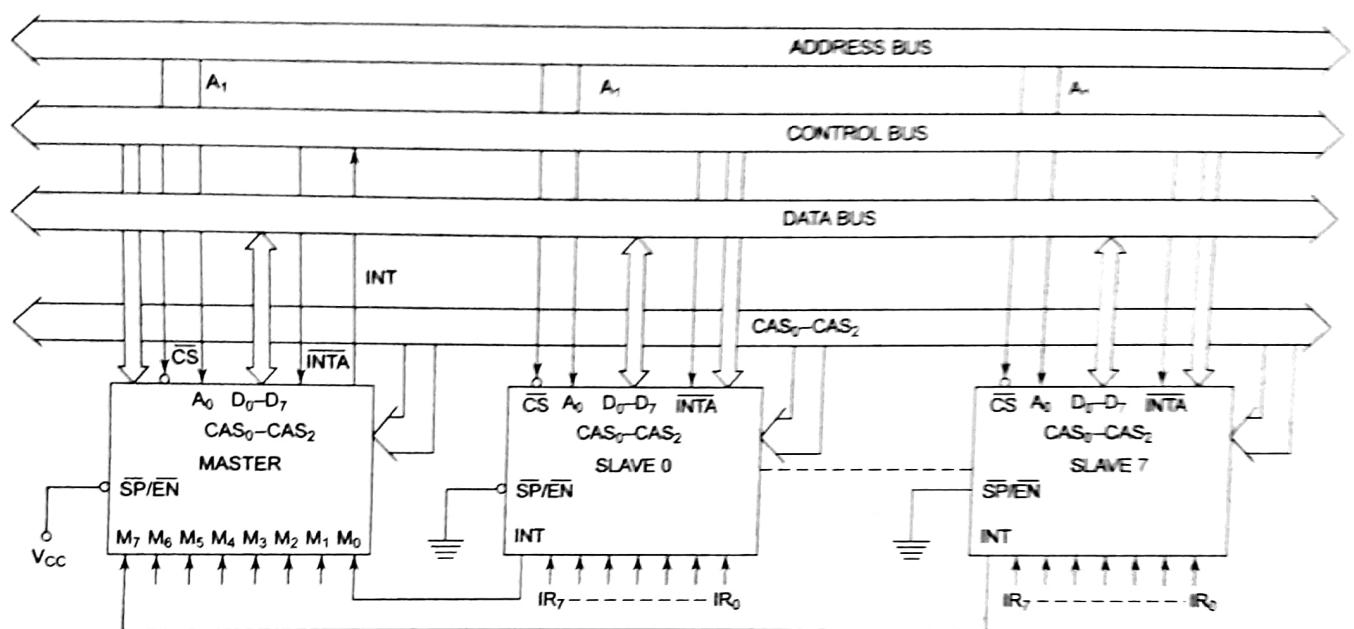


Fig. 6.20 8259A in Cascaded Mode