# Discussion Points from Session 2

Session 2.F

PH435

# Discussion points came up on moodle: Session 2

1. Bit flip errors [S.T,M.M., 8]
Radiation damage

2. Clock speed enhancement [H.R., 5]

3. Decompiling program from opcodes, hacks[M.M,R.S.,A.A, 5]

4. **Tristate logic** [Y.G., 4]

5. Browser performance comparisons [A.R., 9]

# Bit flip errors. Momentary errors (can recover)

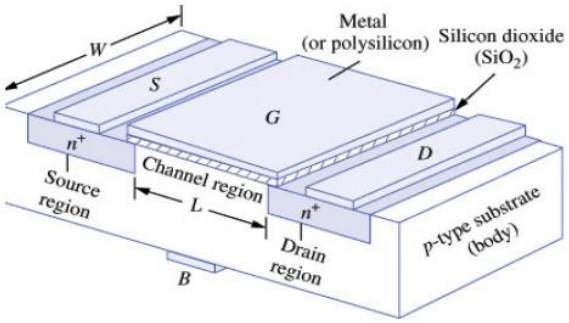
1. Memory bit corruption: some D register in the circuit loses stored bit data
2. Result of an ALU operation has bit error: some gate within some adder has a bit error

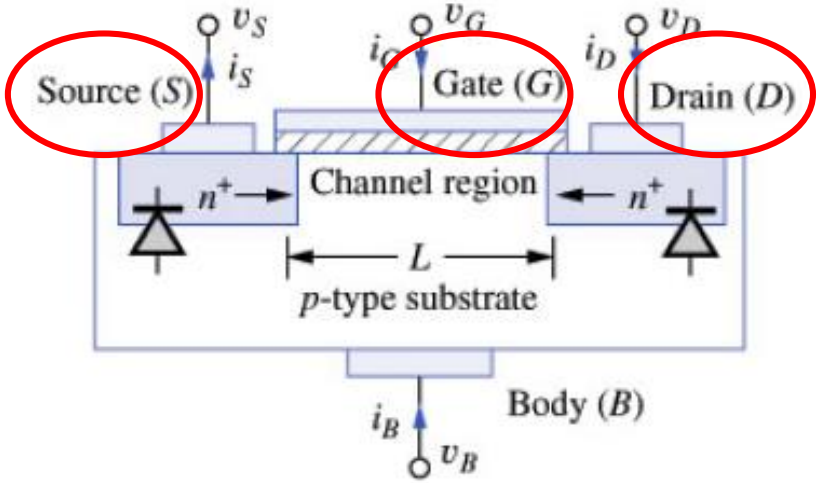
Mainly matters for “mission critical” computations (eg satellite systems controls, autonomous driving algos etc)

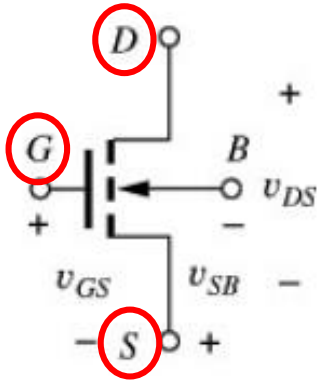
Most other consumer grade electronics can cope with bit-level errors using parity checks etc

# Bit flip errors. How do they happen? Device physics

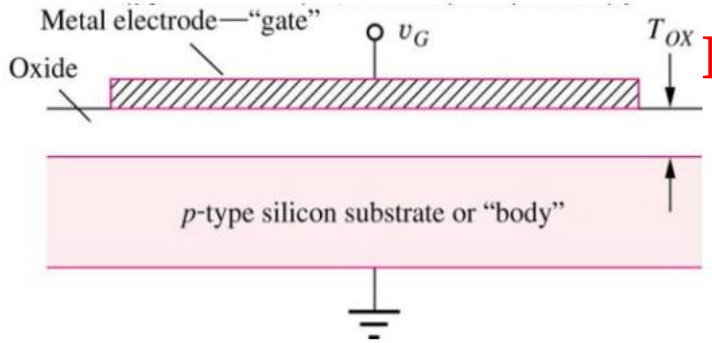
## NMOS transistor structure




## MOS capacitor

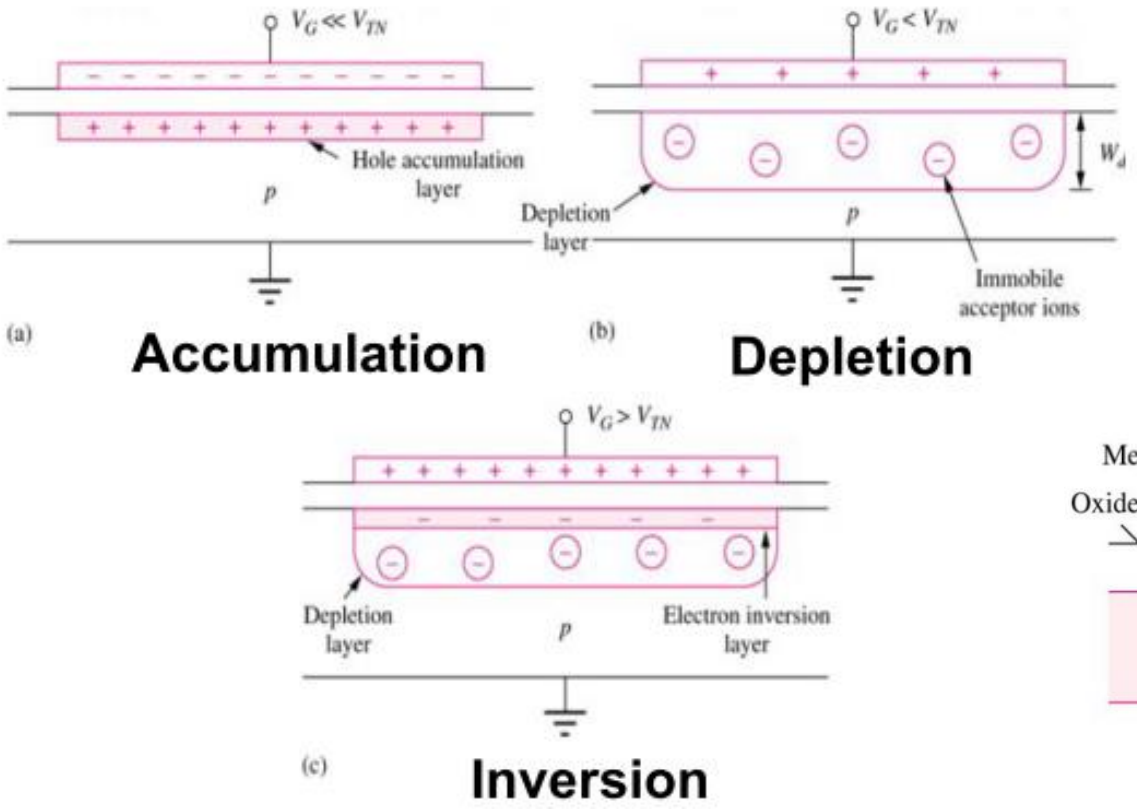



**M**etal

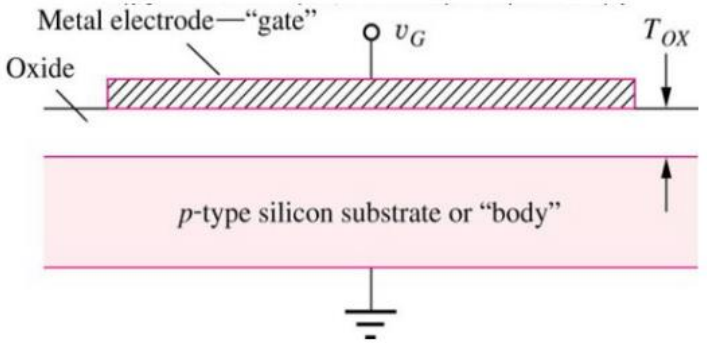
**O**xide

**S**emiconductor

# Bit flip errors. MOS capacitor modes of operation



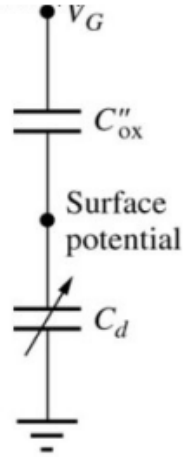

**MOS** capacitor




**M**etal

**O**xide

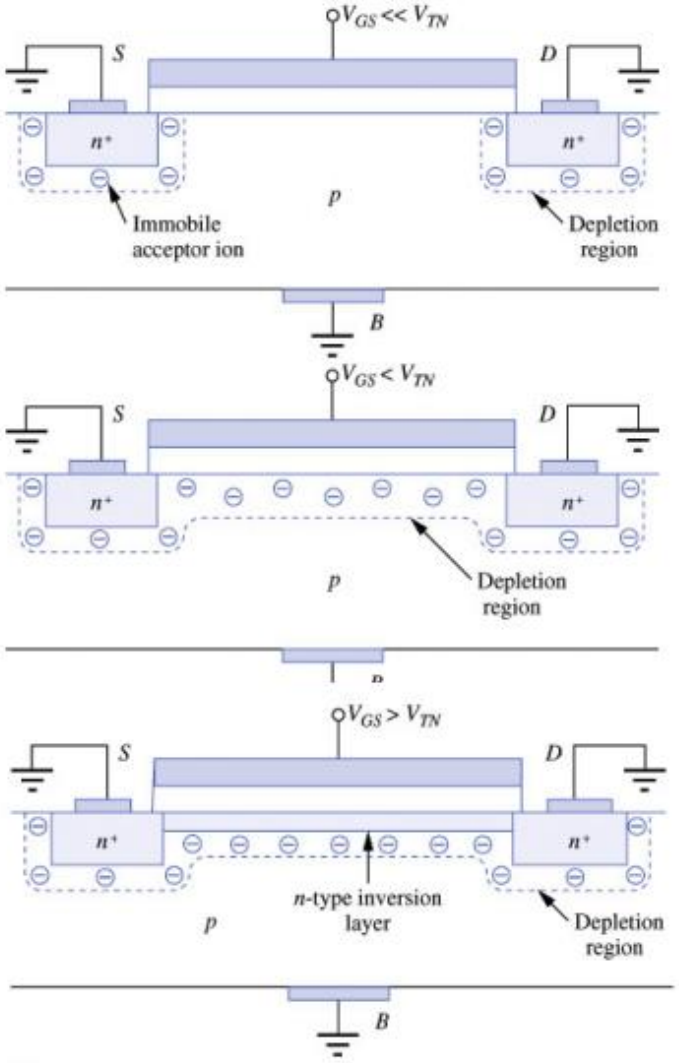
**S**emiconductor

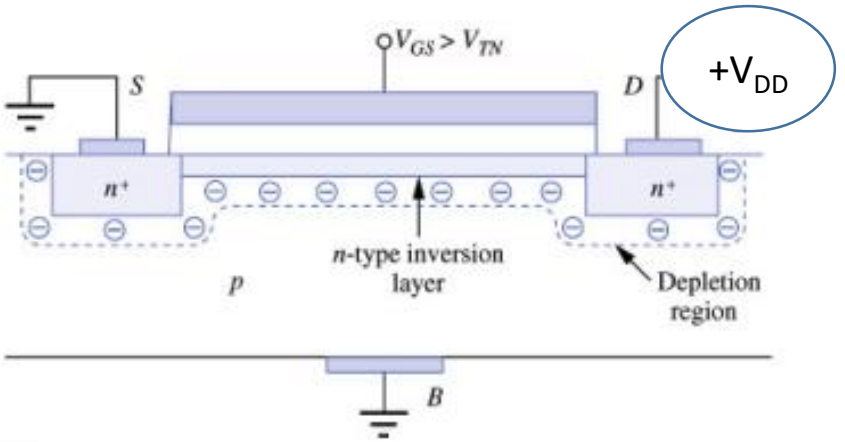



errors!)

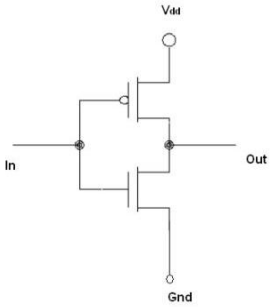
MOS capacitor ref: https:/

# Bit flip errors. MOSFET modes of operation

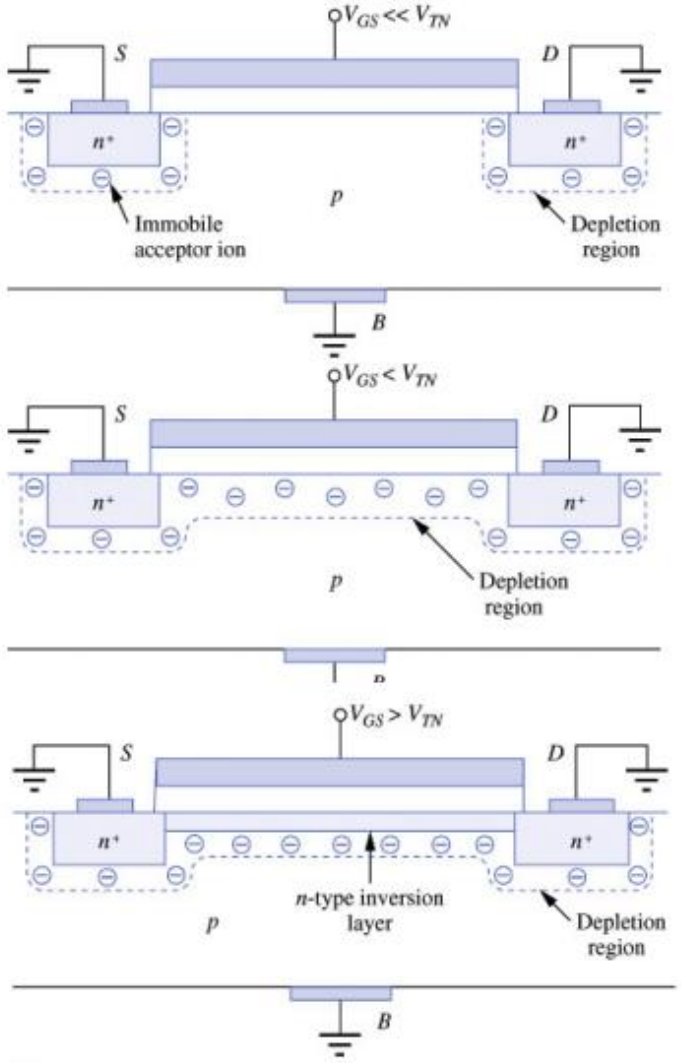


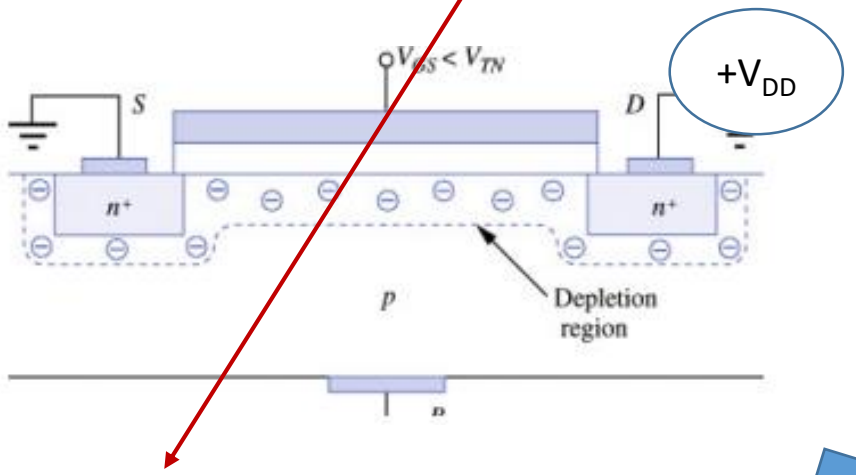

MOSFET is ON



# Bit flip errors. MOSFET mode of MIS-operation

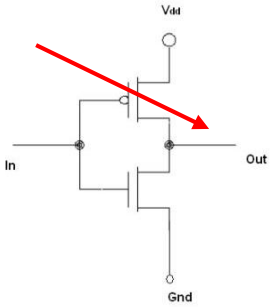



Charged Cosmic ray particle passes through device releases extra e/h

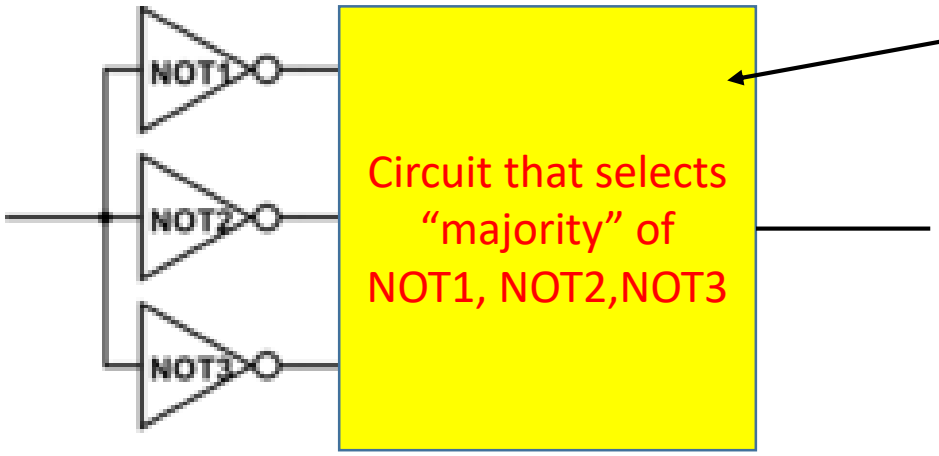



MOSFET is OFF

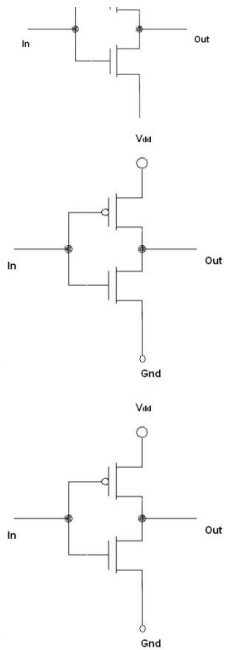
LOGIC IS INVALID



# Bit flip errors. FIX by having parallel calculation paths




Note: this circuit must be highly optimized with minimum number of parts! You don't want a bit flip to happen in here!




**Homework:**

1)

Design a circuit that has: 3 digital inputs & 1 output = 'best 2 of the 3', i.e. pick the value which matches *at least* 2 of the inputs

The circuit must have the smallest possible number of gates/MOSFET devices

2) (advanced)

Further, optimize its layout on 2-dimensional silicon to minimize the surface area used.

Ref: Fig 2.29 from "Design of Analog CMOS Integrated Circuits" by B. Razavi

**Key takeaways:**

1. Bit flip errors caused by direct hit from radiation **particle**

**2.** Possibly also from intense **EM pulse** which can induce intense current in the metal contacts and/or polarize the dielectric oxide to have permanent-ish charge

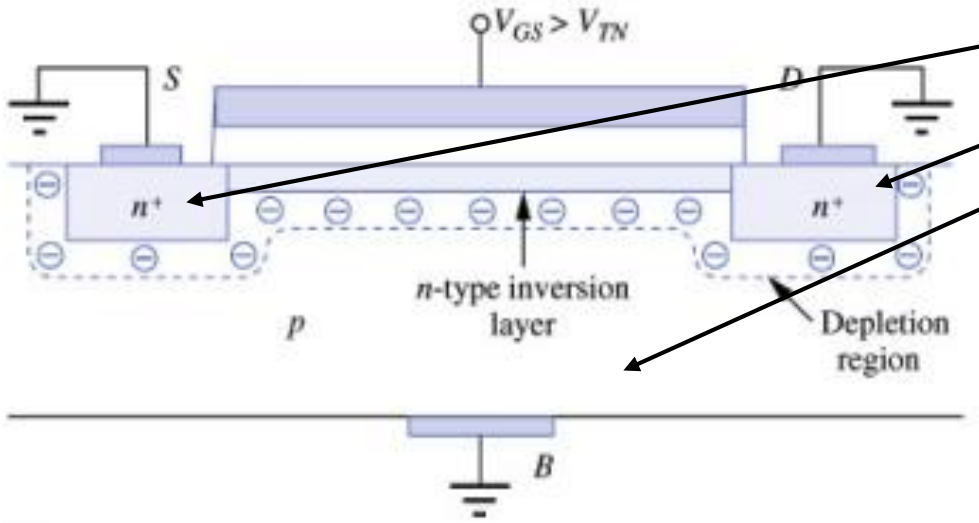
3. Technical term is 'SEU' – **S**ingle **E**vent **U**pset

**How to fix SEU's?**

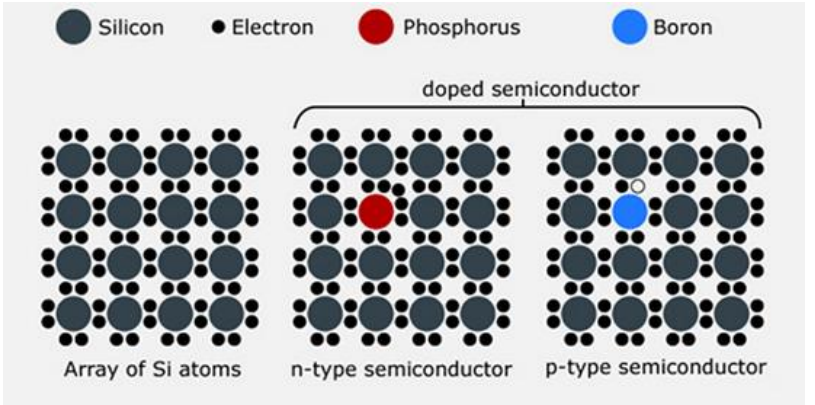
1. Parallel computation paths – majority decision at the cost of increased gate count.

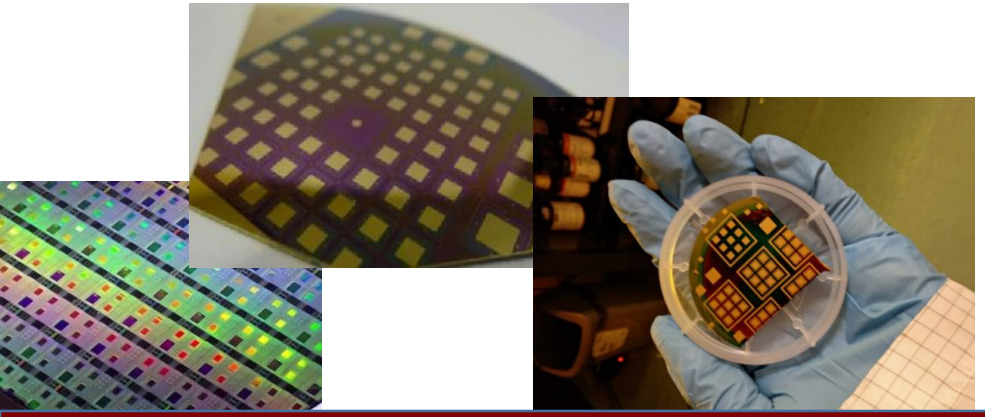
2. Shielding with heavy radiation absorbing material like Pb

# More permanent Radiation damage is caused by overdose of radiation




This is crystalline Silicon doped with n-type (Ph) or p-type (B)



The electronic properties: Band gap, e/h drift etc **ASSUME** crystalline structure with dopant atoms immobile.

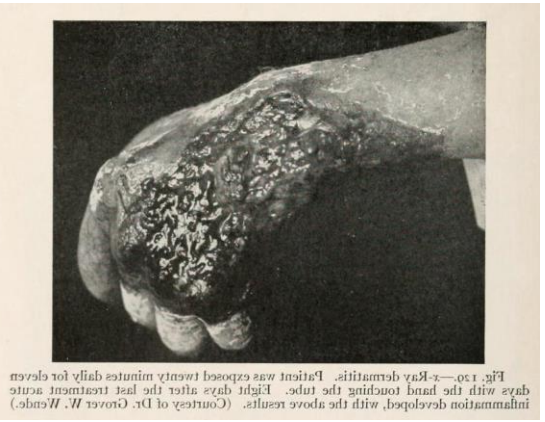


Fig. 129.—X-Ray dermatitis. Patient was exposed twenty minutes daily for eleven days with the hand touching the tube. Eight days after the last treatment acute inflammation developed, with the above results. (Courtesy of Dr. Grover W. Wende.)

# Bombardment of electronics with intense doses of radiation causes damage to crystal structure

High flux of radiation particles in particle accelerator / nuclear reactor environment

High energy gamma rays (X-rays)

Causes crystal atoms to be knocked off from lattice sites..
Electronic properties change dramatically:
- 'n/p-type'ness of n/p-type silicon, dielectric constant of $SiO_2$ etc

Some recovery is possible – but basically new tech, new materials are needed for such harsh environment.

https://meroli.web.cern.ch/lecture_radiation_damage_silicon_detector.html
https://www.researchgate.net/publication/230972197_Effects_of_radiation_damage_in_silicon_p_-_i_-_n_photodiodes

# Topic 2 of discussion:

Enhancing clock speeds of a processor

[H.R. + A.R. started, S.T. put up references]

Screen-shot of Gigabyte BIOS

# Key takeaways from the discussion

Heat is generated in the MOSFET devices by electrons rushing around between S,D bouncing off lattice atoms (elastic collisions)
**[NOTE:** HEAT is **NOT A 'SUBSTANCE':** it is a measure of the vibration/motion of the constituents of the material (Entropy!)

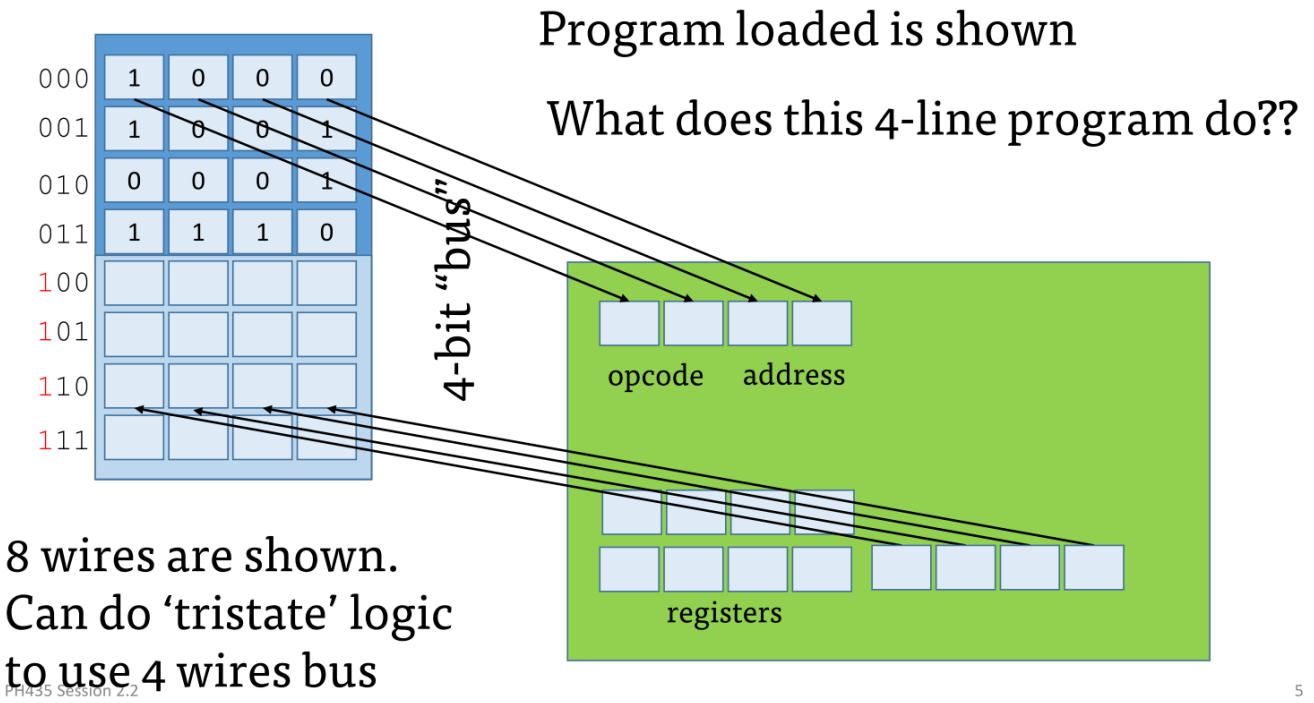
For any imaginable size of the device (micron, nanometer scale) and any 'heat bath' at lower temperature with which the device is in contact, there is a finite physical limit to how much of the heat can be transferred out of the device [Dennard scaling] device/area

Air, which is the substance normally used (big heatsink + fan + air) is the worst possible medium. Using alternative materials like an oil bath / LN2 helps [A.R.]

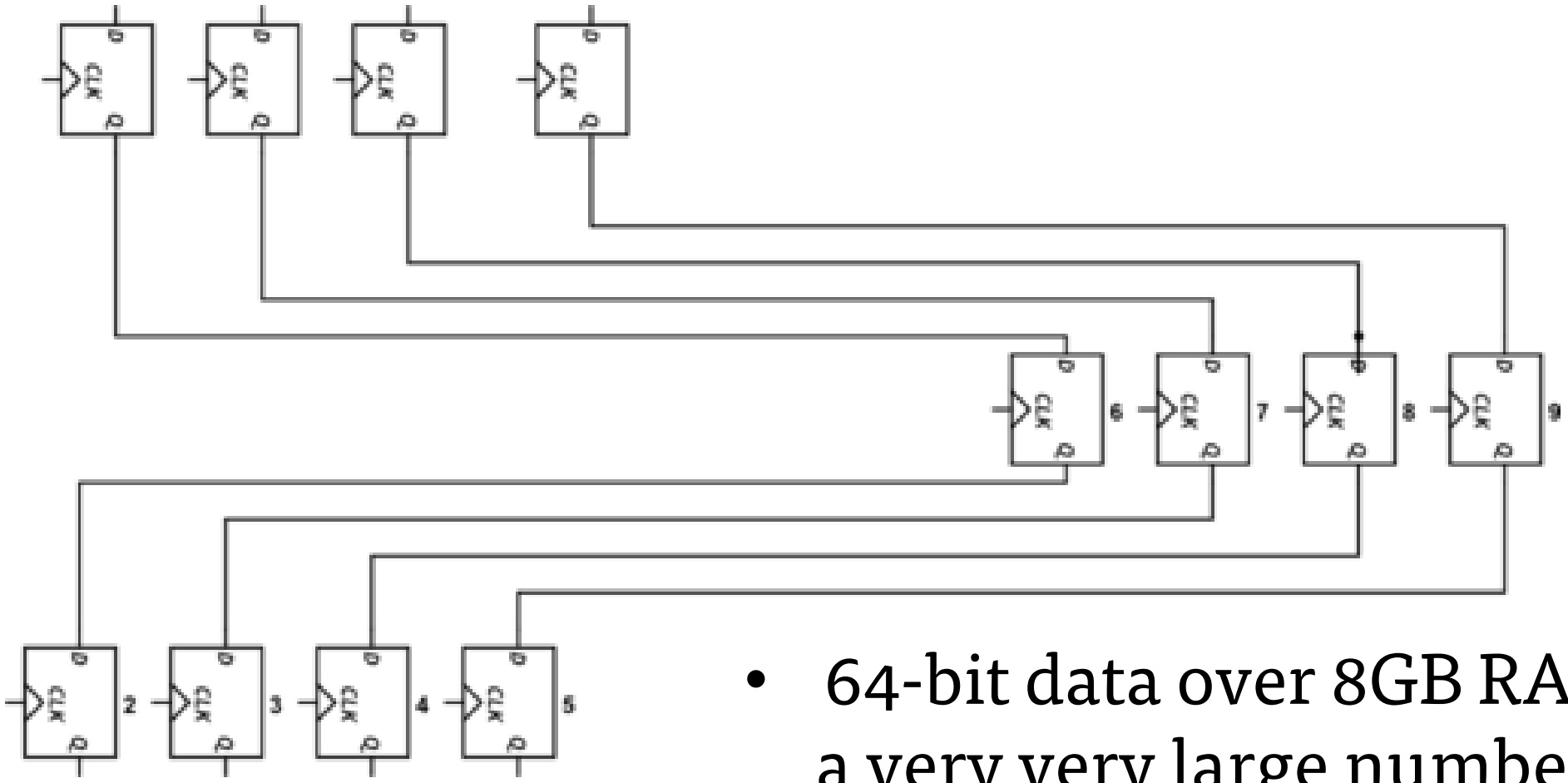
Opto-electronic[S.T.] for inter-circuit communication. Else conductor traces running between devices limit the comm. speed

# Topic 4

# Tri-state logic and its uses [Y.G., A.]



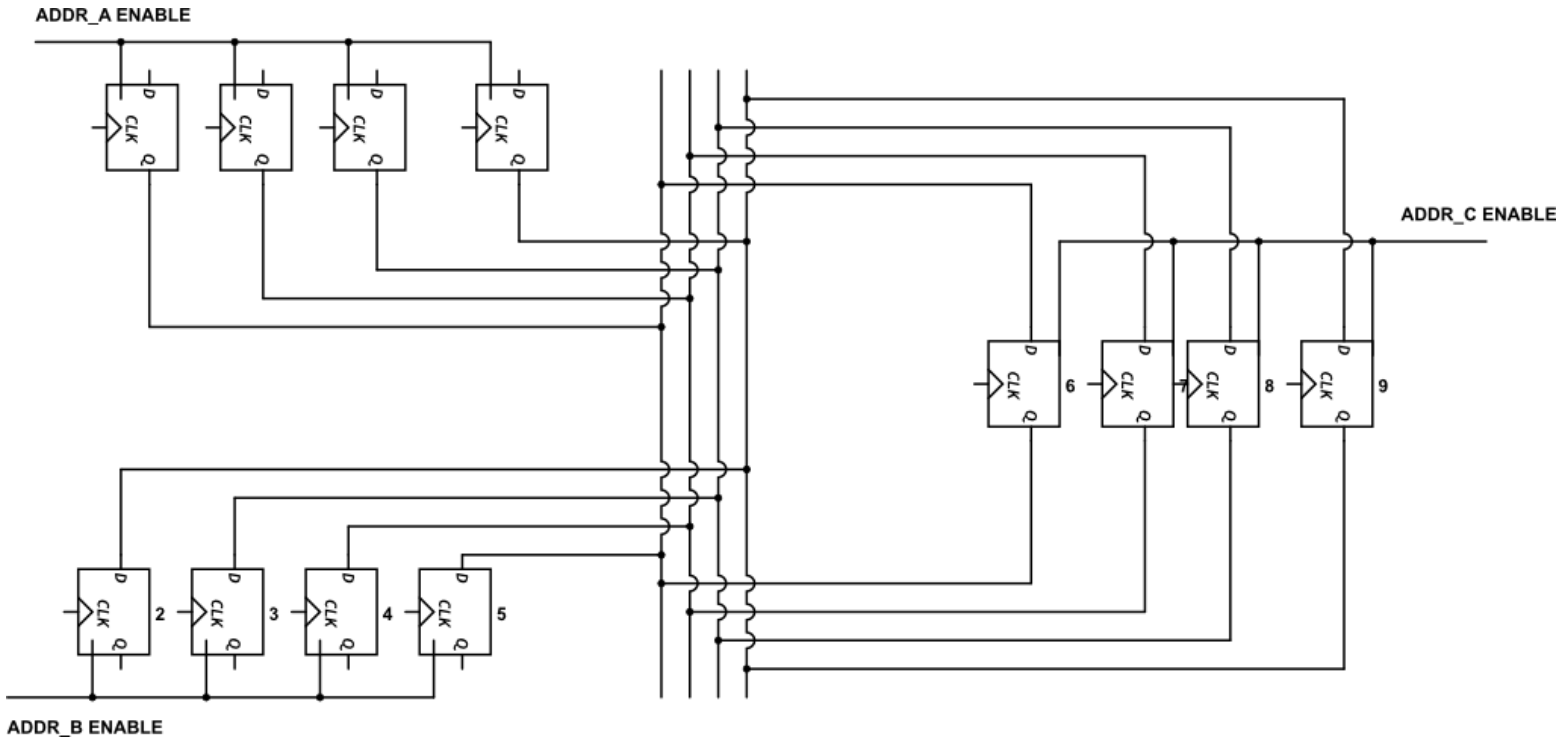
# Moving 4-bit data from address A to B to C : need 8 wires




- 64-bit data over 8GB RAM … ${}^{64G}C_{64}$ a very very large number of wires!

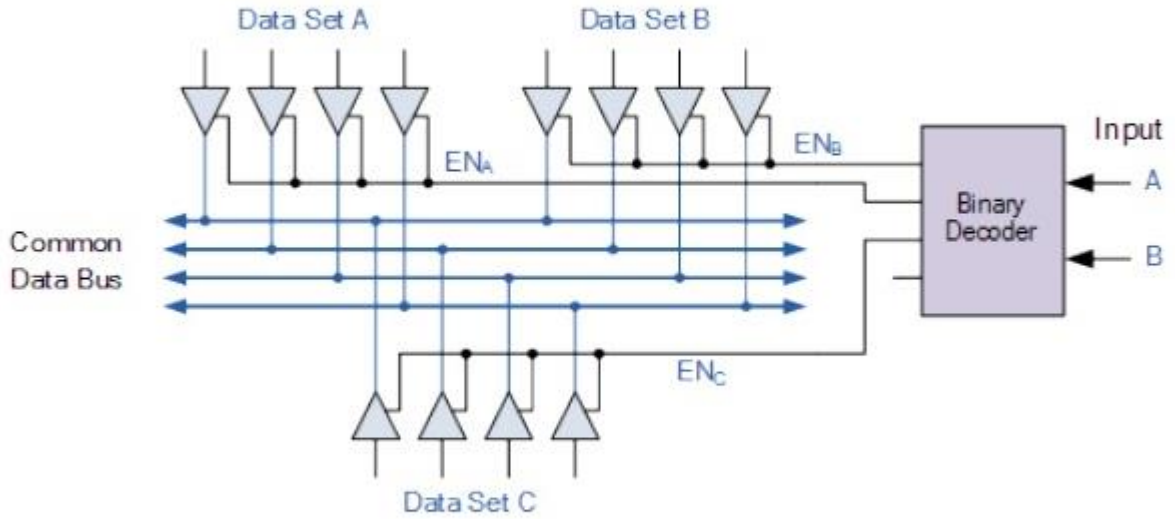
Need VECTOR=(ADDR, DATA)

# Use a BUS: Need Tristate D-registers to selectively ADDR and connect data to bus (read/write)




Above diagram not complete. Need additional R/W control.
Address decoder (i.e. address bus)

# Bus Selection Using Tri-State Buffers




Source: www.electronics-tutorials.ws/logic/logic_9.html

8

https://forums.xilinx.com/t5/Synthesis/tri-state-bus-logic-ceased-to-work-since-Vivado-2015-1-multi/td-p/658590