

Microprocessor Architecture

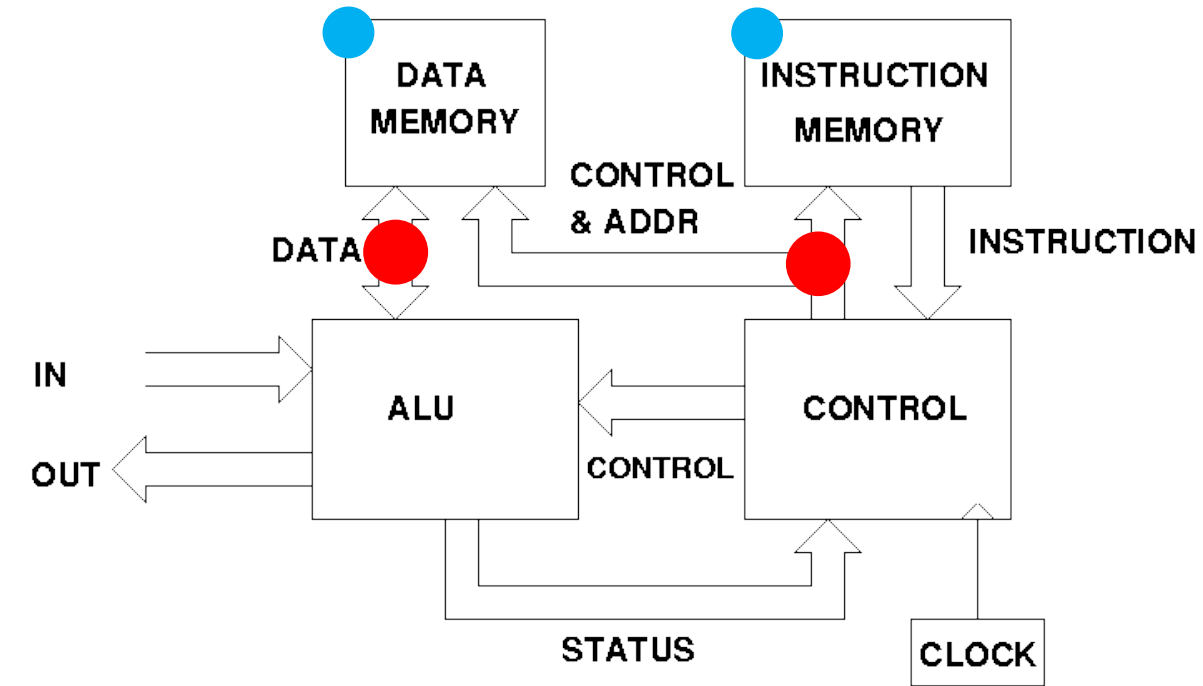
Princeton, Harvard, MIT

Session 2.4

PH435

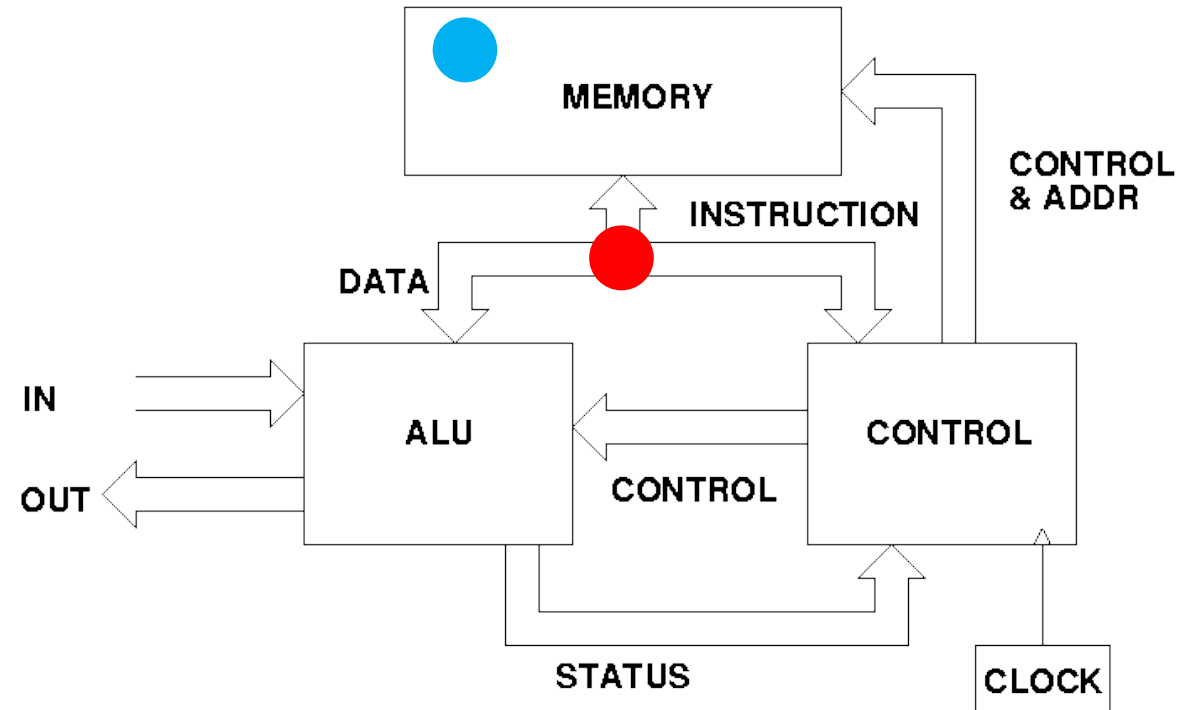
HARVARD ARCHITECTURE

MICROPROCESSOR



PRINCETON (VON NEUMAN) ARCHITECTURE

MICROPROCESSOR



Each manufacturer has specific designs of the wiring layout, address spaces, control lines etc.

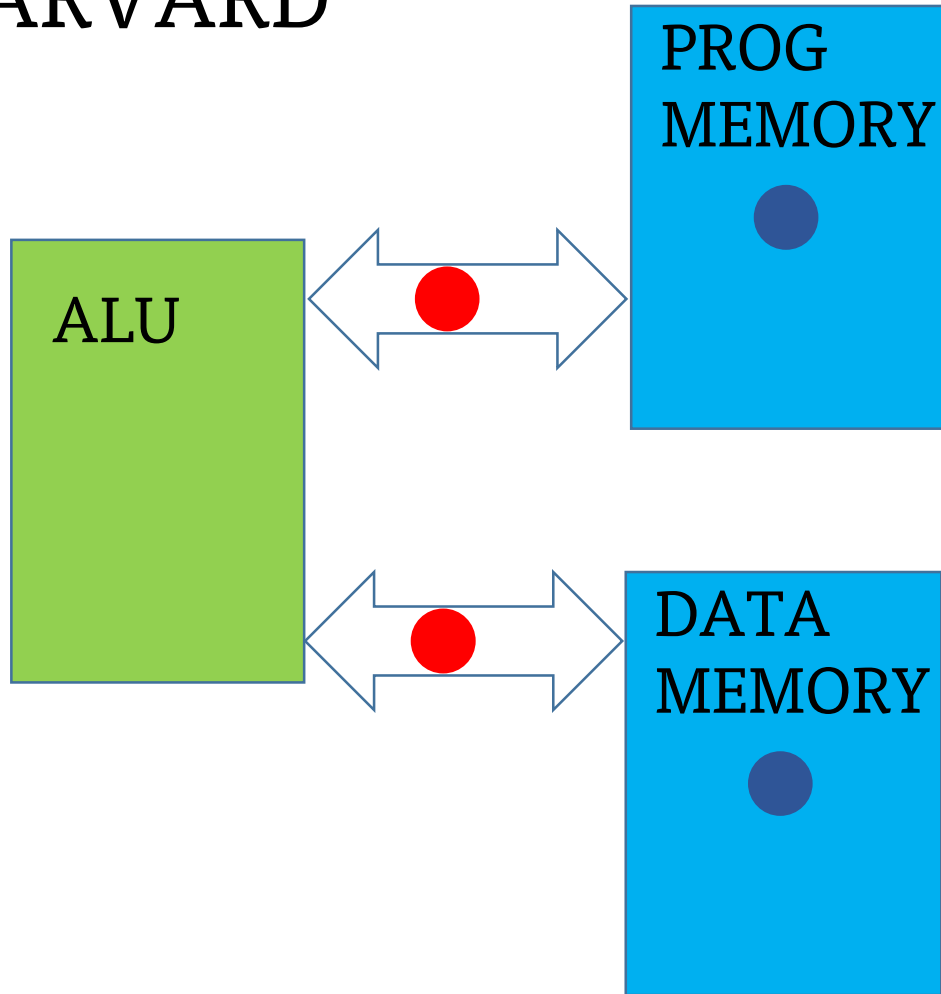
Even the clock speed at which the ALU operates may be different from the memory access clock speed.

Unless you plan to become a CPU designer, it is not interesting to study all the different processor details!
We will focus on the simple Atmega328 in this course

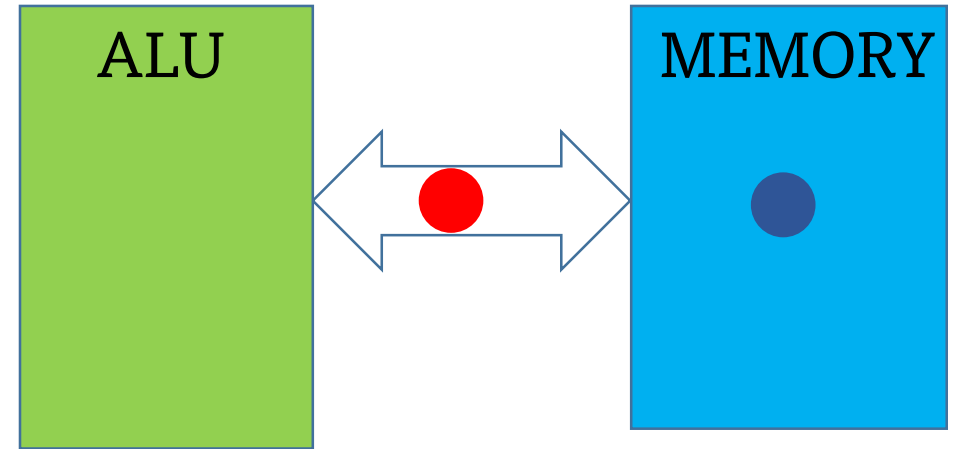
Dominated by a few manufacturers: Intel, ARM, now Apple, Google

- Latest generation hardware details are often proprietary secrets (shared only with OS developers)

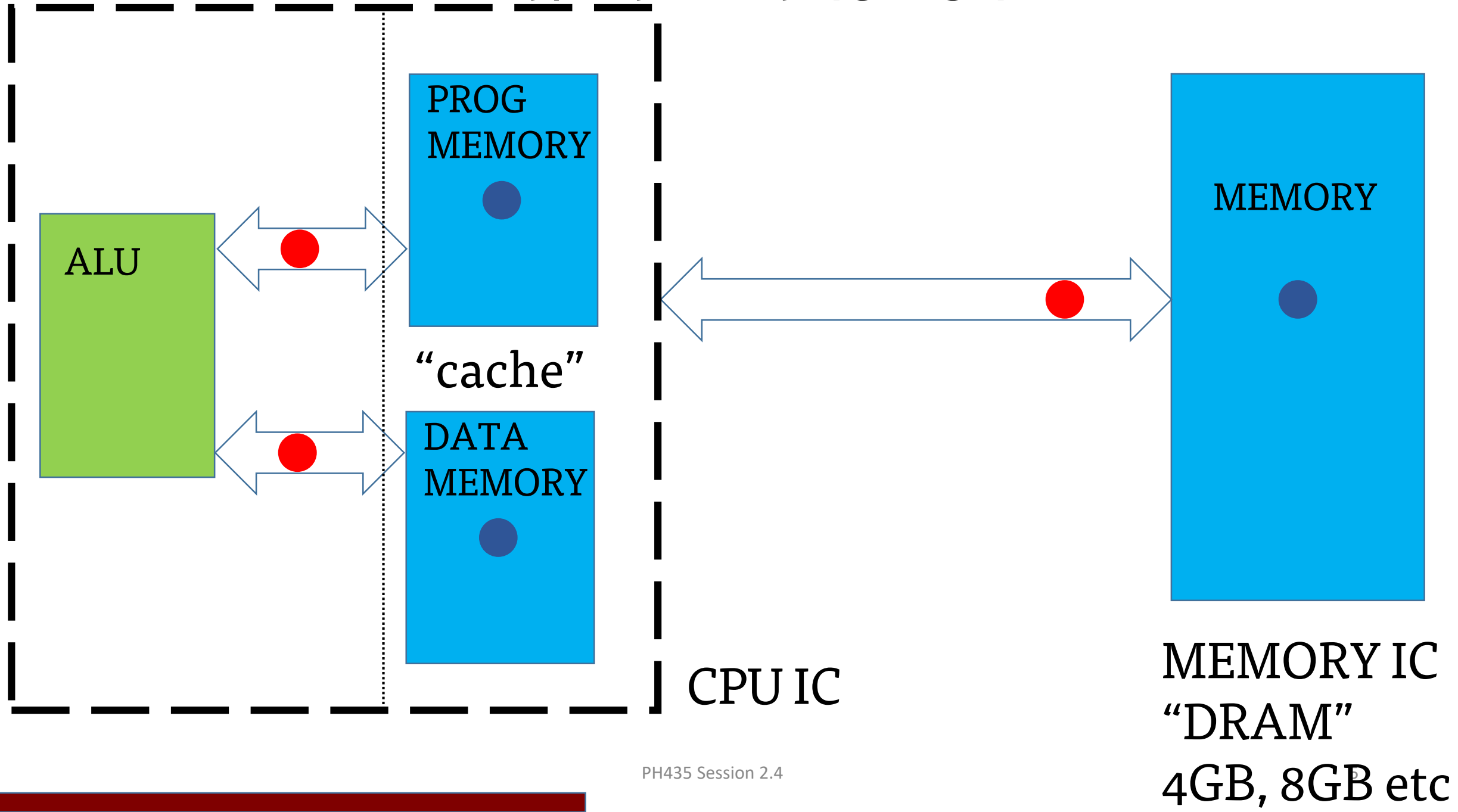
HARVARD



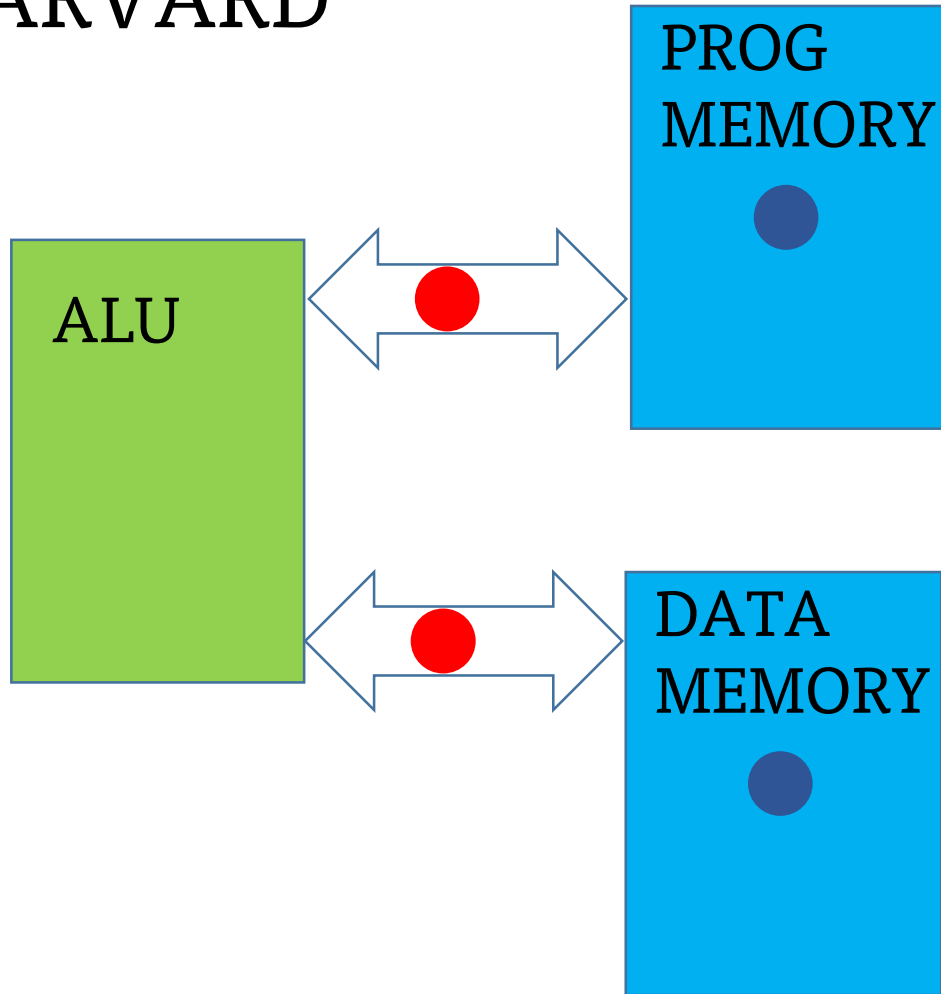
PRINCETON



HARVARD + PRINCETON

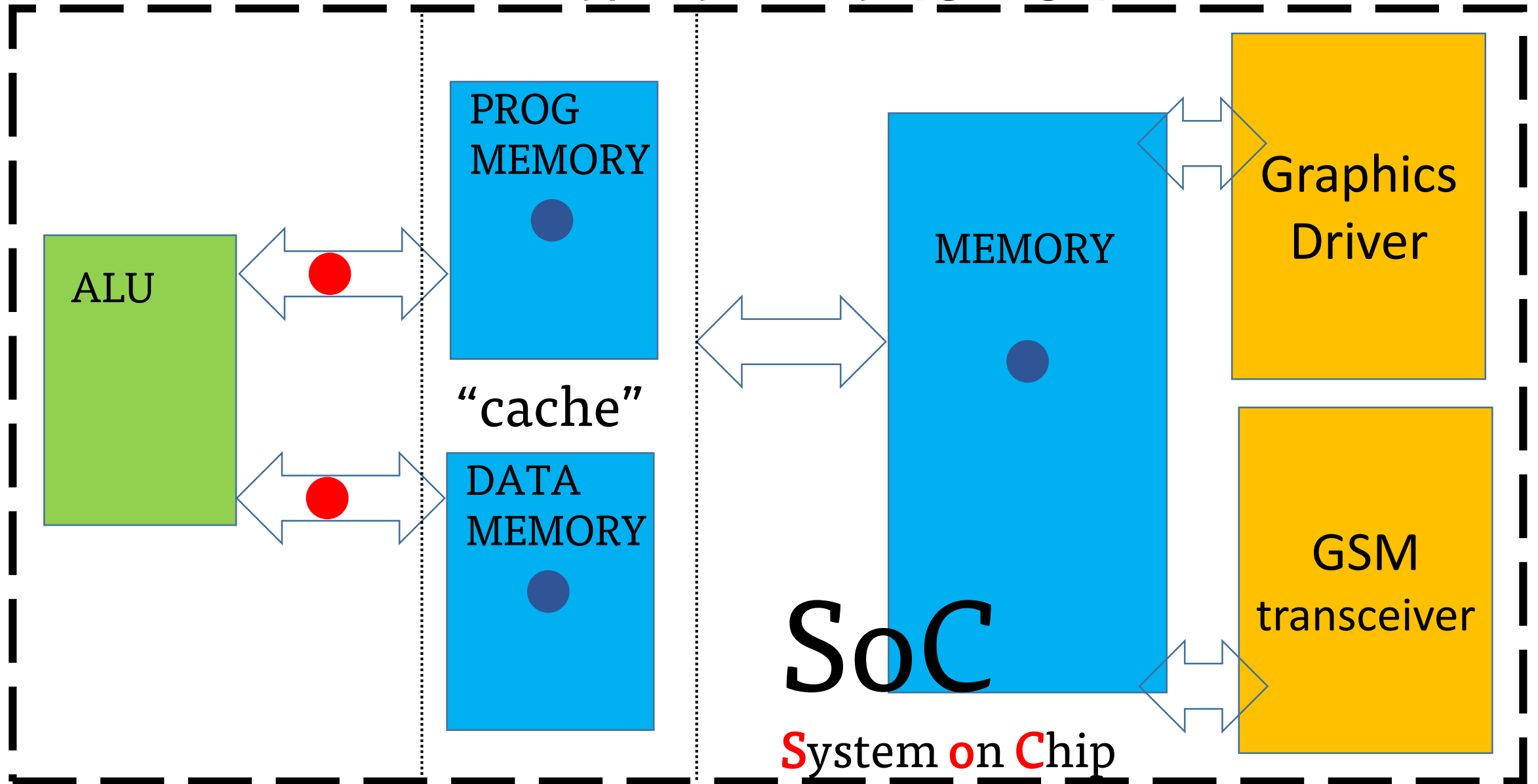


HARVARD



Interlude
– demo on multithreading

HARVARD + PRINCETON+xxx



References:

Real-time Embedded systems: Design principles and Engineering practices, by X. Fan (2015)

Relevant chapters uploaded to Moodle as 2.3_appendix.. With publisher's permission

Set of lecture notes from course EE308 (New Mexico Tech)

http://www.ee.nmt.edu/~rison/ee308_spr00/lectures.html

Linux Kernel Programming:

<http://tldp.org/index.html>

<https://kernelnewbies.org/>

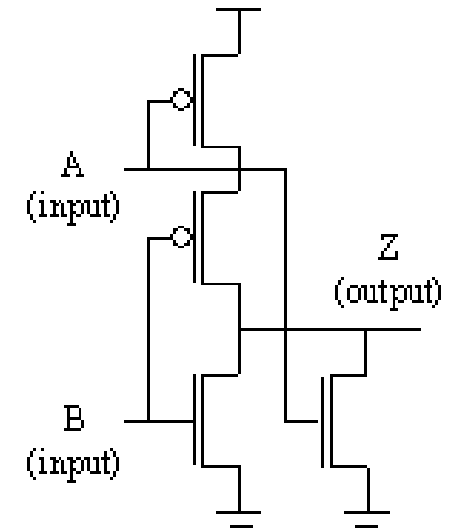
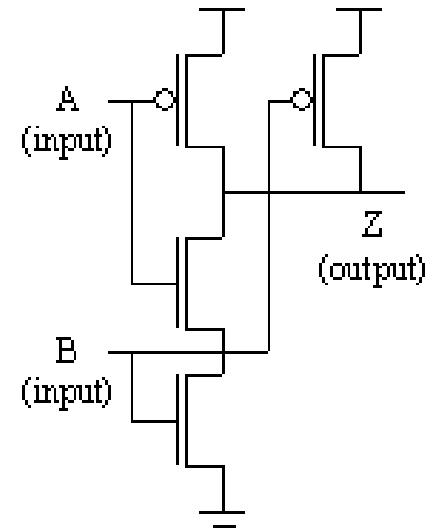
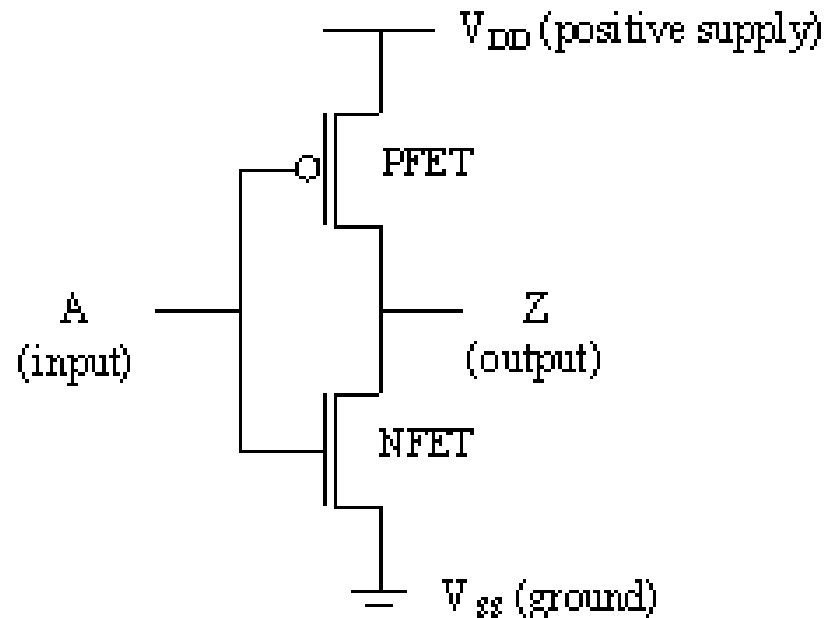
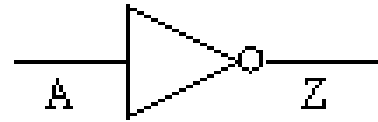
<https://www.cs.utexas.edu/users/ygz/378-03S/> (course on Linux kernel programming)

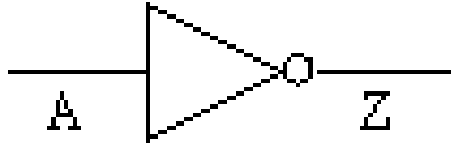
Other websites that discuss bleeding edge technology:

<https://www.tomshardware.com/>

Limits on Computation Speed

ALL Digital Operations are built out of the following 3 Primitive gates





Examine the power consumption of this gate.

Assume that the gates of each MOSFET draw negligible current (i.e. Z drives the gate of a MOSFET in the next gate – hence Z needs to supply negligible current).

