PH435 Assignment 1

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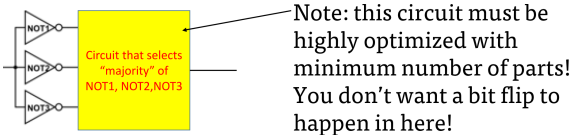
1.



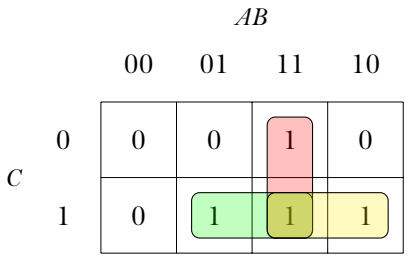
Design a minimal circuit that goes into the yellow box above. It must take 3 digital inputs, and produce 1 digital output. Output = value that matches at least two of the inputs. i.e. Output is the 'majority value' of the 3 inputs. Even if one of the inputs is wrong due to SEU, we will still get the correct answer. [30]

We can construct a simple minimal logic circuit using a Karnaugh Map. First, we establsh the target truth table.

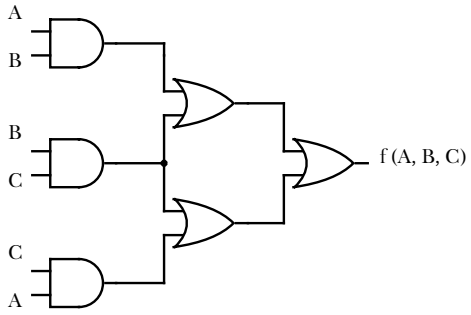
And, the truth table for $f(A, B, C)$

A	B	C	$f(A, B, C)$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Minimizing f using a Karnaugh Map



we get $f(A, B, C) = AB + BC + CA$. The digital logic circuit is thus



2. Optimize the layout of the circuit on a 2D silicon wafer to minimize the surface area. The smaller the 2-D surface area, the lesser the probability of the circuit being hit by a cosmic ray particle. Use the basic source-gate-drain structure of a MOSFET as discussed in class. [70]

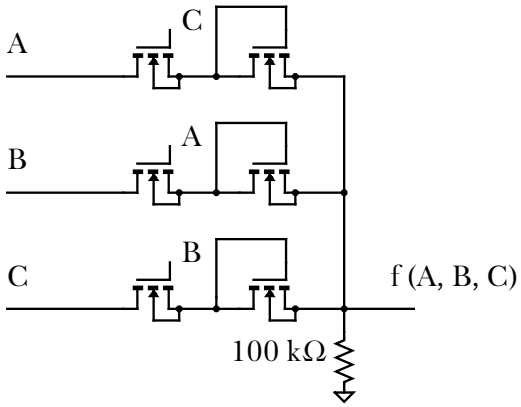
A simple translation of the logic gates to usual MOSFETs is, while a good starting point, leaves much to be desired. A basic but effective change is made, to use the inputs to drive the transistor terminals instead of V_{CC}.

A simple version of the and-gate is given by an NMOS transistor with one of the inputs on the source, and another on the gate. A starting circuit is with three gates of this form, representing AB, BC, and AC in our function, and simply connecting the drain terminals of the three to the result. When either of the three are activated, the respective inputs drive the result. But in the absence of any signal, result is floating! To prevent this, we connect the result to ground via a large resistor.

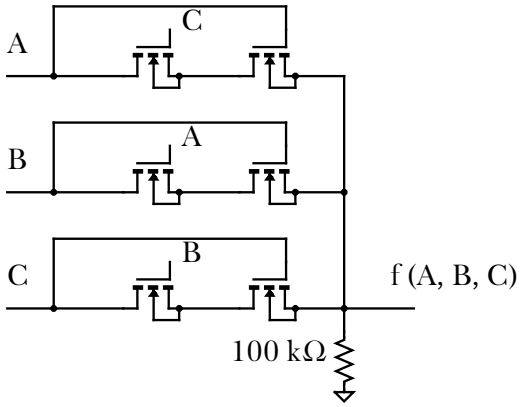
A problem arises if only one of the transistor lines is active, as another line will have its gate high (consider $\langle A, B, C \rangle = \langle 1, 1, 0 \rangle$) and will be shorting V_{CC} to ground. To prevent such a scenario happening, each of the output lines can be gated by their own output (Fig 1a) so that it is open when output is low.

I am not sure if shorting the gate and source of a MOSFET could have unforeseen consequences, another (possibly better, but harder to make into a small PCB due to the longer connection required) solution is to connect the gate to the initial source to the transistor line, as shown in Fig 1b. Another possibility is to

connect the output of the first transistor in each line to the second's gate, and have the source be driven by V_{CC}. I have not considered this here because of the possible required connections to drive it making the arrangement inefficient. That would probably be better if the output needs to drive another circuit, since there would (intuitively) be a casacading loss continuing the input driven circuits.



(a) with short



(b) without short

Figure 1: MOSFET circuits

Finally, drawing the circuit as a possible way to fabricate it on a wafer, trying to minimize the circuit area, to minimize chances of an SEU

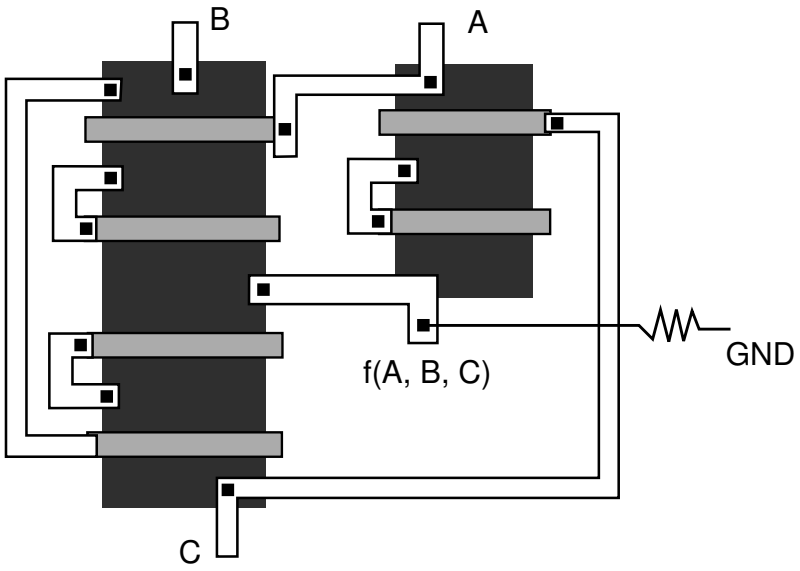


Figure 2: The circuit (with short) from Fig 1a on a wafer

In figure, white represents wires, dark gray, the substrate, while light gray represents the poly (gates). Note — The diagram is meant to only be representative of positioning, so liberties have been taken with spacing for the sake of clarity.