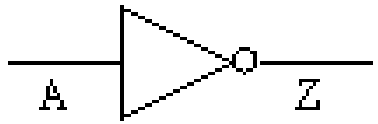
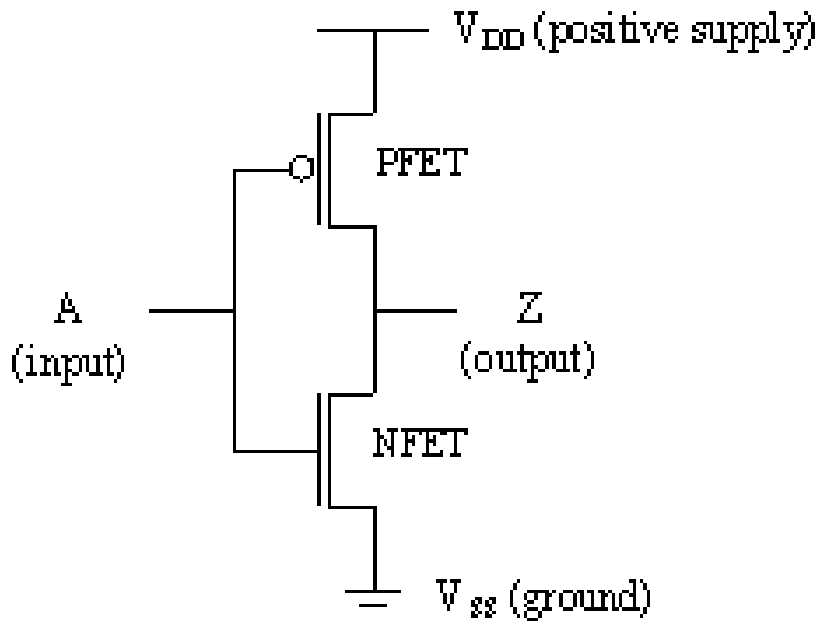
Microprocessor Architecture Speed Limit

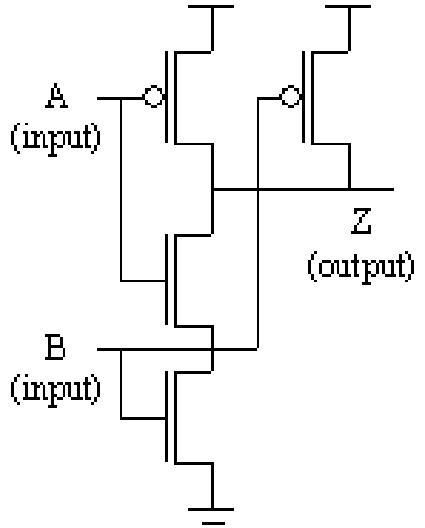
Session 2.4

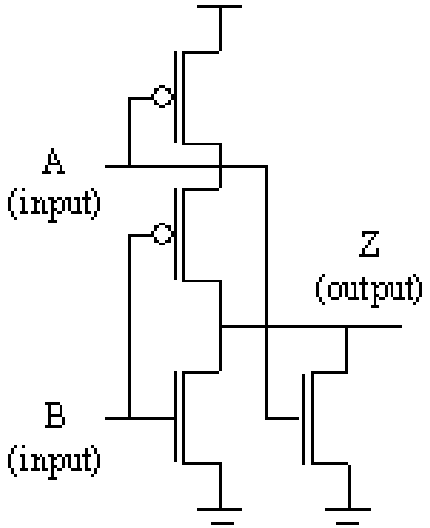
PH435

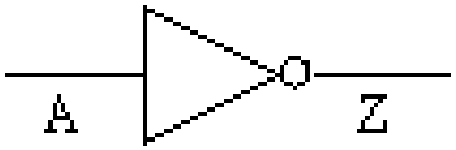
ALL Digital Operations are built out of the following 3 Primitive gates

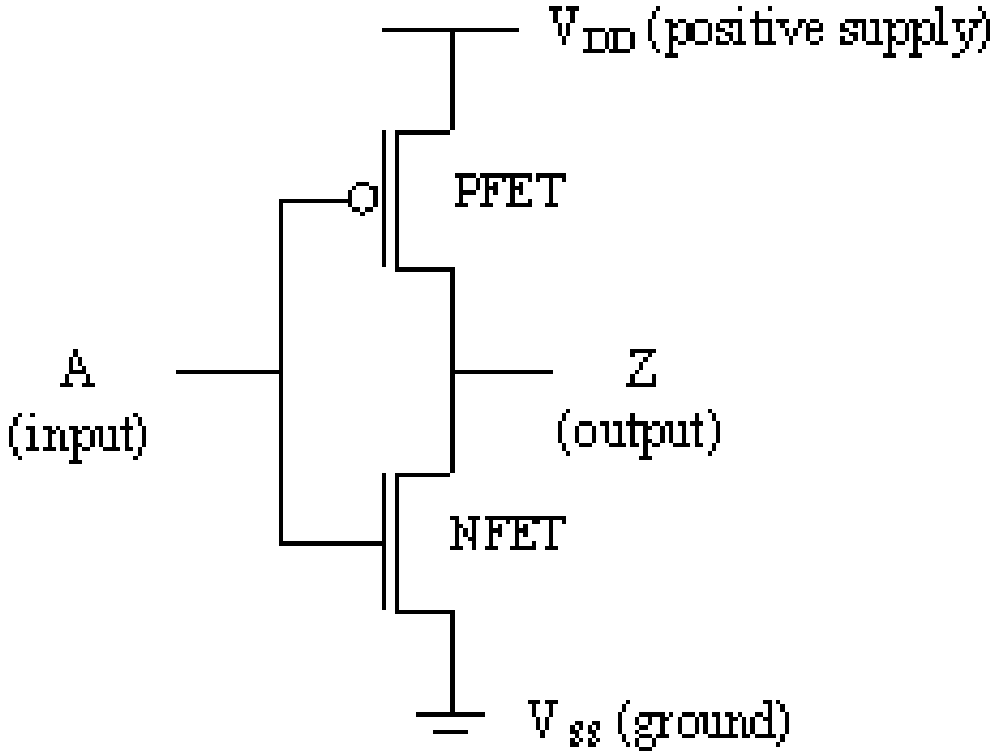












Examine the power consumption of this gate.

Assume that the gates of each MOSFET draw neglible current (i.e. Z drives the gate of a MOSFET in the next gate – hence Z needs to supply neglible current.

?

Static power dissipation of a CMOS gate is negligible.

However, when the gate switches logic (typically in sync with a clock signal), there is a spike in the power consumption

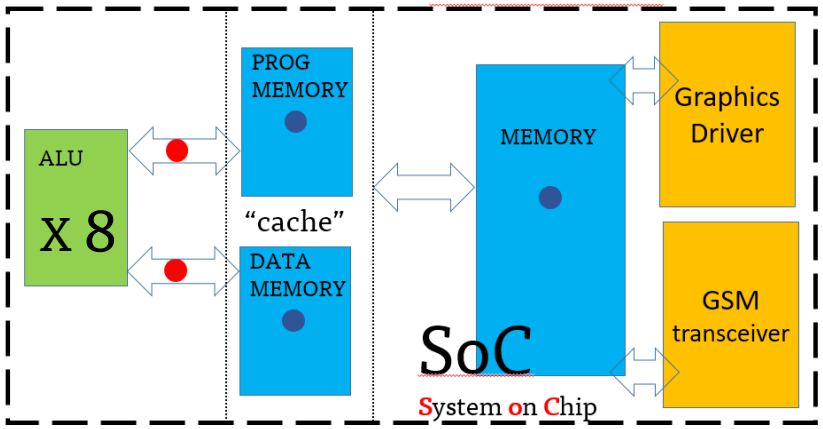
No matter how small you make the individual MOSFETS, the higher you try to drive the clock frequency, i.e. make your CPU work faster – the power dissipation increases beyond the point that:

1) Temperature of the silicon increases so that the fundamental equations governing e/h transport in the silicon are not valid anymore
2) Silicon is not Silicon anymore (black goo!)

Dennard Scaling

https://tinyurl.com/qualcommsd850

What does the 'Octa-core' processor in your flagship smartphone do?



"up to 2.9 GHz" – but actually runs at ~ 1.8 GHz top

Programs are multi-threaded across different cores to reduce power dissipation

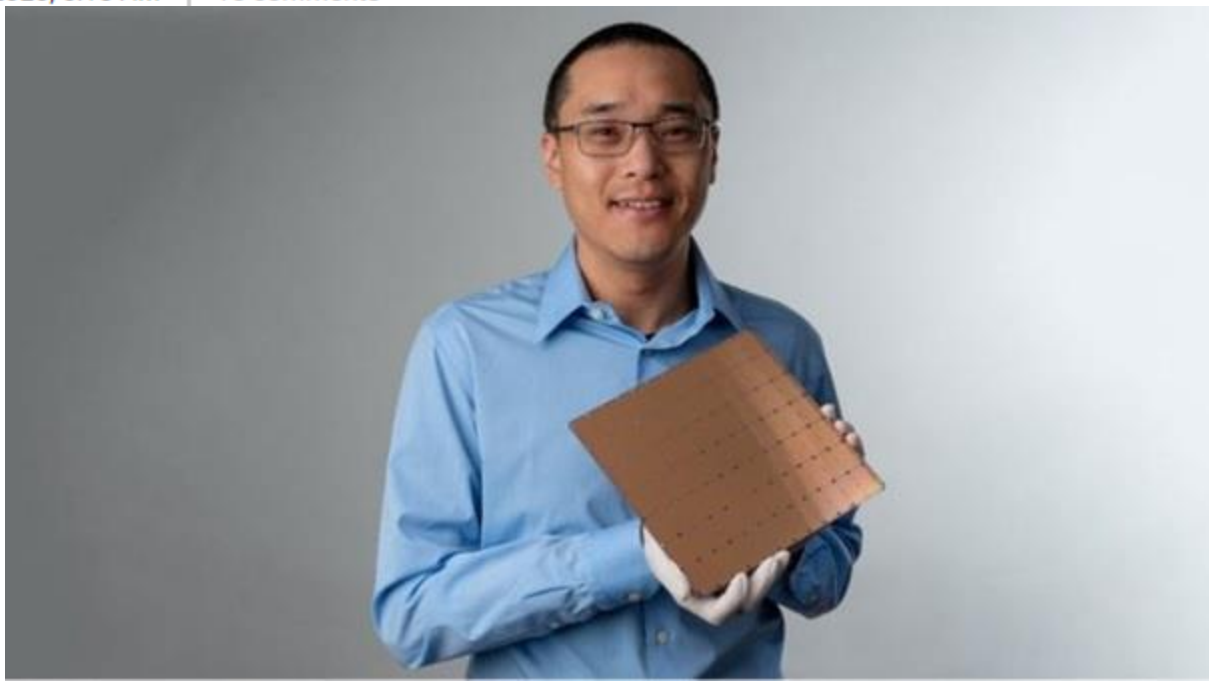
Ever notice your cellphone get hot when running

Dennard Scaling

Cerebras reveals details of the world's largest chip: 2.6 trillion transistors, 850,000 cores

Size matters

By **Rob Thubron** on August 19, 2020, 5:18 AM | 15 comments



18 GB
On chip
cache