PH435 Assignment 1

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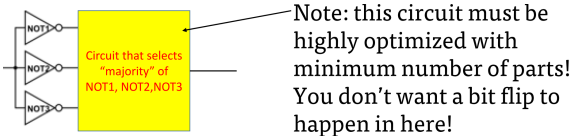
1.



Design a minimal circuit that goes into the yellow box above. It must take 3 digital inputs, and produce 1 digital output. Output = value that matches at least two of the inputs. i.e. Output is the 'majority value' of the 3 inputs. Even if one of the inputs is wrong due to SEU, we will still get the correct answer. [30]

We can construct a simple minimal logic circuit using a Karnaugh Map. First, we establosh the form of the circuit and construct a target truth table.

Figure 1: Expected Circuit

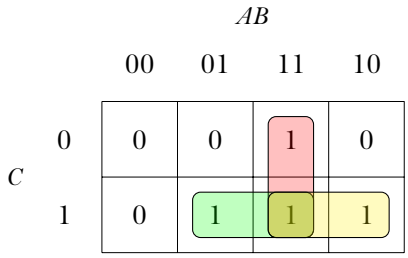
And, the truth table for $f(A, B, C)$

A	B	C	$f(A, B, C)$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Minimizing f using a Karnaugh Map

we get $f(A, B, C) = AB + BC + CA$.

2. Optimize the layout of the circuit on a 2D silicon wafer to minimize the surface area. The smaller the 2-D surface area, the lesser the probability of the circuit being hit by a cosmic ray particle. Use the basic source-gate-drain structure of a MOSFET as discussed in class. [70]


AB
00
01
11
10
C
0
1
0
0
1
0
0
1
1
1