RFIC

Assignment 2

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System specs

Parameters	Given specs	Calculated specs	Achieved specs
Operating frequency	7.295 GHz	7.295 GHz	7.295 GHz
Output IF frequency	200 MHz	200 MHz	200 MHz
Supply voltage	1.2 V	1.2 V	1.2 V
Voltage Gain	≥ 16 dB	16.13 dB	17.74 dB
(1 tone) 1 dB compression	≥ -32 dB	-33.37 dBm	-28.54 dBm
IIP3	≥ -22 dB	-22.16 dBm	-19.02 dBm
NF	≤ 4 dB	2.22 dB	3.93 dB
Bias current	N/A	N/A	1.3 mA
Power consumption	N/A	N/A	18mA x 1.2V = 21.6 mWatt

Mixer specs

Parameters	Calculated specs	Achieved specs
Operating frequency	7.3 GHz	7.3 GHz
Output IF frequency	200 MHz	200 MHz
Supply voltage	1.2 V	1.2 V
Voltage Gain	0.7819 V/V	0.7935 V/V
(1 tone) 1 dB compression	64.1 mV	74.98 mV
IIP3	202.71 mV	≈ 200 mV
NF	8.38 dB	13.37 dB
Bias current	N/A	850 µA
Power consumption	N/A	1.6mA x 1.2V = 1.92 mWatt

I have not tried to increase current and reduce the noise because I wanted to use minimum amount of current for which my circuit meets all the specs including NF. Hence, I have done the increase in current for system only, not for mixer. I did not want to chases ideal mixer NF calculated from equation 8.38 dB, which results in very good NF for system 2.22 dB.

Index

Chapter 1 Design of Mixer

- Choice of topology
- Transistor characterization
- Voltage Gain
- Linearity
- Noise figure

Chapter 2 Design of system (LNA + Mixer)

- Voltage Gain
- Linearity
- Noise figure
- Circuit

Chapter 1 Design of Mixer

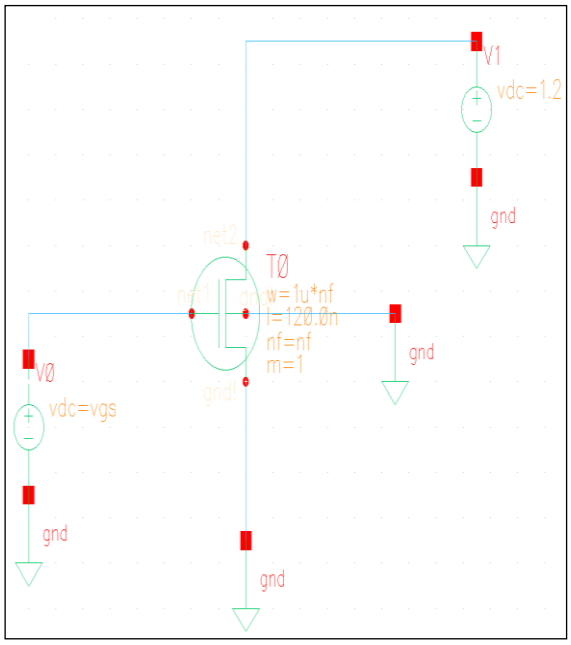
Design steps

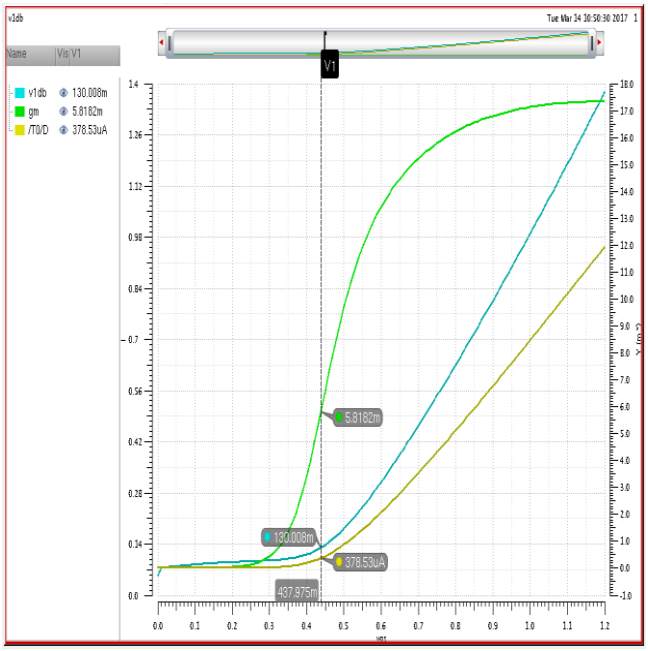
Choice of topology

We are using double-balanced cross-coupled circuit, commonly called the Gilbert cell, as our topology. The Gilbert double-balanced mixer configuration is widely used in RFIC applications because of its compact layout and moderately high performance. For a switching Gilbert cell, the LO input of the mixer does not need to exhibit high linearity (i.e. low intermodulation distortion and harmonic distortion) as it is purely a switching signal. It is the RF input for the Gilbert cell mixer that needs to provide the linearity.

Transistor characterization

Circuit used for characterization of transistor,





Vgs vs Ids, gm and V_{1dB} = 2* Ids / gm for transistor with 25 µm width and 120 nm length and vgs is varing from 0 to 1.2 V.

From this graph we can use value of g_m and $I_0 = 2\ I_{DS}$ for theoretical calculation.

Here I have use this equation to find V_{1dB},

$$V_{1dB} = \frac{I_0}{g_m}$$

Design criteria (getting mixer specs from system and LNA specs)

Voltage Gain:

Input RF referred gain is given with following equation (without degeneration resistance),

$$A_v = \frac{2}{\pi} g_m R_{DL}$$

Gain can be increased by increasing Rd or by increasing gm by changing transistor size or bias current. Assuming dc current is flowing through Rd, as increase of current or in the size of Rd directly results in reduced headroom. Increasing gm by increasing transistor size will mean less voltage drop across the transistor, which is good for headroom, but it makes the transistor itself less linear since linearity is related to the overdrive voltage, Vgs-Vth.

From the above equation we can clearly say that $A_v \propto R_d$. Hence, I have increase my Rd to 520Ω to increase my gain close to specs.

To determine mixer gain specs from LNA and system specs,

$$A_{mix} = \frac{A_{sys}}{A_{LNA}}$$

Where A_{sys} = 16 dB = 6.31 V/V

For 20.83Ω output impedance, open circuit LNA gain is given by,

$$A_{OC} = \left(\frac{20.83 + 50}{50}\right) x6.092 = 8.63\, V/V$$

Where Zout = 20.83Ω and Av = 15.695 dB = 6.0918 V/V

Now we can find LNA gain for 300Ω load,

$$\begin{aligned} A_{LNA} &= \left(\frac{300}{20.83 + 300}\right) A_{oc} \\ &= \left(\frac{300}{20.83 + 300}\right) x8.63 \\ &= \mathbf{8.06969}\, V/V = \mathbf{18.137}\, dB \end{aligned}$$

From the transistor characterization from previous section,

g_m = 5.8182m

I_{DS} = 378.53µA

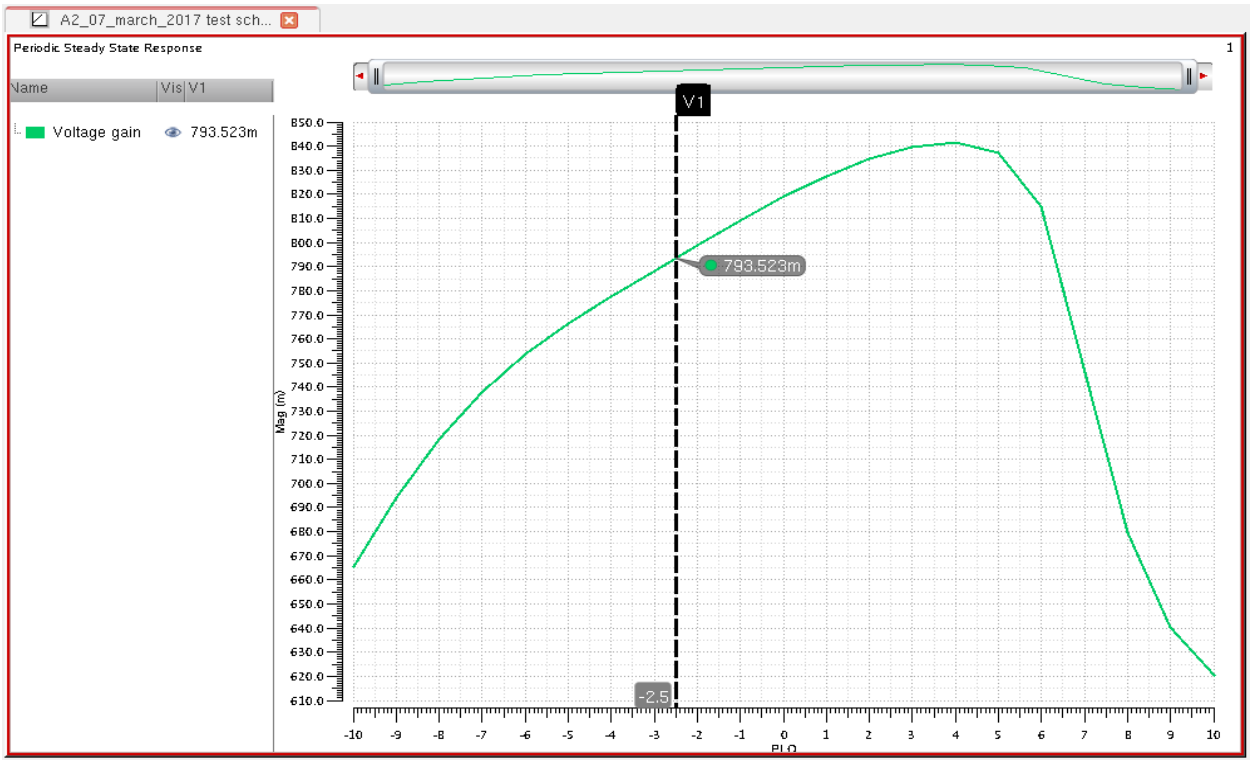
V_{GS} = 437.975mV

Now, gain of mixer is,

$$\begin{aligned} A_{mix} &= \frac{A_{sys}}{A_{LNA}} \\ &= \frac{6.31}{8.07} = \mathbf{0.7819}\, V/V \end{aligned}$$

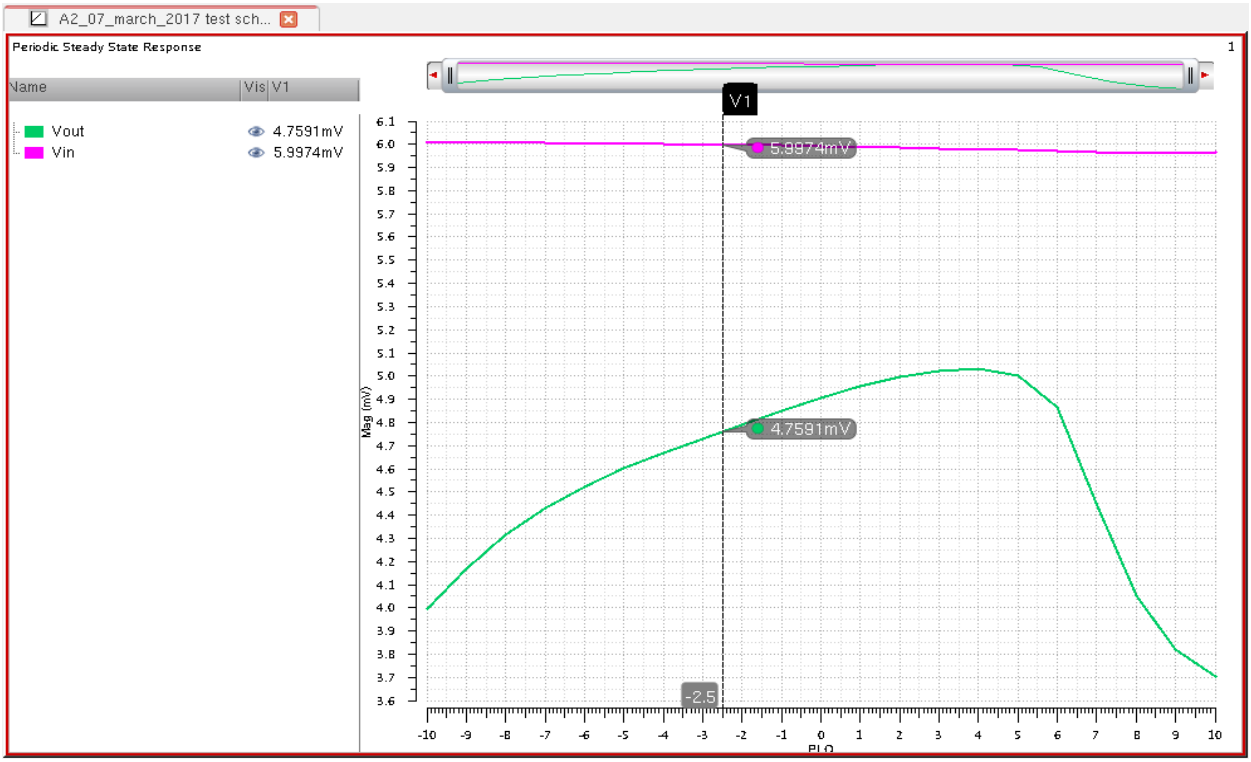
For gain of mixer I have simulated number of graphs,

Frist one is PLO (-10 to 10 dBm) vs voltage gain of mixer,



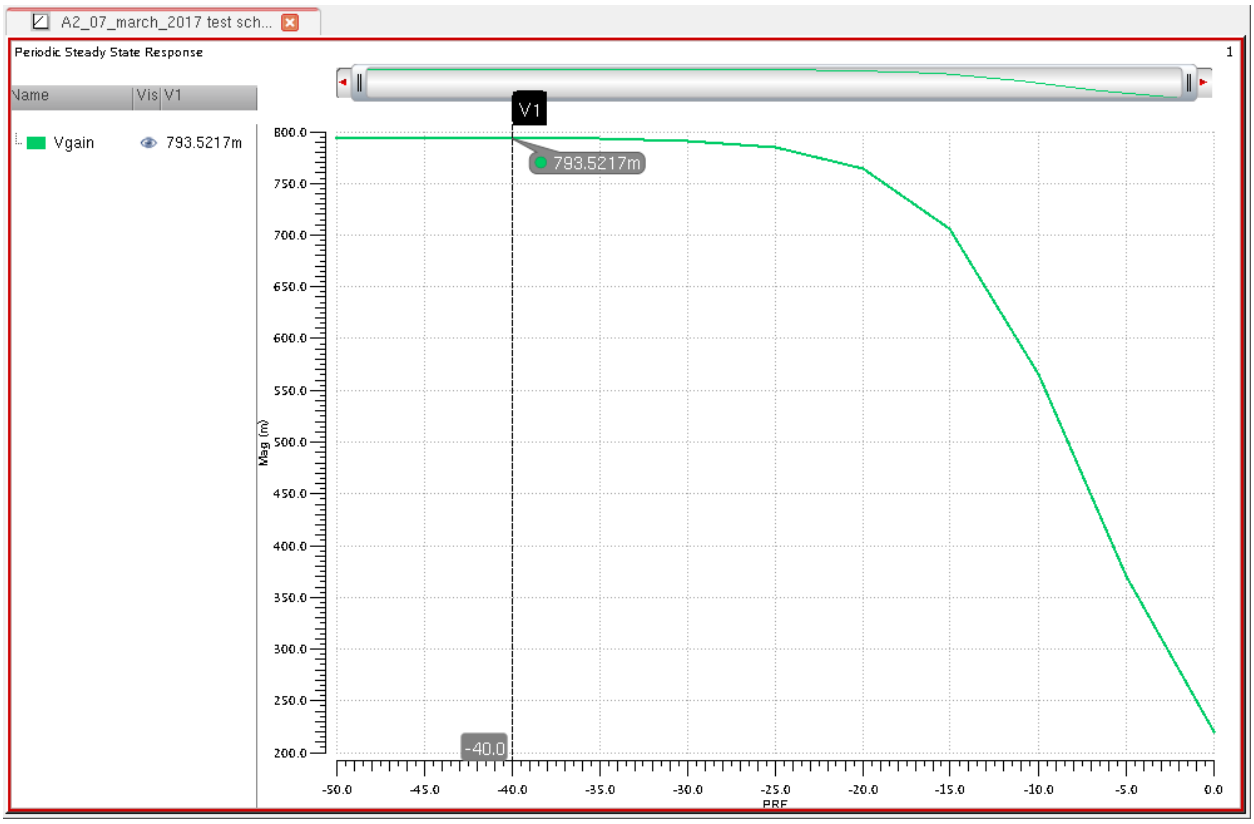
As I am taking -2.5 dBm value of PLO for my circuit I have shown gain at that particular PLO is **0.7935** V/V, which is close to my theoretical calculation of **0.7819** V/V.

Second graph is output and input differential voltage vs PLO,



Here from the ghraph we can clearly say that voltage gain is equal to Vin/ Vout = 5.9974/4.7591 = 0.7819 V/V.

Third graph is PRF(-50 to 0 dBm) vs voltage gain,



$$A_v = \frac{2}{\pi} g_m R_{DL}$$

$$R_{DL} = \frac{0.7819\ x\ \pi}{2x5.8182x10^{-3}}$$

$$\approx \mathbf{212}\Omega$$

Linearity

(1 tone) 1dB compression point

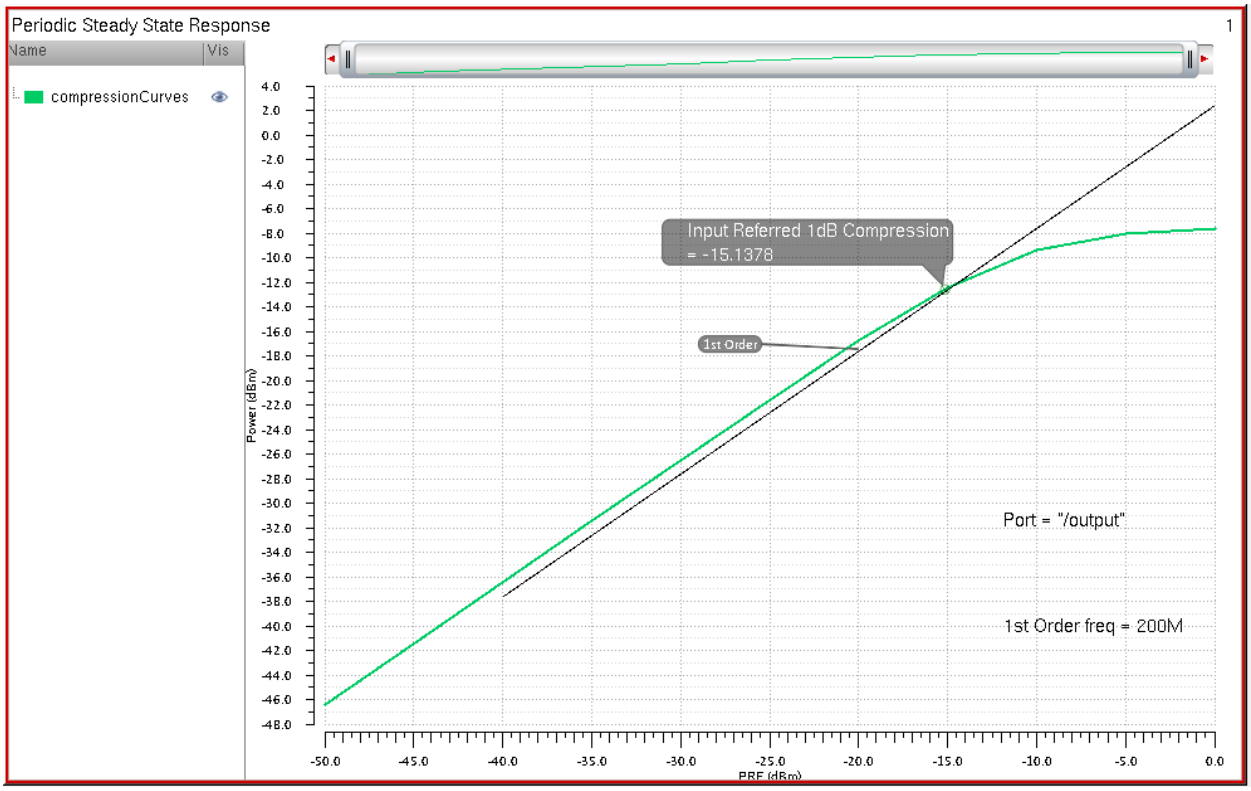
(1 tone) 1dB compression point of mixer is given as,

$$V_{1dB} = A_{LNA} x V_{1dBsys}$$

$$= 8.07x7.943$$

$$= \mathbf{64.1}mV$$

Below is the simulated graph of PRF (-50 to 0 dBm) vs power for (1 tone) 1dB compression point of mixer which is **-15.1378** dBm.



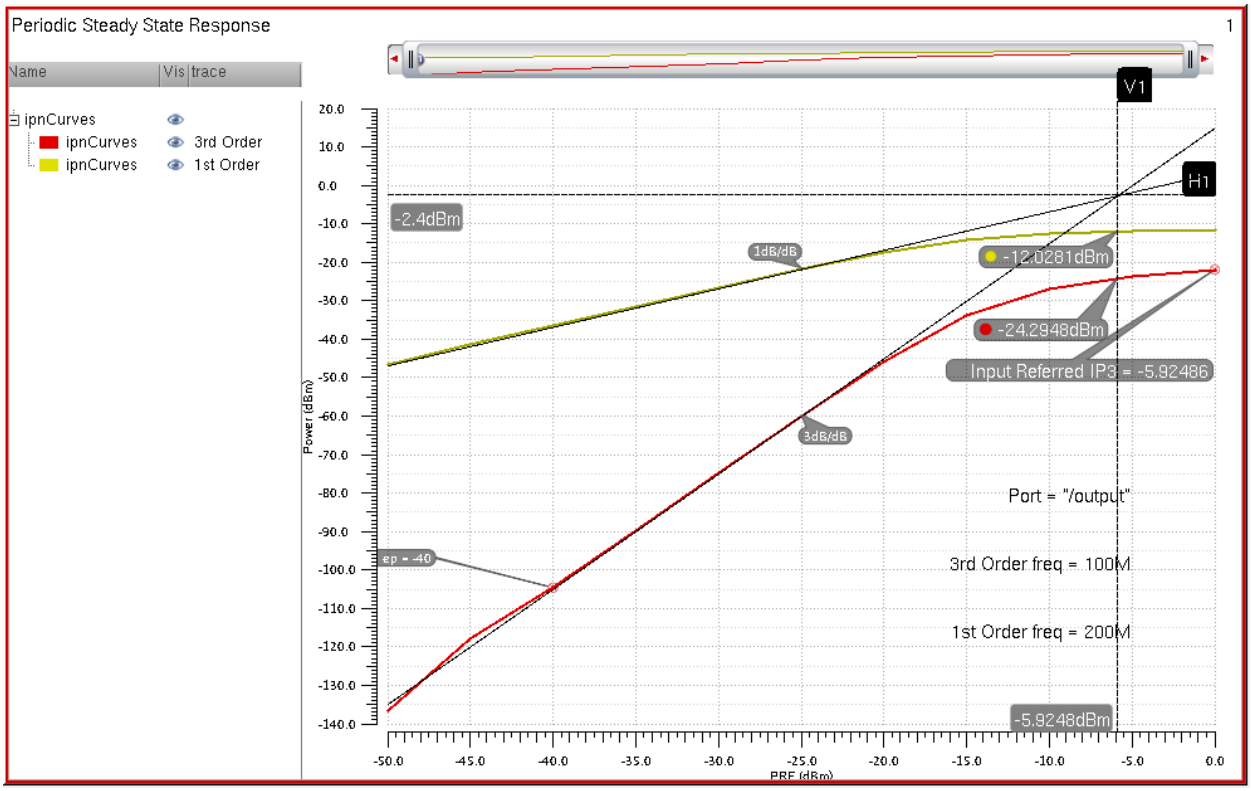
Here we can see that on Y axis value is coming up as -12.5 dBm which is equal to 74.989 mV which is greater than what we derived from the calculation hence the specs been met.

<u>IIP3 (2 tone) of mixer is given as,</u>

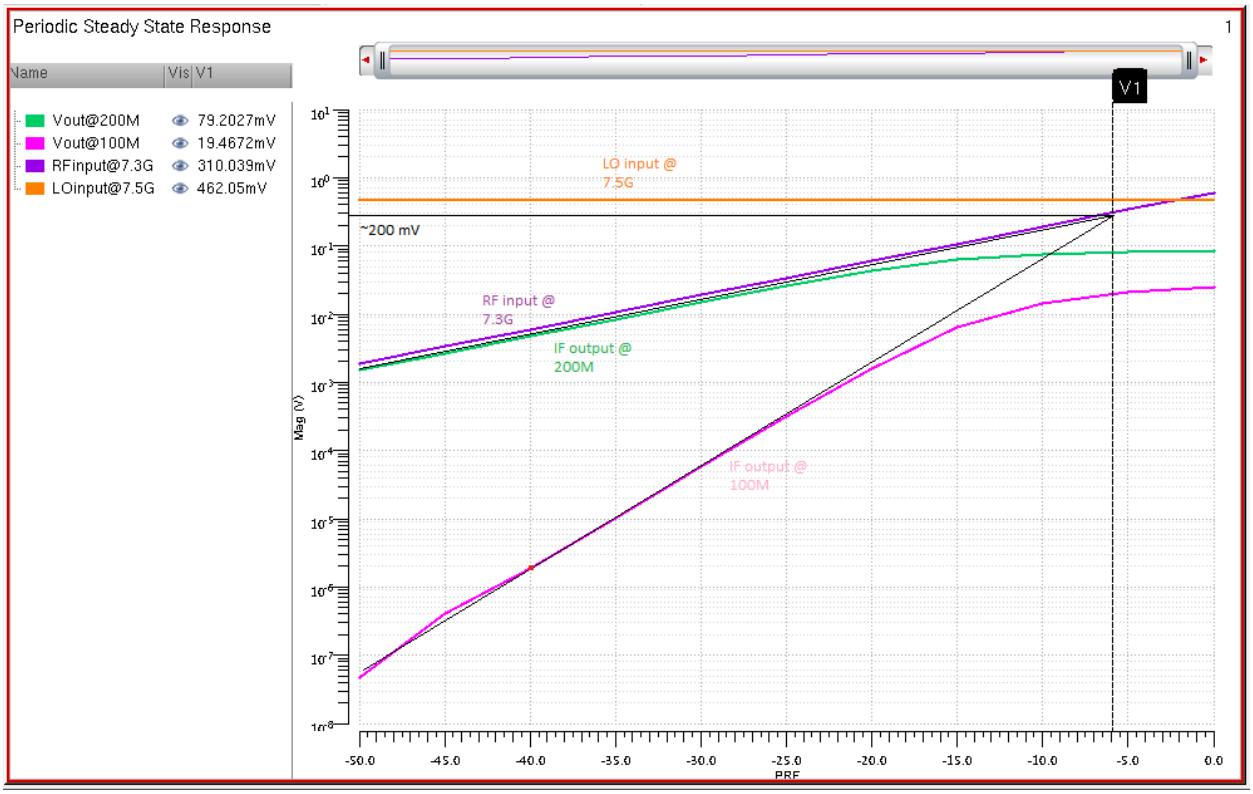
$$V_{IIP3} = A_{LNA} x V_{IIP3sys}$$
$$= 8.07x25.12$$
$$= \mathbf{202.7184}mV$$

There are two graph for IIP3,

First one is for PRF (-50 to 0 dBm) vs power for two tones at output,



Second graph is PRF (-50 to 0 dBm) vs differential output voltage for 100MHz and 200MHz, with LO and RF input.



From the figure above we can clearly see that practical value of IIP3 point ≈200 mV is matching with theoretical value 202.7184 mV.

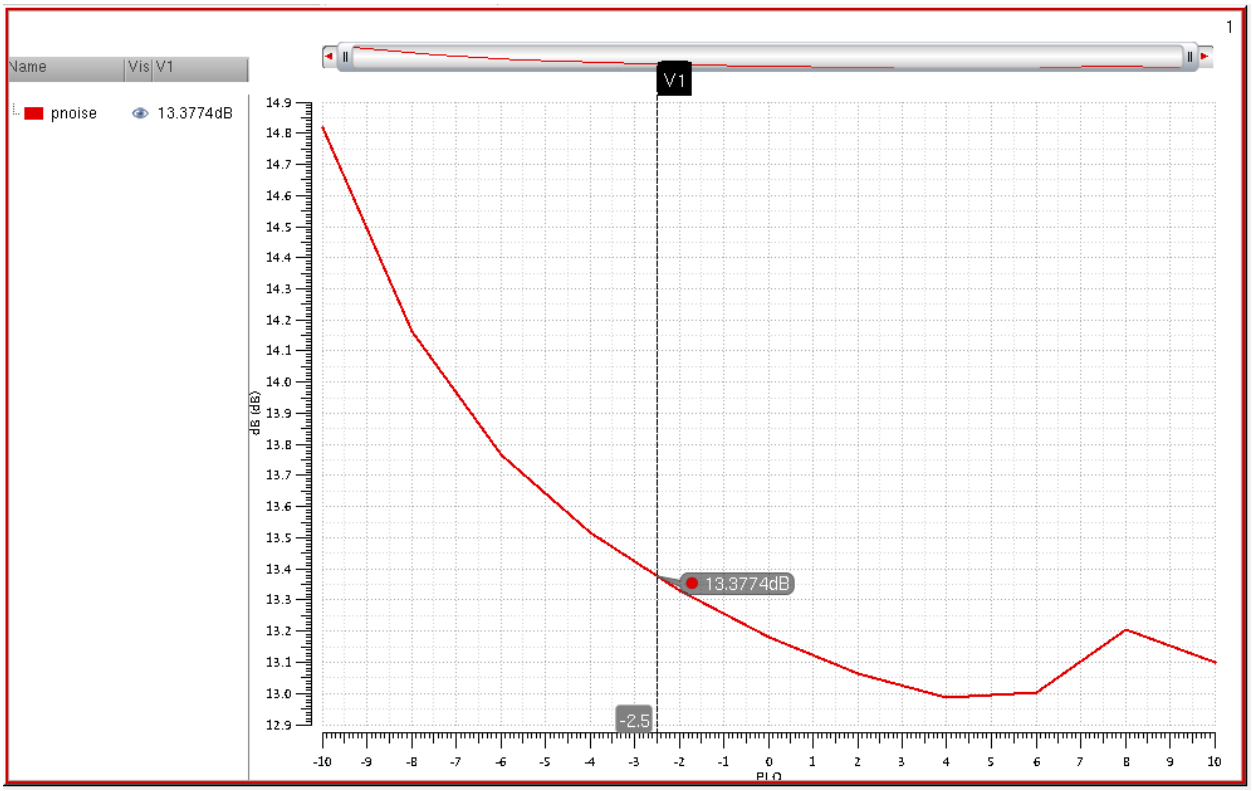
Noise figure

$$F = 1 + \frac{1}{{A_v}^2}\frac{R_{DL}}{R_S} + \frac{2\gamma}{g_m R_S}$$
$$= 1 + \frac{1}{0.7819^2}\frac{180}{50} + \frac{2}{5.8182x50}$$
$$= 6.89$$

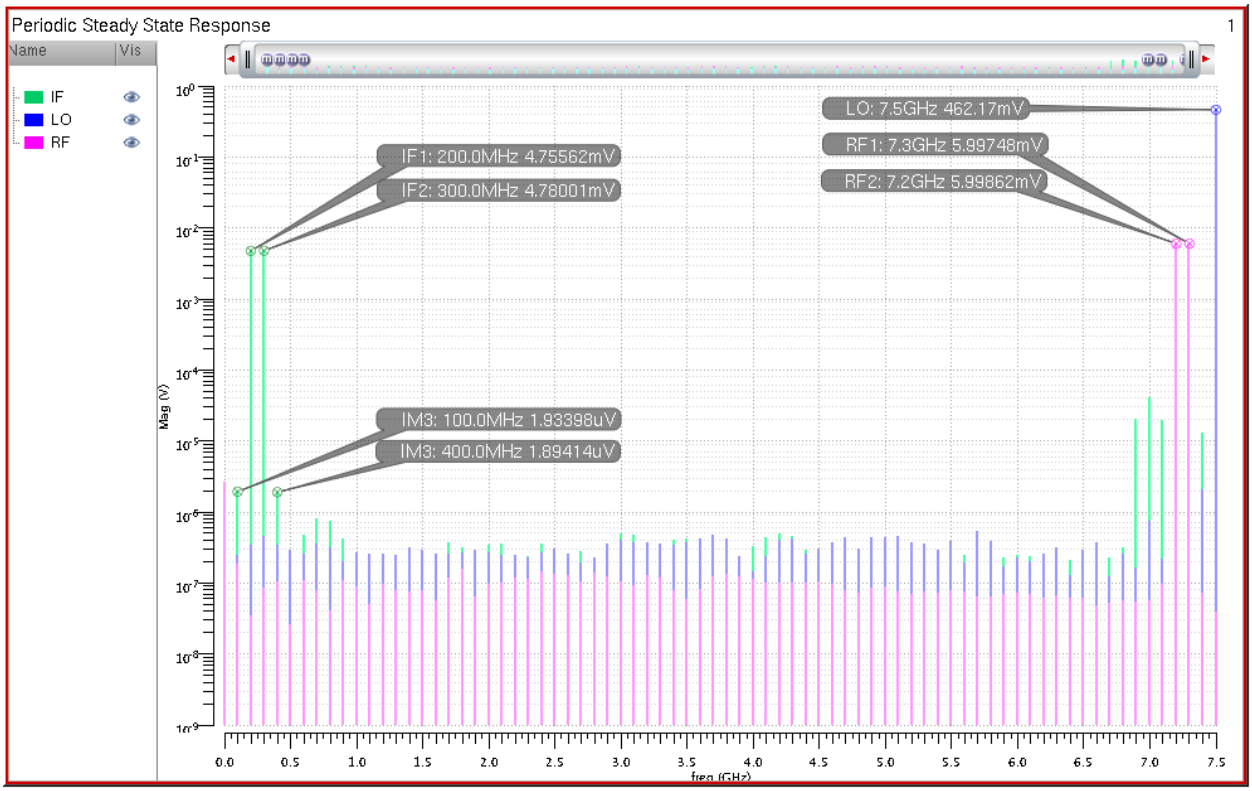
$$NF = 10\log 6.89 = \mathbf{8.38}dB$$

From the simulation I am getting much higher noise figure than calculation. I am going to reduce the noise figure by increasing bias current through the circuit.

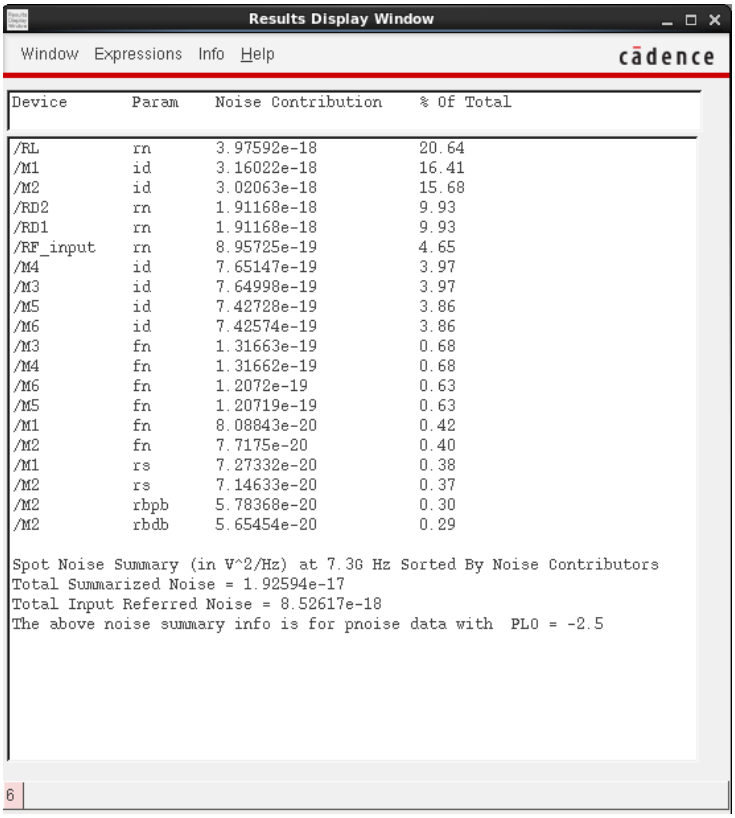
Graph below is PLO (-10 to 10 dBm) vs noise figure(dB),



Voltage vs frequency spectrum is given below for two tone RF input,



Noise summary for he system is given below,



Results Display Window

Window Expressions Info Help cadence

Device	Param	Noise Contribution	% Of Total
/RL	rn	3.97592e-18	20.64
/M1	id	3.16022e-18	16.41
/M2	id	3.02063e-18	15.68
/RD2	rn	1.91168e-18	9.93
/RD1	rn	1.91168e-18	9.93
/RF_input	rn	8.95725e-19	4.65
/M4	id	7.65147e-19	3.97
/M3	id	7.64998e-19	3.97
/M5	id	7.42728e-19	3.86
/M6	id	7.42574e-19	3.86
/M3	fn	1.31663e-19	0.68
/M4	fn	1.31662e-19	0.68
/M6	fn	1.2072e-19	0.63
/M5	fn	1.20719e-19	0.63
/M1	fn	8.08843e-20	0.42
/M2	fn	7.7175e-20	0.40
/M1	rs	7.27332e-20	0.38
/M2	rs	7.14633e-20	0.37
/M2	rbpb	5.78368e-20	0.30
/M2	rbdb	5.65454e-20	0.29

Spot Noise Summary (in V^2/Hz) at 7.3G Hz Sorted By Noise Contributors
Total Summarized Noise = 1.92594e-17
Total Input Referred Noise = 8.52617e-18
The above noise summary info is for pnoise data with PLO = -2.5

6

Chapter 2 Design of system (LNA + Mixer)

Voltage Gain of the system

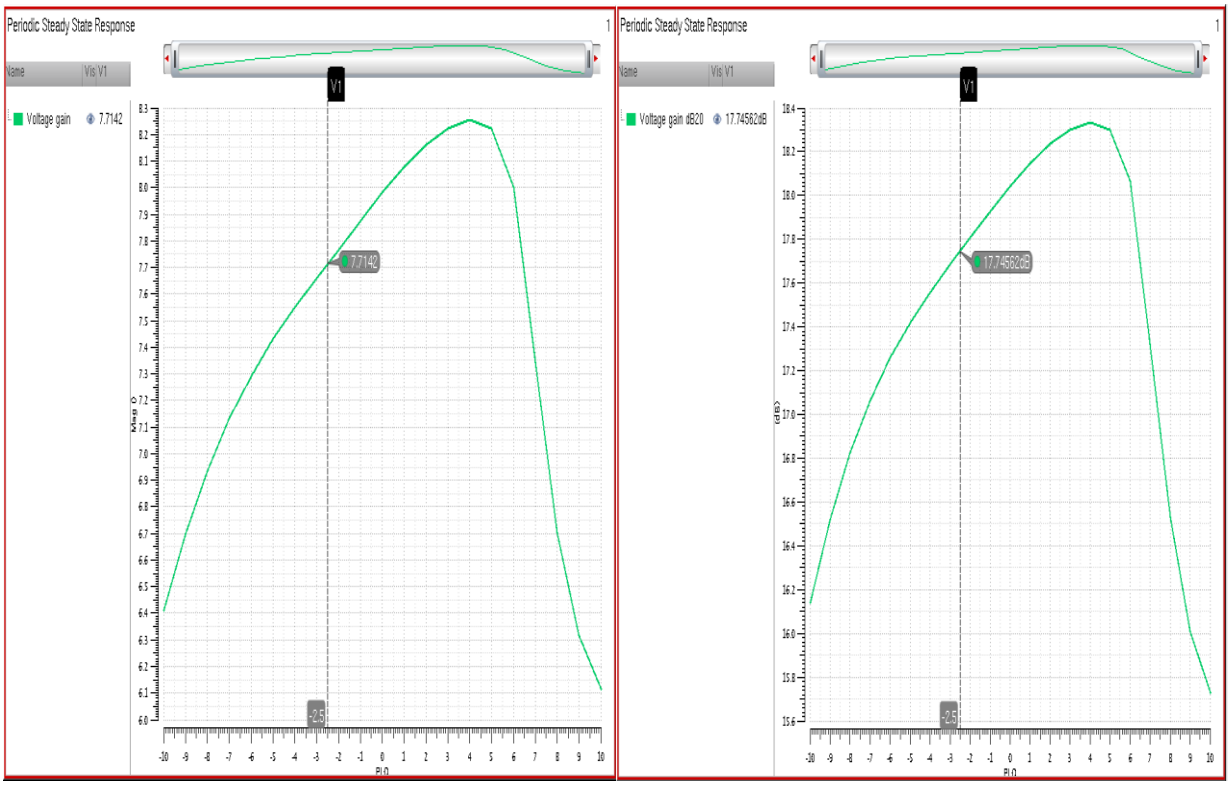
We can find that using the same equation,

$$A_{sys} = A_{LNA} * A_{mix}$$

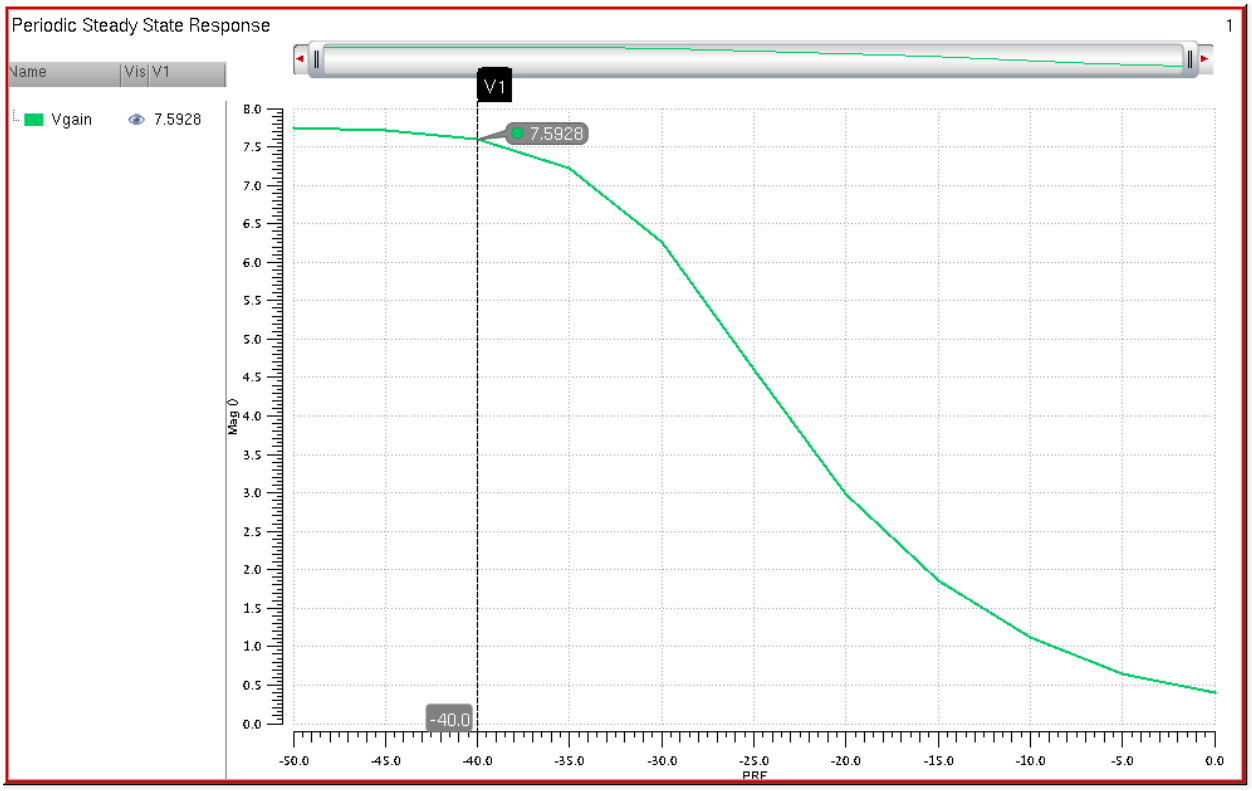
$$A_{sys} = 8.07 * 0.7935 = 6.403\, V/V = 16.13 \text{ dB}$$

From simulation I got voltage gain as 7.71 V/V or 17.74 dB at -2.5dBm PLO, which is above expected value.

Here I have simulated gain vs PLO (-10 to 10 dBm) graph for magnitude and dB value of gain,



Next is the graph of PRF (-50 to 0 dBm) vs voltage gain of system,



Linearity of the system:

I have use equation for one tone 1 dB compression point and IIP3 form text book 3.21 and 3.23,

$$\frac{1}{{V_{IIP3}}^2} = \frac{1}{{V_{IIP3LNA}}^2} + \frac{{A_{LNA}}^2}{{V_{IIP3mix}}^2}$$

$$V_{IIP3} = \sqrt{\frac{{V_{IIP3mix}}^2 * {V_{IIP3LNA}}^2}{{V_{IIP3LNA}}^2 * {A_{LNA}}^2 + {V_{IIP3mix}}^2}}$$

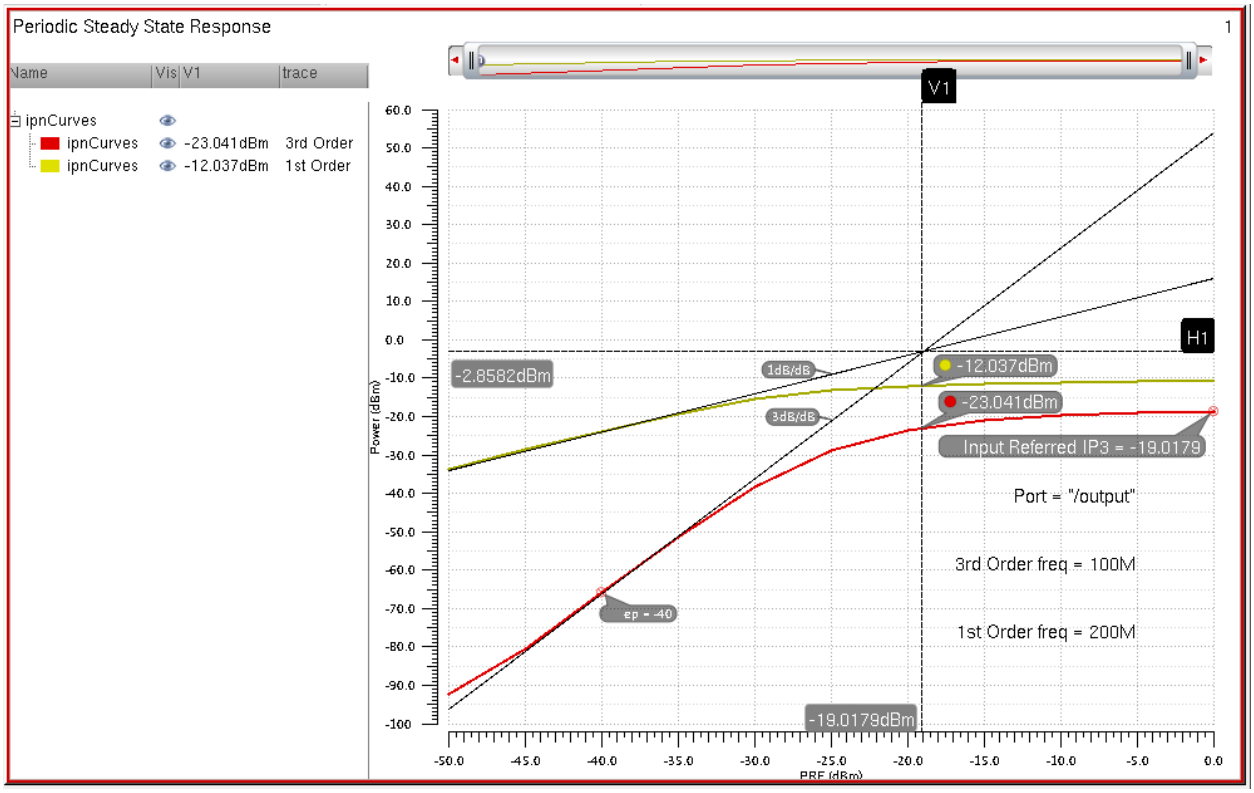
$$= \sqrt{\frac{(202.72)^2 * (130.01)^2}{(130.01)^2 * (8.07)^2 + (202.72)^2}} * 10^{-3}$$

$$= 24.664 * 10^{-3}\ V$$

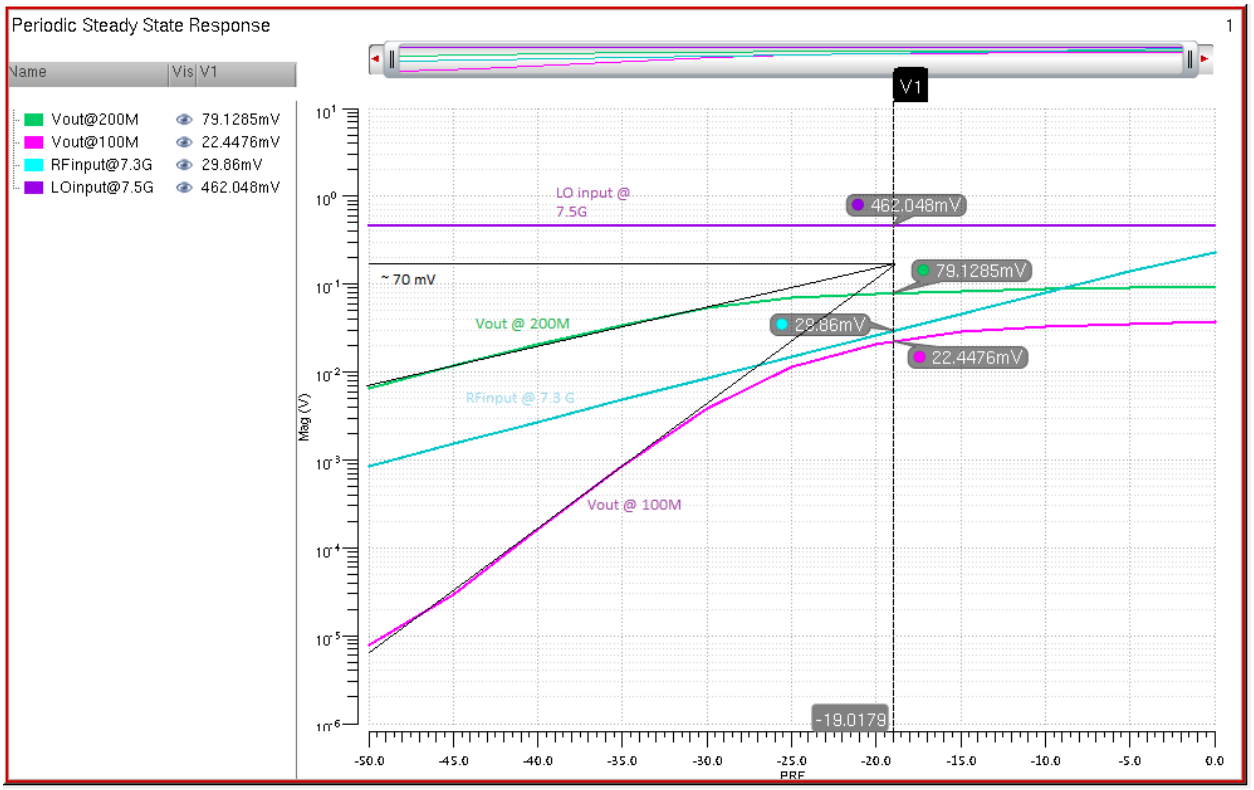
$$= 20 \log 0.02466\ + 10 = -22.16\ dBm$$

From the simulation IIP3 is **-19.0179** dBm or 35.4 mV.

Following is the graph of PRF (-50 to 0 dBm) vs power,



Following is the graph of PRF (-50 to 0 dBm) vs differential voltage at output for 100MHz and 200MHz,



1 tone 1 dB compression point,

$$\frac{1}{{V_{1dB}}^2} = \frac{1}{{V_{1dBLNA}}^2} + \frac{{A_{LNA}}^2}{{V_{1dBmix}}^2}$$

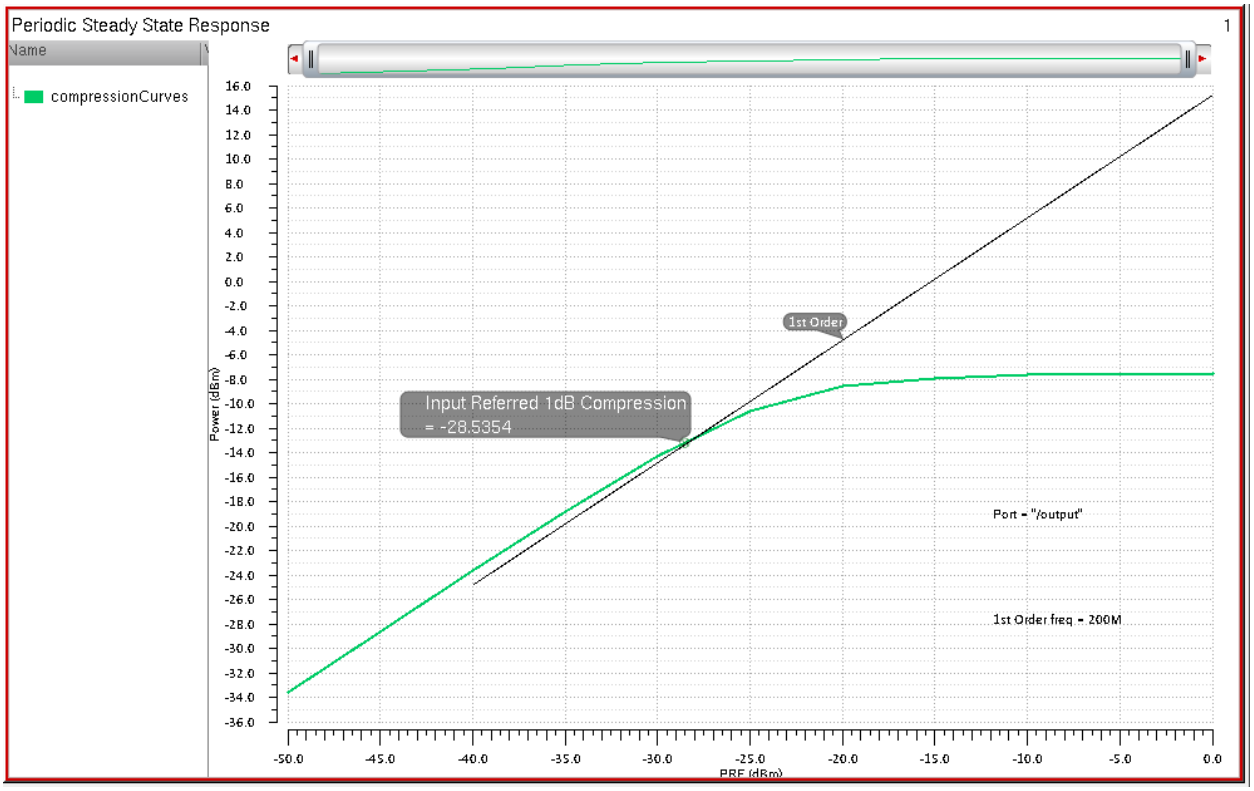
$$V_{1dB} = \sqrt{\frac{{V_{1dBmix}}^2 * {V_{1dBLNA}}^2}{{V_{1dBLNA}}^2 * {A_{LNA}}^2 + {V_{1dBmix}}^2}}$$

$$= \sqrt{\frac{(55.35)^2 * (40.8)^2}{(40.8)^2 * (8.07)^2 + (55.35)^2}} * 10^{-3}$$

$$= 6.76 * 10^{-3} V$$

$$= 20log0.00676 + 10 = -33.39\ dBm$$

From simulation 1 tone 1 dB compression is **-28.5354** dBm which meets the given spec.



Noise figure

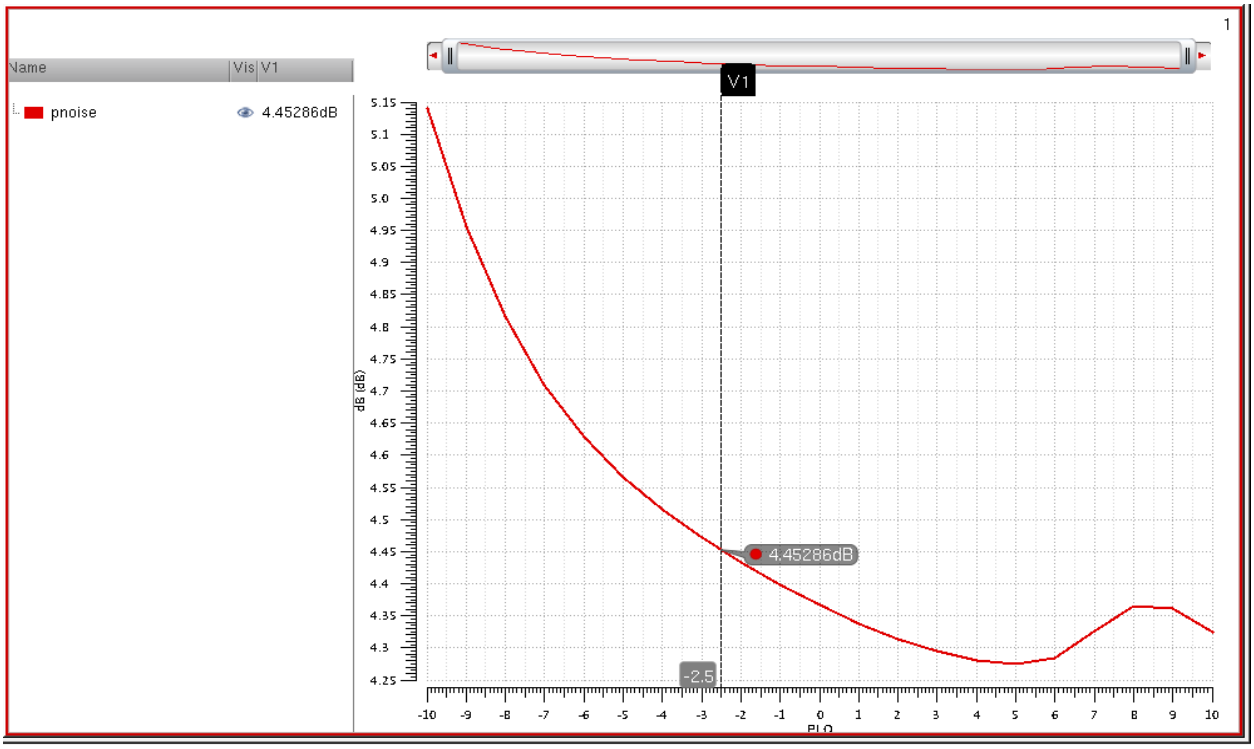
$$F_{sys} = F_{LNA} + \frac{(F_{mix} - 1)}{{A_{OL}}^2} \frac{4 * {R_{OL}}^2}{{R_S}^2}$$

$$= 1.61 + \frac{(6.89 - 1)}{8.63^2} \frac{4 * 20.83^2}{50^2}$$

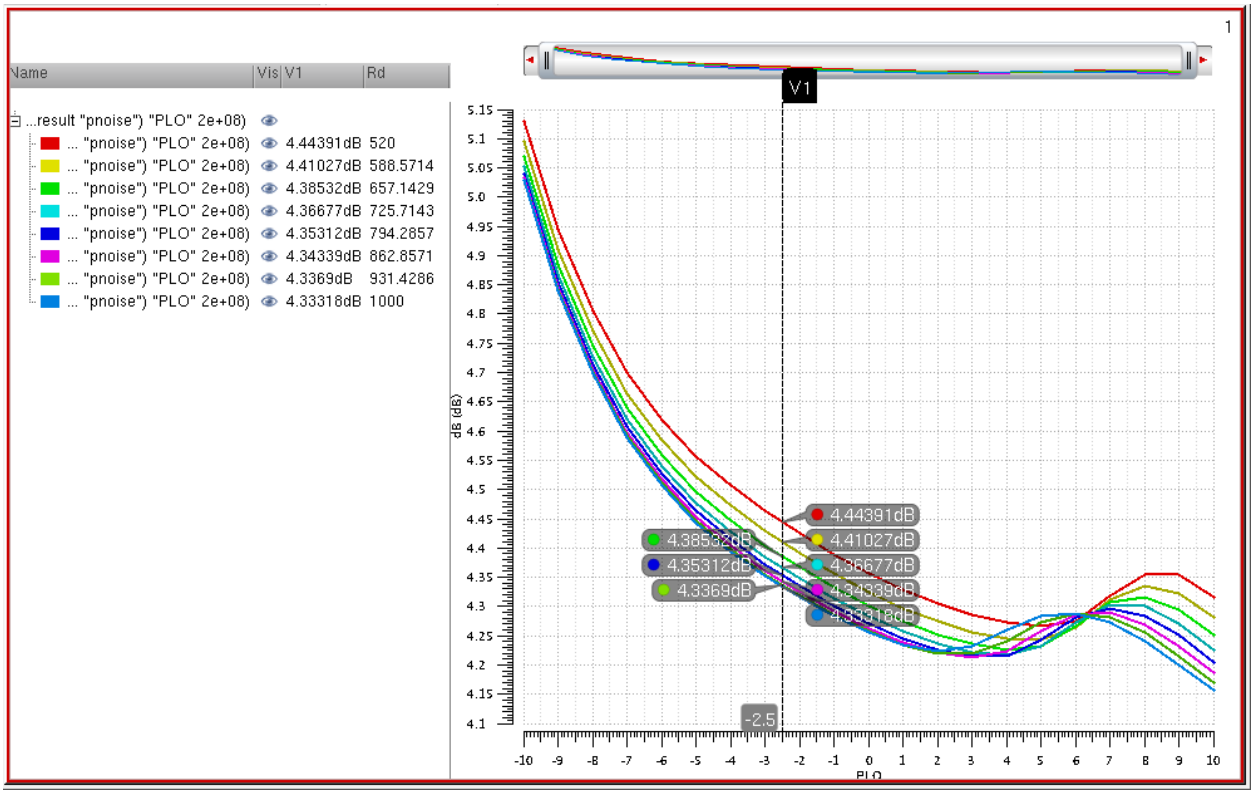
$$= 1.67$$

$$NF = 10 \log 1.67 = \mathbf{2.22}\ dB$$

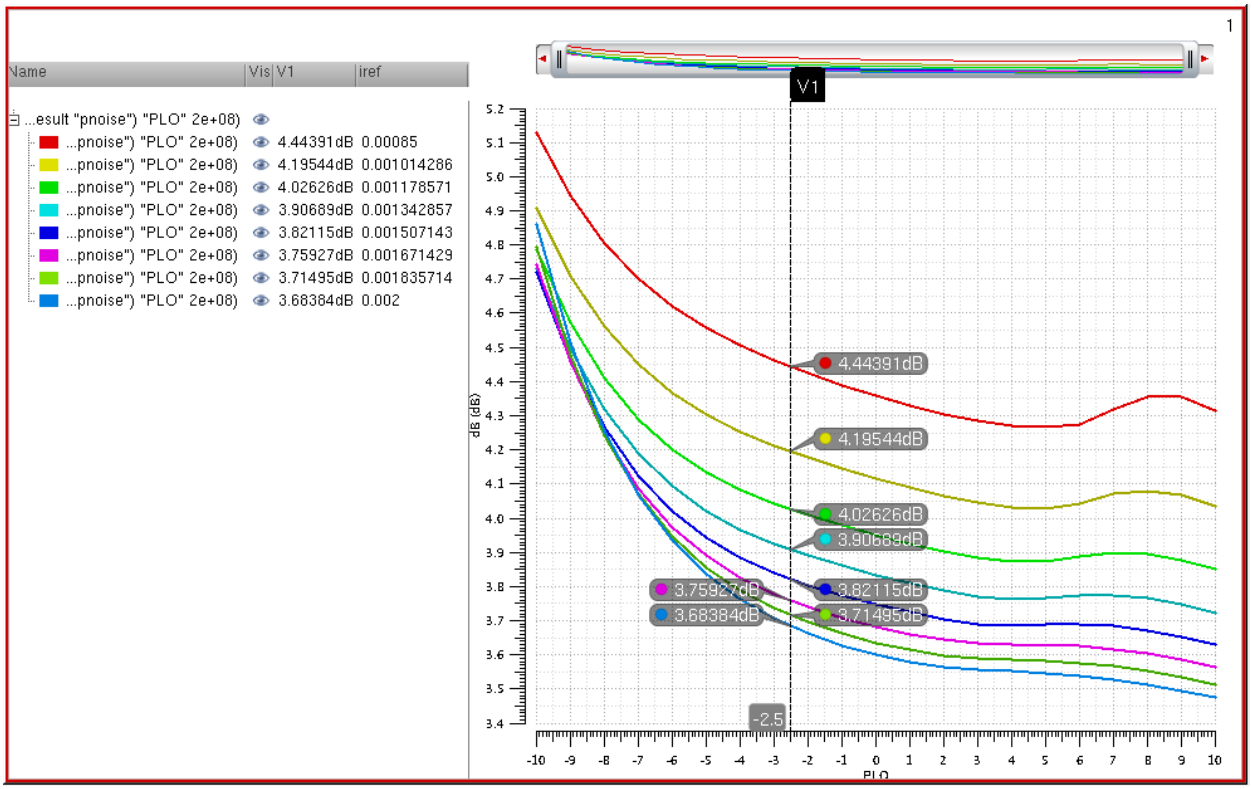
From the simulation I am getting much higher noise figure than calculation. I am going to reduce the noise figure by increasing bias current through the circuit or by increasing Rd.



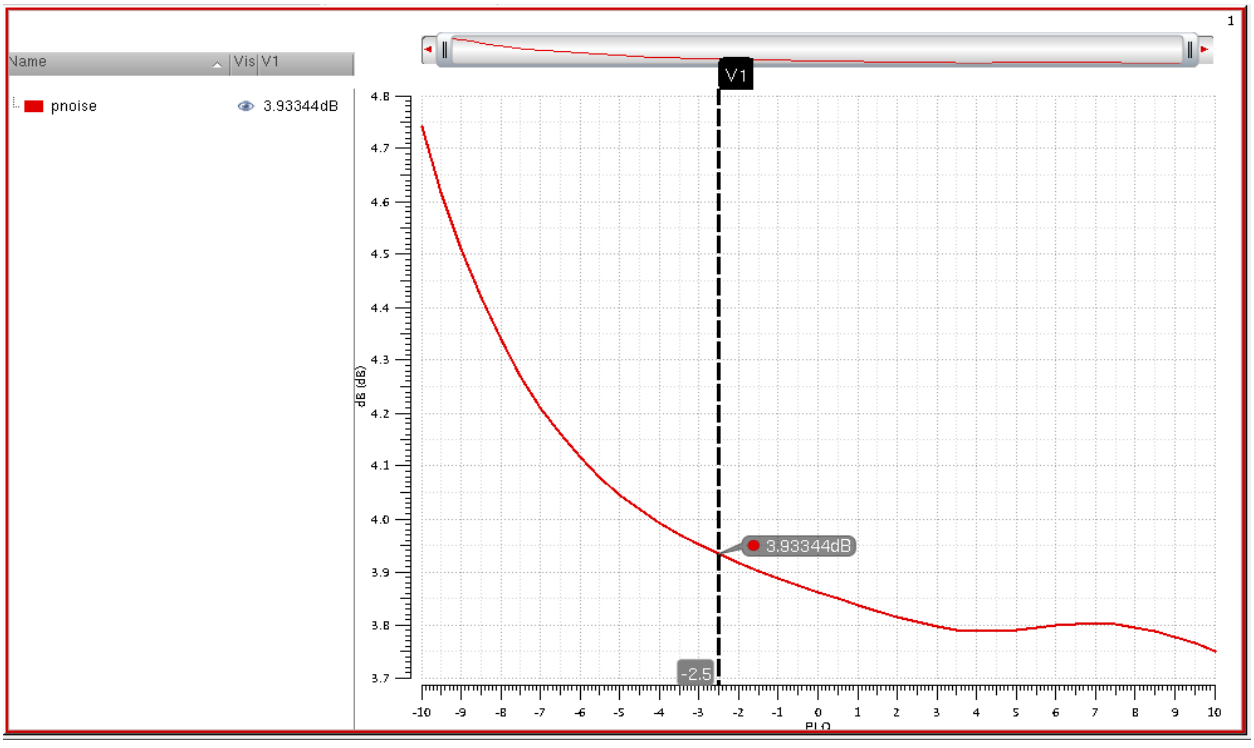
Graph after doing parametric analysis for Rd (520 to 1000 Ω),



Same way I have use parametric simulation for bias current (850µA to 2mA) which had significant effect on noise figure.



I have kept Rd same 520Ω and increase current to 1.3mA to meet noise specs,



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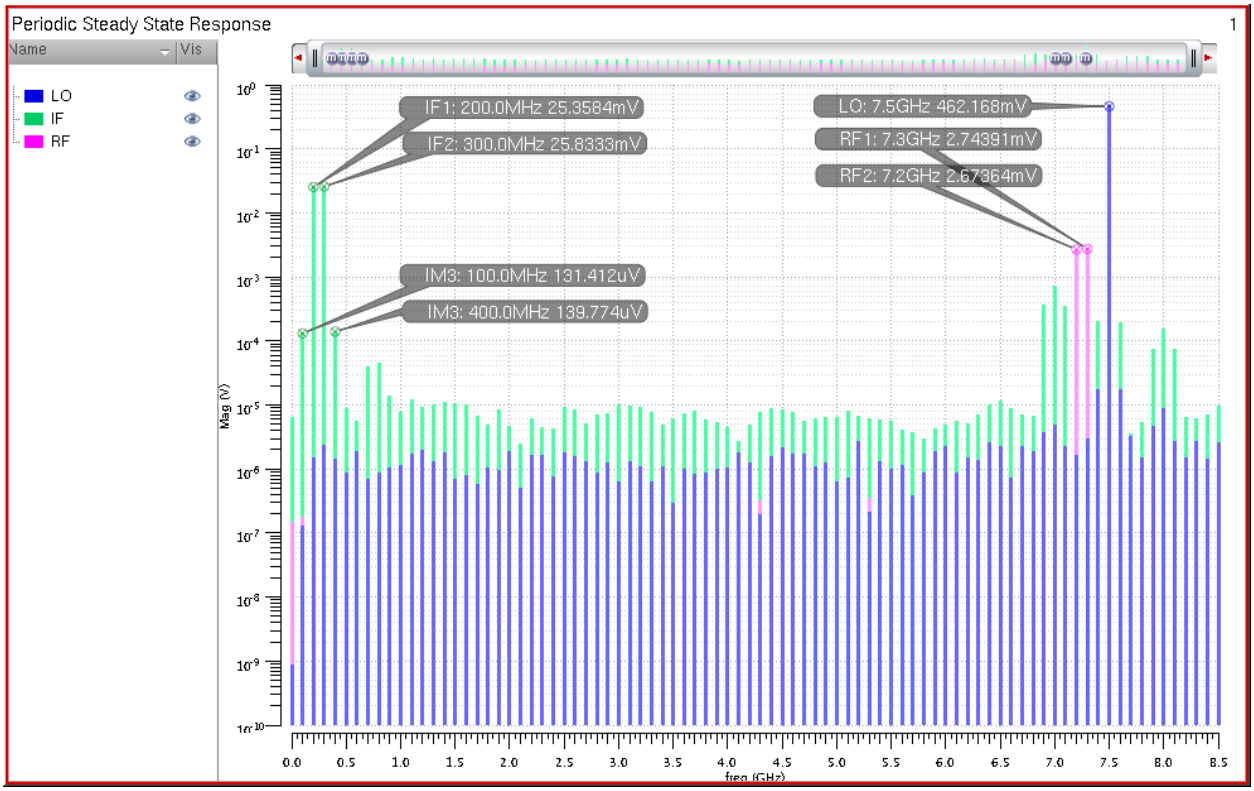

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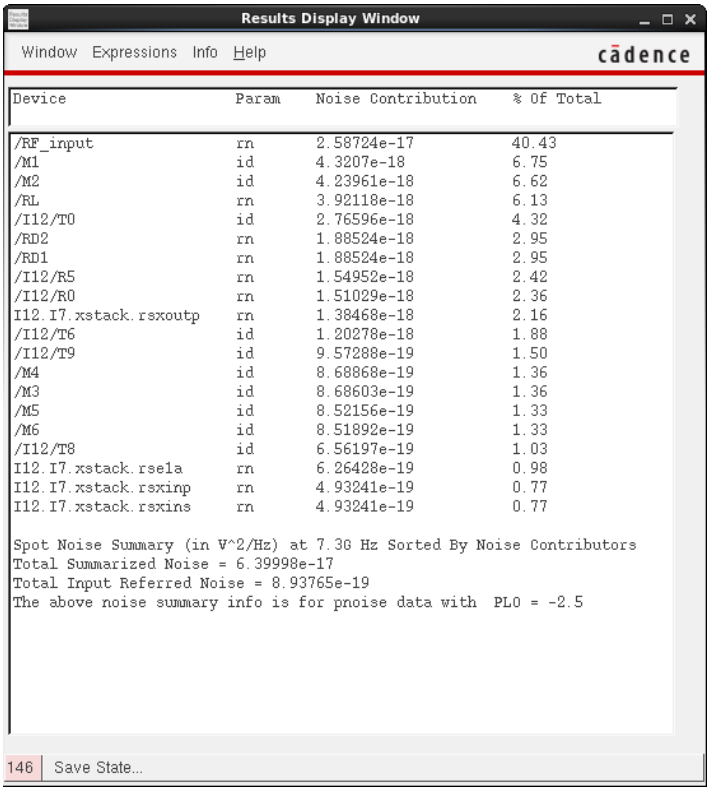
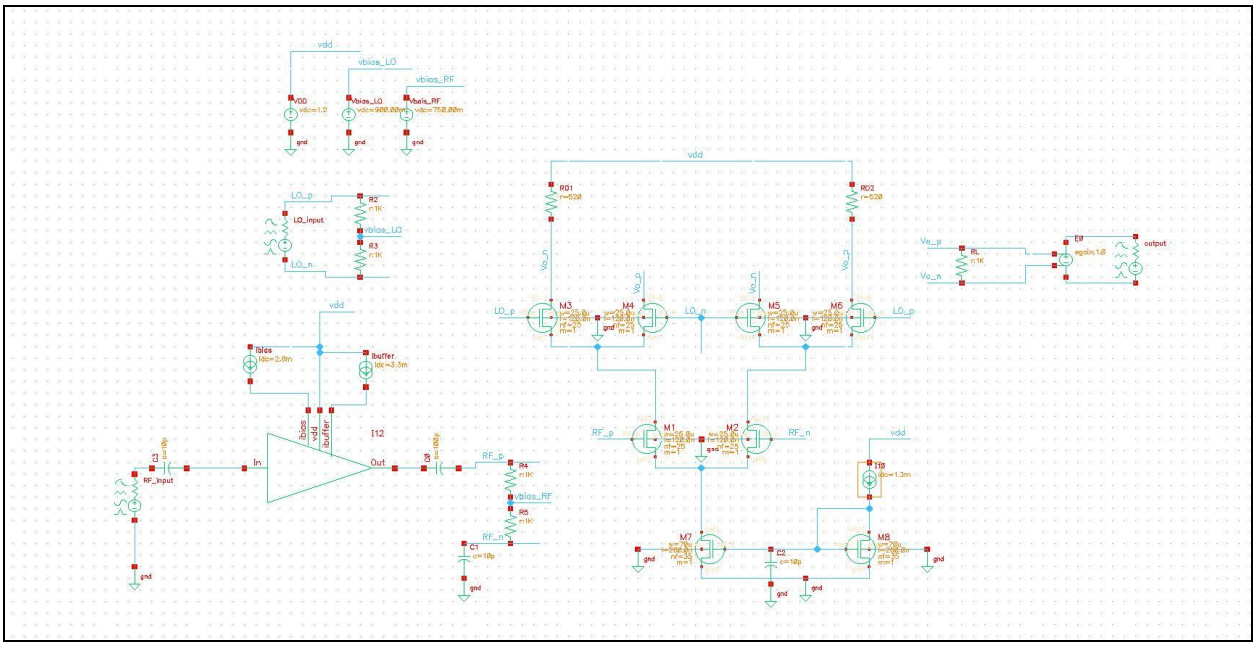
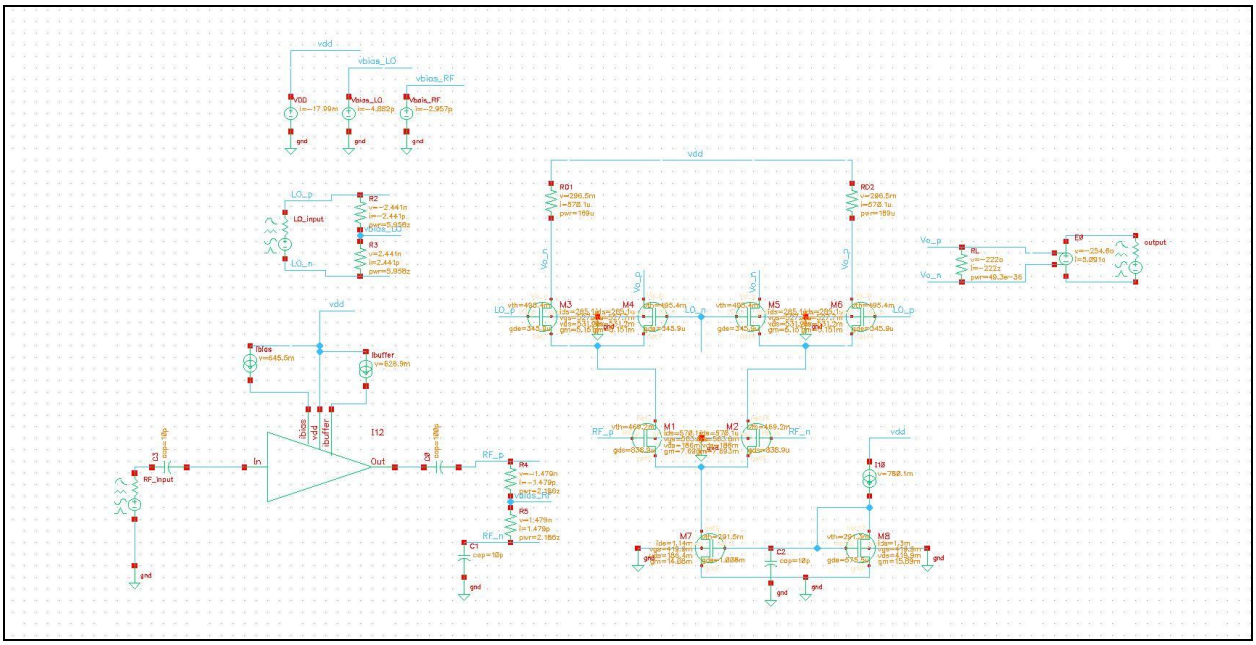


Below is the figure of system circuit with all the component parameter,



Below is the figure of system circuit with all the DC operating points,



Design trade-offs

LO amplitude:

Amplitude of LO signal is related with size and current density of the transistor. Hence, if we want to reduce LO amplitude then we have to use typically large transistor with low current density. But by doing so we will reduce f_T of the transistor. Operating at high frequency it is very important to have high f_T. Thus, in such case there is no choice but to increase amplitude of LO.

Voltage Gain:

It directly depends upon R_D and g_m. Where g_m depends upon transistor size and bias current. Hence, to increase gain we can either increase Rd or current or transistor size.

Noise:

Noise figure is largely determined by choice of topology. Next most important factor is the size of input transistor. Higher gm in the input transistor will generally improve noise but higher current is required to maintain linearity.

Linearity:

Linearity in CMOS depends upon transistor size and current.

Conclusion

Here in this assignment, we have designed system of LNA and Mixer with all desired specs met. We have first designed mixer with specs derived from system specs and then connect it with LNA that we have designed in previous assignment.

Reference

Radio Frequency Integrated Circuit Design 2nd edition by Calvin Plett and John Rogers & Class notes.