RFIC

Assignment 4

Power Amplifier

Submitted by

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Design criteria	Targeted specs	Achieved Specs	Specs From Calculation
Operating frequency	7.3G	7.3G	-
Output power	> 17dBm	17.2dBm	17.1dBm
PAE (%)	As high as possible	21.7 %	22.6 %
Conduction angle	-	274.4^0	237.5^0
Efficiency	-	40.82 %	52.50 %

Choice of Topology

Using IBM 130nm technology I have designed a power amplifier with cascade transistor. Here a nfet33_rf transistor are used to operate at higher voltage (0-3.6V).

Transistor characterization

Here I am doing characterization of small 200/0.4 um transistor. And according to calculation I will derive current required to get a particular output power at given Vop.

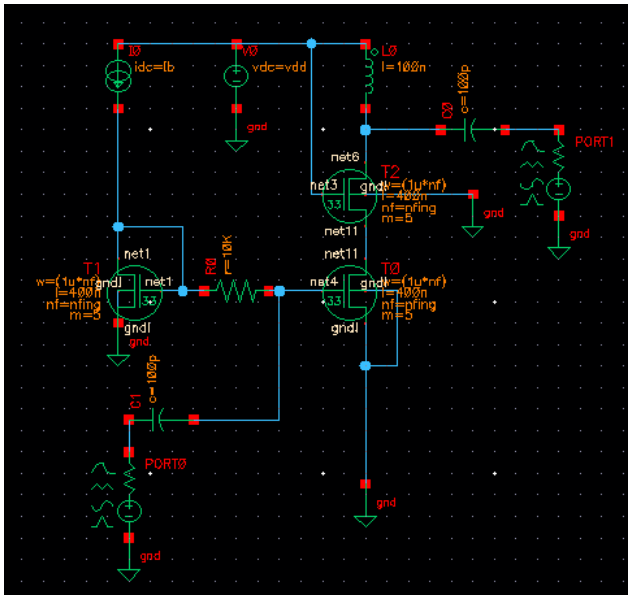

Figure 1 Circuit for transistor characterization

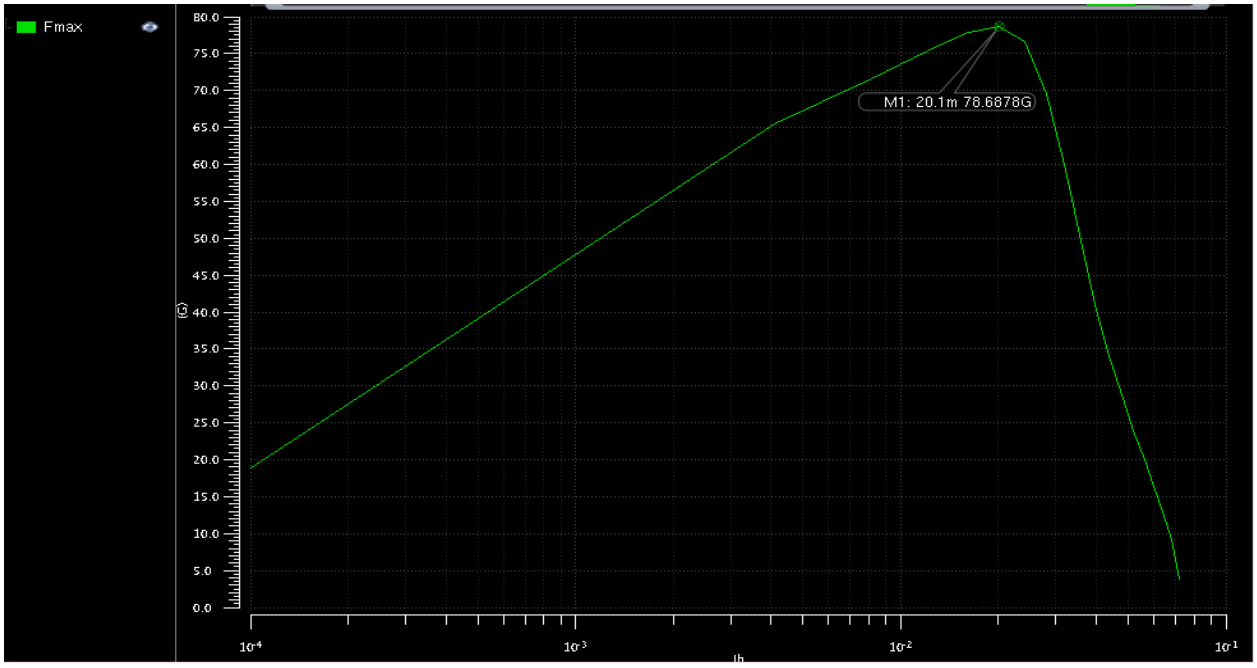

Figure 2 Fmax vs Ib at vdd=1.8 V for 200u transistor

Here I have shown Vop = 1.42V and nominal current for class A and AB for 200/0.4um transistor,

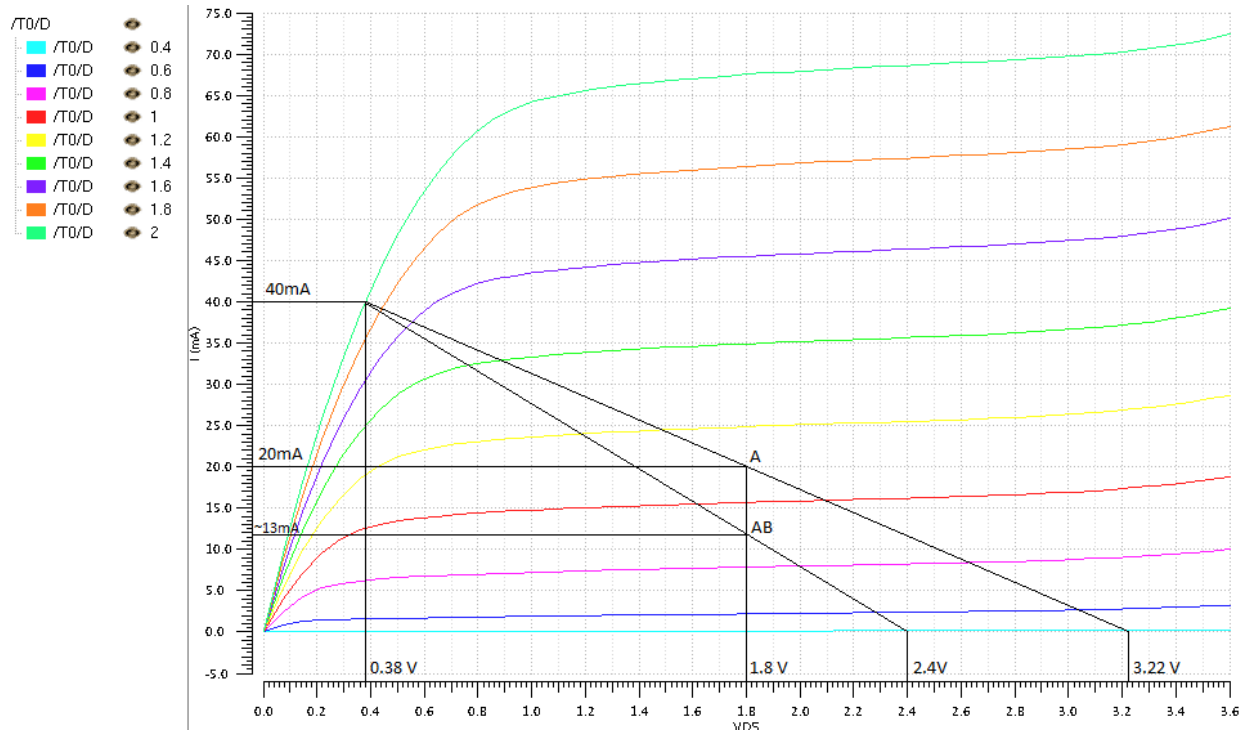

Figure 3 VDS vs Drain current graph for different Vgs

Let's calculate required current from swing above and power requirement given in the specs,

$$I_{CQ} = \frac{2*P_o}{V_{op}} = \frac{2x50mW}{1.42} = 70.42mA$$

Hence from figure 3 we can say that transistor should be scaled by a factor of,

$$k = \frac{70.42}{20} \approx 3.5$$

Thus, new transistor size will be 200um*3.5 = 700um. Here I am keeping the size of the transistor a little higher then calculated. 730/0.4um.

Now for this transistor class AB current will be 13*3.5 = 45mA.

Here I am using a current mirror with ratio of 1:9. Because keeping both transistor size same and keeping the bias current exactly what we want, we will increase total current of the circuit. Hence Pdc increase, which will decrease PAE significantly.

Now lets do the calculation of conduction angle and efficiency,

We have already done this steps in our final examination,

Peak current from class A $I_{c,peak} = I_{CC}(\theta) = 40 * 3.5 = 140mA$

Nominal current for class AB $I_{CQ} = I_{CC}\cos cos\,\theta\ = -\ 45.5mA$

Therefore,

$$I_{c,peak} = I_{CC} - I_{CC}\cos cos\,\theta \quad \cos cos\,\theta\ = \frac{I_{CQ}}{I_{CC}}\theta = \left(\frac{I_{CQ}}{I_{CC}}\right) = \left(\frac{-45.5}{94.5}\right) = 118.78^{0}$$

Conduction angle is $2\theta = 237.56^{0}$

Calculating efficiency,

$$\eta = \frac{V_{op}}{V_{DD}}\frac{(2\theta - \sin sin\,2\theta)}{4(\sin sin\,\theta - \theta\cos cos\,\theta)} \quad = 50.5\%$$

Inductor characterization

Lout = 1.06nH		**Ltank = 550pH**	
Outer dimension	300μ	Outer dimension	300 μ
Metal width	10.4 μ	Metal width	20.8 μ
No.turns	1.25	No.turns	1
Lg = 680pH		**Ls = 100pH**	
Outer dimension	300 μ	Outer dimension	100 μ
Metal width	11.12 μ	Metal width	15 μ
No.turns	1	No.turns	1

Lout=1.06nH

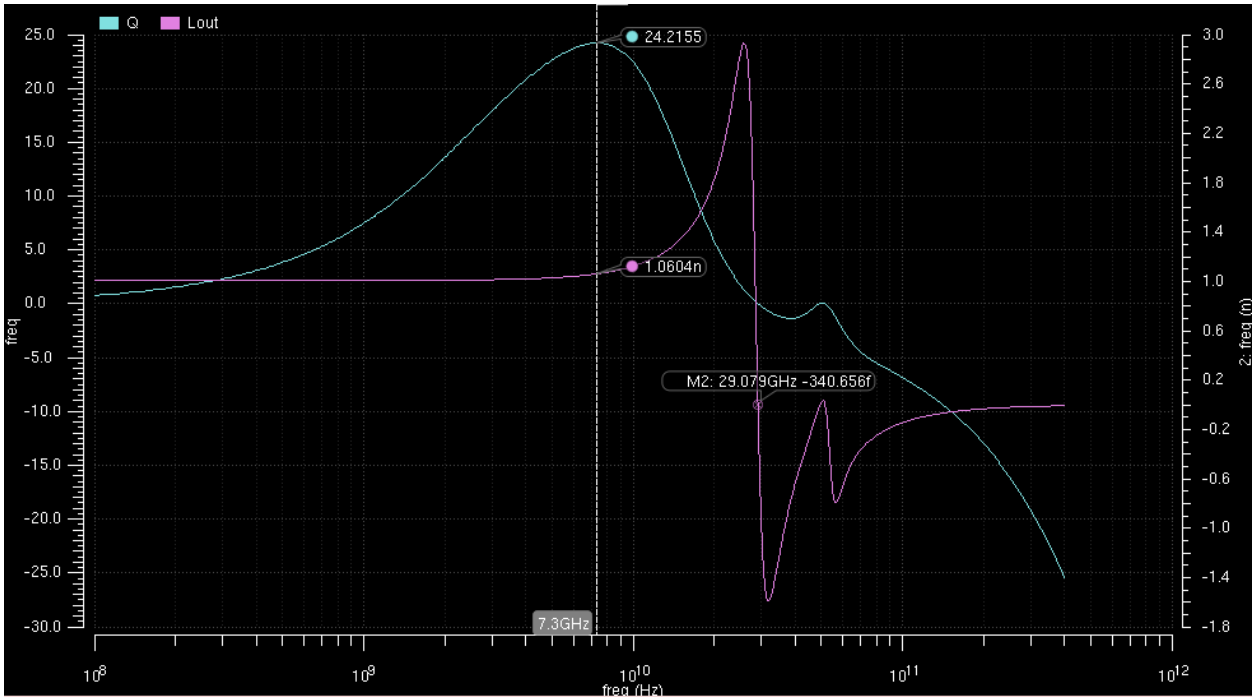

Figure 4 Lout=1.06nH

Ltank=550pH

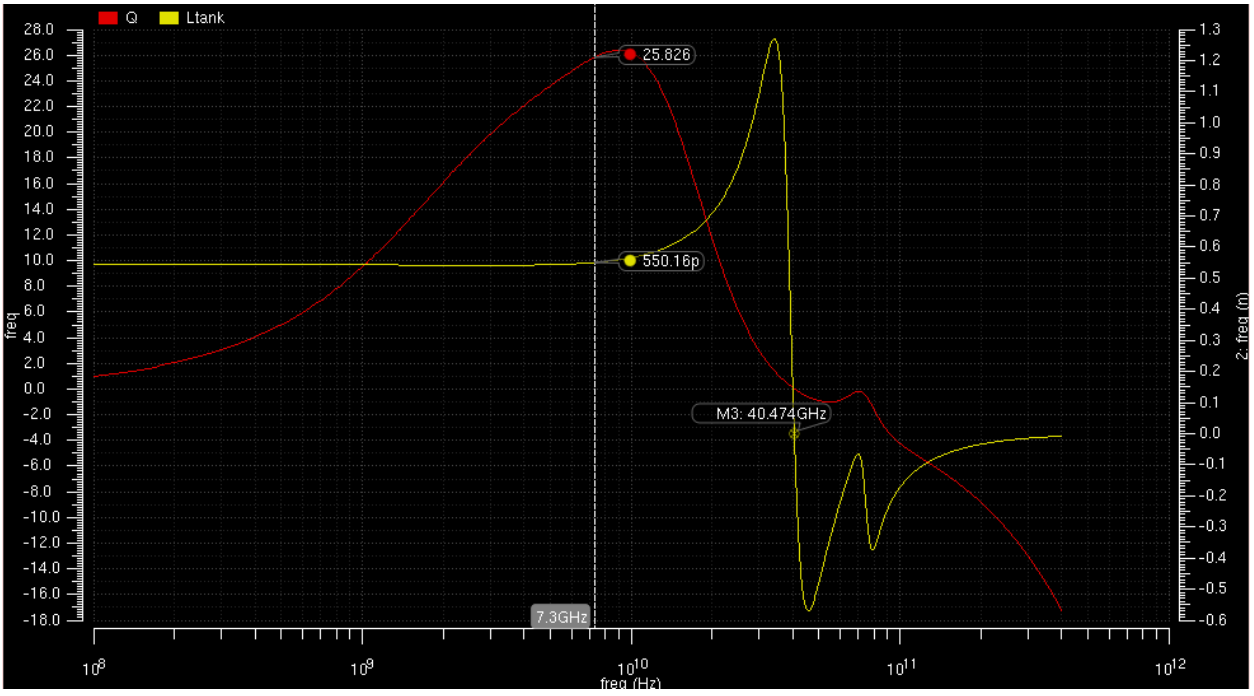

Figure 5 Ltank=550pH

Lg = 680pH

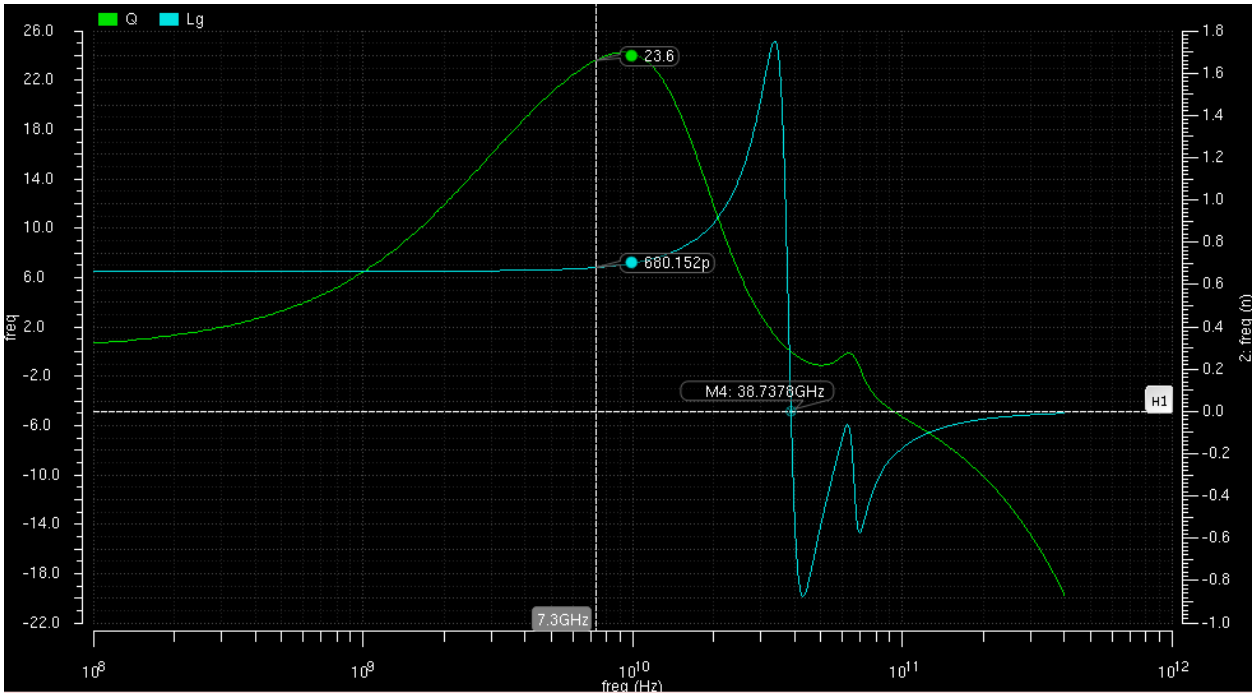

Figure 6 Lg=680pH

Ls = 100pH

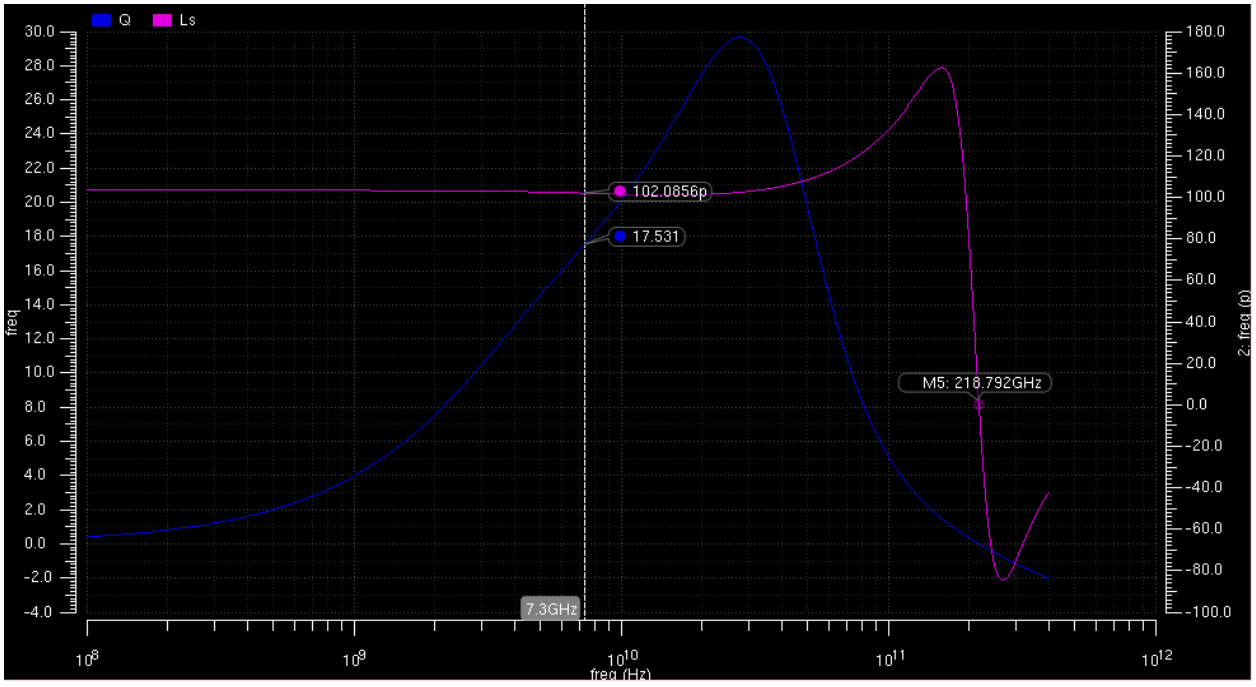

Figure 7 Ls=100pH

Small signal analysis

First of all I have done matching for input and output using below values of capacitor and inductor.

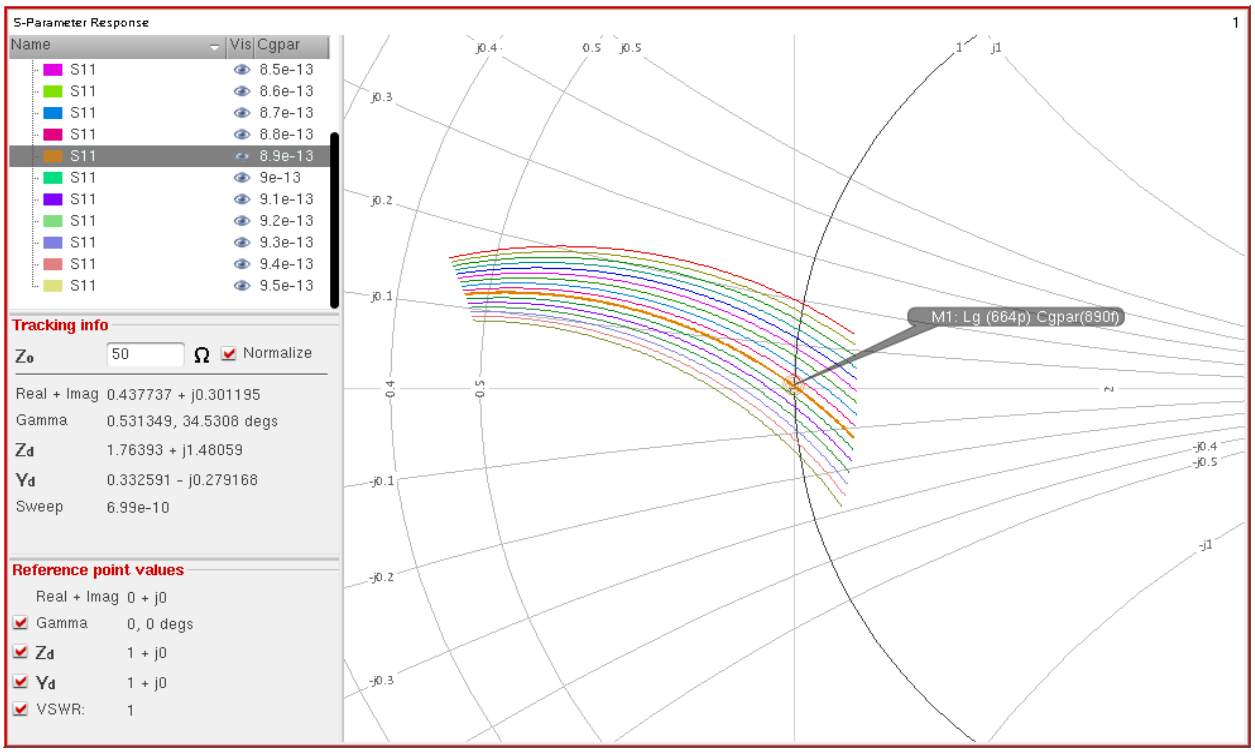

Figure 8 S11 Lg(500p – 700p) and Cgpar(850f – 950f)

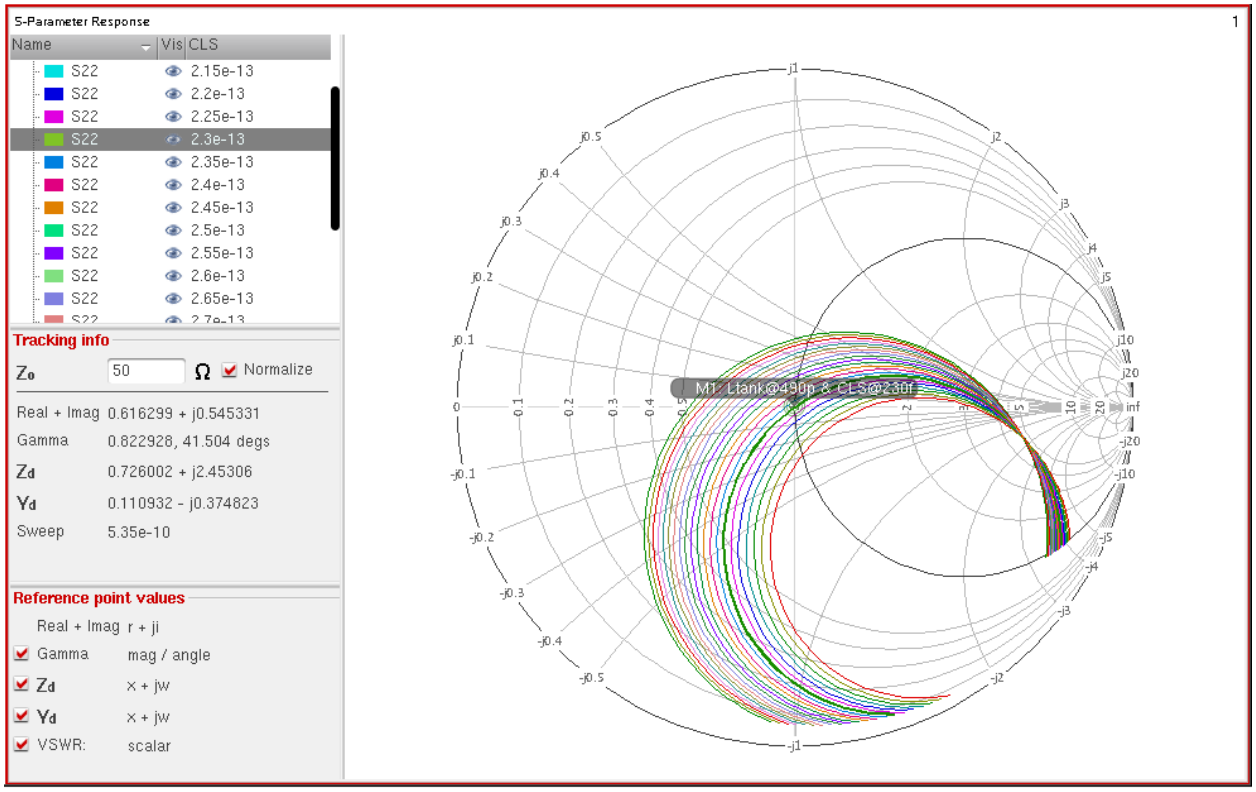

Figure 9 Ltank (300p – 800p) CLS (200f – 300f)

After this I have measured several small signal graphs.

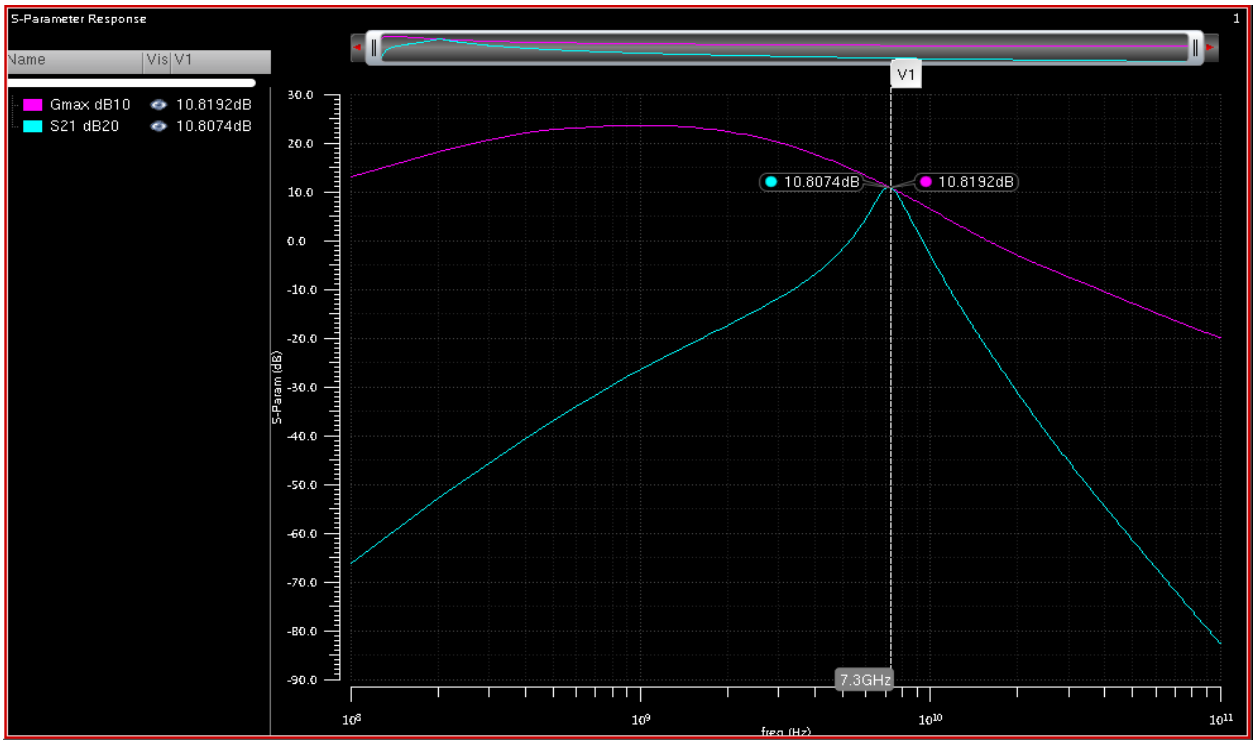

Figure 10 Gmax and S21 at 7.3G

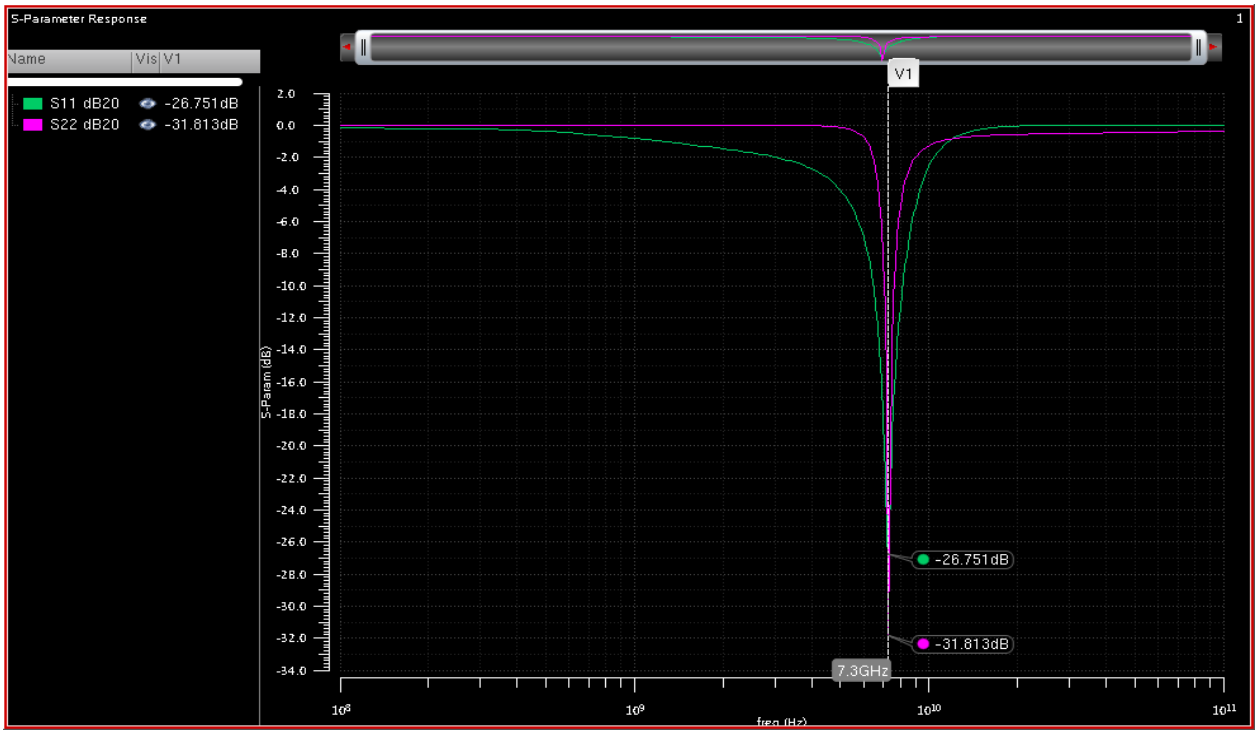

Figure 11 Input output matched

Stability of small signal analysis

Here I have tried to keep the circuit stable. In order to do that I had to include small resistor of 100 mohm in series at output.

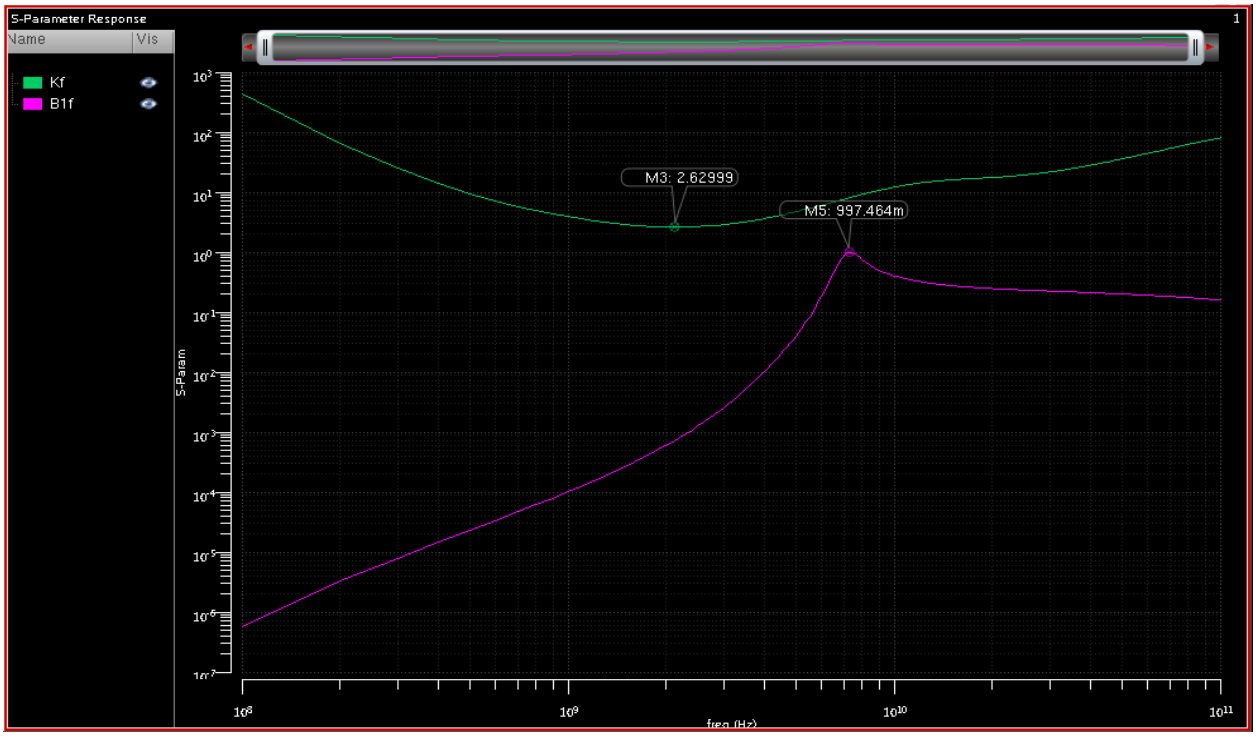

Figure 12 Stability

PAE(%) Po Pin(dBm) Gain(dB)

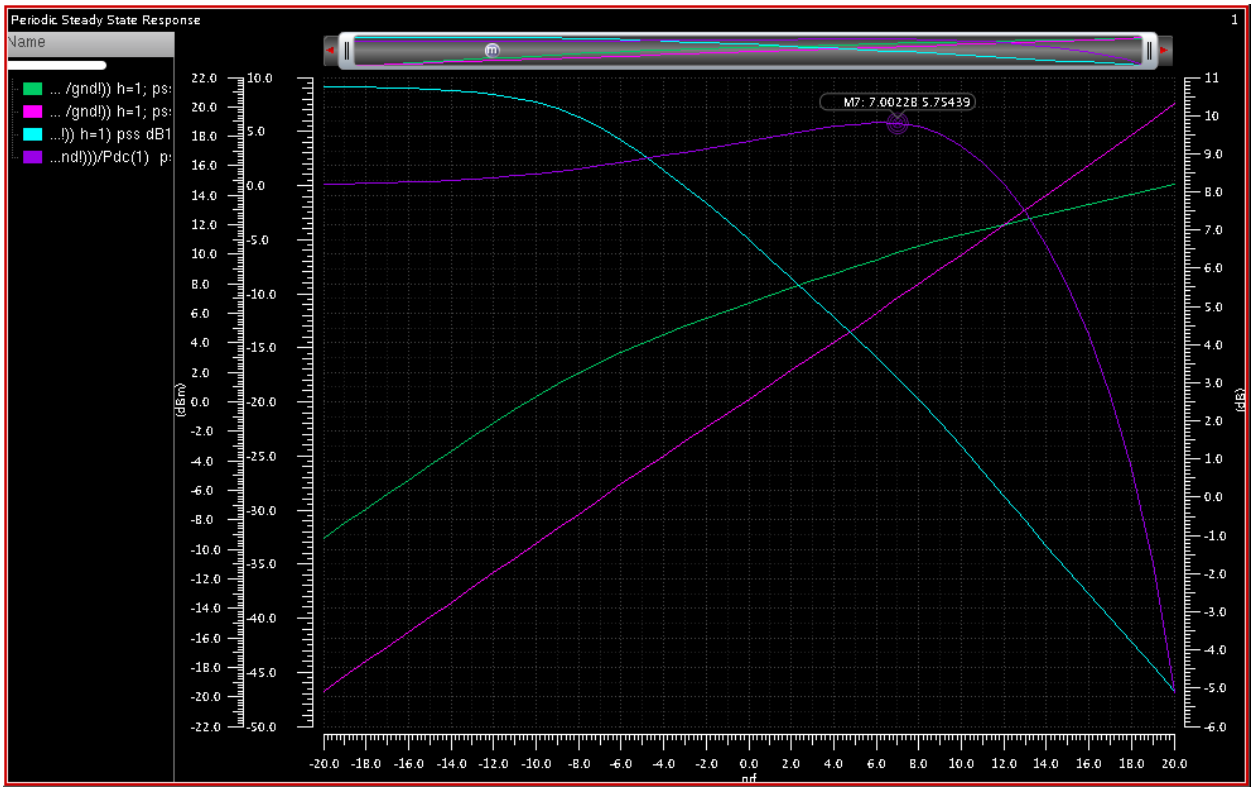

Figure 13 for small signal PAE Po Pin Gain

Large signal analysis

After matching input and output side now I have done large signal analysis. Here, at first I was experimenting with value of Ls. After some simulation I found that Ls should be as low as possible. Lowest inductor achieved by library inductors is 102pH. Hence during ideal inductor I have kept it 100pH. I have increased the value of prf to 15dBm here.

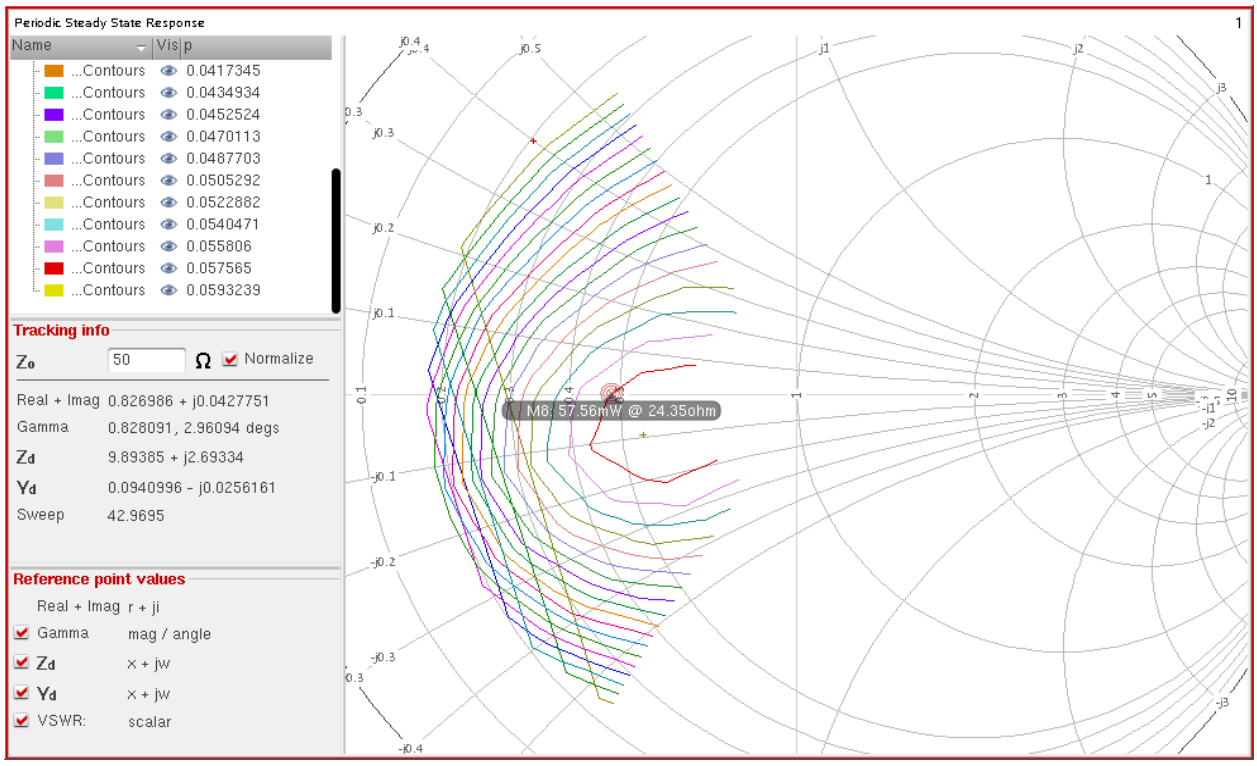

Figure 14 Load pulls

From this Load pull graph I have calculated Ropt for required power to be 24.35 ohm.

Now, matching 24.35ohm to 50ohm I am getting value of CLS and Lout as below,

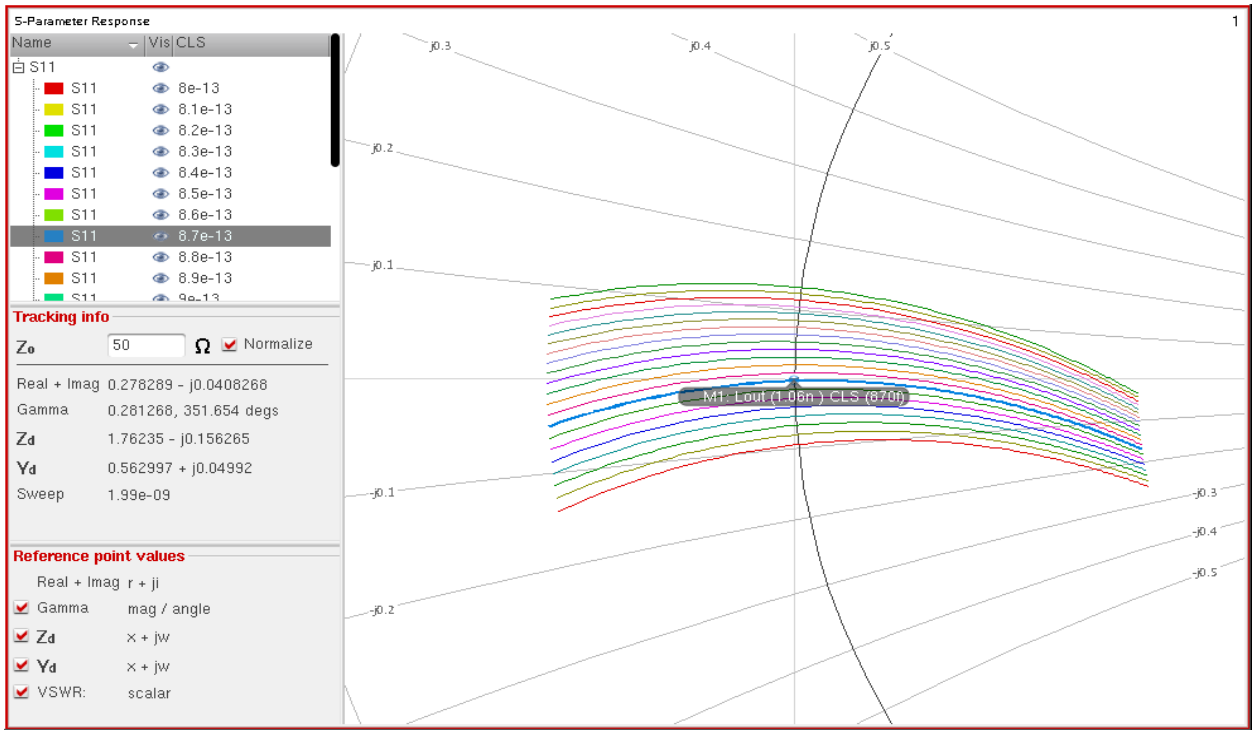

Figure 15 Lout(800p – 2n) and CLS (800f – 1p)

Results

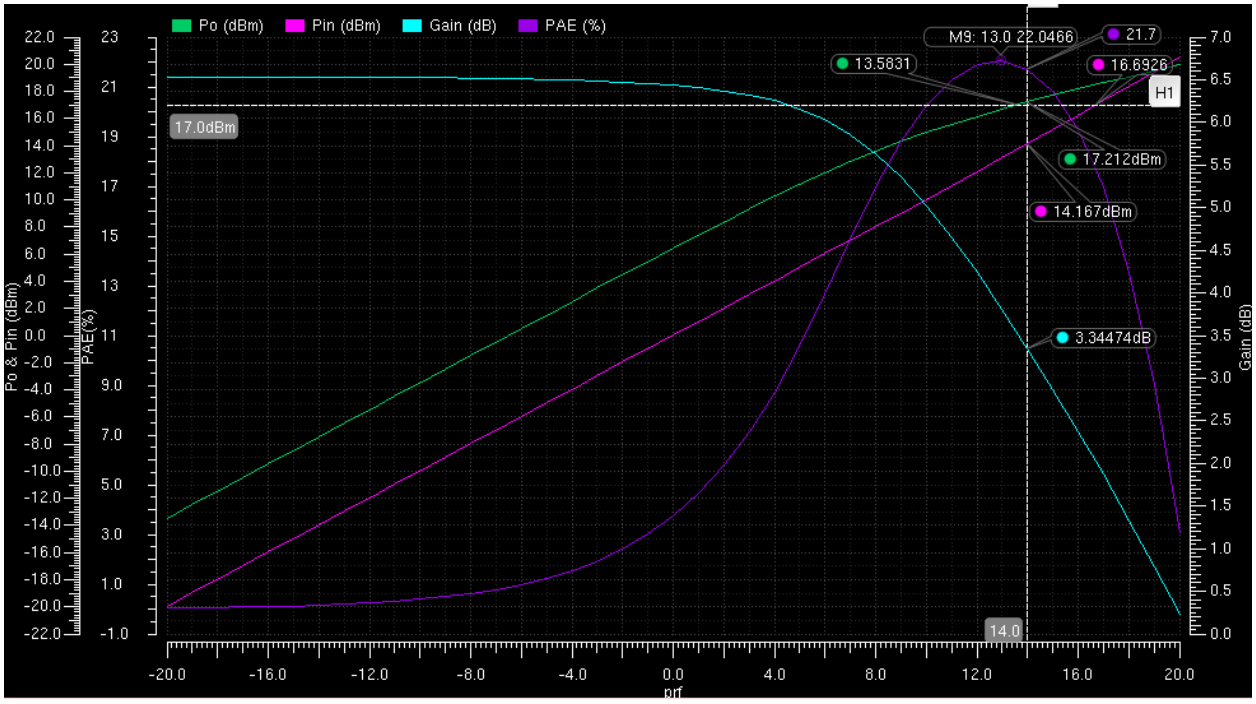

Figure 16 PAE Po Pin Gain vs prf

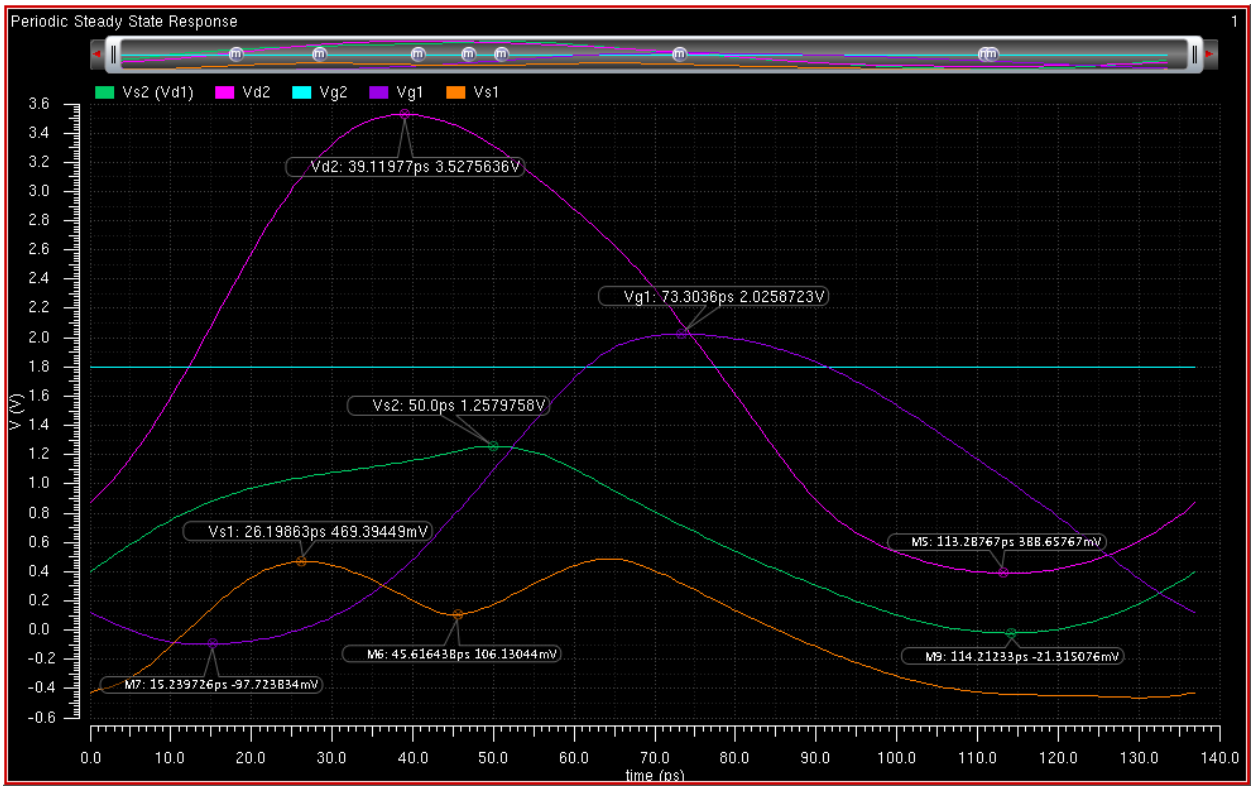

Figure 17 voltage swing vs time

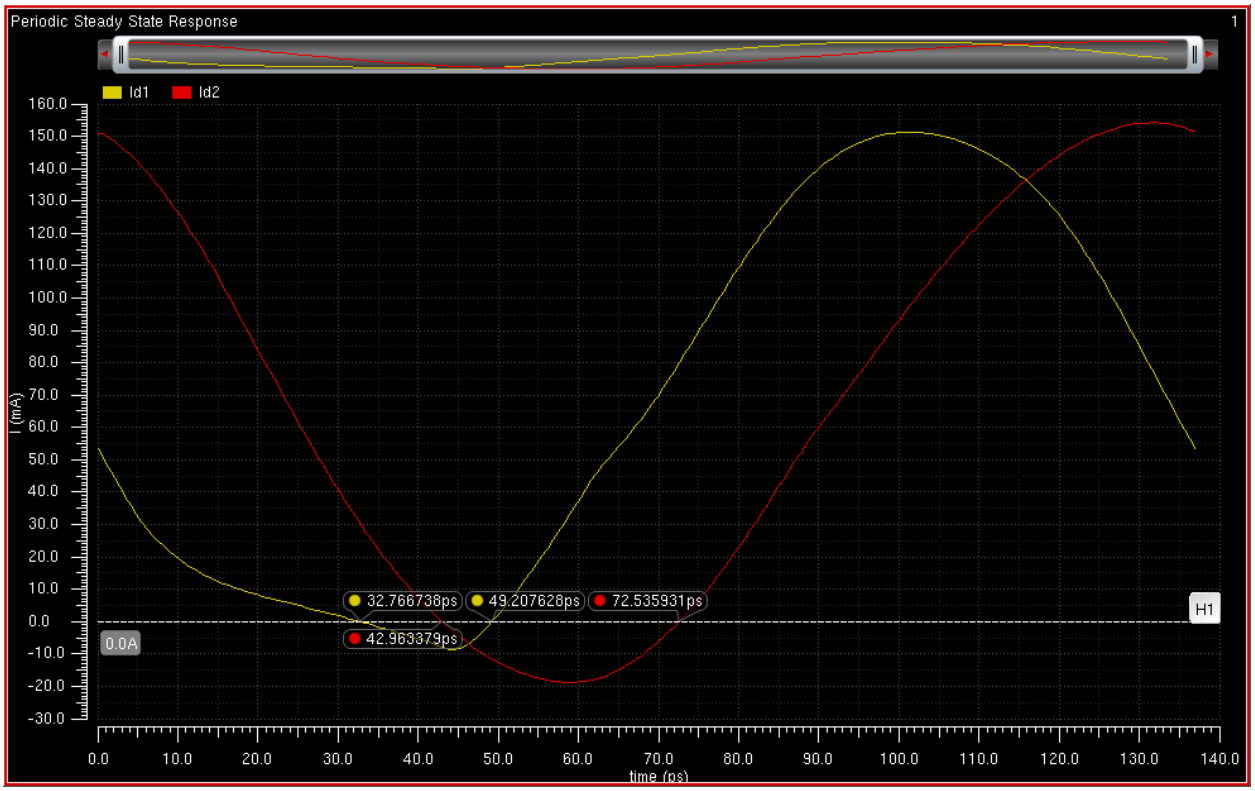

Figure 18 current swing vs time

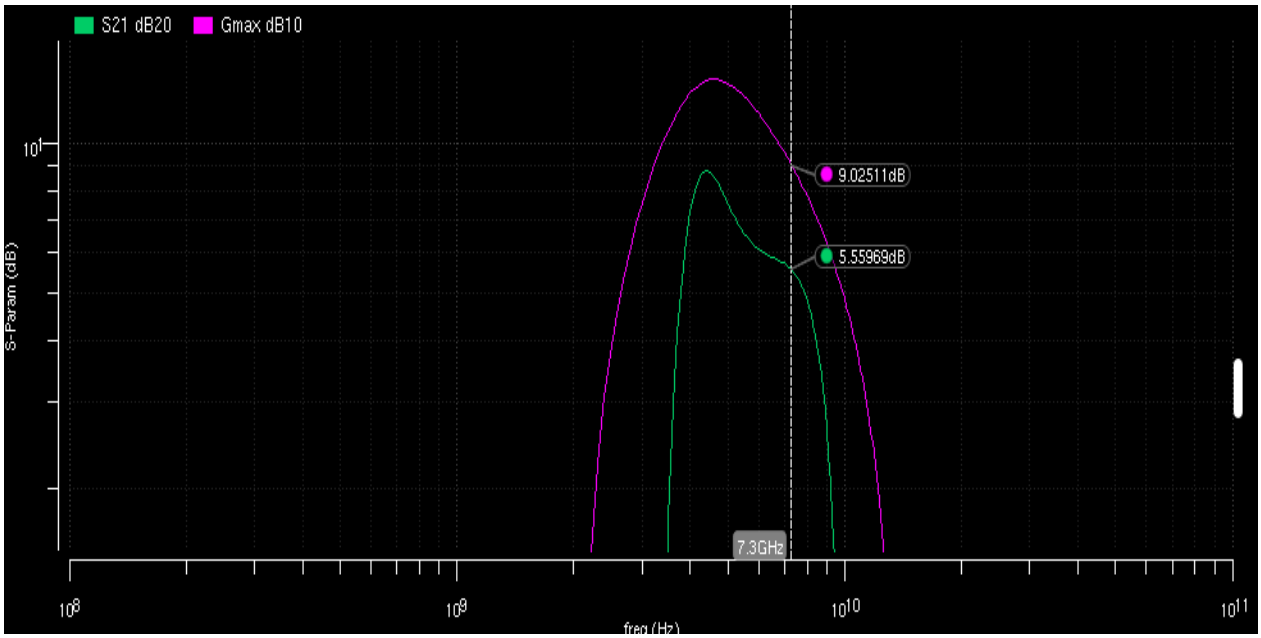

Figure 19 Gmax and S21 at 7.3G

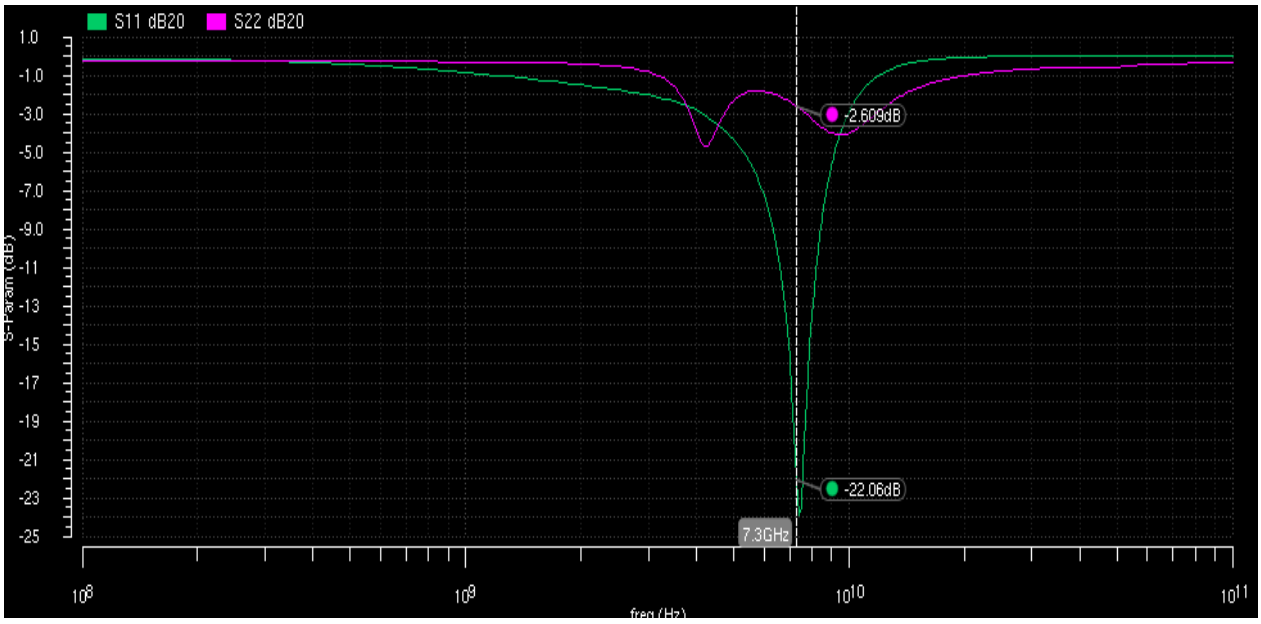

Figure 20 Input and output reflaction coefficient

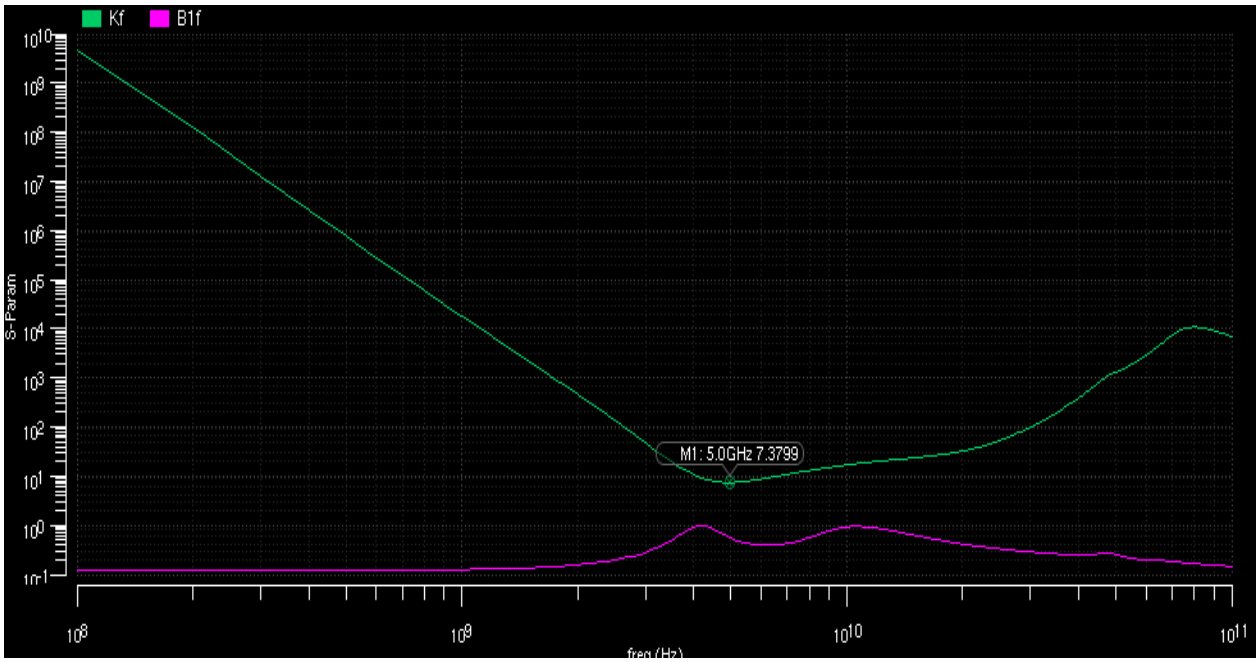

Figure 21 Stability (with real inductors improving)

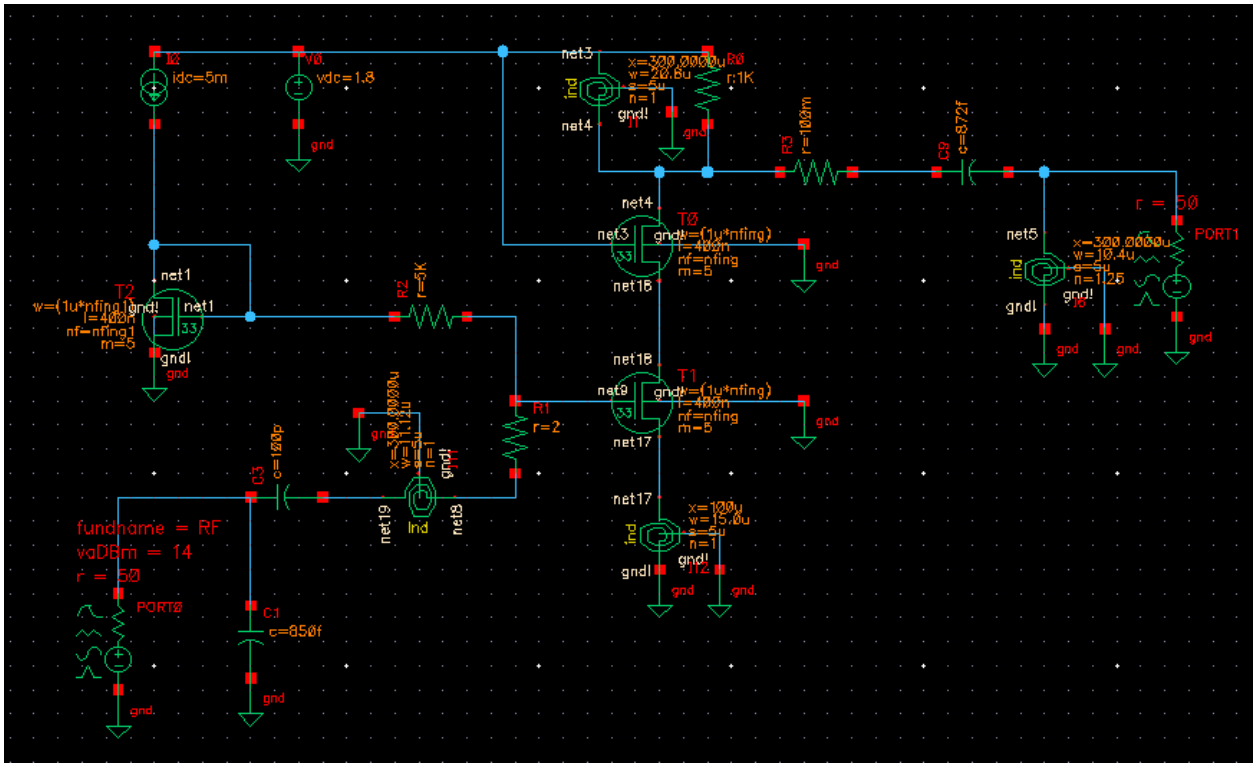

Figure 22 Circuit

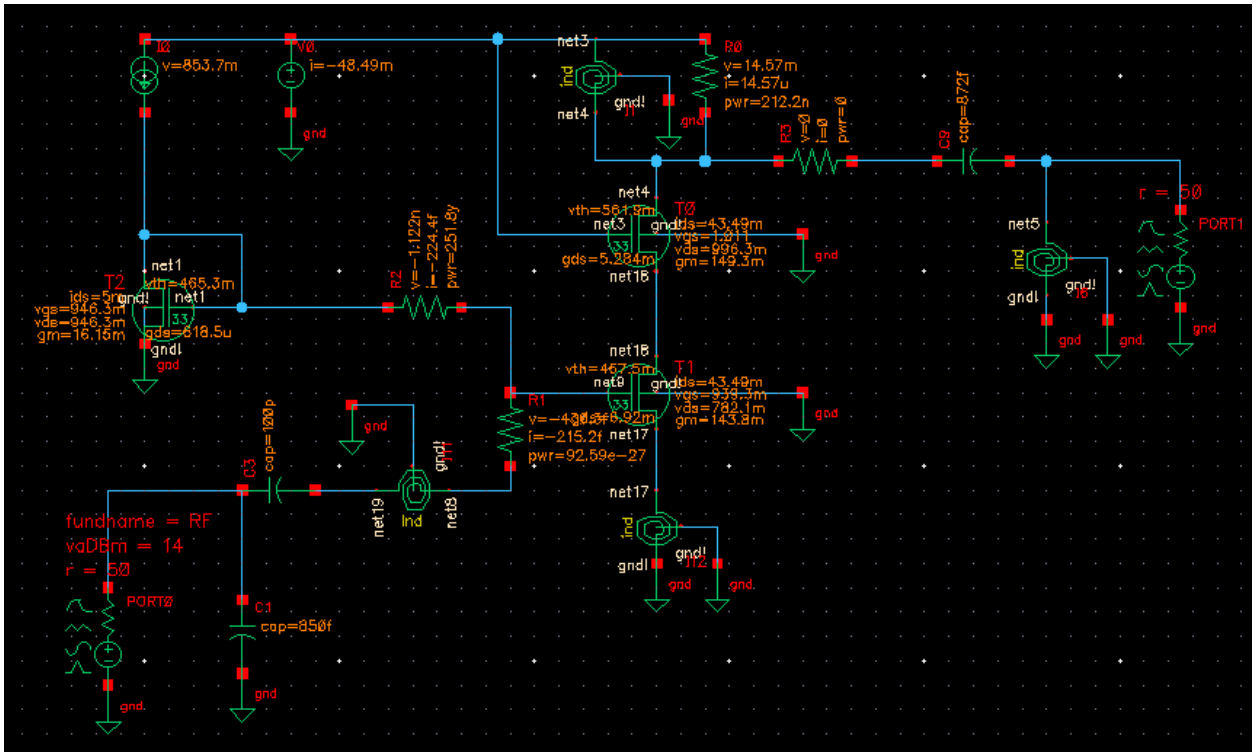

Figure 23 DC operating points

Calculations

Conduction angle (From figure 17 taking id2 for the calculation of conduction angle)

$$2\theta = \frac{T - t_{off}}{T} * 360 \quad = \frac{136.98 - (75.53 - 42.96)}{136.98} * 3602\theta = 274.4^0$$

The Conduction angle is found to be 274.4^0.

Voltage swing can be calculated from the figure 18. Here swing is 0.38V to 3.53 V = 3.15 V.

Output power can be calculated from Vop and R.

$$P_o = \frac{V_{o,peak}^2}{2R} = \frac{1.58^2}{2*24.35} = 51.36mW = 17.1dBm$$

Here you can see that calculated specs are less then achieved, because after matching CLS and Lout, I have changed Ltank to an optimum value for maximum PAE. Hence output resistance should have been changed.

Efficiency

$$\eta = \frac{V_{o,peak}}{V_{DD}} \frac{(2\theta - \sin sin\, 2\theta)}{4(\sin sin\, \theta - \theta \cos cos\, \theta)} \quad = 40.82\%$$

DC power

$$P_{dc} = IV \quad = 48.49mA\, x\, 1.8\, V \quad = 87.28\, mW$$

Input power.

$$P_{in} = 15dBm = 31.62mW$$

PAE

$$PAE = 100 * \frac{P_o - P_{in}}{P_{dc}} = 100 * \frac{51.36 - 31.62}{87.28} = 22.6\%$$

Design trade offs and discrepancies

To maximize output power we have to use Ls as small as possible. Also transistors should be characterized to have enough power at the output. It is quite clear that if we match S22 then PAE will decrease. Peak of PAE can be controlled by proper matching on CLS and Lout and also optimizing the value of the tank inductor.

Furthermore, while designing PA we often come across stability issues. If we use internal resistance to the modal ideal inductor to begin with then we should not have any issues with stability. Library inductors have some parallel or series resistance which will help with stability. Even after that our circuit is not stable, we can decrease the value of the bias resistor. But, by doing so we will allow signals to leak through the current mirror circuit. This will drastically decrease output power and PAE. Stability must be kept at “just stable” state because when we put library inductor stability we are maintained. We don’t want to waste efficiency by having a highly stable circuit.

Proper transistor sizing for required power is necessary because we are not using tank capacitance, instead of that we have very large transistor parasitic capacitance.

Here, in the current mirror circuit, by using the ratio 1:9 we are decreasing total dc current through the circuit. Hence Pdc decreases and PAE increases from the equation mentioned above.

As a discrepancy, we see here efficiency is lower than calculated value. The reason behind this can be some of the transistor losses that have not been calculated with equations. One of the losses could be due to low drain voltage at higher Pin. In the simulation it self I was having warnings above certain prf value, that transistor’s drain body diode is being forward biased by very small positive voltage. If my body is connected at ground then it is clear that drain voltage is getting very low i.e there is a bunch of current flowing through the circuit.

Conclusion

By attempting the design of a power amplifier it is understandable that we have to take the tread off between efficiency, stability and output power. As transistors here are very large, any small effect on one parameter will have a dramatic effect on others.