



PIC32CX-BZ2 and WBZ45 Family

High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Data Sheet

Introduction

The PIC32CX-BZ2 family is a general purpose, low-cost, 32-bit Microcontroller (MCU) family of devices supporting Multiprotocol wireless interfaces (Bluetooth® and Zigbee®), hardware-based security accelerator, transceiver and Power Management Unit (PMU).

The WBZ45 module is a series of fully RF certified wireless modules that contains the PIC32CX-BZ2 wireless MCUs with the following antenna options:

- PCB Antenna
- U.FL Connector for External Antenna

In addition, to the Bluetooth Low Energy (Bluetooth® 5.2) and Zigbee (Zigbee® 3.0) wireless protocol support, the PIC32CX-BZ2 devices and the WBZ45 modules also support a rich set of standard MCU peripherals such as ADC, SPI, I²C, SQI, UART and SWD.

PIC32CX-BZ2 SoC Family Features

The following section lists the PIC32CX-BZ2 SoC related features:

Operating Conditions MCUs

- 1.9V to 3.6V, -40°C to +125°C, DC to 64 MHz
 - AEC Q100 Grade 1 qualified

Core: 64 MHz ARM® Cortex®-M4

- 3.35 Coremark®/MHz
- 4 KB Combined Instruction Cache and Data Cache
- 8-Zone Memory Protection Unit (MPU)
- Thumb®-2 Instruction Set
- Digital Signal Processing ASE Rev 2
- Nested Vector Interrupt Controller (NVIC)
- Embedded Trace Module (ETM) with Instruction Trace Stream
- Core Sight Embedded Trace Buffer (ETB)
- Trace Port Interface Unit (TPIU)
- IEEE 754-Compliant Floating Point Unit (FPU)

Memories

- 1 MB On-Chip Self-programmable Flash With:
 - Error Correction Code (ECC)
 - Prefetch module to speed up Flash accesses
 - 20-years of data retention support
- 32 KB NVR Flash (8 Sectors)
 - Private/public boot code and data
 - NV calibration data
- 128 KB Multi-port Programmable QoS SRAM Main Memory
 - 64 KB of Error Correction Code (ECC) RAM option
- Up to 4 KB of Tightly Coupled Memory (TCM)
- Up to 8 KB Backup SRAM
- Single 32-bit Backup Register

System

- Power-on Reset (POR) and Brown-out Detection (BOD)
- Internal and External Clock Options
- External Interrupt Controller (EIC)
- Up to 4 External Interrupts
- One Non-maskable Interrupt
- 2-pin Serial Wire Debug (SWD) Programming, Test, and Debugging Interface

Supported Connectivity Standards

- Complies With:
 - Bluetooth® v5.2
 - IEEE 802.15.4, Zigbee® 3.0
 - ETSI EN 300 328 and EN 300 440 Class 2
 - FCC CFR47 Part 15 and ARIB STD-T66

Power Supply

- Integrated PMU With:
 - Buck (DC-DC/switching) mode; supports High Power (PWM) and Low Power (PSK) mode
 - MLDO (linear) mode
- On-board 1.2V Voltage Regulator (CLDO)
- Power-on Reset (POR) and Brown Out Detector (BOR) on 3.3V and 1.2V Rails
- Run, Idle, Dream, Sleep, Deep Sleep, and Extreme Deep Sleep Modes
- Sleep Walking Peripherals
- Embedded Buck/LDO Regulator Supporting On-the-fly (OTF) Selection

2.4 GHz RF Transceiver

- Integrated 2.4 GHz Ultra-low Power RF Transceiver shared between Bluetooth and Zigbee Modems and Link (MAC) Controllers
- Integrated 16 MHz \pm 20 ppm Crystal Oscillator (External Low Cost Crystal)
- Two PA Design Architecture (LPA (+4 dBm) and MPA (+10dBm)) to Improve TX Power Efficiency

- Low RBOM Two-port TRX RFFE Architecture
 - Integrated balun (single ended RF output) and TRX switch
- Hardware Radio Arbiter with Programmable QoS:
 - Resolution per packet level
 - Time-division coexistence between Bluetooth and 802.15.4
 - Based on shared transceiver and antenna
 - Maintains connections of 802.15.4 and Bluetooth simultaneously

Bluetooth

- Bluetooth Low Energy 5.2 Certified
- Up to +10 dBm Programmable Transmit Output Power
- Typical Receiver Power Sensitivity:
 - -95 dBm for Bluetooth Low Energy 1 Mbps
 - -92 dBm for Bluetooth Low Energy 2 Mbps
 - -102 dBm for Bluetooth Low Energy 125 Kbps
 - -99 dBm for Bluetooth Low Energy 500 Kbps
 - Digital RSSI indicator (-50 dBm ~ -90 dBm)
- Bluetooth Supported Features:
 - 2M uncoded PHY
 - Long range (Coded PHY)
 - Channel selection algorithm #2
 - Advertising extensions, offloads CPU with hardware based scheduler
 - High duty cycle non-connectable advertising
 - Data length extensions
 - Secure connections
 - Privacy upgrades (with hardware white-list support)
- ECDH P256 Hardware Engine for Link Key Generation When Bluetooth Pairing
- AES128 Hardware Module for Real-Time Bluetooth Payload Data Encryption
- Bluetooth Qualification Test Facility (BQTF) Certification
- Bluetooth Low Energy Profiles:
 - Bluetooth Low Energy peripheral and central roles
 - Bluetooth Low Energy APIs for application layer to implement standard or customize GATT based profiles/services
 - Microchip Transparent UART Service
 - Battery Service
 - Device Information Service
 - Custom Service
 - Multi-link and multi-role
- Bluetooth Low Energy Services:
 - Provisioning
 - Over-the-air (OTA) update (also known as DFU)
 - Advertisement/Beacon
 - Personalized configuration
 - Alert notification service

Zigbee

- Physical Layer Service Unit (PSDU) data rate: 250 Kbps
 - Proprietary data rates: 500 Kbps, 1 Mbps, and 2 Mbps

- Programmable RX Mode
 - -103 dBm RX sensitivity in the Continuous mode
 - -98 dBm sensitivity in the RPC mode
 - RPC mode provides lower power consumption in RX mode to support California Green Energy Specification at the system level
- TX Output Power up to +10 dBm
- Hardware Assisted MAC
 - Auto acknowledge
 - Auto retry
 - Channel access back-off
- SFD Detection; Spreading; De-spreading; Framing; CRC-16 Computation
- Independent TX/RX Buffers for Improved CPU Offloading While Handling Zigbee Data
 - 128-byte TX and 128-byte RX frame buffer
- Hardware Security
 - Advanced Encryption Standard (AES)
 - True Random Number Generator (TRNG)
- Zigbee Stack Support
 - Zigbee 3.0 ready
 - Zigbee Pro 2017
 - Zigbee green power support (proxy, sink, and multi sensor)

High Performance Peripherals

- 16-Channel Direct Memory Access Controller (DMAC)
 - Built-in CRC with memory CRC generation/monitor hardware support
- One Quad I/O Serial Peripheral Interface (QSPI)
 - execute-In-Place (xIP) support
 - Dedicated AHB memory zone

System Peripherals

- 32-Channel Event System
 - All channels can be connected to any event generator
 - All channels provide a pure asynchronous path
 - Twelve channels support synchronous and re-synchronous
- Four Serial Communication Interfaces (SERCOM), Each Configurable to Operate as:
 - USART with full-duplex and single-wire half-duplex configuration
 - ISO7816
 - I²C up to 1 MHz (three SERCOMs support I²C)
 - LIN Master/Slave
 - RS485
 - SPI inter-byte space
- Four 16-bit Timers/Counters (TC), Each Configurable as:
 - 16-bit TC with two compare/capture channels
 - 8-bit TC with two compare/capture channels
 - 32-bit TC with two compare/capture channels
- Two 24-bit Timer/Counters for Control (TCC) with Extended Functions:
 - Up to six compare channels with optional complementary output
 - Generation of synchronized Pulse Width Modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay, and configurable dead-time between complementary output

- Dithering that increase resolution with up to 5 bits and reduce quantization error
- One 16-bit Timer/Counters for Control (TCC) with Extended Functions:
 - Up to two compare channels with optional complementary output
- 32-bit Real Time Counter (RTC) with Clock/Calendar Function
- Up to four Wake-up Pins with Tamper Detection and Debouncing Filter
- Watchdog Timer (WDT) with Window Mode
- Deadman Timer (DMT)
- CRC-32 Generator
- Frequency Meter (FREQM)
- Two Configurable Custom Logic (CCL)
- One Analog Comparator (AC) with Window Compare function
- One Temperature Sensor (Die Temperature)

Advanced Analog

12-bit ADC SAR Module (ADC):

- Up to 8 Analog Channels
- Up to 2 MSPS conversion rate
- Multiple trigger sources
- Supports die temperature sensor built into RF-Analog (not an external “ambient” temperature sensor)
- Two Analog Comparator (AC) with Window Compare Function or single Analog Comparator
- One dedicated AC and second AC is shared with MVREF FSM

Security

- AES Engine with Support for 128/192/256 bit Cryptographic Key
- One AES with 256-bit Key Length and up to 2 MB/s Data Rate
 - Five confidential modes of operation (ECB, CBC, CFB, OFB, and CTR)
 - Supports counter with CBC-MAC mode
 - Galois Counter Mode (GCM)
- True Random Number Generator (TRNG)
- Public Key Cryptography Controller (PUKCC) and Associated Classical Public Key Cryptography Library (PUKCL)
 - RSA and DSA algorithm
 - Elliptic Curves Cryptography (ECC), ECC GF (2ⁿ), and ECCGF (p)
- Integrity Check Module (ICM) Based on Secure Hash Algorithm (SHA1, SHA224, and SHA256), DMA Assisted

Oscillators

- 16 MHz, ±20 PPM Crystal/Resonator Oscillator or External Clock (POSC) for 2.4G RF Transceiver
- Shared System PLL with Bluetooth/Zigbee RF Data Converter PLL
- 32.768 kHz Ultra-low Power Internal Oscillator
 - ±5% trimmed accuracy
- Higher Accuracy 32.768 kHz, ±250 ppm Clock Options
 - POSC derived 32 kHz clock
 - 32.768 kHz crystal/resonator oscillator (SOSC)
 - External 32.768 kHz clock source
- 8 MHz Internal RC Oscillator (FRC)

- Trimmed accuracy under $\pm 1\%$

I/O

- Flexible Peripheral Pin Select (PPS) Support
- High-current Sink/Source on Most I/O Pins
- Configurable Open-Drain Output on Digital I/O Pins
- 5V Tolerant Input Pins (Digital Pins Only)⁽¹⁾
- Up to 27 Programmable I/O Pins ⁽²⁾

Notes:

1. Certain pins are limited to 3.3V tolerance, see Electrical Specifications.
2. Two additional input only pins are available if not using SOSC.

Package

- PIC32CX1012BZ25048
 - 48-pin QFN
 - Size - 7 x 7 x 1 mm
- PIC32CX1012BZ24032
 - 32-pin QFN
 - Size - 5 x 5 x 1 mm

WBZ45 Module Features

The following section lists the WBZ45 Module related features, which complements SoC features:

WBZ45 Module Variants

- WBZ451 based on (PIC32CX1012BZ25048 SoC)
 - WBZ451PE (PCB)
 - WBZ451UE (u.FL)
- WBZ450 based on (PIC32CX1012BZ24032 SoC)
 - WBZ450PE (PCB)
 - WBZ450UE (u.FL)

Antenna

- On-Board PCB Antenna
- External Antenna

Clock Management

- Integrated 16 MHz POSC

System Peripheral, Advanced Analog and Security

- All features of SoC are accessible

Package and Operating Conditions

- WBZ451
 - 39-pin SMD package with Shield CAN
 - Size - 15.5 x 20.7 x 2.8 mm
- WBZ450
 - 30 pin SMD package with Shield CAN
 - Size - 13.4 x 18.7x 2.8 mm
- Operating Conditions
 - 1.9V to 3.6V, -40°C to +85°C, DC to 64 MHz

Certifications

- Certified to FCC, ISED and CE Radio Regulations
- RoHS and REACH Compliant

Note: Certifications in progress.

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PIC32CX-BZ2 and WBZ45 Family

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Preliminary

PIC32CX-BZ2 and WBZ45 Family Configuration Summary

1. Configuration Summary

Table 1-1. PIC32CX-BZ2 and WBZ45 Family Features

Device	Program Memory (KB)		Data Memory (KB)		Pins	Package	Peripherals										Analog	Security	Wireless				
	SERCOM	Timer/Counter (TC)	TCC (24-bit/16-bit)	QSPI			DMA Channels	RTC	CCL/LUT	WDT	DMT	Frequency Measurement	Event System (Channels)	External Interrupt Lines	GPIO Pins	Temperature Sensor	AES	TRNG	Public Key Cryptography (PUKCC)	Integrity Check Monitor	Max TX Power (dBm)	Bluetooth 5.1	802.15.4/Zigbee 3.0
PIC32CX1012BZ25048	1024	128	48	QFN	4	4	2/1	Y	16	Y	1/2	Y	Y	Y	32	4	27	2	8	Y	Y	10	
PIC32CX1012BZ24032	1024	128	32	QFN	2										32	4	16	1	6	4			
WBZ451	1024	128	37	LGA	4										32	4	27	2	8	10			
WBZ450	1024	128	30	LGA	2										32	4	16	1	6	4			

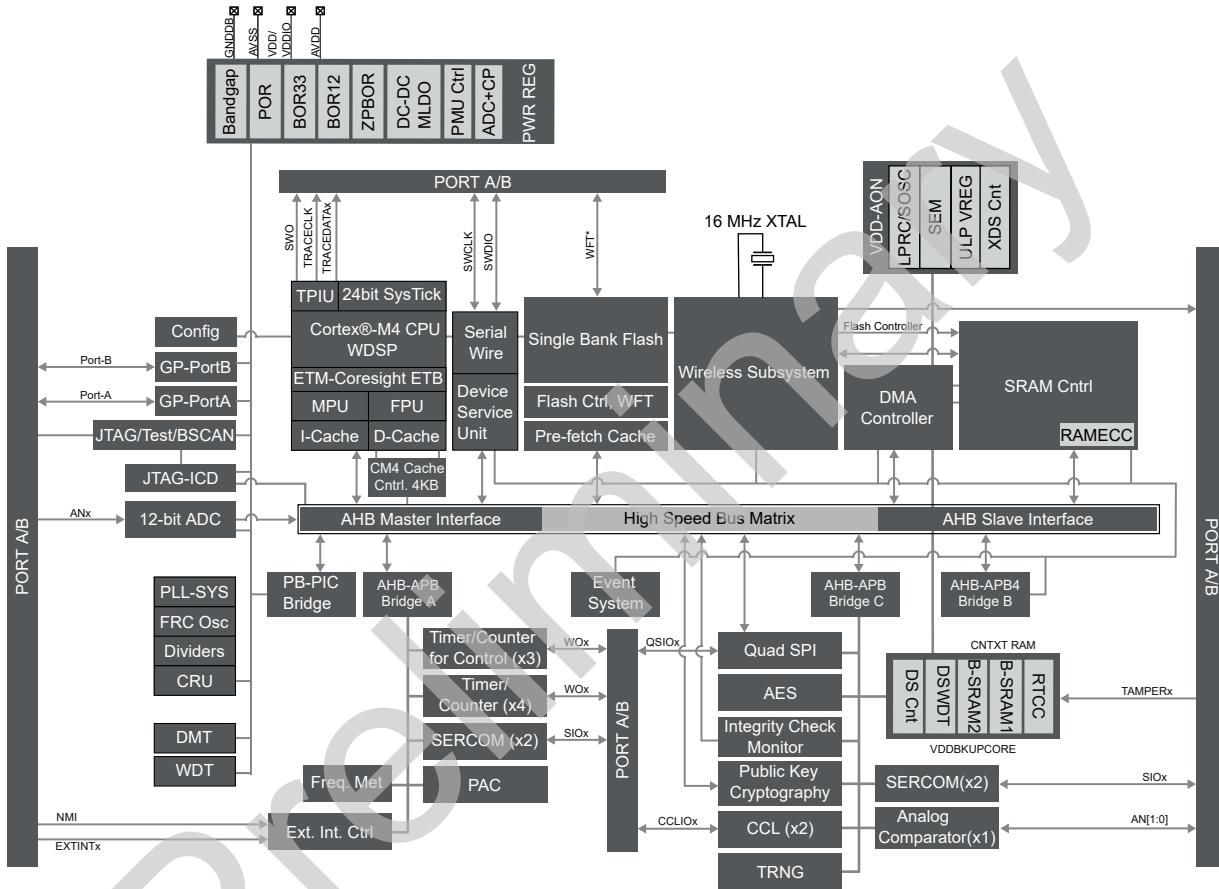
2. PIC32CX-BZ2 SoC Description

This chapter contains device-specific information for PIC32CX-BZ2 SoC.

2.1 PIC32CX-BZ2 SoC Block Diagram

The following figure illustrates the block diagram of the core and peripheral modules in the PIC32CX-BZ2 SoC.

Figure 2-1. PIC32CX-BZ2 SoC Block Diagram



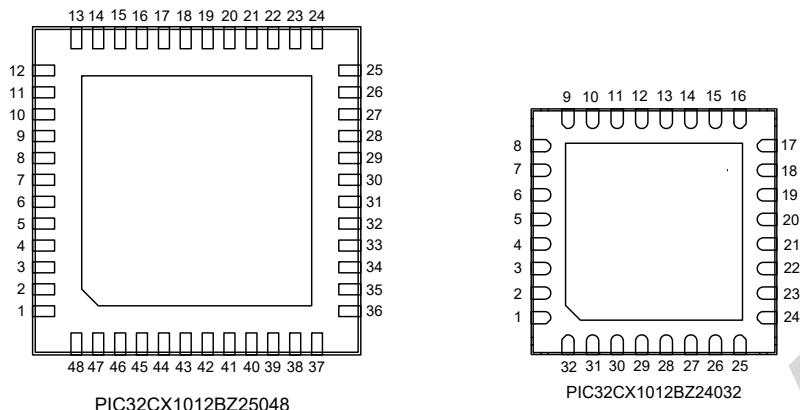
2.2 Pinout Diagram

This section provides details on pin diagrams for each variant of PIC32CX-BZ2 SoC.

PIC32CX-BZ2 and WBZ45 Family

PIC32CX-BZ2 SoC Description

Figure 2-2. PIC32CX1012BZ25048 and PIC32CX1012BZ24032 SoC Pin Diagram (Bottom View)



Note:

1. It is required that the exposed paddle on the bottom of the SoC be connected to ground in the PCB.

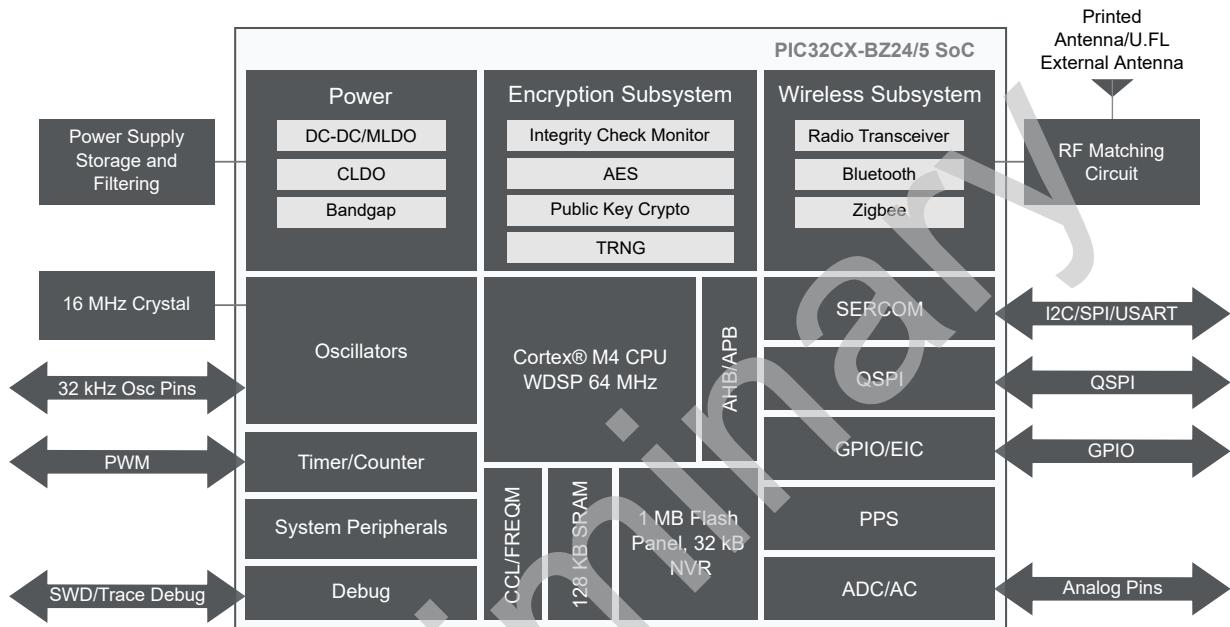
3. WBZ45 Module Description

The WBZ45 (certification in progress) contains the PIC32CX-BZ2 SoC with following antenna options:

- PCB antenna
- U.FL connector for external antenna

The following figure represents the WBZ45 module block diagram.

Figure 3-1. WBZ45 Module Block Diagram



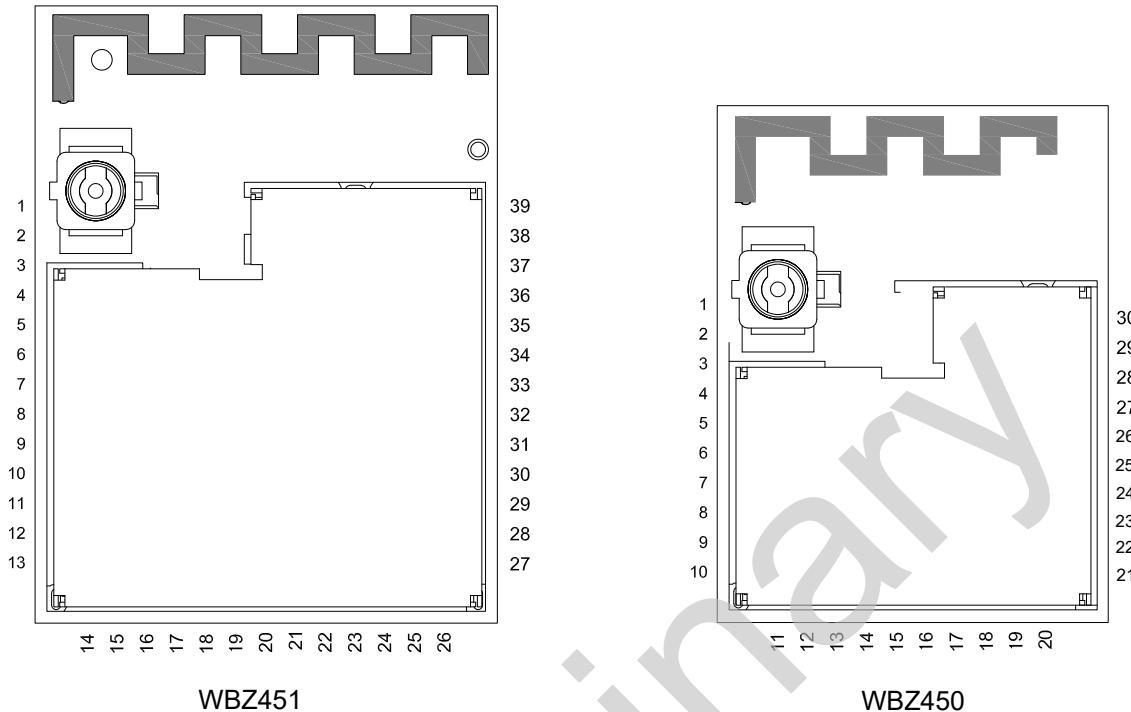
3.1 Pinout Diagram

The following figures illustrate the modules pinout diagrams.

PIC32CX-BZ2 and WBZ45 Family

WBZ45 Module Description

Figure 3-2. WBZ451 and WBZ450 Module Pin Diagram (Top View)

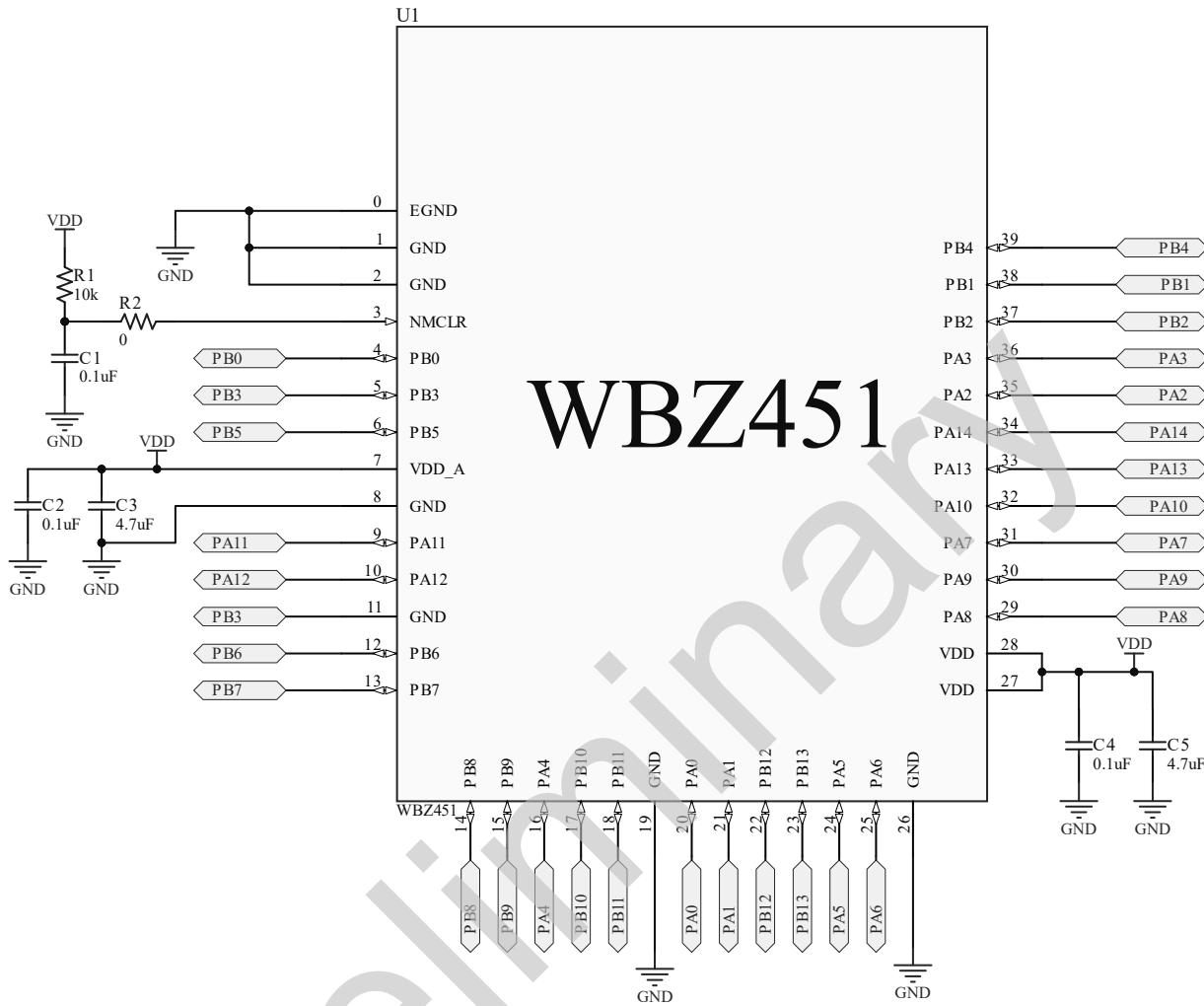


Note: It is required that the exposed paddle on the bottom of the module be connected to ground in the PCB.

3.2 Basic Connection Requirement

The WBZ45 module requires attention to a minimal set of device pin connections before proceeding with development.

Figure 3-3. Module Basic Connection and Interface Diagram



Related Links

[3.2.2. Master Clear \(MCLR\) Pin](#)

3.2.1 Power Pins

It is recommended to add a bulk and a decoupling capacitor at the input supply pin (VDD, VDD_A and GND pins) of the WBZ45 module.

- It is recommended to have a 4.7 μF on the VDD_A pin and 4.7 μF and a 0.1 μF on the VDD pin
- The value of the capacitors are based on typical application requirements and are the minimum recommended values. Depending on the application requirement (in other words, a noisy power line or other known noise sources), the values of capacitors can be adjusted to provide a clean supply to the module
- All capacitors must be placed close to the Module Power supply pins

3.2.2 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

- Device Reset
- Device programming and debugging

PIC32CX-BZ2 and WBZ45 Family

WBZ45 Module Description

Pulling the MCLR pin low, generates a device Reset. Module Basic Connection and Interface Diagram illustrates a typical MCLR circuit, see *Module Basic Connection and Interface Diagram* in the *Basic Connection Requirement* from Related Links.

The module has sufficient filtering (0.1 μ F) and pull-up (10k) on the Reset line. On a typical application no extra filtering is required on this pin.

Related Links

[3.2. Basic Connection Requirement](#)

3.2.3 SWD Lines

The SWDCLK, SWDIO and TRACESWO pins are used for SWD Programming and debugging purposes. It is recommended to use SWDCLK and SWDIO pin for the WBZ45 module for SWD as the default configuration (TRACESWO can be optional).

Keep the trace length between the SWD pins of the WBZ45 module and the SWD header as short as possible. If the SWD connector is expected to experience an ESD event, a series resistor is recommended with the value in the range of a few tens of Ω s , not to exceed 100 Ω .

3.2.4 Unused I/O Pins

Unused I/O pins should not be allowed to float as inputs. They can be configured as input and pulled-up. Alternatively depending on the application can be pulled-down as well.

Note: Pin PA3 has to be pulled-down for optimal power consumption.

3.2.4.1 GPIO Pins/PPS Functions

Most of the WBZ45 module pins can be configured as GPIOs pins or for PPS functionality. To find the functionality supported by each of these GPIOs, see *I/O Ports and Peripheral Pin Select (PPS)* from Related Links. It is recommended to add a series resistor on the host board for all critical, high frequency pins and clocks for EMI considerations GPIOs. The value of the series resistor depends on the actual pin configuration. These resistors must be placed close to the module. Example of Host Board on Top Layer illustrates the placement of series resistor, see *Example of Host Board on Top Layer* figure in the *WBZ45 Module Routing Guidelines* from Related Links.

Related Links

[5. I/O Ports and Peripheral Pin Select \(PPS\)](#)

[3.4. WBZ45 Module Routing Guidelines](#)

3.3 WBZ45 Module Placement Guidelines

- For any Bluetooth Low Energy/Zigbee product, the antenna placement affects the performance of the whole system. The antenna requires free space to radiate RF signals and it must not be surrounded by the ground plane. Thus, for best PCB antenna performance, the WBZ45 module should be placed at the edge of the host board.
- The WBZ45 module ground outline edge should be aligned with the edge of the host board ground plane as shown in the following figure.
- A low-impedance ground plane for the WBZ45 module ensures the best radio performance (best range and lowest noise). The ground plane can be extended beyond the minimum recommendation as required for the host board EMC and noise reduction.
- For best performance, keep metal structures and components (such as mechanical spacers, bump-on, and so on) at least 31.75 mm away from the PCB trace antenna as illustrated in the following figure.
- The antenna on the WBZ45 module should not be placed in direct contact with or close proximity to plastic casing or objects. Keep a minimum clearance of 10 mm in all directions around the PCB antenna as shown in the following figure. Keeping Metallic and Plastic objects close to the antenna can detune the antenna and reduce the performance of the device.
- Exposed GND pads on the bottom of the WBZ45 module must be soldered to the host board (see *Example of Host Board on Top Layer* figure in the *WBZ45 Module Routing Guidelines* from Related Links).
- A PCB cutout or a Copper keepout is required under RF test point (see [43.2. WBZ45 Module Packaging Information](#)).

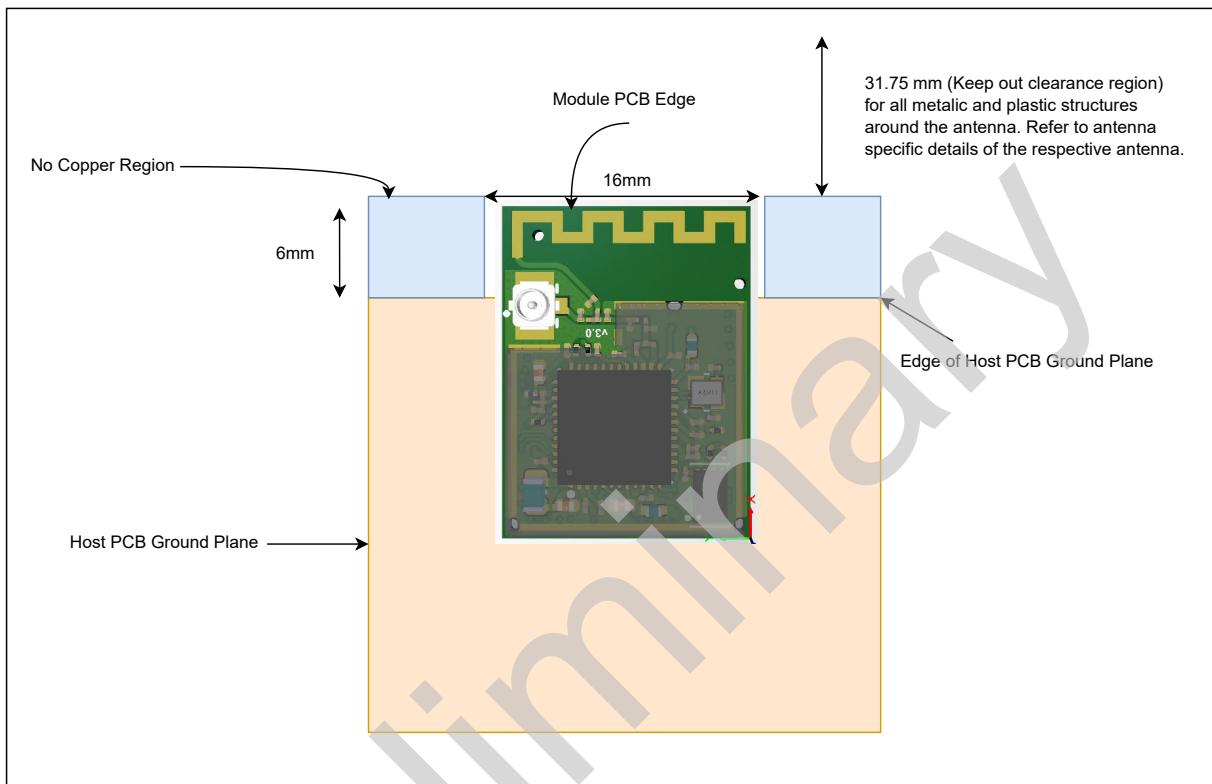
PIC32CX-BZ2 and WBZ45 Family

WBZ45 Module Description

- Copper keepout areas are required on the top layer under voltage test points (see [43.2. WBZ45 Module Packaging Information](#)).
- Alternatively, the entire region except the exposed ground paddle can be solder-masked.

The following figure illustrates the examples of WBZ45 module placement on a host board with a ground plane. Refer to the following figure for placement specific guidance.

Figure 3-4. Module Placement Guidelines



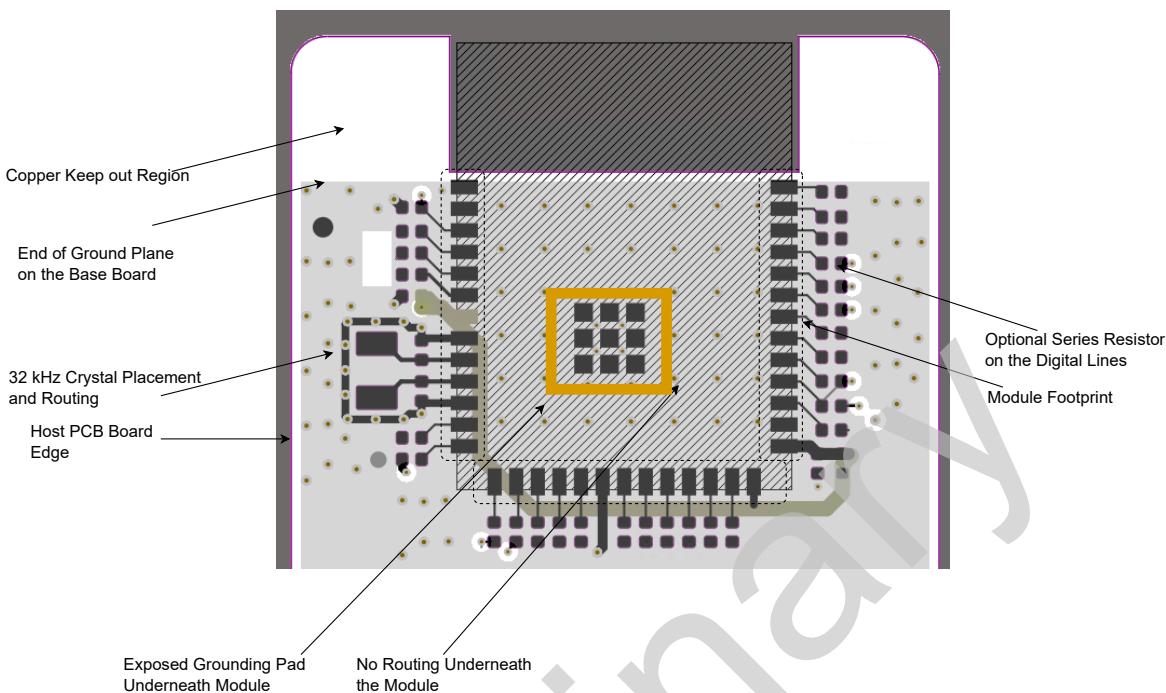
Related Links

[3.4. WBZ45 Module Routing Guidelines](#)

3.4 WBZ45 Module Routing Guidelines

- Use the multi-layer host board for routing signals on the inner layer and the bottom layer.
- The top layer (underneath the module) of the host board must be ground with as many GND vias as possible shown in the following figure.
- Avoid fan-out of the signals under the module or antenna area. Use a via to fan-out signals to edge of the WBZ45 module.
- For better GND connection to the WBZ45 module, solder the exposed GND pads of the WBZ45 module on the host board.
- For module GND pad, use a GND via of a minimum 10 mil (hole diameter) for good ground to all the layers and thermal conduction path.
- It is recommended to have a series resistor on the host board for all GPIOs. These resistors must be placed close to the WBZ45 module. Refer to the following figure for the placement of the series resistor.
- SOSC crystal (32.768 kHz) on host board should be placed close to the WBZ45 module and follow the shortest trace routing length with minimum number of vias (see the following figure).

Figure 3-5. Example of Host Board on Top Layer



Related Links

- [3.2.4.1. GPIO Pins/PPS Functions](#)
- [3.3. WBZ45 Module Placement Guidelines](#)

3.5 WBZ45 Module RF Considerations

The overall performance of the system is significantly affected by the product design, environment and application. The product designer must ensure system level shielding (if required) and verify the performance of the product features and applications.

Consider the following guidelines for optimal RF performance:

- The WBZ45 module must be positioned in a noise-free RF environment and must be kept far away from high-frequency clock signals and any other sources of RF energy
- The antenna must not be shielded by any metal objects
- Power supply must be clean and noise-free
- Make sure that the width of the traces routed to GND, VDD rails are sufficiently large for handling peak TX current consumption.

Note: The WBZ45 module includes RF shielding on top of the board as a standard feature.

3.6 WBZ45 Module Antenna Considerations

3.6.1 PCB Antenna

For the WBZ45 module, the PCB antenna is fabricated on the top copper layer and covered in solder mask. The layers below the antenna do not have copper trace. It is recommended that the module is mounted on the edge of the host board and to have no PCB material below the antenna structure of the module and no copper traces or planes on the host board in that area.

The following table lists the technical specification of the PCB antenna and tested with the WBZ45 module mounted on a Evaluation Board.

PIC32CX-BZ2 and WBZ45 Family

WBZ45 Module Description

Table 3-1. PCB Antenna Specification for WBZ45

Parameter	Specification
Operating frequency	2400 to 2480 MHz
Peak gain	2.36 dBi at 2420 MHz
Efficiency	50%

3.6.2 External Antenna Placement Recommendations

The following recommendations must be applied for the placement of the antenna and its cable:

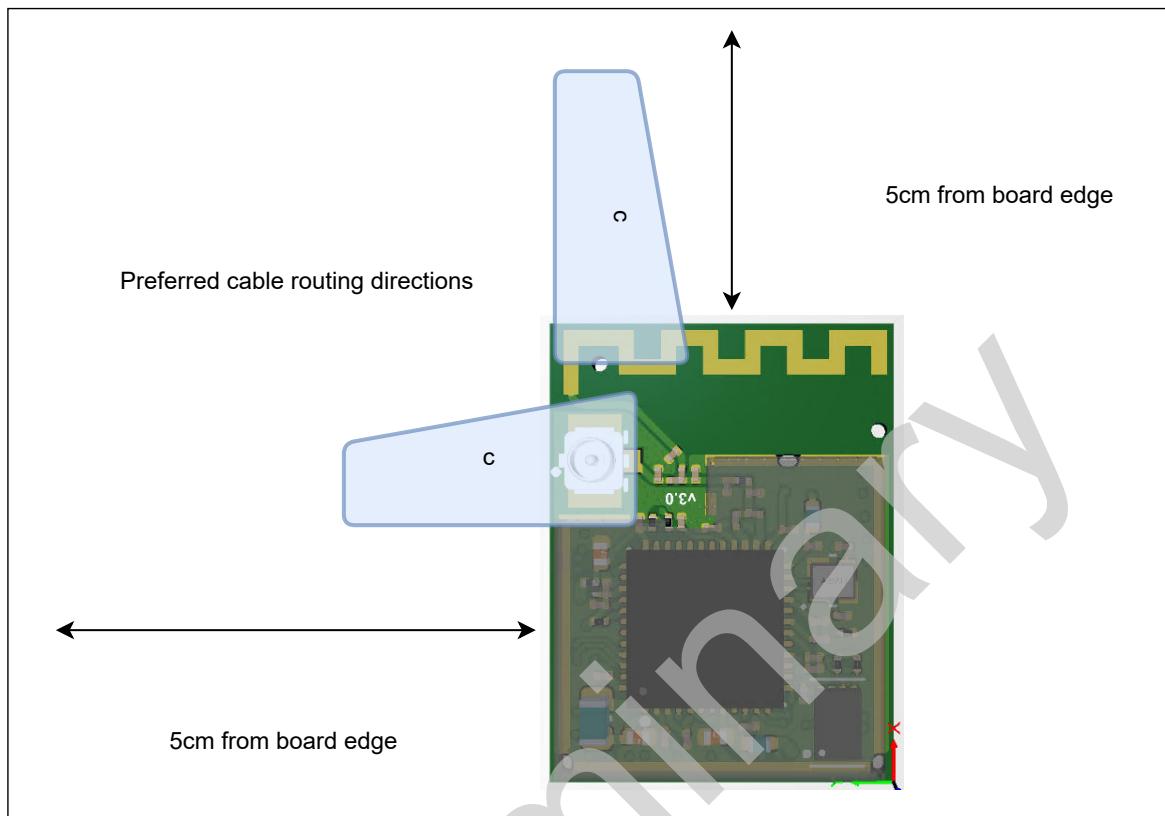
- The antenna cable must not be routed over circuits generating electrical noise on the host board or alongside or underneath the module. It is preferred that the cable is routed straight out of the module.
- The antenna must not be placed in direct contact or in close proximity of the plastic casing/objects. (Except in case, when the selected antenna specifically recommends).
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise, signals or harmonics within the 2.4 GHz to 2.5 GHz frequency band away from the antenna and, if possible, shield those components. Any noise radiated from the host board in this frequency band degrades the sensitivity of the module.
- The antenna should preferably be placed at a distance greater than 5 cm away from the module. The following figure shows the antenna keep out area indication where the antenna must not be placed.

These recommendations are based on an open-air measurement and does not take into account any metal shielding of the customer end product. When a metal enclosure is used, the antenna can be located closer to the WBZ45 module.

Note: These are generic guidelines and it is recommended that customers check and fine-tune the antenna positioning in the final host product based on RF performance.

The following figure provides an indication on how the antenna cable should be routed depending on the location of the antenna with respect to the WBZ45 PCB, there are two possible options for the optimum routing of the cable.

Figure 3-6. WBZ45 Antenna Placement Guidelines



3.7 WBZ45 Module Reflow Profile Information

The WBZ45 module was assembled using the IPC/JEDEC J-STD-020 Standard lead free reflow profile. The WBZ45 module can be soldered to the host board using standard leaded or lead free solder reflow profiles. To avoid damaging the module, adhere to the following recommendations:

- For Solder Reflow Recommendations, refer to the *Solder Reflow Recommendation Application Note (AN233)*.
- Do not exceed a peak temperature (TP) of 250°C.
- Refer to the solder paste data sheet for specific reflow profile recommendations from the vendor.
- Use no-clean flux solder paste.
- Do not wash as moisture can be trapped under the shield.
- Use only one flow. If the PCB requires multiple flows, apply the module on the final flow.

3.7.1 Cleaning

The Exposed GND pad helps to self-align the module, avoiding pad misalignment. The use of no clean solder pastes is recommended. Full drying of no-clean paste fluxes as a result of the reflow process must be ensured. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. The uncured flux residues may lead to corrosion and/or shorting in accelerated testing and possibly the field.

3.8 WBZ45 Module Assembly Considerations

The WBZ45 module is assembled with an EMI shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions such as IPA and similar solvents can be used to clean this module. Cleaning solutions containing acid must never be used on the module.

3.8.1 Conformal Coating

The modules are not intended for use with a conformal coating and the customer assumes all risks (such as the module reliability, performance degradation and so on) if a conformal coating is applied to the modules.

Preliminary

PIC32CX-BZ2 and WBZ45 Family

Pinout and Signal Descriptions List

4. Pinout and Signal Descriptions List

The following table provides details on signal names classified by the peripherals along with the device pinout for each variant of PIC32CX-BZ2 SoC and WBZ45 Module.

Table 4-1. Pinout and Signal Descriptions List

PIC32CX-BZ2 SoC		WBZ45 Module		Pad Name	Peripherals										
24032	25048	450	451		AC	ADC	EIC ⁽⁴⁾	GPIO (1, 2)	QSPI	RTCC	SERCOM	OSC	RF	DEBUG	
		1, 5, 8, 18, 21, 27	1, 2, 8, 11, 19, 26	GND											
32	1			PMU_BK											
1	2			VPMU_VDD											
2	3			PMU_MLDO											
	4		20	PA0				RA0	QSPI_DATA2	RTC_IN3					
	5		21	PA1	AC_CMP1			RA1	QSPI_DATA3	RTC_IN2					
	6		35	PA2	AC_CMP0			RA2		RTC_IN1					
3	7	19	24	PA5				RA5			SERCOM0_PAD0				
4	8	16, 17	27, 28	VDD											
5	9	20	25	PA6	AC_CMP1_ALT			RA6			SERCOM0_PAD1			PGC2ENTRY	
6	10	25	31	PA7				RA7			SERCOM1_PAD0			TRACECLK	
7	11	24	29	PA8				RA8			SERCOM1_PAD1		FECTRL0	PGD2ENTRY	
8	12	22	30	PA9				RA9		RTC_IN0_ALT	SERCOM1_PAD2		FECTRL1		
9	13	23	32	PA10				RA10		RTC_OUT_ALT	SERCOM1_PAD3		FECTRL2		
	14		22	PB12				RB12	QSPI_DATA0						
	15		23	PB13				RB13	QSPI_DATA1	RTC_EVENT					
	16		33	PA13				RA13			SERCOM2_PAD0		COEXCTRL0		
	17		34	PA14				RA14			SERCOM2_PAD1		COEXCTRL1		
10	18			CLDO_O											
11	19			BUCK_CLDO											
12	20			EXTR(8)											
13	21			BUCK_BB											
14	22			XO_N								XO-			
15	23			XO_P								XO+			
16	24			BUCK_PLL											
17	25			BUCK_LPA											
18	26			LPA_OUT								LPA			
	27			MPA_OUT								MPA			
	28			BUCK_MPA											
	29	2	3	NMCLR											
20	30	3	4	PB0	AC_AIN2	AN4		RB0					COEXCTRL2		
21	31	10	38	PB1	AC_AIN3	AN5		RB1							
	32		37	PB2	AC_AIN0	AN6		RB2							
	33		5	PB3	AC_AIN1	AN7		RB3							
22	34	11	39	PB4			AN0	INT0	RB4					FECTRL3	TRACEDATA3, PGC1

PIC32CX-BZ2 and WBZ45 Family

Pinout and Signal Descriptions List

.....continued

PIC32CX-BZ2 SoC	WBZ45 Module	Pad Name	Peripherals									
			AC	ADC	EIC ⁽⁴⁾	GPIO (1, 2)	QSPI	RTCC	SERCOM	OSC	RF	DEBUG
24032	25048	450	451									
23	35	9	6	PB5		AN1	RB5				FECTRL4	TRACEDATA0, PGC4
24	36	4	7	AVDD								
25	37	12	12	PB6		ANN0,AN2	RB6				FECTRL5	TRACEDATA1, PGD1
26	38	15	13	PB7	LVDIN	AN3	RB7					TRACEDATA2, CM4_SWO, PGD4
	39			VDD								
27	40	14	15	PB9			RB9					CM4_SWDIO
28	41	13	14	PB8			RB8					CM4_SWCLK
29 ⁽⁶⁾	42	6	16	PA4			RA4		RTC_OUT	SERCOM0_PAD3		
	43		17	PB10			RB10	QSPI_CS				
	44		18	PB11			RB11	QSPI_SCK				
29	45		9	PA11			RA11 ⁽⁵⁾			SOSCI		
30	46		10	PA12			RA12 ⁽⁵⁾			SOSCO		
30 ⁽⁶⁾	47	7	36	PA3			RA3		RTC_IN0	SERCOM0_PAD2	SCLKI	
31	48			VPMU_VDD								
		26, 28, 29, 30		NC								

Notes:

1. All GPIOs (RAn and RBn) can be used by remappable peripherals via PPS.
2. All GPIOs (RAn and RBn) can be used as IO Change Notification (IOCAN and IOCBBn).
3. The metal paddle at the bottom of the device must be connected to system ground.
4. These peripherals have signals that are only available via the PPS remappable pins.
5. This pin can be used as Input only pin if not using SOSC.
6. For 24032 only, pin 29 and pin 30 act as GPIO PA4/PA3 respectively ONLY if CFGCON0.GPSOSCE = 0. If CFGCON0.GPSOSCE=1, these pins are SOSC 32 kHz crystal inputs OR as digital input only RA11/RA12 respectively.
7. These I/O pins are 5.5V tolerant: NMCLR, PA0, PA1, PA2, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA13, PA14, PB10, PB11, PB12, PB13. All other I/O pins are 3.3V tolerant.
8. External resistor used to set internal reference current of the SOC.

5. I/O Ports and Peripheral Pin Select (PPS)

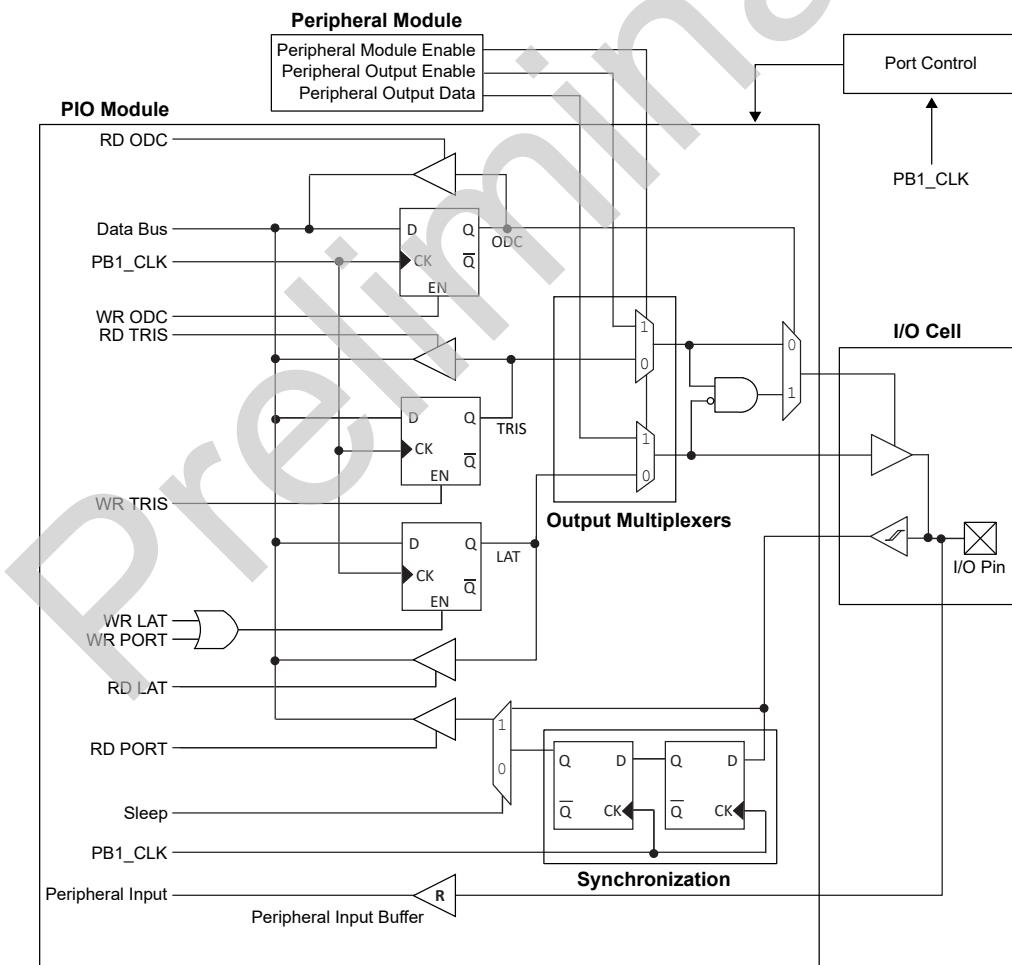
General purpose I/O (GPIO) pins allow the PIC32CX-BZ2 devices to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin. For more details on pin multiplexing, see *GPIO Pins/PPS Functions* from Related Links. There are default priorities for each GPIO pin as well. For details on priorities, see *Function Priority for Device Pins* from Related Links. It must be noted that 'fuse' values stored in NVR memory can be used to alter the power-on default function for certain GPIO pin. See *System Configuration Registers (CFG)* from Related Links.

Some of the key features of the I/O ports are:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
 - Fast bit manipulation using CLR, SET and INV registers
 - Slew rate control (not available on all devices)

The following figure illustrates a block diagram of a typical multiplexed I/O port.

Figure 5-1. Typical Multiplexed Port Structure Block Diagram



Related Links

- 3.2.4.1. GPIO Pins/PPS Functions
- 3.2.4.1. GPIO Pins/PPS Functions
- 17. System Configuration and Locking (CFG)

5.1 Control Registers

Before reading and writing any I/O port, the desired pin(s) must be properly configured for the application. Each I/O port has nine registers directly associated with the operation of the port and one control register. Each I/O port pin has a corresponding bit in these registers. Throughout this section, the letter 'x', denotes any or all port module instances. For example, TRISx represents TRISA or TRISB. Any bit and its associated data and control registers that is not valid for a particular device will be disabled and will read as zeros.

5.1.1 Registers for Configuring Tri-state Functions (TRISx)

The TRISx registers configure the data direction flow through port I/O pins. The TRISx register bits determine whether a PORTx I/O pin is an input or an output:

- If a data direction bit is '1', the corresponding I/O port pin is an input.
- If a data direction bit is '0', the corresponding I/O port pin is an output.
- A read from a TRISx register reads the last value written to that register.
- All I/O port pins are defined as inputs after a Power-on Reset (POR).

5.1.2 Registers for Configuring Port Functions (PORTx)

The PORTx registers allow I/O pins to be accessed:

- A write to a PORTx register writes to the corresponding LATx register (PORTx data latch). Those I/O port pin(s) configured as outputs are updated.
- A write to a PORTx register is effectively the same as a write to a LATx register.
- A read from a PORTx register reads the synchronized signal applied to the port I/O pins.

5.1.3 Registers for Configuring Latch Functions (LATx)

The LATx registers (PORTx data latch) hold data written to port I/O pins:

- A write to a LATx register latches data to corresponding port I/O pins. Those I/O port pins configured as outputs are updated.
- A read from a LATx register reads the data held in the PORTx data latch, not from the port I/O pins.

5.1.4 Registers for Open-Drain Configuration (ODCx)

Each I/O pin can be individually configured for either normal digital output or open-drain output. This is controlled by the open-drain control register, ODCx, associated with each I/O pin. If the ODCx bit for an I/O pin is a '1', the pin acts as an open-drain output. If the ODCx bit for an I/O pin is a '0', the pin is configured for a normal digital output (the ODCx bit is valid only for output pins). After a Reset, the status of all the bits of the ODCx register is set to '0'.

The open-drain feature allows the generation of outputs higher than VDD (for example, 5V) on any desired 5V tolerant pins using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification. The ODCx register setting functions in all of the I/O modes, allowing the output to behave as an open-drain even if a peripheral is controlling the pin. Although, the user may achieve the same result by manipulating the corresponding LATx and TRISx bits, this procedure does not allow the peripheral to operate in the Open-Drain mode (except for the default operation of the I²C™ pins). Since I²C pins are already open-drain pins, the ODCx settings do not influence the I²C pins. Also, the ODCx settings do not influence the JTAG output characteristics as the JTAG scan cells are inserted between the ODCx logic and the I/O.

5.1.5 Registers for Configuring Analog and Digital Port Pins (ANSELx)

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRISx bits set. To use port pins for I/O functionality with digital modules such as Timers, SERCOMs, and so on, the corresponding ANSELx bit must be cleared. The ANSELx

register has a default value of 0xFFFF; therefore, all pins that share analog functions are by default analog and not digital.

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (V_{OH} or V_{OL}) is converted by an analog peripheral, such as the ADC module or the comparator module. When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low-level). Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

5.1.6 Registers for Input Change Notification (CN)

The input Change Notification (CN) function of the I/O ports allows PIC32CX-BZ2 devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled.

The following control registers are associated with the CN functionality of each I/O port:

- Change Notice Pull-up Enable (CNPUE_x)
- Change Notice Pull-down Enable (CNPD_x)
- Change Notice Control (CNCON_x)
- Change Notice Enable (CNEN_x/CNNEX)
- Change Notice Status (CNSTAT_x/CNFx) or the positive edge control

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUE_x and the CNPD_x registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins must always be disabled when the port pin is configured as a digital output

The CNCON_x registers provide change notice control.

The CNEN_x/CNNEX registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins. CNEN_x enables a mismatch CN interrupt condition when EDGEDETECT is not set. When EDGEDETECT is set, CNNEX controls the negative edge while CNEN_x controls the positive. On devices that do not have EDGEDETECT, this CN logic acts as if EDGEDETECT is not set.

The CNSTAT_x/CNFx registers indicate whether a change occurred on the corresponding pin since the last read of the PORT_x bit. The CNFx registers indicate the type of change that occurred.

5.1.7 Registers for Peripheral Pin Select

The Peripheral Pin Select [pin name]R register ([pin name]R) and the Peripheral Pin Select Output (RPnR) register (RPnR) provide the control bits for peripheral pin select input and output. See [pin name]R and RPnR from Related Links. For more details on configuring these registers, see *Remappable Inputs and Output Mapping* from Related Links.

5.1.8 Registers for Slew Rate Control

Some I/O pins can be configured for various types of slew rate control on its associated port. This is controlled by the slew rate control bits in the SRCON1x and SRCON0x registers that are associated with each I/O port. The slew rate control is configured using the corresponding bit in each register, as shown in the following table.

As an example, writing 0x0001, 0x0000 to SRCON1A and SRCON0A, respectively, can enable slew rate control on the RA0 pin and sets the slew rate to the slow edge rate.

Table 5-1. Slew Rate Control Bit Settings⁽¹⁾

SRCON1x	SRCON0x	Description
1	1	Slew rate control is enabled and is set to the slowest edge rate.
1	0	Slew rate control is enabled and is set to the slow edge rate.

.....continued

SRCON1x	SRCON0x	Description
0	1	Slew rate control is enabled and is set to the medium edge rate.
0	0	Slew rate control is disabled and is set to the fastest edge rate.
1. By default, all of the port pins are set to the fastest edge rate.		

5.1.9 CLR, SET, and INV Registers

Every I/O module register has a corresponding SET, CLR, and INV register, which provide atomic bit manipulations. As the name of the register means, a value written to a SET, CLR, or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

- Writing 0x0001 to TRISASET register sets only bit 0 in the base register TRISA
- Writing 0x0020 to PORTDCLR register clears only bit 5 in the base register PORTD
- Writing 0x9000 to LATCINV register inverts only bits 15 and 12 in the base register LATC

Reading SET, CLR, and INV registers returns an undefined value. To see the influences of a write operation to a SET, CLR, or INV register, the base register must be read instead.

A typical method to toggle an I/O pin requires a read-modify-write operation performed on a PORTx register in software. For example, a read from a PORTx register, mask and modify the desired output bit or bits, and write the resulting value back to the PORTx register. This method is vulnerable to a read-modify-write issue where the port value may change after it is read and before the modified data can be written back, thus changing the previous state. This method also requires more instructions.

A more efficient and atomic method uses the PORTxINV register. A write to the PORTxINV register effectively performs a read-modify-write operation on the target base register, equivalent to the software operation described previously; however, it is done in hardware. To toggle an I/O pin using this method, a '1' is written to the corresponding bit in the PORTxINV register. This operation reads the PORTx register, invert only those bits specified as '1', and write the resulting value to the LATx register, thus toggling the corresponding I/O pins all in a single atomic instruction cycle. PORTAINV = 0x0001;

5.2 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application, where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, the users can better modify the device to their entire application, rather than trimming the application to fit the device.

This feature operates over a fixed subset of digital I/O pins. The users may independently map the input and/or output of most digital peripherals to these I/O pins. The PPS configuration is performed in the software and generally does not require the device to be reprogrammed. The hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once the PPS configuration is established.

5.2.1 Re-mappable Pin Groupings

The remappable pins, as well as the available input and output functions are divided into four groups. The remappable pins of group k may be assigned pin functions only from group k, k = 1,2,3,4. The pins used by each peripheral are spread across all four groups when possible to maximize flexibility.

5.2.2 Enabling Remap Pins

Each remap pin (RPx) must be enabled by disabling all higher priority pin functions on that pin before it can be used. Typically, all functions other than GPIO are considered higher priority than remap pins.

5.2.3 RP Register Protection

The <INPUT>R and RPxxR registers are implemented with two levels of protection:

- I/O Lock Feature – All PPS registers may only be written, while CFGCON0.IOLOCK = 0; once the IOLOCK is set, the registers cannot be written.
- IOLOCK Protection – The state of the IOLOCK bit can only be changed, once it is unlocked using the CFGCON0.CFGLOCK[1:0] register.

These features prevent the RP registers from being inadvertently written during normal operation, since changing the pinout functionality may have detrimental system level outcome.

5.2.4 Available Pins

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where:

- RP – designates a remappable peripheral.
- n – is the remappable port number.

5.2.5 Available Peripherals

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (SERCOM), general purpose timer clock inputs, timer-related peripherals (input capture and output compare), interrupt-on-change inputs, and reference clocks (input and output).

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the ADC.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

5.2.6 Controlling PPS

The PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is mapped.

5.2.7 Remappable Inputs

5.2.7.1 Enabling Remappable Peripheral Inputs

With PPS, each remappable input pin function (EXTINT0, SERCOM0_PAD3 and so on.) is assigned to be driven from a specific device pin by programming the corresponding <INPUT>R[3:0] register (meaning, EXTINT0R[3:0], SCOM0P3R[3:0], and so on.) with a value defined in the *Input Pin Selection Group 1*, *Input Pin Selection Group 2*, *Input Pin Selection Group 3*, *Input Pin Selection Group 4* tables and [pin name]R register. See these tables in the *Remappable Input Example* and [pin name]R from Related Links.

Assigning a remappable input pin function does not automatically enable the digital input buffer on the pin. The buffer must be enabled for each remap pin (RPx) by disabling all higher priority pin functions on that pin. Typically, all functions other than GPIO are considered higher priority than remap pins. See *Function Priority for Device Pins* for the list and priority of pin functions on each pin from Related Links.

The mapping is dynamic; therefore in order to avoid glitching outputs, the user is responsible for turning off the appropriate peripherals before remapping the pin functions associated with that peripheral. Since on Reset all inputs

are mapped to a default value and all outputs are disabled, the mapping may safely be performed after any device Reset.

Related Links

[5.2.7.3. Remappable Input Example](#)

5.2.7.2 Remappable Input Priority

Since only a single pin can be selected for any of the remappable peripheral inputs, priority encoding is not needed for RP inputs.

Note: A remappable input function does not have any control over the output of the RPx pin.

In this way, it is possible to drive a remappable output function on a RPx pin and a completely different remappable input function on the same pin. This can be useful, for instance, in driving a EVSYS output back into a Timer clock or gating input by assigning both functions to the same remap pin.

Note: To allow flexibility on a 32 or 48-pin devices, same input functions are repeated in multiple groups. Therefore, in order to differentiate between them "Off" code is provided in the *Input Pin Selection Group 1*, *Input Pin Selection Group 2*, *Input Pin Selection Group 3*, and *Input Pin Selection Group 4* tables. See these tables in the *Remappable Input Example* from Related Links.

The software must ensure that unused group register offset of a (repeated) input function is programmed to 4' h0 for proper operation. Failure to do so will lead to unknown behavior.

Related Links

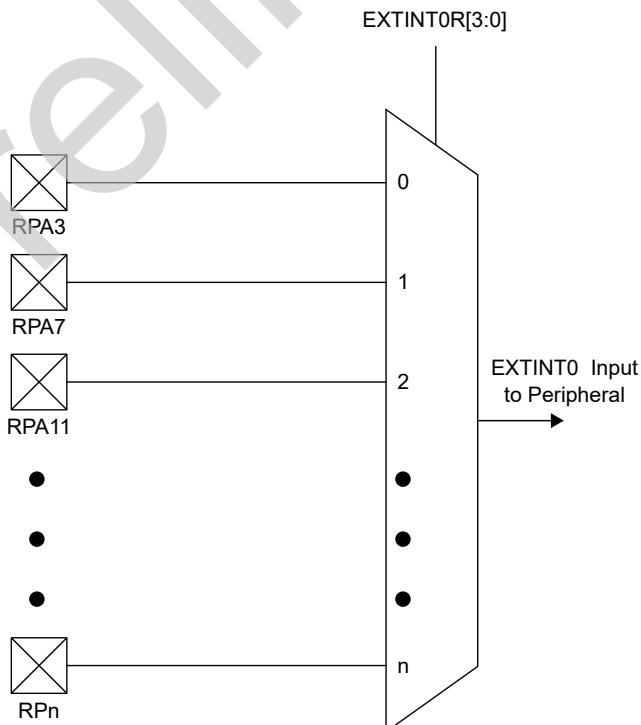
[5.2.7.3. Remappable Input Example](#)

5.2.7.3 Remappable Input Example

For example, following figure illustrates the remappable pin selection for the EXTINT0 input. In order to remap the EXTINT0 input to a particular pin, the EXTINT0R remap register must be programmed. Since EXTINT0 is in group 1, it can be mapped to any pin that is in group 1 (RPA3, RPA7, RPA9, RPA11, RPB0, RPB4, RPB8, and so on).

In order to map it to RPB0, then program the value 4 (4'b0100) into the EXINTR0R SFR register. See the following *Input Pin Selection Group 1* table.

Figure 5-2. EXTINT0 Remappable Pin Selection



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Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

Note: * in the following tables denotes that these pins and associated registers are not available in the 32-pin package.

Table 5-2. Input Pin Selection Group 1

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
EXTINT0	EXTINT0R	EXTINT0[3:0]	0000 = OFF
SERCOM0_PAD3	SCOM0P3R	SCOM0P3R[3:0]	0001 = RPA3
SERCOM1_PAD2	SCOM1P2R	SCOM1P2R[3:0]	0010 = RPA7
SERCOM2_PAD1	SCOM2P1R	SCOM2P1R[3:0]	0011 = RPA11*
SERCOM3_PAD0	SCOM3P0R	SCOM3P0R[3:0]	0100 = RPB0*
QSCK	QSCKR	QSCKR[3:0]	0101 = RPB4
QD1	QD1R	QD1R[3:0]	0110 = RPB8
REFI	REFIR	REFIR[3:0]	0111 = RPB12*
CCLIN0	CCLIN0R	CCLIN0R[3:0]	1000 = RPA2*
CCLIN3	CCLIN3R	CCLIN3R[3:0]	1001 = RPA6
TC0_WO0G1	TC0WO0G1R	TC0WO0G1R[3:0]	1010 = RPA10
TC1_WO0G1	TC1WO0G1R	TC1WO0G1R[3:0]	1011 = RPA14*
TC2_WO0G1	TC2WO0G1R	TC2WO0G1R[3:0]	1100 = RPB3*
TC3_WO0G1	TC3WO0G1R	TC3WO0G1R[3:0]	1101 = RPB7 1110 = RPB11* 1111 = RPA9

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Table 5-3. Input Pin Selection Group 2

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
EXTINT1	EXTINT1R	EXTINT1R[3:0]	0000 = OFF
SERCOM0_PAD0	SCOM0P0R	SCOM0P0R[3:0]	0001 = RPA4
SERCOM1_PAD3	SCOM1P3R	SCOM1P3R[3:0]	0010 = RPA8
SERCOM2_PAD2	SCOM2P2R	SCOM2P2R[3:0]	0011 = RPA12*
SERCOM3_PAD1	SCOM3P1R	SCOM3P1R[3:0]	0100 = RPB1*
QD2	QD2R	QD2R[3:0]	0101 = RPB5
CCLIN1	CCLIN1R	CCLIN1R[3:0]	0110 = RPB9
CCLIN4	CCLIN4R	CCLIN4R[3:0]	0111 = RPB13*
TC0_WO0G2	TC0WO0G2R	TC0WO0G2R[3:0]	1000 = RPA3
TC1_WO1G2	TC1WO1G2R	TC1WO1G2R[3:0]	1001 = RPA7
TC2_WO1G2	TC2WO1G1R	TC2WO1G1R[3:0]	1010 = RPA11*
TC3_WO1G2	TC3WO1G1R	TC3WO1G1R[3:0]	1011 = RPB0*
			1100 = RPB4
			1101 = RPB8
			1110 = RPB12*
			1111 = RPA0*

Table 5-4. Input Pin Selection Group 3

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
EXTINT2	EXTINT2R	EXTINT2R[3:0]	0000 = OFF
SERCOM0_PAD1	SCOM0P1R	SCOM0P1R[3:0]	0001 = RPA5
SERCOM1_PAD0	SCOM1P0R	SCOM1P0R[3:0]	0010 = RPA9
SERCOM2_PAD3	SCOM2P3R	SCOM2P3R[3:0]	0011 = RPA13*
SERCOM3_PAD2	SCOM3P2R	SCOM3P2R[3:0]	0100 = RPB2*
QD3	QD3R	QD3R[3:0]	0101 = RPB6
CCLIN2	CCLIN2R	CCLIN2R[3:0]	0110 = RPB10*
CCLIN5	CCLIN5R	CCLIN5R[3:0]	0111 = RPA0*
TC0_WO1G3	TC0WO1G3R	TC0WO1G3R[3:0]	1000 = RPA4
TC2_WO0G3	TC2WO0G3R	TC2WO0G3R[3:0]	1001 = RPA8
TC3_WO0G3	TC3WO0G3R	TC3WO0G3R[3:0]	1010 = RPA12*
			1011 = RPB1*
			1100 = RPB5
			1101 = RPB9
			1110 = RPB13*
			1111 = RPA1*

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Table 5-5. Input Pin Selection Group 4

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
EXTINT3	EXTINT3R	EXTINT3R[3:0]	0000 = OFF 0001 = RPA6 0010 = RPA10 0011 = RPA14*
NMI	NMIR	NMIR[3:0]	0100 = RPB3* 0101 = RPB7 0110 = RPB11* 0111 = RPA1*
SERCOM0_PAD2	SCOM0P2R	SCOM0P2R[3:0]	1000 = RPA5 1001 = RPA9 1010 = RPA13*
SERCOM1_PAD1	SCOM1P1R	SCOM1P1R[3:0]	1011 = RPB2* 1100 = RPB6 1101 = RPB10*
SERCOM2_PAD0	SCOM2P0R	SCOM2P0R[3:0]	1110 = RPA8 1111 = RPA2*
SERCOM3_PAD3	SCOM3P3R	SCOM3P3R[3:0]	
QD0	QD0R	QD0R[3:0]	
TC0_WO1G4	TC0WO1G4R	TC0WO1G4R[3:0]	
TC2_WO1G4	TC2WO1G4R	TC2WO1G4R[3:0]	
TC3_WO1G4	TC3WO1G4R	TC3WO1G4R[3:0]	

5.2.7.4 Peripheral Pin Select Input Register

Name: [pin name]R
Offset: See the following Note
Reset: 0x00
Property: -

Notes:

1. For Offset address, see *Peripheral Pin Select Input Registers* table in the *I/O Ports Control Registers* from Related Links.
2. Register values can only be changed if the IOLOCK Configuration bit (CFGCON0[13]) = 0.

Bit	31	30	29	28	27	26	25	24
[27:20]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[19:12]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[11:4]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[3:0]								
Access	R	R	R	R	R/W-0	R/W-0	R/W-0	R/W-0
Reset	0	0	0	0	0	0	0	0

Bits 31:4 – [27:0]

Unimplemented: Read as '0'

Bits 3:0 – [pin name]R[3:0] Peripheral Pin Select Input bits

Where [pin name] refers to the pins that are used to configure peripheral input mapping. See *Input Pin Selection Group 1*, *Input Pin Selection Group 2*, *Input Pin Selection Group 3*, and *Input Pin Selection Group 4* tables in the *Remappable Input Example* for input pin selection values from Related Links.

Note: This field is only writable, when CFGCON0.IOLOCK = 0.

Related Links

[5.2.7.3. Remappable Input Example](#)

[5.4. I/O Ports Control Registers](#)

5.2.8 Output Mapping

The remappable pin output assigns a peripheral output function to an output pin. Once the group for the output pin is identified, see the following table which shows peripheral output functions and its group.

Each remappable output can be programmed to an output function that is from its same output group number. As an example, if RPA0 is part of GROUP2, then it can be programmed to have any GROUP2 output function on its pin. Therefore, for a given output peripheral signal, the user must first choose which remappable pin to use, choose a Group number for that pin, and then program the control registers for that pin. For example, RPA<0-10, 13, 14> G<1, 2, 3, 4> R or RPB<0-13> G<1, 2, 3, 4>R. See *Remappable Output Pin Configuration – Group1*, *Remappable Output Pin Configuration – Group2*, *Remappable Output Pin Configuration – Group3*, and *Remappable Output Pin Configuration – Group4* tables in the *Pin Output RP Registers* from Related Links.

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The rules for which group belong to which pin must be followed, such that multiple peripherals are not driving the same pin from different groups. For instance, pin RPA0 (PA0) as an output belongs to Group2 and Group3. If the peripheral driving the signal to RPA0 is coming from Group2, the software must ensure that all Group3 signals for RPA0 are disabled with an 'OFF' value in the corresponding RPA0G3R control register.

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins, by default.

Table 5-6. PPS Output Groups

Group1	Group2	Group3	Group4
SERCOM0_PAD3	SERCOM0_PAD0	SERCOM0_PAD1	SERCOM0_PAD2
SERCOM0_PAD2	SERCOM0_PAD3	SERCOM0_PAD0	SERCOM0_PAD1
SERCOM0_PAD1	SERCOM0_PAD2	SERCOM0_PAD3	SERCOM0_PAD0
SERCOM1_PAD0	SERCOM1_PAD1	SERCOM1_PAD2	SERCOM1_PAD3
SERCOM1_PAD2	SERCOM1_PAD3	SERCOM1_PAD0	SERCOM1_PAD1
SERCOM1_PAD1	SERCOM1_PAD2	SERCOM1_PAD3	SERCOM1_PAD0
SERCOM2_PAD0	SERCOM2_PAD1	SERCOM2_PAD2	SERCOM2_PAD3
SERCOM2_PAD1	SERCOM2_PAD2	SERCOM2_PAD3	SERCOM2_PAD0
SERCOM3_PAD0	SERCOM3_PAD1	SERCOM3_PAD2	SERCOM3_PAD3
SERCOM3_PAD3	SERCOM3_PAD0	SERCOM3_PAD1	SERCOM3_PAD2
TCC0_WO0	TCC0_WO1	TCC0_WO2	TCC0_WO3
TCC0_WO4	TCC0_WO5	TCC0_WO0	TCC0_WO1
TCC0_WO2	TCC0_WO3	TCC0_WO4	TCC0_WO5
TCC1_WO0	TCC1_WO1	TCC1_WO2	TCC1_WO3
TCC1_WO4	TCC1_WO5	TCC1_WO0	TCC1_WO1
TCC1_WO2	TCC1_WO3	TCC1_WO4	TCC1_WO5
TCC2_WO0	TCC2_WO1	TCC2_WO0	TCC2_WO1
TC0_WO1	TC0_WO1	TC0_WO0	TC0_WO0
REF01	REF02	REF03	REF04
TC1_WO0	TC1_WO1	TC1_WO0	TC1_WO1
TC2_WO0	TC2_WO1	TC2_WO0	TC2_WO1
TC3_WO0	TC3_WO1	TC3_WO0	TC3_WO1
QSPI_SCK	QSPI_SCK	QSPI_SCK	QSPI_SCK
QSPI_CS	QSPI_CS	QSPI_CS	QSPI_CS
QSPI_DATA3	QSPI_DATA0	QSPI_DATA1	QSPI_DATA2
QSPI_DATA2	QSPI_DATA3	QSPI_DATA0	QSPI_DATA1
QSPI_DATA1	QSPI_DATA2	QSPI_DATA3	QSPI_DATA0
CCL_OUT0	CCL_OUT1	CCL_OUT0	CCL_OUT1

Related Links

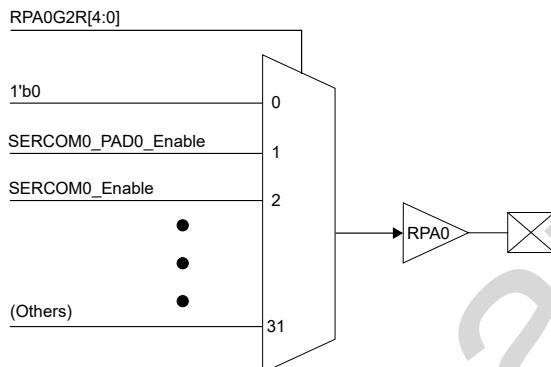
5.2.9. Pin Output RP Registers

5.2.9 Pin Output RP Registers

Register *RPnR* shows the RP Remap Register format for output functions. See *RPnR* from Related Links. Each RP pin has a 4-bit field that can be assigned to the desired output function. See the following tables for a complete list of output function values and its associated register names.

The mapping is dynamic, therefore in order to avoid glitching outputs, the user must ensure to turn off the appropriate peripherals before remapping the functions. Since on Reset, all inputs are mapped to a default value and all outputs are disabled, the mapping must be performed after any device Reset.

Figure 5-3. Example Multiplexing of Remappable Output Signal for RPA0 (Map Output Function to Pin)



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Table 5-7. Remappable Output Pin Configuration – Group1

Output Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
RPA2*	RPA2G1R*	RPA2G1R[4:0]	00000 = OFF
RPA3	RPA3G1R	RPA3G1R[4:0]	00001 = SERCOM0_PAD3
RPA5	RPA5G1R	RPA5G1R[4:0]	00010 = SERCOM0_PAD2
RPA6	RPA6G1R	RPA6G1R[4:0]	00011 = SERCOM0_PAD1
RPA7	RPA7G1R	RPA7G1R[4:0]	00100 = SERCOM1_PAD0
RPA9	RPA9G1R	RPA9G1R[4:0]	00101 = SERCOM1_PAD2
RPA10	RPA10G1R	RPA10G1R[4:0]	00110 = SERCOM1_PAD1
RPA14*	RPA14G1R*	RPA14G1R[4:0]	00111 = SERCOM2_PAD0
RPB0*	RPB0G1R*	RPB0G1R[4:0]	01000 = SERCOM2_PAD1
RPB3*	RPB3G1R*	RPB3G1R[4:0]	01001 = SERCOM3_PAD0
RPB4	RPB4G1R	RPB4G1R[4:0]	01010 = SERCOM3_PAD3
RPB7	RPB7G1R	RPB7G1R[4:0]	01011 = TCC0_WO0
RPB8	RPB8G1R	RPB8G1R[4:0]	01100 = TCC0_WO4
RPB11*	RPB11G1R*	RPB11G1R[4:0]	01101 = TCC1_WO2
RPB12*	RPB12G1R*	RPB12G1R[4:0]	01110 = TCC1_WO0
			01111 = TCC1_WO4
			10000 = TCC1_WO2
			10001 = TCC2_WO0
			10010 = TC0_WO1
			10011 = REFO1
			10100 = TC1_WO0
			10101 = TC2_WO0
			10110 = TC3_WO0
			10111 = QSCK
			11000 = QCS
			11001 = QD3
			11010 = QD2
			11011 = QD1
			11100 = CCLOUT0
			11101 = RESERVED
			11110 = RESERVED
			11111 = RESERVED

Note: * denotes that these pins and its associated registers are not available in the 32-pin package.

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Table 5-8. Remappable Output Pin Configuration – Group2

Output Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
RPA0*	RPA0G2R*	RPA0G2R[4:0]	00000 = OFF 00001 = SERCOM0_PAD0
RPA3	RPA3G2R	RPA3G2R[4:0]	00010 = SERCOM0_PAD3
RPA4	RPA4G2R	RPA4G2R[4:0]	00011 = SERCOM0_PAD2
RPA6	RPA6G2R	RPA6G2R[4:0]	00100 = SERCOM1_PAD1
RPA7	RPA7G2R	RPA7G2R[4:0]	00101 = SERCOM1_PAD3
RPA8	RPA8G2R	RPA8G2R[4:0]	00110 = SERCOM1_PAD2
RPB0*	RPB0G2R*	RPB0G2R[4:0]	00111 = SERCOM2_PAD1
RPB1*	RPB1G2R*	RPB1G2R[4:0]	01000 = SERCOM2_PAD2
RPB4	RPB4G2R	RPB4G2R[4:0]	01001 = SERCOM3_PAD1
RPB5	RPB5G2R	RPB5G2R[4:0]	01010 = SERCOM3_PAD0
RPB8	RPB8G2R	RPB8G2R[4:0]	01011 = TCC0_WO1
RPB9	RPB9G2R	RPB9G2R[4:0]	01100 = TCC0_WO5
RPB12*	RPB12G2R*	RPB12G2R[4:0]	01101 = TCC0_WO3
RPB13*	RPB13G2R*	RPB13G2R[4:0]	01110 = TCC1_WO1 01111 = TCC1_WO5 10000 = TCC1_WO3 10001 = TCC2_WO1 10010 = TC0_WO1 10011 = REFO2 10100 = TC1_WO1 10101 = TC2_WO1 10110 = TC3_WO1 10111 = QSCK 11000 = QCS 11001 = QD0 11010 = QD3 11011 = QD2 11100 = CCLOUT1 11101 = RESERVED 11110 = RESERVED 11111 = RESERVED

Note: * denotes that these pins and its associated registers are not available in the 32-pin package.

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Table 5-9. Remappable Output Pin Configuration - Group3

Output Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
RPA0*	RPA0G3R*	RPA0G3R[4:0]	00000 = OFF
RPA1*	RPA1G3R*	RPA1G3R[4:0]	00001 = SERCOM0_PAD1
RPA3	RPA3G3R	RPA3G3R[4:0]	00010 = SERCOM0_PAD0
RPA4	RPA4G3R	RPA4G3R[4:0]	00011 = SERCOM0_PAD3
RPA5	RPA5G3R	RPA5G3R[4:0]	00100 = SERCOM1_PAD2
RPA8	RPA8G3R	RPA8G3R[4:0]	00101 = SERCOM1_PAD3
RPA9	RPA9G3R	RPA9G3R[4:0]	00111 = SERCOM2_PAD2
RPA13*	RPA13G3R*	RPA13G3R[4:0]	01000 = SERCOM2_PAD3
RPB1*	RPB1G3R*	RPB1GX3R[4:0]	01001 = SERCOM3_PAD2
RPB2*	RPB2G3R*	RPB2G3R[4:0]	01010 = SERCOM3_PAD1
RPB5	RPB5G3R	RPB5G3R[4:0]	01011 = TCC0_WO2
RPB6	RPB6G3R	RPB6G3R[4:0]	01100 = TCC0_WO0
RPB9	RPB9G3R	RPB9G3R[4:0]	01101 = TCC0_WO4
RPB10*	RPB10G3R*	RPB10G3R[4:0]	01110 = TCC1_WO2
RPB13*	RPB13G3R*	RPB13G3R[4:0]	01111 = TCC1_WO0 10000 = TCC1_WO4 10001 = TCC2_WO0 10010 = TC0_WO0 10011 = REFO3 10100 = TC1_WO0 10101 = TC2_WO0 10110 = TC3_WO0 10111 = QSCK 11000 = QCS 11001 = QD1 11010 = QD0 11011 = QD3 11100 = CCLOUT0 11101 = RESERVED 11110 = RESERVED 11111 = RESERVED

Note: * denotes that these pins and its associated registers are not available in the 32-pin package.

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Table 5-10. Remappable Output Pin Configuration – Group4

Output Pin	[pin name]R SFR	[pin name]R Value to RPn Pin Selection
RPA1*	RPA1G4R*	00000 = OFF 00001 = SERCOM0_PAD2
RPA2	RPA2G4R	00010 = SERCOM0_PAD1
RPA4	RPA4G4R	00011 = SERCOM0_PAD0
RPA5	RPA5G4R	00100 = SERCOM1_PAD3
RPA6	RPA6G4R	00101 = SERCOM1_PAD1
RPA8	RPA8G4R	00110 = SERCOM1_PAD0
RPA9	RPA9G4R	00111 = SERCOM2_PAD3
RPA10	RPA10G4R	01000 = SERCOM2_PAD0
RPA13*	RPA13G4R*	01001 = SERCOM3_PAD3
RPA14*	RPA14G4R*	01010 = SERCOM3_PAD2
RPB2*	RPB2G4R*	01011 = TCC0_WO3
RPB3*	RPB3G4R*	01100 = TCC0_WO1
RPB6	RPB6G4R	01101 = TCC0_WO5
RPB7	RPB7G4R	01110 = TCC1_WO3
RPB10*	RPB10G4R*	01111 = TCC1_WO1 10000 = TCC1_WO5
RPB11*	RPB11G4R*	10001 = TCC2_WO1 10010 = TC0_WO0 10011 = REFO4 10100 = TC1_WO1 10101 = TC2_WO1 10110 = TC3_WO1 10111 = QSCK 11000 = QCS 11001 = QD2 11010 = QD1 11011 = QD0 11100 = CCLOUT1 11101 = RESERVED 11110 = RESERVED 11111 = RESERVED

Note: * denotes that these pins and its associated registers are not available in the 32-pin package.

Related Links

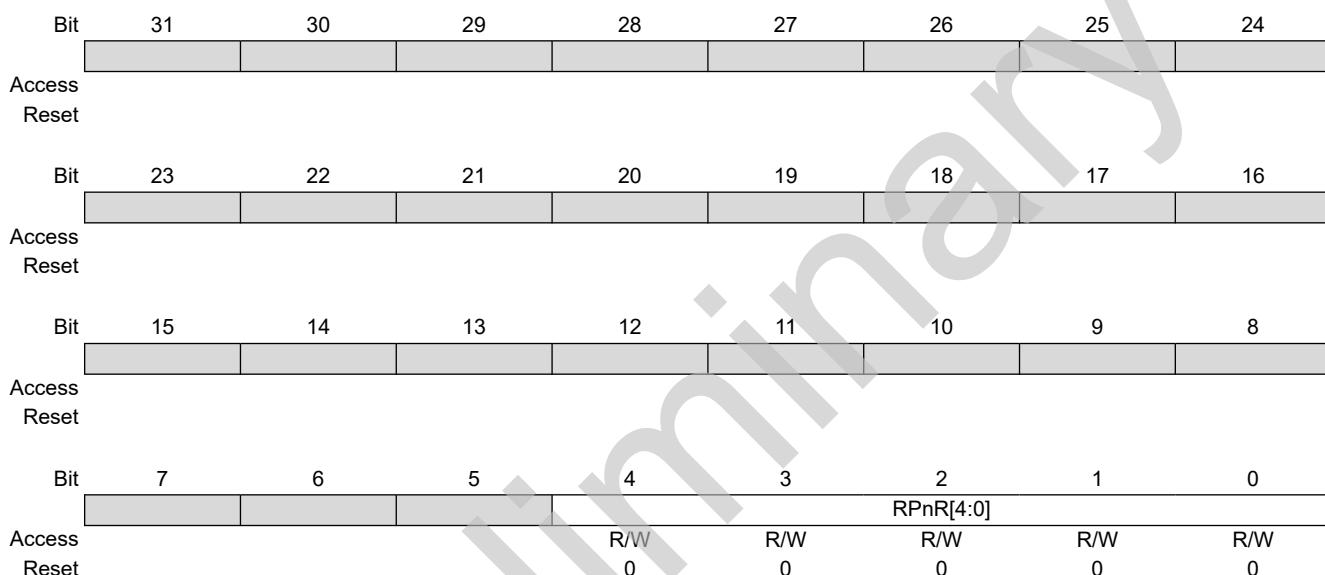
5.2.9.1. RPnR

5.2.9.1 Peripheral Pin Select Output Register

Name: RPnR
Offset: See the following Note
Reset: 0x0
Property: -

Notes:

1. For Offset address, see *Peripheral Pin Select Output Registers* table in the *I/O Ports Control Registers* from Related Links.
2. Register values can only be changed if the IOLOCK Configuration bit (CFGCON0[13]) = 0.
3. RPn can have values of RPA0...RPA10, RPA13, RPA14, RPB0...RPB13 some values are not valid for 32-pin devices.



Bits 4:0 – RPnR[4:0] Peripheral Pin Select Output Register

Output bits. For output pin selection values, see *Remappable Output Pin Configuration – Group1*, *Remappable Output Pin Configuration – Group2*, *Remappable Output Pin Configuration – Group3*, and *Remappable Output Pin Configuration – Group4* tables in the *Pin Output RP Registers* from Related Links.

Note: This field is only writable, when CFGCON0.IOLOCK = 0.

Related Links

[5.4. I/O Ports Control Registers](#)

[5.2.9. Pin Output RP Registers](#)

5.3 Function Priority for Device Pins

The device pins have an associated priority order in which functionality is exhibited on each pin. This priority order impacts the availability of PPS functionality. For example, if SERCOM0 is enabled with outputs chosen to be High Speed mode in the DEVCFG1 fuses (bit 17), pins PA3, PA4, PA5, and PA6 are given priority to be used as SERCOM0 pins instead of GPIO/PPS pins. See the following tables for the priority in which functions are brought out on each device pin.

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Table 5-11. Priority for Device Pins PA_n (n=0-14)

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pa0*	QSPI_DATA2	QSPI	4	N/A	I/O	DIG/ST
	RTC_IN3	RTC			I	ST/STMV
	RPA0	PPS			I/O	DIG/ST
	IOCA0	Change Notification			I	ST
	RA0	GPIO			I/O	DIG/ST
pa1*	QSPI_DATA3	QSPI	5	N/A	I/O	DIG/ST
	AC_CMP1	Analog Comparator			O	DIG
	RTC_IN2	RTC			I	ST/STMV
	RPA1	PPS			I/O	DIG/ST
	IOCA1	Change Notification			I	ST
	RA1	GPIO			I/O	DIG/ST
pa2*	AC_CMP0	Analog Comparator	6	N/A	O	DIG
	RTC_IN1	RTC			I	ST/STMV
	RPA2	PPS			I/O	DIG/ST
	IOCA2	Change Notification			I	ST
	RA2	GPIO			I/O	DIG/ST
pa3	SCLKI	Secondary Oscillator - Digital	47	30	I	ST/STMV
	SERCOM0_PAD2	SERCOM0			I/O	DIG/ST
	RTC_IN0	RTC			I	ST/STMV
	RPA3	PPS			I/O	DIG/ST
	IOCA3	Change Notification			I	ST
	RA3	GPIO			I/O	DIG/ST
pa4	SERCOM0_PAD3	SERCOM0	42	29	I/O	DIG/ST
	RTC_OUT	RTC			O	DIGMV
	RPA4	PPS			I/O	DIG/ST
	IOCA4	Change Notification			I	ST
	RA4	GPIO			I/O	DIG/ST
pa5	SERCOM0_PAD0	SERCOM0	7	3	I/O	DIG/ST/I2C/SMB
	RPA5	PPS			I/O	DIG/ST
	IOCA5	Change Notification			I	ST
	RA5	GPIO			I/O	DIG/ST

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I/O Ports and Peripheral Pin Select (PPS)

.....continued

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pa6	PGC2ENTRY	DEBUG	9	5	I	ST
	SERCOM0_PAD1	SERCOM0			I/O	DIG/ST/I2C/SMB
	AC_CMP1_ALT	Analog Comparator			O	DIG
	RPA6	PPS			I/O	DIG/ST
	IOCA6	Change Notification			I	ST
	RA6	GPIO			I/O	DIG/ST
pa7	TRACECLK	DEBUG	10	6	I	DIG
	SERCOM1_PAD0	SERCOM1			I/O	DIG/ST/I2C/SMB
	RPA7	PPS			I/O	DIG/ST
	IOCA7	Change Notification			I	ST
	RA7	GPIO			I/O	DIG/ST
pa8	PGD2ENTRY	DEBUG	11	7	I	ST
	FECTRL0	RF Radio			O	DIG
	SERCOM1_PAD1	SERCOM1			I/O	DIG/ST/I2C/SMB
	RPA8	PPS			I/O	DIG/ST
	IOCA8	Change Notification			I	ST
	RA8	GPIO			I/O	DIG/ST
pa9	FECTRL1	RF Radio	12	8	O	DIG
	SERCOM1_PAD2	SERCOM1			I/O	DIG/ST
	RTC_IN0_ALT	RTC			I	ST/STMV
	RPA9	PPS			I/O	DIG/ST
	IOCA9	Change Notification			I	ST
	RA9	GPIO			I/O	DIG/ST
pa10	FECTRL2	RF Radio	13	9	O	DIG
	SERCOM1_PAD3	SERCOM1			I/O	DIG/ST
	RTC_OUT_ALT	RTC			O	DIGMV
	RPA10	PPS			I/O	DIG/ST
	IOCA10	Change Notification			I	ST
	RA10	GPIO			I/O	DIG/ST
pa11	SOSCI	Secondary Oscillator	45	29**	-	-
pa12	SOSCO	Secondary Oscillator	46	30**	-	-

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I/O Ports and Peripheral Pin Select (PPS)

.....continued

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pa13*	COEXCTRL0	RF Radio	16	N/A	I/O	DIG/ST
	SERCOM2_PAD0	SERCOM2			I/O	DIG/ST/I2C/SMB
	RPA13	PPS			I/O	DIG/ST
	IOCA13	Change Notification			I	ST
	RA13	GPIO			I/O	DIG/ST
pa14*	COEXCTRL1	RF Radio	17	N/A	I/O	DIG/ST
	SERCOM2_PAD1	SERCOM2			I/O	DIG/ST/I2C/SMB
	RPA14	PPS			I/O	DIG/ST
	IOCA14	Change Notification			I	ST
	RA14	GPIO			I/O	DIG/ST

1. * indicates pins not available on 32-pin package, only on 48-pin package
2. ** Pins 29 and 30 are double bonded with other I/O pins on the 32-pin package

Table 5-12. Priority for Device Pins PBn (n=0-13)

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pb0*	COEXCTRL2	RF Radio	30	20	I/O	DIG/ST
	AN4	ADC			I	ANALOG
	AC_AIN2	Analog Comparator			I	ANALOG
	RPB0	PPS			I/O	DIG/ST
	IOCB0	Change Notification			I	ST
	RB0	GPIO			I/O	DIG/ST
pb1*	AN5	ADC	31	21	I	ANALOG
	AC_AIN3	Analog Comparator			I	ANALOG
	RPB1	PPS			I/O	DIG/ST
	IOCB1	Change Notification			I	ST
	RB1	GPIO			I/O	DIG/ST
pb2*	AN6	ADC	32	N/A	I	ANALOG
	AC_AIN0	Analog Comparator			I	ANALOG
	RPB2	PPS			I/O	DIG/ST
	IOCB2	Change Notification			I	ST
	RB2	GPIO			I/O	DIG/ST

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I/O Ports and Peripheral Pin Select (PPS)

.....continued

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pb3*	AN7	ADC	33	N/A	I	ANALOG
	AC_AIN1	Analog Comparator			I	ANALOG
	RPB3	PPS			I/O	DIG/ST
	IOCB3	Change Notification			I	ST
	RB3	GPIO			I/O	DIG/ST
pb4	PGC1ENTRY	Debug	34	22	I	ST
	FECTRL3	RF Radio			O	DIG
	AN0	ADC			I	ANALOG
	TP4	DO NOT USE			-	-
	RPB4	PPS			I/O	DIG/ST
	INT0	Edge Interrupt			I	ST/STMV
	IOCB4	Change Notification			I	ST
	RB4	GPIO			I/O	DIG/ST
pb5	PGC4ENTRY	Debug	35	23	I	ST
	TRACEDAT0	Debug			O	DIG
	FECTRL4	RF Radio			O	DIG
	AN1	ADC			I	ANALOG
	TP5	DO NOT USE			-	-
	RPB5	PPS			I/O	DIG/ST
	IOCB5	Change Notification			I	ST
	RB5	GPIO			I/O	DIG/ST
pb6	PGD1ENTRY	Debug	37	25	I	ST
	TRACEDAT1	Debug			O	DIG
	FECTRL5	RF Radio			O	DIG
	AN2	ADC			I	ANALOG
	ANNO	ADC (Differential)			I	ANALOG
	RPB6	PPS			I/O	DIG/ST
	IOCB6	Change Notification			I	ST
	RB6	GPIO			I/O	DIG/ST

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

.....continued

Pin Name ⁽¹⁾	Functions in Priority Order	Reference Peripheral	Pin Number (48-pin)	Pin Number (32A-pin)	I/O	Type
pb7	PGD4ENTRY	Debug	38	26	I	ST
	CM4_SWO	Debug			O	DIG
	TRACEDAT2	Debug			O	DIG
	AN3	ADC			I	ANALOG
	LVDIN	LVD Voltage Reference			I	ANALOG
	RPB7	PPS			I/O	DIG/ST
	IOCB7	Change Notification			I	ST
	RB7	GPIO			I/O	DIG/ST
pb8	CM4_SWCLK	DEBUG	41	28	I	ST
	RPB8	PPS			I/O	DIG/ST
	IOCB8	Change Notification			I	ST
	RB8	GPIO			I/O	DIG/ST
pb9	CM4_SWDIO	DEBUG	40	27	I/O	DIG/ST
	RPB9	PPS			I/O	DIG/ST
	IOCB9	Change Notification			I	ST
	RB9	GPIO			I/O	DIG/ST
pb10*	QSPI_CS	QSPI	43	N/A	O	DIG
	RPB10	PPS			I/O	DIG/ST
	IOCB10	Change Notification			I	ST
	RB10	GPIO			I/O	DIG/ST
pb11*	QSPI_SCK	QSPI	44	N/A	I/O	DIG/ST
	RPB11	PPS			I/O	DIG/ST
	IOCB11	Change Notification			I	ST
	RB11	GPIO			I/O	DIG/ST
pb12*	QSPI_DATA0	QSPI	14	N/A	I/O	DIG/ST
	RPB12	PPS			I/O	DIG/ST
	IOCB12	Change Notification			I	ST
	RB12	GPIO			I/O	DIG/ST
pb13*	QSPI_DATA1	QSPI	15	N/A	I/O	DIG/ST
	RTC_EVENT	RTC			O	DIGMV
	RPB13	PPS			I/O	DIG/ST
	IOCB13	Change Notification			I	ST
	RB13	GPIO			I/O	DIG/ST

1. * indicates pins not available on 32-pin package UNLESS OTHERWISE NOTED.

5.4 I/O Ports Control Registers

Notes: Following conventions are used in the following tables:

- x = Unknown value on Reset.
- — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Preliminary

Table 5-13. PortA Register Map

	Register	Bit Range	Bits																	AI Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	TRISA14	TRISA13	TRISA12*	TRISA11*	TRISA10	TRISA9	TRISA8	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	0000	
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	RA14	RA13	RA12*	RA11*	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0000	
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	LATA14	LATA13	LATA12*	LATA11*	LATA10	LATA9	LATA8	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	0000	
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	ODCA14	ODCA13	—	—	ODCA10	ODCA9	ODCA8	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000	
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CNPUA14	CNPUA13	—	—	CNPUA10	CNPUA9	CNPUA8	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000	
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CNPDA14	CNPDA13	—	—	CNPDA10	CNPDA9	CNPDA8	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000	
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	FRZ	SIDL	—	EDGEDETECT	—	—	—	—	—	—	—	—	—	—	—	0000	
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CNENA14	CNENA13	—	—	CNENA10	CNENA9	CNENA8	CNENA7	CNENA6	CNENA5	CNENA4	CNENA3	CNENA2	CNENA1	CNENA0	0000	
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CN STATA14	CN STATA13	CN STATA12	CN STATA11	CN STATA10	CN STATA9	CN STATA8	CN STATA7	CN STATA6	CN STATA5	CN STATA4	CN STATA3	CN STATA2	CN STATA1	CN STATA0	0000	
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CNNEA14	CNNEA13	—	—	CNNEA10	CNNEA9	CNNEA8	CNNEA7	CNNEA6	CNNEA5	CNNEA4	CNNEA3	CNNEA2	CNNEA1	CNNEA0	0000	
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	CNFA14	CNFA13	—	—	CNFA10	CNFA9	CNFA9	CNFA7	CNFA7	CNFA6	CNFA5	CNFA4	CNFA3	CNFA2	CNFA1	CNFA0	0000

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

.....continued		Virtual Address (0x4400_2200)	Register	Bit Range	Bits																All Resets
31/15	30/14				29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	SR014	SR013	—	—	SR010	SR09	SR08	SR07	SR06	SR05	SR04	SR03	—	SR01	SR00	0000		
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	SR114	SR113	—	—	SR110	SR19	SR18	SR17	SR16	SR15	SR14	SR13	—	SR11	SR10	0000		

PIC32CX-BZ2 and WBZ45 Family I/O Ports and Peripheral Pin Select (PPS)

-
1. All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR*, *SET*, and *INV Registers* from Related Links.

Note:

* - For 32A(PIC32CX1012BZ24032) device only.

Preliminary

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

Table 5-14. PortB Register Map

Virtual Address (0x4400-2300)	Register	Bit Range	Bits																AI Presets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFFF
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	0000
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	0000
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	FRZ	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	0000	
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNENB13	CNENB12	CNENB11	CNENB10	CNENB9	CNENB8	CNENB7	CNENB6	CNENB5	CNENB4	CNENB3	CNENB2	CNENB1	CNENB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNSTATB13	CNSTATB12	CNSTATB11	CNSTATB10	CNSTATB9	CNSTATB8	CNSTATB7	CNSTATB6	CNSTATB5	CNSTATB4	CNSTATB3	CNSTATB2	CNSTATB1	CNSTATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

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.....continued		Virtual Address (0x400-2300)	Register	Bit Range	Bits																All Resets
31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0						
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	—	0000	
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	SR013	SR012	SR011	SR010	—	—	—	—	—	—	—	—	—	—	—	0000	
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	SR113	SR112	SR111	SR110	—	—	—	—	—	—	—	—	—	—	—	0000	

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

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1. All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Notes: Following conventions are used in the following tables:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

Preliminary

Table 5-15. Peripheral Pin Select Input Registers

Virtual Address (4400 - 1000) (1)	Register Name	Bit Range	Bits																AI Presets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000h	EXTINT0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTINT0R[3:0]	0000		
0004h	EXTINT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTINT1R[3:0]	0000	
0008h	EXTINT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTINT2R[3:0]	0000	
000Ch	EXTINT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTINT3R[3:0]	0000	
003Ch	NMIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NMIR[3:0]	0000	
0040h	SCOM0P0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM0P0R[3:0]	0000	
0044h	SCOM0P1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM0P1R[3:0]	0000	
0048h	SCOM0P2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM0P2R[3:0]	0000	
004Ch	SCOM0P3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM0P3R[3:0]	0000	
0050h	SCOM1P0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM1P0R[3:0]	0000	
0054h	SCOM1P1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM1P1R[3:0]	0000	
0058h	SCOM1P2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM1P2R[3:0]	0000	

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Virtual Address (4400_1000) (1)continued	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
005Ch	SCOM1P3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM1P3R[3:0]	0000
0060h	SCOM2P0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM2P0R[3:0]	0000
0064h	SCOM2P1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM2P1R[3:0]	0000
0068h	SCOM2P2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM2P2R[3:0]	0000
006Ch	SCOM2P3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM2P3R[3:0]	0000
0070h	SCOM3P0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM3P0R[3:0]	0000
0074h	SCOM3P1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM3P1R[3:0]	0000
0078h	SCOM3P2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM3P2R[3:0]	0000
007Ch	SCOM3P3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCOM3P3R[3:0]	0000
0080h	QSCKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QSCKR[3:0]	0000
0084h	QD0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QD0R[3:0]	0000
0088h	QD1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QD1R[3:0]	0000

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Virtual Address (4400_1000) (1)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
008Ch	QD2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QD2R[3:0]	0000
0090h	QD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QD3R[3:0]	0000
0094h	REFIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REFIR[3:0]	0000
0098h	CCLIN0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN0R[3:0]	0000
009Ch	CCLIN1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN1R[3:0]	0000
00A0h	CCLIN2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN2R[3:0]	0000
00A4h	CCLIN3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN3R[3:0]	0000
00A8h	CCLIN4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN4R[3:0]	0000
00ACh	CCLIN5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCLIN5R[3:0]	0000
00B0h	TC0WO0G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TC0WO0G1R[3:0]	0000
00B4h	TC0WO0G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TC0WO0G2R[3:0]	0000
00B8h	TC0WO1G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TC0WO1G3R[3:0]	0000

.....continued

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

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Virtual Address (4400_1000) (1)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00BCh	TC0WO1G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC0WO1G4R[3:0]	—	0000		
00C0h	TC1WO0G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC1WO0G1R[3:0]	—	0000		
00C4h	TC1WO1G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC1WO0G2R[3:0]	—	0000		
00C8h	TC2WO0G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC2WO0G1R[3:0]	—	0000		
00CCh	TC2WO0G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC2WO0G3R[3:0]	—	0000		
00D0h	TC2WO1G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC2WO1G2R[3:0]	—	0000		
00D4h	TC2WO1G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC2WO1G4R [3:0]	—	0000		
00D8h	TC3WO0G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC3WO0G1R [3:0]	—	0000		
00DCh	TC3WO0G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC3WO0G3R[3:0]	—	0000		
00E0h	TC3WO1G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC3WO1G2R [3:0]	—	0000		
00E4h	TC3WO1G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TC3WO1G4R[3:0]	—	0000		

.....continued

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

1. * These registers are not available in the 32-pin package.

Preliminary

Table 5-16. Peripheral Pin Select Output Registers

Virtual Address (4400-1000) (1)	Register Name	Bit Range	Bits																AI Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200h	RPA0G2R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA0G2R[4:0]	—	—	0000	
0204h	RPA0G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA0G3R[4:0]	—	—	0000	
0208h	RPA1G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA1G3R[4:0]	—	—	0000	
020Ch	RPA1G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA1G4R[4:0]	—	—	0000	
0210h	RPA2G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA2G1R[4:0]	—	—	0000	
0214h	RPA2G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA2G4R [4:0]	—	—	0000	
0218h	RPA3G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA3G1R[4:0]	—	—	0000	
021Ch	RPA3G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA3G2R[4:0]	—	—	0000	
0220h	RPA3G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA3G3R[4:0]	—	—	0000	
0224h	RPA4G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA4G2R[4:0]	—	—	0000	
0228h	RPA4G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA4G3R[4:0]	—	—	0000	
022Ch	RPA4G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	RPA4G4R[4:0]	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA4G4R[4:0]	—	—	0000	

PIC32CX-BZ2 and WBZ45 Family I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

Virtual Address (4400_1000) (1)continued	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0230h	RPA5G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA5G1R[4:0]	—	—	0000	
0234h	RPA5G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA5G3R[4:0]	—	—	0000	
0238h	RPA5G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA5G4R[4:0]	—	—	0000	
023Ch	RPA6G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA6G1R[4:0]	—	—	0000	
0240h	RPA6G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA6G2R[4:0]	—	—	0000	
0244h	RPA6G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA6G4R[4:0]	—	—	0000	
0248h	RPA7G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA7G1R[4:0]	—	—	0000	
024Ch	RPA7G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA7G2R[4:0]	—	—	0000	
0250h	RPA8G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA8G2R[4:0]	—	—	0000	
0254h	RPA8G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA8G3R[4:0]	—	—	0000	
0258h	RPA8G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA8G4R[4:0]	—	—	0000	
025Ch	RPA9G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA9G1R[4:0]	—	—	0000	

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

Virtual Address (4400_1000) (1)continued	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0260h	RPA9G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA9G3R[4:0]	0000		
0264h	RPA9G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA9G4R[4:0]	0000		
0268h	RPA10G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA10G1R[4:0]	0000		
026Ch	RPA10G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA10G4R[4:0]	0000		
0278h	RPA13G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA13G3R[4:0]	0000		
027Ch	RPA13G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA13G4R[4:0]	0000		
0280h	RPA14G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA14G1R[4:0]	0000		
0284h	RPA14G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPA14G4R[4:0]	0000		
028Ch	RPB0G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB0G1R[4:0]	0000		
0290h	RPB0G2R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB0G2R[4:0]	0000		
0294h	RPB1G2R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB1G2R[4:0]	0000		
0298h	RPB1G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB1G3R[4:0]	0000		

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

Virtual Address (4400_1000) (1)continued	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
029Ch	RPB2G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB2G3R[4:0]	0000
02A0h	RPB2G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB2G4R[4:0]	0000
02A4h	RPB3G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB3G1R[4:0]	0000
02A8h	RPB3G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB3G4R[4:0]	0000
02ACh	RPB4G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB4G1R[4:0]	0000
02B0h	RPB4G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB4G2R[4:0]	0000
02B4h	RPB5G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB5G2R[4:0]	0000
02B8h	RPB5G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB5G3R[4:0]	0000
02BCh	RPB6G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB6G3R[4:0]	0000
02C0h	RPB6G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB6G4R[4:0]	0000
02C4h	RPB7G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB7G1R[4:0]	0000
02C8h	RPB7G4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPB7G4R[4:0]	0000

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Draft Advance Information Datasheet

Virtual Address (4400_1000) (1)continued	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
02CCh	RPB8G1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02D0h	RPB8G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02D4h	RPB9G2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02D8h	RPB9G3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02DCh	RPB10G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02E0h	RPB10G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02E4h	RPB11G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02E8h	RPB11G4R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02EcH	RPB12G1R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02F0h	RPB12G2R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02F4h	RPB13G2R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
02F8h	RPB13G3R*	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	

PIC32CX-BZ2 and WBZ45 Family

I/O Ports and Peripheral Pin Select (PPS)

Related Links

[5.1.9. CLR, SET, and INV Registers](#)

Preliminary

5.4.1 Change Notice Control for PORTx Register

Name: CNCONx
Offset: See the following Note
Reset: 0x0
Property: -

Note:

1. For Offset address, see *PortA Register Map* and *PortB Register Map* tables in the *I/O Ports Control Registers* from Related Links.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W		R/W			
Reset	0	0	0		0			
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON Change Notice (CN) Control ON bit

- 1 = Change Notice is enabled
 0 = Change Notice is disabled

Bit 14 – FRZ Freeze in the Debug mode bit

- 1 = Freezes the module operation when the emulator is in the Debug mode
 0 = Continues the module operation when the emulator is in the Debug mode

Bit 13 – SIDL Stop in the Idle mode bit

- 1 = Discontinues the module operation when device enters the Idle mode
 0 = Continues the module operation even in the Idle mode

Bit 11 – EDGEDETECT Change Notification Style bit

- 1 = Edge Style. Detects edge transitions (CNFx used for CN Event).
 0 = Mismatch Style. Detects change from last PORTx read (CNSTATx used for CN Event).

Related Links

[5.4. I/O Ports Control Registers](#)

5.5 Operation in Power Saving Modes

5.5.1 I/O Port Operation in Sleep Mode

As the device enters the Sleep mode, the system clock is disabled; however, the CN module continues to operate. If one of the enabled CN pins changes state, the corresponding interrupt flag is set in NVIC and device wakes from the Sleep (or Idle) mode and executes the CN Interrupt Service Routine.

5.5.2 I/O Port Operation in Idle Mode

As the device enters the Idle mode, the system clock sources remain functional. The SIDL bit (CNCONx[13]) selects whether the module will stop or continues to function in the Idle mode.

- If SIDL = 1, the module continues to sample Input CN I/O pins in the Idle mode; however, synchronization is disabled.
- If SIDL = 0, the module continues to synchronize and samples input CN I/O pins in the Idle mode.

5.6 Results of Various Resets

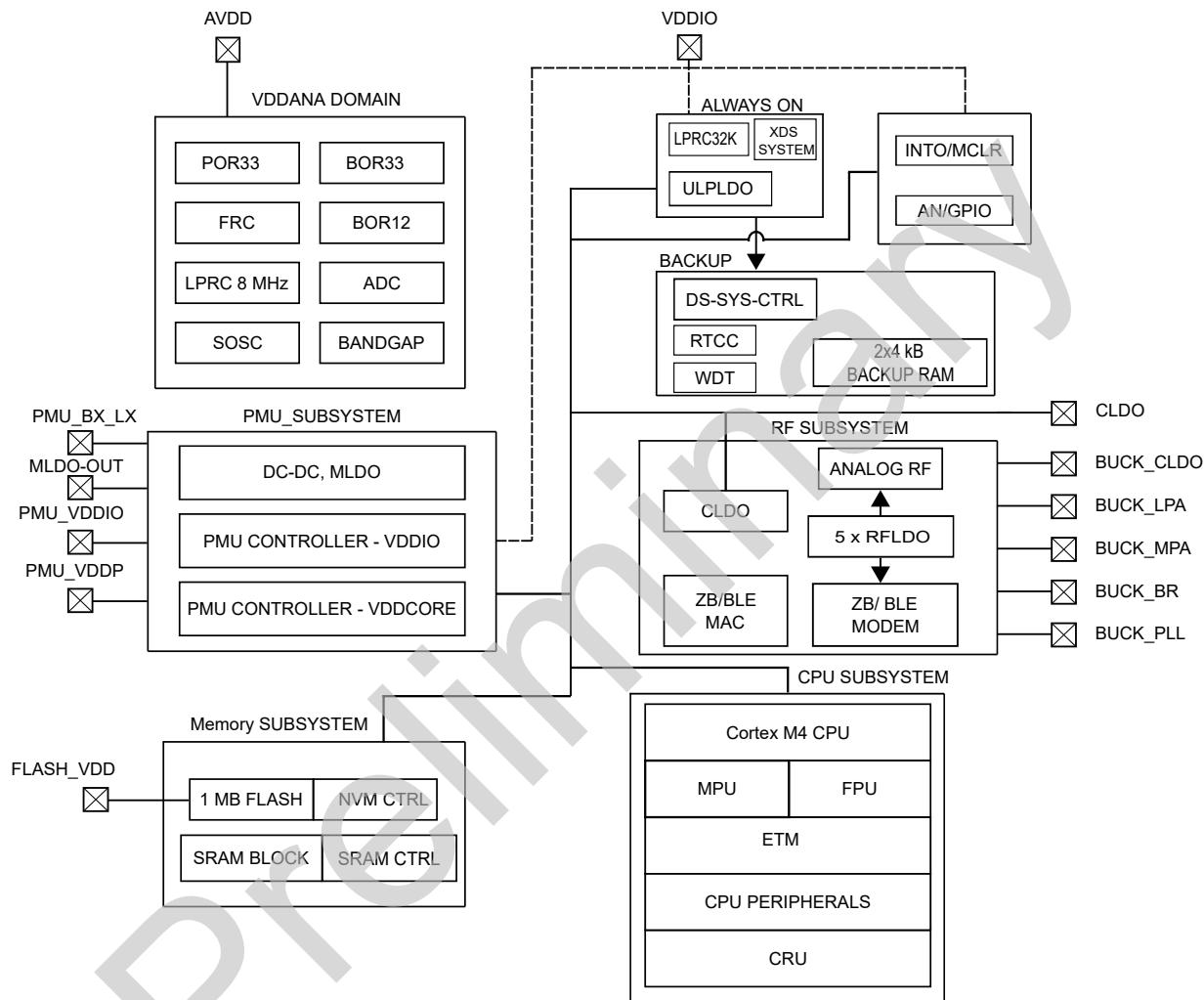
Table 5-17. Results of Resets Available

Reset Name	Description
Device Reset	All I/O registers are forced to their reset states upon a device Reset.
Power-on Reset (PoR)	All I/O registers are forced to their reset states upon a Power-on Reset (POR).
Watchdog Reset	All I/O registers are unchanged upon a Watchdog Reset.

6. Power Subsystem

6.1 Block Diagram

Figure 6-1. Power Subsystem Block Diagram



The power domains of PIC32CX-BZ2 and WBZ45 is as follows:

- VDD - 1.9V to 3.6V, Main Supply powering VDDIO, FLASH_VDD, AVDD, PMU_VDDIO, PMU_VDDP
 - VDDIO
 - 1.9V to 3.6, powering the AON, PMU-CTRL, AOnN AN/GPIO, INT0/MCLR, BKUP
 - FLASH_VDD
 - 1.9V to 3.6V, Filtered version of VDD (powering the flash)
 - AVDD
 - 1.9V to 3.6V, Filtered version of VDD for system analog functionality
 - PMU_VDDIO
 - 1.9V to 3.6V, Filtered version of VDD (powering the PMU sub-system)
 - PMU_VDDP
 - 1.9V to 3.6V, Filtered version of VDD (powering the PMU sub-system)

- GND
 - Common GND for digital, analog and RF sub-systems

Other power supply pins as follows:

- CLDO
 - Output pin for the internal voltage regulator for decoupling, this pin should not be used as an external power supply source
 - CLDO output is 1P2V
 - CLDO powers the VDDCORE
 - VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals
- PMU_BK_LX
 - Pin for connecting the inductor for the internal switching regulator
- PMU_MLDO_OUT
 - 1P35V output pin from the internal LDO. This is the shared output pin for both MLDO and the DC-DC converter
 - MLDO_OUT powers the LDO's in the BT_ZB_Subsystem (BUCK_LPA, BUCK_MPA, BUCK_PLL, BUCK_BB and BUCK_CLDO)

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

6.2 Voltage Regulators

The following voltage regulators are available in power subsystem:

- MLDO – Linear voltage regulator generating 1.35V for powering CLDO and other RF LDO's operates from 1.9V to 3.6V
- DC-DC – Switching voltage regulator generating 1.35V operates from 2.3V to 3.6V
- ULP_VREG – Ultra low power voltage regulator for operation in back-up mode
- RF LDO's – Powering the different blocks of the RF subsystem
- CLDO – Powering the VDDCORE of PIC32CX-BZ2

6.3 Power Supply Modes

The PIC32CX-BZ2 supports a single power supply from 1.9V to 3.6V. The IO supply cannot be decoupled from main supply. The same voltage must be applied to VDDx, PMU_VDDIO, VPMU_VDDC, and AVDD with different levels of filtering. The internal voltage regulator has following four different modes:

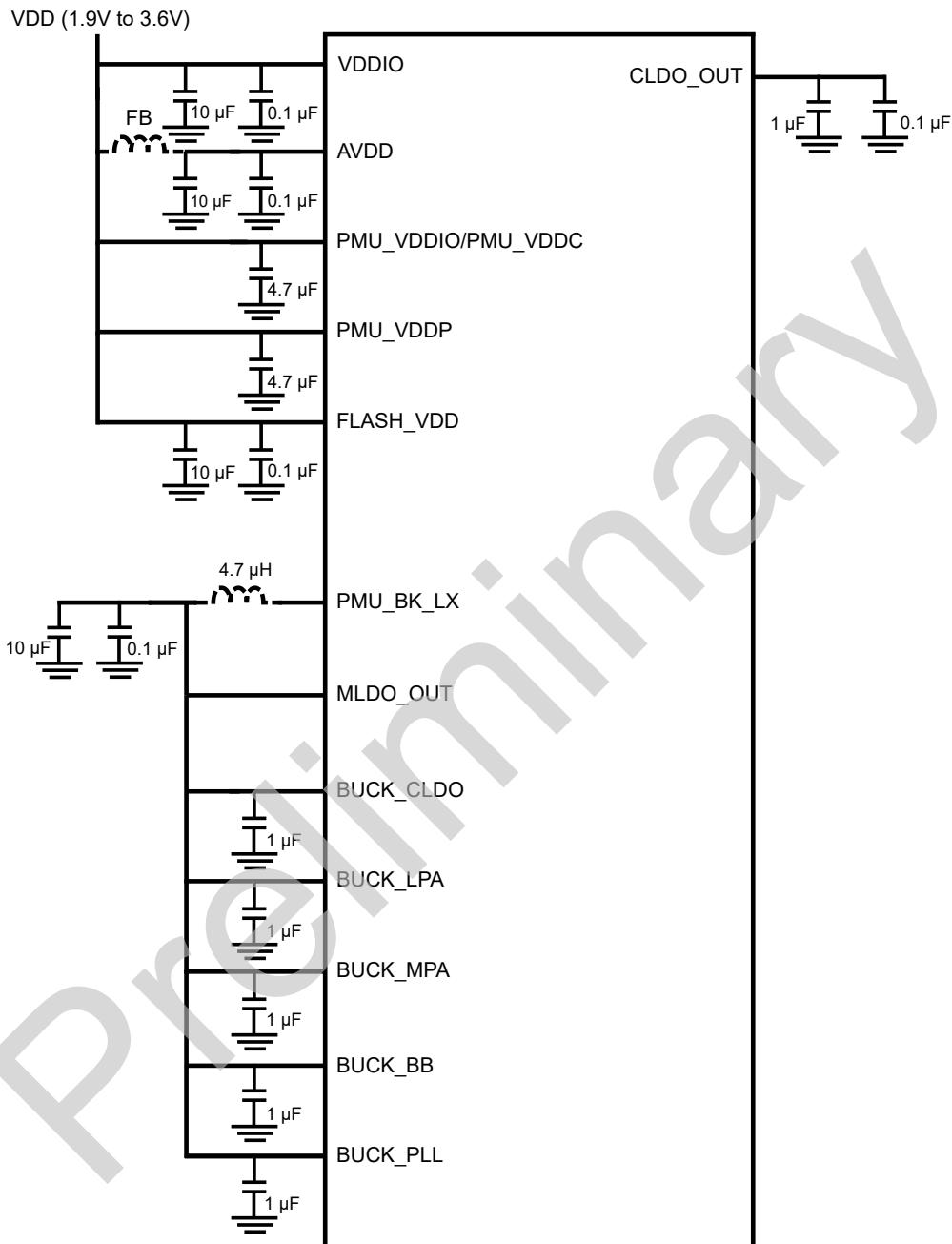
- Linear mode: This mode does not require any external inductor. This is the default mode when CPU and peripherals are running. In this mode, the SoC is powered through the MLDO mode
- Switching mode (Buck): The most efficient mode when the CPU and peripherals are running. In this mode, the SoC is powered by the DC-DC converter
- Low Power (LP) mode: This is the default mode used when the device is in Standby mode
- Shutdown mode: When the device is in Backup mode, the internal regulator is turned off

Selecting between Switching mode and Linear mode can be done by software on the fly, but the power supply must be designed according to which mode is to be used.

6.4

Typical Power Supply Connection for SoC

Figure 6-2. Typical Power Supply Connection for SoC



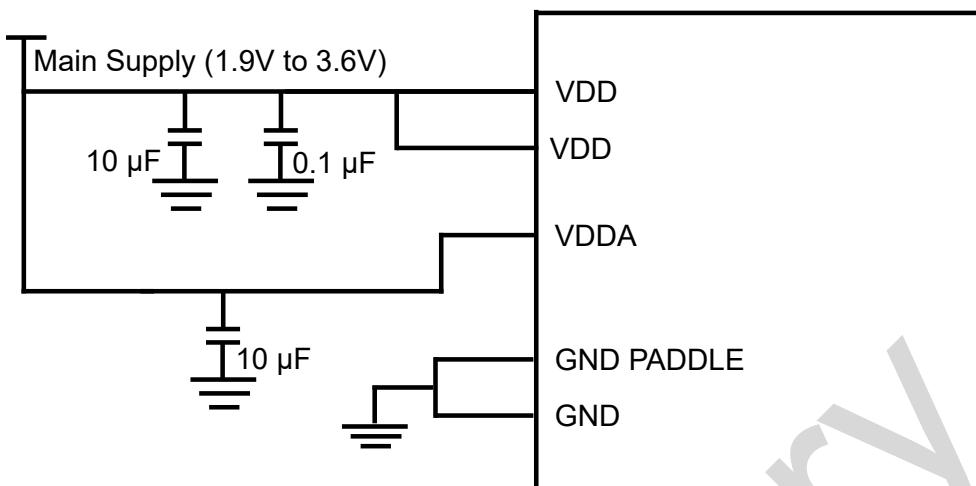
6.5

Typical Power Supply Connection for Module

The module requires only a single power supply on the VDD pins of the module.

- VDD can be from 1.9V to 3.6V for non-ECC modules

Figure 6-3. Module Schematics with VDD and Optional Bulk Capacitors



6.6 Power-Up Sequence

Characteristics of power-up sequence are as follows:

- The VDD/AVDD domains should rise at the same time
- On power-up, PIC32CX-BZ2 always start-up on the MLDO mode
- After power-up in MLDO the software can initiate the switch to Buck mode

6.6.1 Starting of Voltage Regulators

Characteristics of power-up voltage regulators are as follows:

- On power-up, the internal regulator starts in MLDO mode and gets stabilized after <<SY01 time>>
- After MLDO boots up, the CLDO initializes after a <<SY02 time>>
- Now the code execution can start
- The RF system is maintained in sleep-mode during the power-up time

6.6.2 Starting-up of Crystals

Characteristics of power-up crystals is as follows:

- The power-up of the SOC happens with the internal oscillators. After the power-up the user software can request to switch on the SOSC and the XOSC crystals.

6.6.3 BOR and POR

The Brown-out Reset (BOR) monitors the VDD supply voltage. On detection of a brown-out condition the BOR re-arms the POR. In this device the min BOR trip point is the voltage below which the IO is deemed to be un-trusted, thus it generates a reset. There are three BOR in PIC32CX-BZ2 and WBZ45:

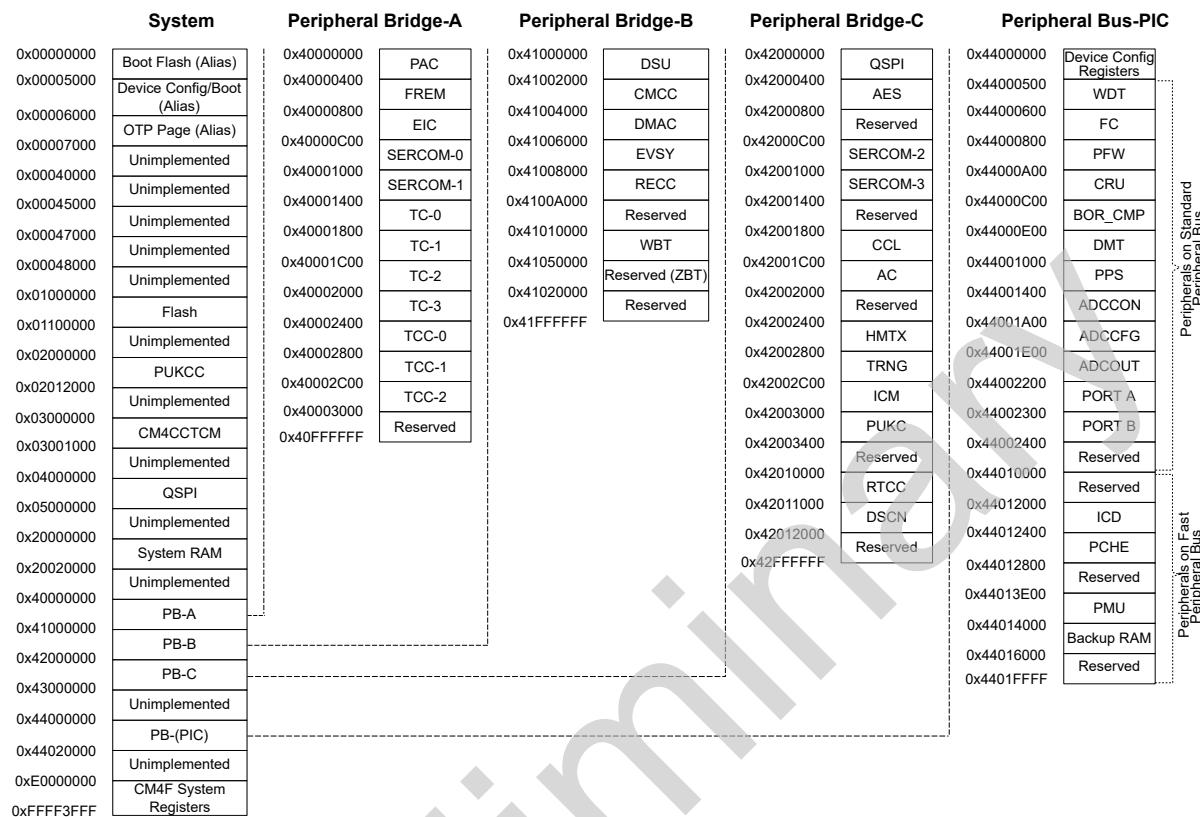
- BOR3V3 to monitor VDD
- BOR1P2 to monitor VDDCORE
- ZPBOR monitors VDD during deep sleep and extreme deep sleep mode if enabled

PIC32CX-BZ2 and WBZ45 Family

Product Memory Mapping Overview

7. Product Memory Mapping Overview

Figure 7-1. Product Mapping



Notes:

- Access attempts to any unimplemented memory location generates a bus error.
- PUKCC space is fixed as non-cacheable and bufferable.
- QSPI space "cacheable and bufferable" attribute is controlled using CFGCON1.QSCHE_EN.

PIC32CX-BZ2 and WBZ45 Family

Product Memory Mapping Overview

Table 7-1. Device Configuration Map

Register Name		Reset value from NVR memory?	Writable in User Mode?	Corresponding Write Lock Bit(s)	Purpose
SYSTEM CONFIGURATION					
CFGCON0(L)	0x4400_0000	X	X	CFGLOCK[1:0]	Misc. System Configuration
CFGCON1(L)	0x4400_0010	X	X	CFGLOCK[1:0]	Misc. System Configuration
CFGCON2(L)	0x4400_0020	X	X	CFGLOCK[1:0]	Misc. System Configuration
CFGCON3	0x4400_0030		X	CFGLOCK[1:0]	Misc. System Configuration
CFGCON4(L)	0x4400_0040	X	X	CFGLOCK[1:0]	Misc. System Configuration
CFGPGQOS	0x4400_0050		X	CFGCON0.PGLOCK	Bus Matrix Permission Groups
CFGPCLKGEN1	0x4400_0060		X	CFGLOCK[1:0]	Peripheral Clock Gen Reg-1
CFGPCLKGEN2	0x4400_0070		X	CFGLOCK[1:0]	Peripheral Clock Gen Reg-2
CFGPCLKGEN3	0x4400_0080		X	CFGLOCK[1:0]	Peripheral Clock Gen Reg-3
ID ²	0x4400_0090	X		N/A- Read Only	32-bit Device ID
USER_ID(L)	0x4400_00A0	X	X	CFGLOCK[1:0]	16-bit User ID
SYSKEY	0x4400_00B0		X	Sequence	System Lock feature
PMD1	0x4400_00C0		X	CFGCON0.PMDLOC K	Peripheral Module Disable
PMD2	0x4400_00D0		X	CFGCON0.PMDLOC K	Peripheral Module Disable
PMD3	0x4400_00E0		X	CFGCON0.PMDLOC K	Peripheral Module Disable
BOOT CONFIGURATION					
BCFG0	0x4400_0200	X		None	Pre-boot user configuration

Notes:

- Registers marked with (L) are loadable from Flash and they can be controlled by software after the boot with correct unlock sequence.
- ID Register is a JTAB ID register, maintained for legacy reasons. Actual external facing ID register is DSU.DID register. See *DID* register in the *Device Service Unit (DSU)* from Related Links.

Table 7-2. CM4 System Components Register Offset Map

Peripheral		TA Clock	Size (Bytes)	Virtual Address		Physical Address			
ABRV.	Description			Start	End	Start	End		
CM4 System Components accessible via CM4 PPB Bus (OnlyDAP and CM4 can access the registers)				Base Address		Base Address			
				0xE000_0000		0xE000_0000			
ITM	Inst. TM	SYS_CLK	4 KB	0000_0000	0000_0FFF	0000_0000	0000_0FFF		
DWT	Data WT	SYS_CLK	4 KB	0000_1000	0000_1FFF	0000_1000	0000_1FFF		
FPB	Flash PB	SYS_CLK	4 KB	0000_2000	0000_2FFF	0000_2000	0000_2FFF		
RSVD	Reserved		4 KB*n	0000_3000	0000_DFFF	0000_3000	0000_DFFF		

PIC32CX-BZ2 and WBZ45 Family

Product Memory Mapping Overview

.....continued

Peripheral		TA Clock	Size (Bytes)	Virtual Address		Physical Address	
ABRV.	Description			Start	End	Start	End
SCS	Sys. CS	SYS_CLK	4 KB	0000_E000	0000_EFFF	0000_E000	0000_EFFF
RSVD	Reserved		4 KB*n	0000_F000	0003_FFFF	0000_F000	0003_FFFF
TPIU	Trace PIU	SYS_CLK	4 KB	0004_0000	0004_0FFF	0004_0000	0004_0FFF
ETM	ETM	SYS_CLK	4 KB	0004_1000	0004_1FFF	0004_1000	0004_1FFF
ETB	ETB	SYS_CLK	4 KB	0004_2000	0004_2FFF	0004_2000	0004_2FFF
RSVD	Reserved		4 KB*n	0004_3000	000F_EFFF	0004_3000	000F_EFFF
CROM	CSight ROM	SYS_CLK	4 KB	000F_F000	000F_FFFF	000F_F000	000F_FFFF
RSVD	Reserved		4 KB*n	0010_0000	FFFF_FFFF	0010_0000	FFFF_FFFF

Notes:

1. All system and debug components carry unique ID accessible via its own register space.
2. The DAP derives the base address of the components from CROM entry values.
3. Component Base address = CROM Base address + CROM Entry value.
4. Core sight ROM entries are not provided in this document.
5. Refer to CM4F documentation for details on each component register space (developer.arm.com/documentation/ddi0439/b/System-Control/Register-summary).

Related Links

[11.13.8. DID](#)

8. Prefetch Cache

8.1 Introduction

The Prefetch Cache is a performance enhancing module, included in the PIC32CX-BZ2 devices, along with the L1 cache (Cortex M Cache Controller CMCC) to the Cortex M4 CPU.

8.2 Features

The Prefetch module increases the system performance for most of the applications.

The Prefetch module includes the following features:

- Fully Associative Lines for:
 - Four Lines for CPU Instructions Cache
 - Two Lines for CPU Data Cache
 - Two Lines for Peripheral Data Cache
- 16-byte Cache Line Sand 128-bits Parallel Memory Fetch
- Configurable Predictive Prefetch for CPU Instructions Cache
- Error Detection and Correction (ECC)

8.3 Overview

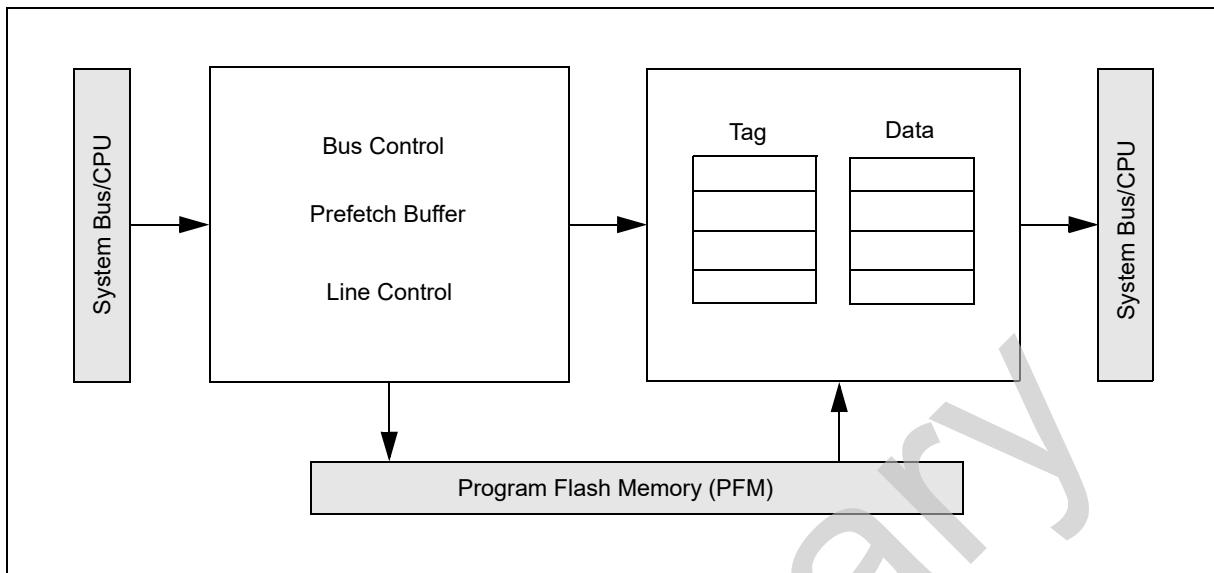
When running the Prefetch module at high-clock rates, insert the Wait states into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. The user can hide the Wait states to the core by prefetching and storing the instructions in a temporary holding area that the CPU can access quickly. Although, the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without the Wait states.

The CPU or a peripheral may request the data located in the PFM. If the requested data is not currently stored in the Prefetch module line, a read is performed to the PFM at the correct address, and the data is supplied to the Prefetch module and to the CPU or peripheral. If the requested data is stored in the Prefetch module and is valid, the data is supplied to the CPU or peripheral without Wait states.

Following figure shows a block diagram of the Prefetch module. Logically, the Prefetch module fits between the System Bus module and the PFM.

Figure 8-1. Prefetch Cache Block Diagram



8.3.1 Line Organization

The Prefetch module consists of two arrays, data and tag, each of which hold four lines. A data array consists of program instructions, program data, or peripheral data. Address matches are based on the physical address, not the virtual address.

Each line in the tag array contains the following information:

- Tag – Physical address of the data held in the data line
- Valid bit

Each line in the data array, contains 16 bytes of data. Depending on the line, the data can be, CPU instructions, CPU data, or peripheral data.

Following figures illustrate the organization of a line.

Figure 8-2. Tag Line

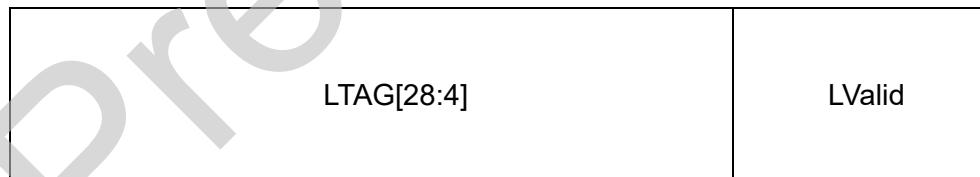
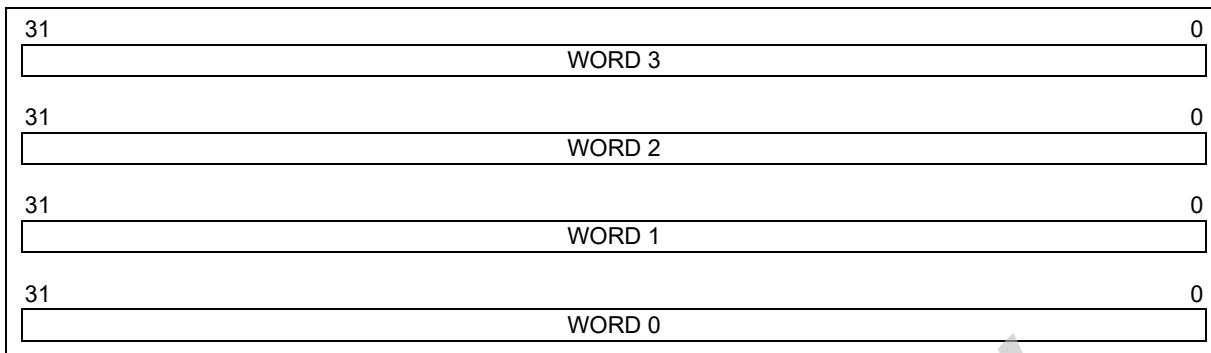


Figure 8-3. Data Line



8.4 Prefetch Behaviour

The Prefetch module complements an L1 CPU (CMCC) cache rather than to replace it. A four 128-bit (16-byte) lines hold instructions and two 128-bit (16-byte) lines hold CPU data and two 128-bit (16-byte) lines hold peripheral data from the PFM. The Prefetch module uses the Wait states value from the PFMWS[3:0] bits (CHECON[3:0]) and Address wait state ADRWS bit (CHECON[8]) to determine how long it must wait for a Flash access, when it reads instructions or data from the PFM.

If the instructions or data already reside in the Prefetch module line, the Prefetch module returns the instruction or data in zero Wait states. For CPU instructions, if predictive prefetch is enabled and the code is 100% linear, the Prefetch module will provide instructions back to the CPU with the Wait states only on the first instruction of the Prefetch module line.

If CPU accesses uncachable addresses, it bypasses the cache. During bypass, the prefetch module accesses the PFM for every instruction, incurring an address setup time defined by ADRWS and a Flash access time as defined by PFMWS bits. Therefore, the total Flash wait states is a sum of ADRWS and PFMWS. The Bypass mode is also forced for a cache if its associated I/D/A CHEEN bit (CHECON) is zero.

To allow caching for I and/or D caches, set the I and/or D *CHEEN bit to one. To enable a cache, set the ACHEEN bit to one.

8.5 Configurations

The CHECON register controls the general configurations available for accelerating the instruction and data accesses to the Flash memory system.

The Prefetch module implements the following general options:

- The PFMWS[3:0] bits (CHECON[3:0]) control the number of system clock cycles, required to access the PFM. Total flash wait states is a sum of ADRWS and PFMWS.
- The PREFEN[1:0] bits (CHECON[5:4]) control the predictive and prefetched instruction, which allows the cache controller to fetch the next 16-byte aligned set of instructions.
- The PFMSECEN bit (CHECON[7]) controls the Prefetch module, that, generates an interrupt event on a specific count of single bit errors corrected by the Flash Error Correction Code (ECC).
- The ADRWS bit (CHECON[8]) controls the number of system clock cycles required for address setup to PFM.
- The CHEPERF bit (CHECON[12]) controls the gathering statistics of the CPU instruction cache.
- The ICHECOH bit (CHECON[16]) controls the auto invalidate for the CPU instruction cache.
- The DCHECOH bit (CHECON[17]) controls the auto invalidate for the CPU data cache.
- The ACHECOH bit (CHECON[18]) controls the auto invalidate for the peripheral data cache.
- The ICHEINV bit (CHECON[20]) controls the manual invalidate for the CPU instruction cache.
- The DCHEINV bit (CHECON[21]) controls the manual invalidate for the CPU data cache.
- The ACHEINV bit (CHECON[22]) controls the manual invalidate for the peripheral data cache.

- The ICHEEN bit (CHECON[24]) controls the CPU instruction cache enable.
- The DCHEEN bit (CHECON[25]) controls the CPU data cache enable.
- The ACHEEN bit (CHECON[26]) controls the peripheral data cache enable.

8.6 Predictive Prefetch Behavior

When the user configures the module for predictive prefetch, the module predicts the next line address, fetches the instruction, and then stores it in the prefetch buffer. If the requested instruction is not in a Prefetch module line, and the read address matches the predicted address, the content of the prefetch buffer are loaded in the Prefetch module line, while simultaneously returning the critical word to the read initiator.

On enabling the predictive prefetch, the prefetch function starts predicting based on the first address read to the PFM. When the user places the first line in the Prefetch module, the module increments the address to the next 16-byte aligned address and starts a PFM access.

The predictive prefetches, like all PFM read accesses are never aborted. If a new address request does not match the predicted address, a new PFM access occurs after the current access finishes. The PREFEN [1:0] bits (CHECON[5:4]) can start a predictive prefetch. This allows the cache controller to speculatively fetch the next 16-byte aligned set of instructions. The predictive prefetch feature is available only for CPU instruction but not for CPU data and peripheral.

If the selected system clock speed is sufficiently low enough to access the Flash at zero Wait states, the predictive prefetch is detrimental and may be disabled.

8.7 Coherency Support

When a PFM programming event occurs flash programming initiated by Flash Controller, the Prefetch module invalidates all lines and the contents of the prefetch buffer. If a transaction is in progress, the invalidation occurs after completion. When programming or erasing a Flash page, a read of that Flash page will cause the transaction to stall until the erase or program event completes.

Prefetch module provides two methods for coherency control: Auto Invalidate via I/D/A CHECOH and Manual Invalidate via I/D/A CHEINV. The user can choose to auto invalidate the each/any cache on a PFM programming event by setting *CHECOH=1. This is the safest option. However, the user has the option to never auto invalidate each/any cache by setting *CHECOH = 0.

In addition to using *CHECOH, *CHEINV can be used as an alternate invalidate method to invalidate each/any cache manually. If using *CHEINV to invalidate manually each/any cache due to a PFM programming event, stop all instruction/data fetches from the desired flash, set *CHEINV, wait for it to clear, and then start programming sequence. When using *CHEINV to invalidate each/any cache for reasons other than programming, it can be set at any time but only takes effect after any pending transactions complete.

8.8 Effects of Reset

8.8.1 On Reset

Upon a device Reset, the following occurs:

- All lines are invalidated
- All tag bits are cleared

8.8.2 After Reset

The module operates as per the values in the CHECON register. See *CHECON* register from Related Links.

Related Links

8.12.1. [CHECON](#)

8.9 Error Conditions

The Prefetch module handles and reports information about two error types: ECC Double-bit Error Detected (DED) and ECC Single-bit Error Corrected (SEC). The ECC Error detection logic is enabled and disabled using the configuration bits, ECCCTL[1:0] (DEVCFG0[29:28]).

The ECC logic increases the read access delay from the PFM. Depending on the frequency of the system clock, the wait states may be different between ECC enabled and ECC disabled.

Note: ECC errors are captured for predictive prefetch reads of the PFM. However, those errors are not reported until, and unless, that data is used by the system.

8.9.1 ECC Double-bit Error Detected (DED)

A read from the Flash memory that results in a PFM ECC DED causes the Prefetch module to return a bus exception error to the initiator. If that initiator is the CPU, it recognizes the bus exception error, prevents the instruction from executing, or read data from loading, and generates an exception using the bus exception error vector.

When an ECC DED error occurs, the PFMDED bit (CHESTAT[27]) is set. The exception handling code can then check this bit to determine whether the exception was caused by a PFM ECC DED event. This bit must be cleared in software by the exception handler.

Note: CPU instructions or data prefetched from the PFM will always be loaded into the Prefetch module, even if a DED error is generated. The Prefetch module line containing the DED data will be tagged as valid until the line is replaced.

8.9.2 ECC Single Error Corrected (SEC)

A PFM ECC SEC event is not a critical error and as such is reported through an interrupt. The user has the option to enable or disable this interrupt through the PFMSECEN bit (CHECON[7]). The data in the Prefetch module is correct, and no further ECC events are generated for addresses that hit the data line as long as that data is in the Prefetch module.

Each read that returns from the PFM with an ECC SEC status causes the PFMSECCNT[7:0] bits (CHESTAT[7:0]) to decrement by one. If PFMSECCNT[7:0] is zero and a PFM ECC SEC event occurs, the PFMSEC bit (CHESTAT[26]) is set and an interrupt is generated. Therefore, the PFMSECCNT[7:0] bits should be set to the number of PFM ECC SEC events desired for an interrupt minus 1. For example, to generate an interrupt after five PFM ECC SEC events, PFMSECCNT[7:0] should be set to four ('00000100'). The Prefetch module does not reload the PFMSECCNT[7:0] bits when it reaches zero. Software must write the desired count each time it services the PFMSEC interrupt.

Software can generate an ECC SEC interrupt by setting the PFMSECEN bit and then setting the PFMSEC bit. If the PFMSEC bit is already set when PFMSECEN is set, the Prefetch module will also generate an ECC SEC interrupt. The ECC SEC interrupt persists as long as the PFMSECEN and PFMSEC bits remain set. Refer to PCACHE Interrupt in Nested Vector Interrupt Controller (NVIC) map. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

8.10 Operation in Power-saving Modes

8.10.1 Sleep Mode

When the device enters Sleep mode, the Prefetch module is disabled and placed into a low-power state where no clocking occurs in the module.

8.10.2 Idle Mode

When the device enters Idle mode, iCache, Prefetch, and dCache clocks are internally gated off, the aCache (peripheral data) clock remains functional for peripheral accesses and the CPU stops executing code. Any outstanding prefetch completes before the Prefetch module stops its clock through automatic clock gating.

8.10.3 Debug Mode

The behavior of the Prefetch module is unaltered in Debug mode.

Preliminary

8.11 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CHECON	7:0	PFMSECEN		PREFEN[1:0]			PFMWS[3:0]		
		15:8				CHEPERF				ADRWS
		23:16		ACHEINV	DCHEINV	ICHEINV		ACHECOH	DCHECOH	ICHECOH
		31:24						ACHEEN	DCHEEN	ICHEEN
0x04 ... 0x0F	Reserved									
0x10	CHESTAT	7:0			PFMSECCNT[7:0]					
		15:8								
		23:16								
		31:24					PFMDED	PFMSEC		
0x14 ... 0x1F	Reserved									
0x20	CHEHIT	7:0			CHEHIT[7:0]					
		15:8			CHEHIT[15:8]					
		23:16			CHEHIT[23:16]					
		31:24			CHEHIT[31:24]					
0x24 ... 0x2F	Reserved									
0x30	CHEMIS	7:0			CHEMIS[7:0]					
		15:8			CHEMIS[15:8]					
		23:16			CHEMIS[23:16]					
		31:24			CHEMIS[31:24]					

8.12 Register Description

The Prefetch module for PIC32CX-BZ2 devices with L1 CPU cache contains the following Special Function Registers (SFRs):

- CHECON: Prefetch Module Control Register
 - This register manages configuration of the Prefetch module and controls Wait states.
- CHESTAT: Prefetch Module Status Register
 - This register contains status information for error correction and detection.
- CHEHIT: Prefetch Module Hit Statistics Register
 - This register contain status information for cache hit count statistics.
- CHEMIS: Prefetch Module Miss Statistics Register
 - This register contain status information for cache miss count statistics.

Note: CHECON and CHESTAT registers in the Register Summary table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Related Links

[5.1.9. CLR, SET, and INV Registers](#)

8.12.1 CHECON - Prefetch Module Control Register

Name: CHECON
Offset: 0x00
Reset: 0x0700010F
Property: -

Bit	31	30	29	28	27	26	25	24
Access						ACHEEN	DCHEEN	ICHEEN
Reset						R/W	R/W	R/W
						1	1	1
Bit	23	22	21	20	19	18	17	16
Access		ACHEINV	DCHEINV	ICHEINV		ACHECOH	DCHECOH	ICHECOH
Reset		R/S/HC	R/S/HC	R/S/HC		R/W	R/W	R/W
	0	0	0			0	0	0
Bit	15	14	13	12	11	10	9	8
Access				CHEPERF				R/W
Reset								1
Bit	7	6	5	4	3	2	1	0
Access	PFMSECEN		PREFEN[1:0]			PFMWS[3:0]		R/W
Reset	R/W		R/W	R/W	R/W	R/W	R/W	R/W
	0		0	0	1	1	1	1

Bit 26 – ACHEEN Peripheral Data Cache Enable bit

Value	Description
1	Caching enabled
0	Caching disabled (and all lines invalidated)

Bit 25 – DCHEEN Data Cache Enable bit

Value	Description
1	Caching enabled
0	Caching disabled (and all lines invalidated)

Bit 24 – ICHEEN Instruction Data Cache Enable bit

Value	Description
1	Caching enabled
0	Caching disabled (and all lines invalidated)

Bit 22 – ACHEINV Manual Invalidate Control for Peripheral Data Cache

Note:

1. Hardware auto clears this bit when cache invalidate completes. Bits may clear at different times.

Value	Description
1	Force invalidate cache/invalidate busy
0	Cache invalidation follows ACHECOH/invalid complete

Bit 21 – DCHEINV Manual Invalidate Control for Data Cache

Note:

1. Hardware auto clears this bit when cache invalidate completes. Bits may clear at different times.

Value	Description
1	Force invalidate cache/invalidate busy
0	Cache invalidation follows DCHECOH/invalid complete

PIC32CX-BZ2 and WBZ45 Family

Prefetch Cache

Bit 20 – ICHEINV Manual Invalidate Control for Instruction Cache

Notes:

1. Predictive Prefetch Buffer (PFB) is included with iCache invalidate.
2. Hardware auto clears this bit when cache invalidate completes. Bits may clear at different times.

Value	Description
1	Force invalidate cache/invalidate busy
0	Cache invalidation follows ICHECOH/invalid complete

Bit 18 – ACHECOH Auto Cache Coherency Control for Peripheral Data Cache

Note: ACHECOH must be stable before initiation of programming to ensure correct invalidation of data.

Value	Description
1	Auto invalidate cache on a programming event
0	No auto invalidated cache on a programming event

Bit 17 – DCHECOH Auto Cache Coherency Control for Data Cache

Note: DCHECOH must be stable before initiation of programming to ensure correct invalidation of data.

Value	Description
1	Auto invalidate cache on a programming event
0	No auto invalidated cache on a programming event

Bit 16 – ICHECOH Auto Cache Coherency Control for Instruction Cache

Note: ICHECOH must be stable before initiation of programming to ensure correct invalidation of data.

Value	Description
1	Auto invalidate cache on a programming event
0	No auto invalidated cache on a programming event

Bit 12 – CHEPERF Cache Performance Counters Enable

Note: Performance counters are reset on 0 to 1 transition of this bit.

Value	Description
1	Performance counters is enabled
0	Performance counters is disabled

Bit 8 – ADRWS Address Wait State Enable

Total Flash wait states are ADRWS + PFMWS.

Value	Description
1	Add 1 address Wait state - allowing for higher clock frequencies
0	Add 0 address Wait states - allowing for higher performance at lower clock frequencies

Bit 7 – PFMSECEN Flash Single-bit Error Corrected (SEC) Interrupt Enable bit

Value	Description
1	Generate an interrupt when PFMSEC is set
0	Do not generate an interrupt when PFMSEC is set

Bits 5:4 – PREFEN[1:0] Instruction Predictive Prefetch Enable

Value	Description
01	Instruction predictive prefetch enabled for cacheable regions only
00	Instruction predictive prefetch disabled

Note: Other values are unavailable.

Bits 3:0 – PFMWS[3:0] PFM Access Time Defined in Terms of SYSCLK Wait States bits

Total Flash Wait states are ADRWS + PFMWS.

Value	Description
1111	Fifteen Wait states

PIC32CX-BZ2 and WBZ45 Family

Prefetch Cache

Value	Description
1110	Fourteen Wait states
...	
0001	One Wait state
0000	Zero Wait state

Notes:

1. This is not the Wait state seen by the CPU.
2. For the Wait states to SYSCLK relationship, refer to the Electrical Specifications.

Preliminary

8.12.2 CHESTAT - Prefetch Module Status Register

Name: CHESTAT
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access					PFMDED	PFMSEC		
Reset					HS, R/C 0	HS, R/W 0		
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PFMSECCNT[7:0]							
Access	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W	HS, HC, R/W
Reset	0	0	0	0	0	0	0	0

Bit 27 – PFMDED Flash Double-bit Error Detected (DED) Status bit

This bit is set in hardware and can only be cleared (i.e., set to '0') in software.

Value	Description
1	A DED error has occurred
0	A DED error has not occurred

Bit 26 – PFMSEC Flash Single-bit Error Corrected (SEC) Status bit

Note: The error event is reported to the CPU via using the PCACHE interrupt event (See *Nested Vector Interrupt Controller (NVIC)* from Related Links).

Value	Description
1	A SEC error occurred when PFMSECCNT[7:0] was equal to zero
0	A SEC error has not occurred

Bits 7:0 – PFMSECCNT[7:0] Flash SEC Count bits

Decrements by 1 its count value each time an SEC error occurs. Holds at zero. When an SEC error occurs when PFMSECCNT[7:0] is zero, the PFMSEC status bit is set. If PFMSECEN is also set, a Prefetch module interrupt event is generated.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

PIC32CX-BZ2 and WBZ45 Family

Prefetch Cache

8.12.3 CHEHIT - Prefetch Module Hit Statistics Register

Name: CHEHIT
Offset: 0x20
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
CHEHIT[31:24]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEHIT[23:16]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEHIT[15:8]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEHIT[7:0]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CHEHIT[31:0] Instruction Cache Hit Count bits

When CHECON.CHEPERF = 1, CHEHIT increments once per iCache or Predictive Prefetch Buffer (PFB) hit.

Note: CHEHIT is reset on 0 to 1 transition of CHECON.CHEPERF.

8.12.4 CHEMIS - Prefetch Module Miss Statistics Register

Name: CHEMIS
Offset: 0x30
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
CHEMIS[31:24]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEMIS[23:16]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEMIS[15:8]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0
CHEMIS[7:0]								
Access	R/HC							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CHEMIS[31:0] Instruction Cache Miss Count bits

When CHECON.CHEPERF = 1, CHEMIS increments once per iCache or Predictive Prefetch Buffer (PFB) miss.

Note: CHEMIS is reset on 0 to 1 transition of CHECON.CHEPERF.

9. Processor and Architecture

9.1 Cortex M4 Processor

The ARM®Cortex™ -M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers the following significant benefits to developers:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultra low-power consumption with integrated sleep modes
- Platform security robustness, with integrated memory protection unit (MPU).

The implemented ARM Cortex-M4 is revision r0p1

For additional information, refer to <http://www.arm.com>

The Cortex-M4 processor is built on a high-performance processor core with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE 754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex-M4 processor implements tightly-coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4 processor implements a version of the Thumb instruction set based on Thumb®-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex-M4 processor closely integrates a configurable NVIC, to deliver industry-leading interrupt performance. The NVIC includes a *Non-Maskable interrupt* (NMI), and provides up to 8 interrupt priority levels. The tight integration of the processor core and NVIC provides fast execution of *Interrupt Service Routines* (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to suspend load-multiple and store-multiple operations. Interrupt handlers do not require wrapping in assembler code, removing any code overhead from the ISRs. A tail-chain optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to be rapidly powered down while still retaining program state.

9.1.1 System Level Interface

The Cortex-M4 processor provides multiple interfaces using AMBA technology to provide high-speed, low-latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

The Cortex-M4 processor has a memory protection unit (MPU) that provides fine grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

9.1.2 Integrated Configurable Debug

The Cortex-M4 processor implements a complete hardware debug solution. This provides high system visibility of the processor and memory through a 2-pin *Serial Wire Debug* (SWD) port that is ideal for microcontrollers and other small package devices.

For system trace the processor integrates an *Instrumentation Trace Macrocell* (ITM) alongside data watchpoints and a profiling unit. The *Embedded Trace Macrocell* (ETM) delivers unrivaled instruction trace capture in an area far smaller than traditional trace units, enabling many low cost MCUs to implement full instruction trace for the first time.

To enable simple and cost-effective profiling of the system events these generate, a stream of software-generated messages, data trace, and profiling information is exported over three different ways:

- Output off chip using the TPIU, through a single pin, called *Serial Wire Viewer* (SWV). Limited to ITM system trace
- Output off chip using the TPIU, through a 4-bit pin interface. Bandwidth is limited
- Internally stored in RAM, using the CoreSight ETB. Bandwidth is then optimal but capacity is limited

The *Flash Patch and Breakpoint Unit* (FPB) provides up to 8 hardware breakpoint comparators that debuggers can use. The comparators in the FPB also provide remap functions of up to 8 words in the program code in the CODE memory region. This enables applications stored on a non-erasable, ROM-based microcontroller to be patched if a small programmable memory, for example flash, is available in the device. During initialization, the application in ROM detects, from the programmable memory, whether a patch is required. If a patch is required, the application programs the FPB to remap a number of addresses. When those addresses are accessed, the accesses are redirected to a remap table specified in the FPB configuration, which means the program in the non-modifiable ROM can be patched.

9.1.3 Cortex-M4 Processor Features and Configuration

- Thumb® instruction set combines high code density with 32-bit performance
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Integrated sleep modes for low power consumption
- Fast code execution permits slower processor clock or increases Sleep mode time
- Hardware division and fast digital-signal-processing orientated multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory Protection Unit (MPU) for safety-critical applications
- Extensive debug and trace capabilities: Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging, tracing, and code profiling.

Features	Cortex-M4 Options	PIC32CX-BZ2 Configuration
Interrupts	1 to 240	40
Number of priority bits	3 to 8	3 = eight levels of priority
Data endianness	Little-endian or big-endian	Little-endian
SysTick Timer calibration value		0x80000000
MPU	Present or Not present	Present
Debug support level	0 = No debug. No DAP, breakpoints, watchpoints, Flash patch, or halting debug. 1 = Minimum debug. Two breakpoints, one watchpoint, no Flash patch. 2 = Full debug minus DWT data matching. 3 = Full debug plus DWT data matching.	3 = Full debug plus DWT data matching.
Trace support level	0 = No trace. No ETM, ITM or DWT triggers and counters. 1 = Standard trace. ITM and DWT triggers and counters, but no ETM. 2 = Full trace. Standard trace plus ETM. 3 = Full trace plus HTM port.	2 = Full trace. Standard trace plus ETM.
JTAG	Present or Not present	Not present

.....continued

Features	Cortex-M4 Options	PIC32CX-BZ2 Configuration
Bit Banding	Present or Not present	Not present
FPU	Present or Not present	Present

9.1.4 Cortex-M4 Core Peripherals

Nested Vectored Interrupt Controller	The Nested Vector Interrupt Controller (NVIC) is an embedded interrupt controller that supports low latency interrupt processing.
System Control Block	The System Control Block (SCB) is the programmers model interface to the processor. It provides system implementation information and system control, including configuration, control, and reporting of system exceptions. Refer to the <i>Cortex-M4 Technical Reference Manual</i> for more details (http://www.arm.com).
System Timer	The system timer, SysTick, is a 24-bit count-down timer. Use this as a Real-Time Operating System (RTOS) tick timer or as a simple counter. The SysTick timer runs on the processor clock and it does not decrement when the processor is halted for debugging. Refer to the <i>Cortex-M4 Technical Reference Manual</i> for more details (http://www.arm.com).
Memory Protection Unit	The Memory Protection Unit (MPU) improves system reliability by defining the memory attributes for different memory regions. It provides up to eight different regions, and an optional predefined background region. Refer to the <i>Cortex-M4 Technical Reference Manual</i> for more details (http://www.arm.com).
Floating-Point Unit	The Floating Point Unit (FPU) provides IEEE 754-compliant operations on single-precision, 32-bit, floating-point values. Refer to the <i>Cortex-M4 Technical Reference Manual</i> for more details (http://www.arm.com).

9.1.5 Cortex-M4 Address Map

Address	Core Peripheral
0xE000E008-0xE000E00F	System control block
0xE000E010-0xE000E01F	System timer
0xE000E100-0xE000E4EF	Nested Vectored Interrupt Controller
0xE000ED00-0xE000ED3F	System control block
0xE000ED90-0xE000ED93	MPU Type Register
0xE000ED94-0xE000EDB8	Memory Protection Unit
0xE000EF00-0xE000EF03	Nested Vectored Interrupt Controller
0xE000EF30-0xE000EF44	Floating Point Unit

9.2 Nested Vector Interrupt Controller (NVIC)

9.2.1 Overview

The Nested Vectored Interrupt Controller (NVIC) in the PIC32CX-BZ2 family devices supports 40 interrupts with eight different priority levels. For more details, refer to the *Cortex-M4 Technical Reference Manual* (www.arm.com).

9.2.2 Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

PIC32CX-BZ2 and WBZ45 Family Processor and Architecture

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a '1' to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing '1' to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

Depending on their criticality, the interrupt requests for one peripheral are either ORed together on system level, generating one interrupt or directly connected to an NVIC interrupt lines. This is described in the table below.

An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Module	Source	Line
EIC NMI - External Interrupt Control	NMI	NMI
RTC - Real-Time Counter	CMP A 0	0
	CMP A 1	
	CMP A 2	
	CMP A 3	
	OVF A	
	PER A 0	
	PER A 1	
	PER A 2	
	PER A 3	
	PER A 4	
EIC - External Interrupt Controller	PER A 5	
	PER A 6	
	PER A 7	
	TAMPER A	
FREQM - Frequency Meter	EXTINT 0	1
	EXTINT 1	
	EXTINT 2	
	EXTINT 3	
Flash Subsystem	DONE	2
PORT-A	Flash Controller	3
	PFW	
	PCACHE	
PORT-B	PortA Input Change Interrupt	4
	PortB Input Change Interrupt	5

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.....continued

Module	Source	Line
DMAC - Direct Memory Access Controller	SUSP 0..3	6
	TCMPL 0..3	
	TERR 0..3	
	SUSP 4..15	7
	TCMPL 4..15	
	TERR 4..15	
EVSYS - Event System Interface	EVD 0..3	8
	OVR 0..3	
	EVD 4..11	9
	OVR 4..11	
PAC - Peripheral Access Controller	ERR	10
RAM ECC	SINGLEE-0	11
	DualE-1	
SERCOM0 - Serial Communication Interface 0 ⁽¹⁾ Order: USART, I2CM, I2CS, SPI	0	12
	1	
	2	
	3	
	4	
	5	
	7	
SERCOM1 - Serial Communication Interface 1 ⁽¹⁾ Order: USART, I2CM, I2CS, SPI	0	13
	1	
	2	
	3	
	4	
	5	
	7	
SERCOM2 - Serial Communication Interface 2 ⁽¹⁾ Order: USART, I2CM, I2CS, SPI	0	14
	1	
	2	
	3	
	4	
	5	
	7	

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.....continued

Module	Source	Line
SERCOM3 - Serial Communication Interface 3 ⁽¹⁾ Order: USART, I2CM, I2CS, SPI	0	15
	1	
	2	
	3	
	4	
	5	
	7	
TCC0 - Timer Counter Control 0	CNT A DFS A ERR A FAULTA A FAULTB A FAULT0 A FAULT1 A OVF TRG UFS A MC 0 MC 1 MC 2 MC 3 MC 4 MC 5	16

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.....continued

Module	Source	Line
TCC1 - Timer Counter Control 1	CNT A	17
	DFS A	
	ERR A	
	FAULTA A	
	FAULTB A	
	FAULT0 A	
	FAULT1 A	
	OVF	
	TRG	
	UFS A	
	MC 0	
	MC 1	
	MC 2	
	MC 3	
	MC 4	
	MC 5	
TCC2 - Timer Counter Control 2	CNT A	18
	DFS A	
	ERR A	
	FAULTA A	
	FAULTB A	
	FAULT0 A	
	FAULT1 A	
	OVF	
	TRG	
	UFS A	
	MC 0	
	MC 1	
TC0 - Basic Timer Counter 0	ERR A	19
	MC 0	
	MC 1	
	OVF	

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.....continued

Module	Source	Line
TC1 - Basic Timer Counter 1	ERR A	20
	MC 0	
	MC 1	
	OVF	
TC2 - Basic Timer Counter 2	ERR A	21
	MC 0	
	MC 1	
	OVF	
TC3 - Basic Timer Counter 3	ERR A	22
	MC 0	
	MC 1	
	OVF	
ADCTRL	ADC_GIRQ	23
	ADC_DIRQ0, ADC_DIRQ1	
	ADC_AIRQ0, ADC_AIRQ1	
	ADC_FLT	34
	ADC_FCC	35
	ADC_BGVR_RDY	36
AC - Analog Comparators	COMP 0	24
	COMP 1	
	WIN 0	
AES - Advanced Encryption Standard	ENCCMP	25
	GFMCMP	
TRNG - True Random Generator	IS0	26
ICM - Integrity Check Monitor	ICM	27
PUKCC - Public-Key Cryptography Controller	PUKCC	28
QSPI - Quad SPI interface	QSPI	29
Wireless Radio	ZB_INT0	30
	BT_INT0	
	BT_INT1	32
	ARBITER	33
	CLKI_WAKEUP_NMI	37
	BT_LC	38
	BT_RC	39

Note:

1. The integer number specified in the source refers to the respective bit position in the INTFLAG register of respective peripheral.

9.3 High-Speed Bus System

9.3.1 Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

9.3.2 Configuration

Figure 9-1. Master-Slave Relations High-Speed Bus Matrix

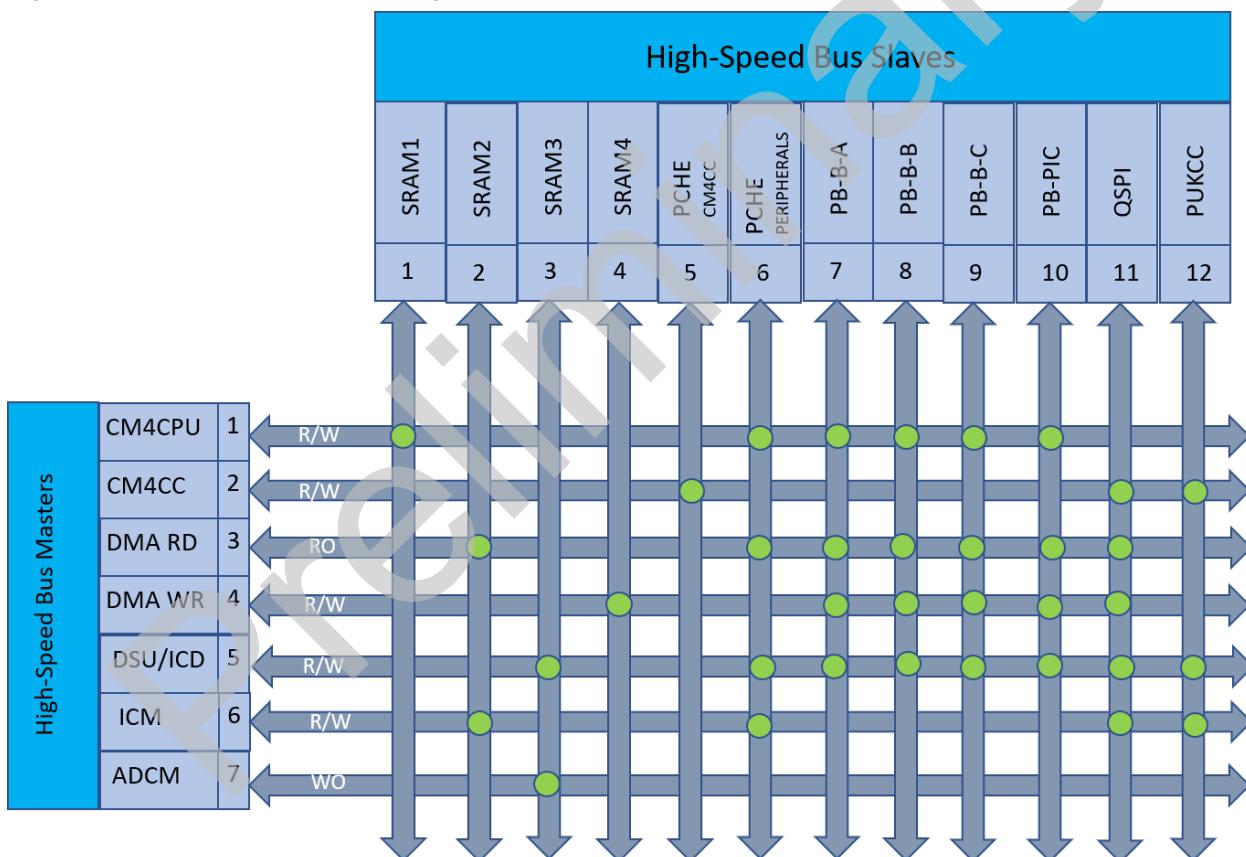


Table 9-1. High Speed Bus Matrix Master

High-Speed Bus Matrix Master	Master ID
CM4CPU - Cortex M4 Processor	1
CM4CC - Cortex-M Cache Controller	2
DMA RD - DMA-Read	3
DMA-WR - DMA-Write	4

PIC32CX-BZ2 and WBZ45 Family Processor and Architecture

.....continued

High-Speed Bus Matrix Master	Master ID
DSU/ICD (private test mode only) - Device Service Unit/In-Chip Debugger	5
ICM - Integrity Check Monitor	6
ADCM - ADC Controller Module	7

Table 9-2. High-Speed Bus Matrix Slave

High-Speed Bus Matrix Slave	Slave ID
SRAM1 - SRAM Port 1	1
SRAM2 - SRAM Port 2	2
SRAM3 - SRAM Port 3	3
SRAM4 - SRAM Port 4	4
PCHE - Pre-fetch Cache of CM4CC	5
PCHE - Pre-fetch Cache of Peripherals	6
PB-B-A - Peripheral Bridge A	7
PB-B-B - Peripheral Bridge B	8
PB-B-C - Peripheral Bridge C	9
PB-PIC - Peripheral Bus PIC	10
QSPI - Quad SPI Interface	11
PUKCC - Public Key Cryptography Controller	12

10. CMCC - Cortex M Cache Controller

10.1 Overview

The Cortex M Cache Controller provides an L1 cache to the Cortex M CPU. The CMCC sits transparently between the CPU and the cache leading to improved performance.

The CMCC interfaces with the CPU through the AHB, and is connected to the APB bus interface for its configuration.

10.2 Features

- Physically addressed and physically tagged
- L1 data and instruction cache set to 4 KB
- L1 cache line size set to 16 Bytes
- L1 cache integrates 32-bit bus master interface
- Unified 4-Way set associative cache architecture
- Lock-Down feature, which allows cached to be locked per way
- Write through cache operations, read allocate
- Configurable as data and instruction Tightly Coupled Memory (TCM)
- Round Robin victim selection policy
- Event Monitoring, with one programmable 32-bit counter
- Cache Interface includes cache maintenance operations registers

10.3 Block Diagram

Figure 10-1. CMCC Block Diagram

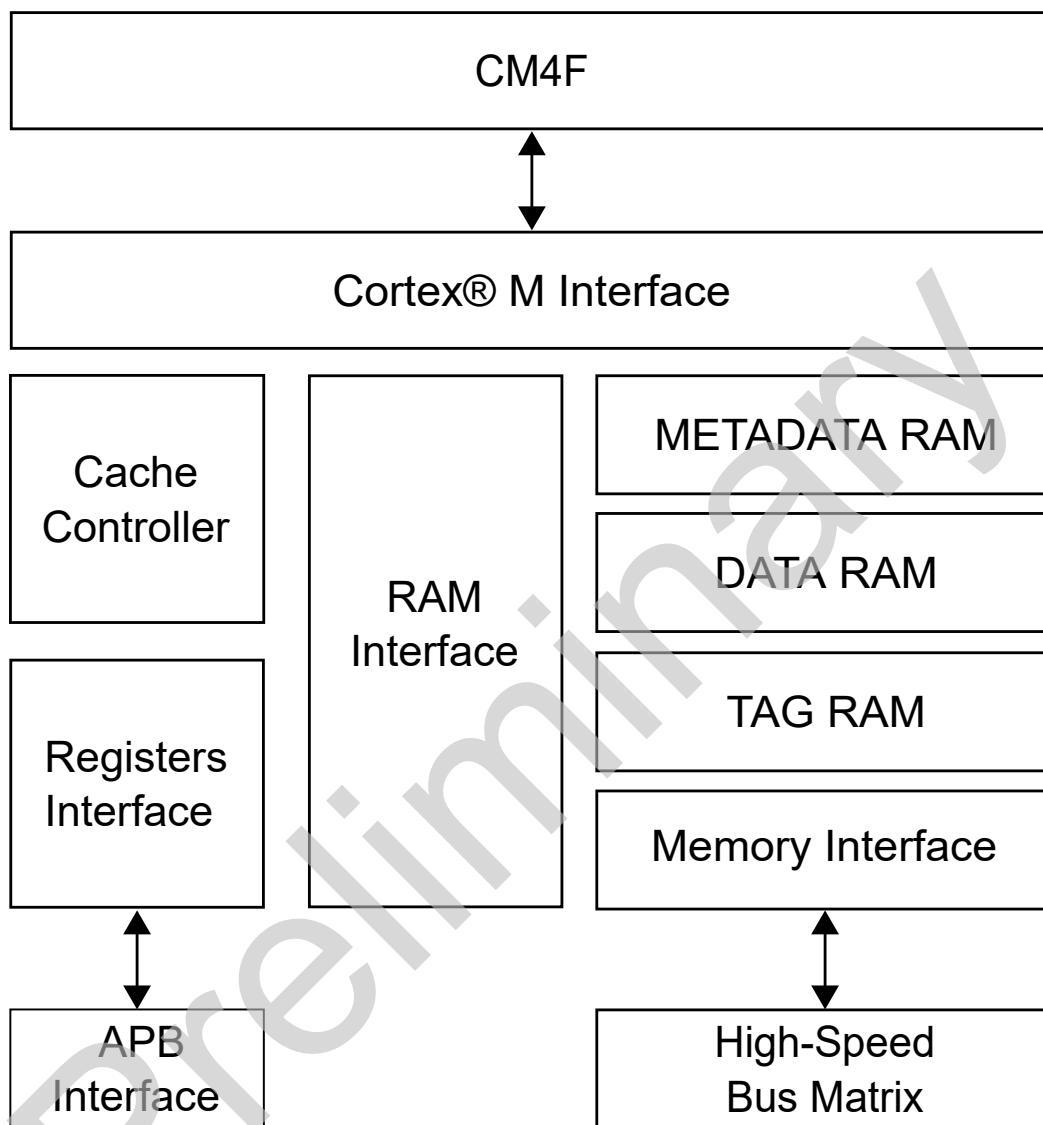
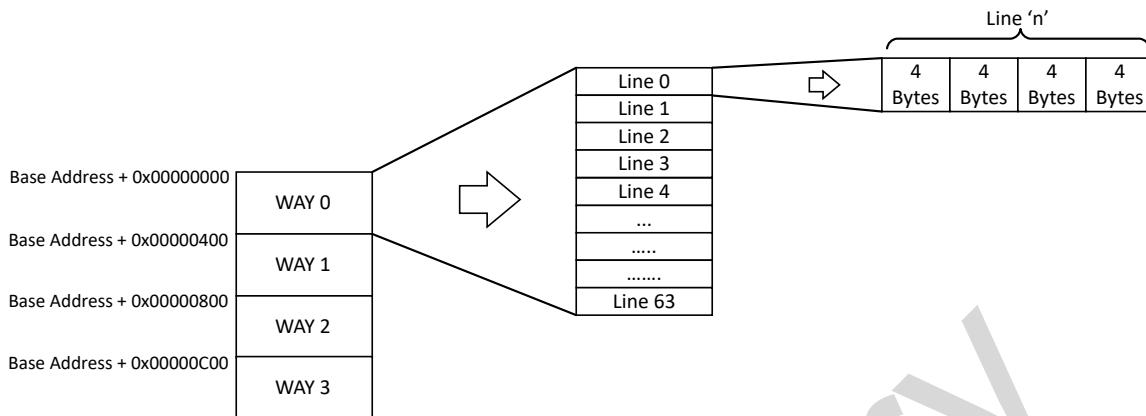


Figure 10-2. CMCC Organization



10.4 Signal Description

Not applicable.

10.5 Product Dependencies

Not applicable.

10.5.1 I/O Lines

Not applicable.

10.5.2 Power Management

The CMCC will continue to function as long as the CPU is not sleeping and CMCC is enabled.

10.5.3 Clocks

Not applicable.

10.5.4 DMA

Not applicable.

10.5.5 Interrupts

Not applicable.

10.5.6 Events

Not applicable.

10.5.7 Debug Operation

When the CPU is halted in debug mode, the CMCC is halted. Any read access by the debugger in cached zones are not cached.

10.5.8 Register Access Protection

Not applicable.

10.5.9 Analog Connections

Not applicable.

10.6 Functional Description

10.6.1 Principle of Operation

10.6.2 Initialization and Normal Operation

On reset, the cache controller data entries are all invalidated, and the cache is disabled. The cache is transparent to processor operations. The cache controller is activated through the use of its configuration registers. The configuration interface is memory mapped in the APB bus.

Use the following sequence to enable the cache controller:

- Verify that the CMCC is disabled, reading the value of the SR.CSTS.
- Enable the CMCC by writing '1' in CTRL.CEN. The MODULE is disabled by writing a '0' in CTRL.CEN.

10.6.3 Change Cache Size

It is possible to change the cache size by writing to the Cache Size Configured By Software bits in the Cache Configuration register (CFG.CSIZESW).

Use the following sequence to change the cache size:

- Disable the CMCC controller by writing a zero to the Cache Controller Enable bit in the Cache Control register (CTRL.CEN=0).
- Check the Cache Controller Status bit in the Cache Status register to verify that the CMCC is successfully disabled (SR.CSTS=0).
- Change CFG.CSIZESW to its new value.
- Enable the CMCC by writing CTRL.CEN=1.

10.6.4 Data Cache Disable

The Instructions alone can be cached by disabling the Data cache, as described in the following steps:

1. Disable the cache controller by writing a '0' to CTRL.CEN.
2. Check SR.CSTS to verify whether the CMCC is successfully disabled.
3. Write CFG.DCDIS = 1.
4. Enable the CMCC by writing CTRL.CEN = 1.

10.6.5 Instruction Cache Disable

The Data alone can be cached by disabling the Instruction cache, as described in the following steps:

1. Disable the cache controller by writing CTRL.CEN = 0.
2. Check SR.CSTS to verify that the CMCC is successfully disabled.
3. Write CFG.ICDIS = 1.
4. Enable the CMCC by writing CTRL.CEN = 1.

10.6.6 Cache Load and Lock

It is possible to lock a specific way for code optimization by writing the Lock Way register (LCKWAY.LCKWAY). The locked way will not be updated by the CMCC as part of cache operations.

The load and lock mechanism can be implemented to use cache memory in a deterministic way. Follow these steps to load and lock a way:

1. Disable cache controller by clearing the CTRL.CEN bit.
2. Invalidate the desired WAY line by line. This will reset the round robin algorithm of the invalidated line, that will become eligible for the next load operation.
3. Disable the Instruction cache, but keep the Data cache enabled.

4. Enable the cache by setting the CTRL.CEN bit.
5. Place the respective piece of code and/or data to the corresponding WAY due to simple LOAD operations. Loading the piece of code and/or data will force the cache to refill the previous invalidated line in the right way. No need to load all the bytes of the line, only the first byte. The cache will automatically refill the complete line.
6. Lock the specific WAY by setting LCKWAY.LCKWAY[3:0].
7. Re-enable the instruction cache. The locked WAY is now loaded and ready to operate. The remaining WAYS can be used as I-cache or D-cache as required.

10.6.7 Tightly Coupled Memory

Users can use a part of the cache as Tightly Coupled Memory (TCM). The cache size is determined by the Cache Size Configuration by Software bits in the Cache Configuration register (CFG.CSIZESW). The relation between cache and TCM is as given below:

TCM size = maximum Cache size - configured Cache size.

The TCM start address can be obtained from the product memory mapping. The cache memory starts first from the address followed by the TCM memory. Size of the Way is fixed and the number of ways varies according to the available size for the cache memory. See *Product Memory Mapping Overview* from Related Links.

Table 10-1. TCM Sizes

Max. Cache	Configured Cache	TCM Size
4 KB	4 KB	0 KB
4 KB	1 KB	3 KB
4 KB	2 KB	2 KB
4 KB	0 KB	4 KB

The TCM is also accessible in its maximum size when the CMCC is disabled. The TCM does not need to be locked in order to operate.

Note: Writing into the cache DATA RAM region through the CPU can overwrite the valid cache lines. This can result in data corruption when the cache controller is accessing the data for cache transactions. Access the DATA RAM region only after configuring it as TCM.

Related Links

[7. Product Memory Mapping Overview](#)

10.6.8 Cache Maintenance

10.6.8.1 Cache Invalidate by Line Operation

When an invalidate by line command is issued, the CMCC resets the valid bit information of the decoded cache line. As the line is no longer valid, the replacement counter points to that line.

- Disable the cache controller by writing a zero to the Cache Controller Enable bit in the Cache Control register (CTRL.CEN).
- Check SR.CSTS to verify that the CMCC is successfully disabled.
- Perform an invalidate by line by writing the set {index,way} in the Cache Maintenance 1 register (MAINT1.INDEX, MAINT1.WAY).
- Enable the CMCC by writing a '1' to CTRL.CEN.

10.6.8.2 Cache Invalidate All Operation

Use the following sequence to invalidate all cache entries.

- Disable the cache controller by writing a zero to the Cache Enable bit in the Cache Control register (CTRL.CEN).
- Check SR.CSTS to verify that the CMCC is successfully disabled.
- Perform a full invalidate operation by writing a '1' to the Cache Controller Invalidate All bit in the Cache Maintenance 0 register (MAINT0INVALL).

- Enable the CMCC by writing a '1' to CTRL.CEN.

10.6.9 Cache Performance Monitoring

The Cortex M cache controller includes a programmable monitor/32-bit counter. The monitor can be configured to count the number of clock cycles, the number of data hit or the number of instruction hit.

It is important to know that the Cortex-M4 processor prefetches instructions ahead of execution. It performs only 32-bit read access on the Instruction Bus, which means:

- One arm instruction is fetched per bus access
- Two thumb instructions are fetched per bus access

As a consequence, two thumb instructions (e.g., NOP) need one bus access, which results in the HIT counter incrementing by 1.

Use the following sequence to activate the counter:

- Configure the monitor counter by writing the MCFG.MODE.
 - CYCLE_COUNT is used to increment the counter along with the program counter, to count the number of cycles.
 - IHIT_COUNT is the instruction Hit counter, which increments the counter when there is a hit for the instruction in the cache.
 - DHIT_COUNT is the data Hit counter which increments the counter when there is a hit for the data in the cache.
- Enable the counter by writing a '1' to the Cache Controller Monitor Enable bit in the Cache Monitor Enable register (MEN.MENABLE).
- If required, reset the counter by writing a '1' to the Cache Controller Software Reset bit in the Cache Monitor Control register (MCTRL.SWRST).
- Check the value of the monitor counter by reading the MSR.EVENT_CNT bit field.

10.7 DEBUG Mode

In Debug mode, TAG and METADATA RAM blocks content is read/written through the AHB bus interface if the CMCC is disabled. When the CMCC is enabled, the TAG and METADATA RAM blocks are non readable.

Debug access has the same R/W properties as the CPU access for the DATA RAM block.

The TAG, METADATA and DATA RAM blocks' R/W properties are summarized in RAM Properties, see *RAM Properties* from the Related Links.

Use the following sequence to perform read access with the Debugger to the three RAM blocks:

- Disable the cache controller by writing a zero to the Cache Controller Enable bit in the Cache Control register (CTRL.CEN).
- Check the Cache Controller Status bit in the Cache Status register (SR.CSTS) to verify that the CMCC is successfully disabled.
- Perform a read or write access through Debugger:
 - @ CMCC_AHB_ADDR for DATA RAM,
 - @ CMCC_AHB_ADDR_TAG for TAG RAM,
 - @ CMCC_AHB_ADDR_MTDATA for METADATA RAM.
- If a write access has been performed in the TAG, METADATA, or DATA RAM in the cache section, an invalid operation must be performed before re-enabling the CMCC.

10.8 RAM Properties

The following table shows the different access properties of the three RAM blocks, according the different modes described in the previous chapters.

PIC32CX-BZ2 and WBZ45 Family

CMCC - Cortex M Cache Controller

Table 10-2. Access to RAM

Access Condition	DATA RAM	TAG RAM	METADATA RAM
CPU access when CMCC DISABLED	R/W	no R/W - hardfault	no R/W - hardfault
CPU access when CMCC ENABLED	CACHE section configured: R/W ⁽¹⁾ TCM section configured: R/W	no R/W - hardfault	no R/W - hardfault
Debugger access when CMCC DISABLED	R/W	R/W	R/W
Debugger access when CMCC ENABLED	CACHE section configured: R/W ⁽¹⁾ TCM section configured: R/W	no R/W	no R/W

Note:

1. A write operation in this zone can corrupt the coherency of the cache. An invalidate operation may be needed.

10.9 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0	
0x00	TYPE	7:0	LCKDOWN	WAYNUM[1:0]		RRP	LRUP	RANDP	GCLK	AP	
		15:8		CLSIZE[2:0]			CSIZE[2:0]				
		23:16									
		31:24									
0x04	CFG	7:0	CSIZESW[2:0]			DCDIS		ICDIS			
		15:8									
		23:16									
		31:24									
0x08	CTRL	7:0							CEN		
		15:8									
		23:16									
		31:24									
0x0C	SR	7:0							CSTS		
		15:8									
		23:16									
		31:24									
0x10	LCKWAY	7:0				LCKWAY[3:0]					
		15:8									
		23:16									
		31:24									
0x14 ... 0x1F	Reserved										
0x20	MAINT0	7:0							INVALL		
		15:8									
		23:16									
		31:24									
0x24	MAINT1	7:0	INDEX[3:0]						INDEX[7:4]		
		15:8									
		23:16									
		31:24	WAY[3:0]								
0x28	MCFG	7:0							MODE[1:0]		
		15:8									
		23:16									
		31:24									
0x2C	MEN	7:0							MENABLE		
		15:8									
		23:16									
		31:24									
0x30	MCTRL	7:0							SWRST		
		15:8									
		23:16									
		31:24									
0x34	MSR	7:0	EVENT_CNT[7:0]								
		15:8	EVENT_CNT[15:8]								
		23:16	EVENT_CNT[23:16]								
		31:24	EVENT_CNT[31:24]								

10.10 Register Description

10.10.1 Cache Type

Name: TYPE
Offset: 0x00
Reset: 0x000012D2
Property: R

Access	Bit	31	30	29	28	27	26	25	24
Reset									
Access	Bit	23	22	21	20	19	18	17	16
Reset									
Access	Bit	15	14	13	12	11	10	9	8
Reset				CLSIZE[2:0]		CSIZE[2:0]			
Access				R	R	R	R	R	R
Reset				0	1	0	0	1	0
Access	Bit	7	6	5	4	3	2	1	0
Reset		LCKDOWN		WAYNUM[1:0]	RRP	LRUP	RANDP	GCLK	AP
Access		R	R	R	R	R	R	R	R
Reset		1	1	0	1	0	0	1	0

Bits 13:11 – CLSIZE[2:0] Cache Line Size

This field configures the Cache Line Size.

Value	Name	Description
0x2	CLSIZE_16B	Cache Line Size is 16 bytes
0x3-0x7	-	Reserved

Bits 10:8 – CSIZE[2:0] Cache Size

This bit field configures the cache size.

Value	Name	Description
0x0	CSIZE_1KB	Cache Size is 1 KB
0x1	CSIZE_2KB	Cache Size is 2 KB
0x2	CSIZE_4KB	Cache Size is 4 KB
0x3-0x7	-	Reserved

Bit 7 – LCKDOWN Lock Down Supported

Writing a '0' to this bit disables the Lock Down feature.

Writing a '1' to this bit enables the Lock Down feature.

Bits 6:5 – WAYNUM[1:0] Number of Way

This bit field configures the mapping of the cache.

Value	Name	Description
0x0	DMAPPED	Direct Mapped Cache
0x1	ARCH2WAY	2-WAY set associative
0x2	ARCH4WAY	4-WAY set associative
0x3	ARCH8WAY	8-WAY set associative

Bit 4 – RRP Round Robin Policy Supported

Writing a '0' to this bit disables Round Robin Policy.

Writing a '1' to this bit enables Round Robin Policy.

Bit 3 – LRUP Least Recently Used Policy Supported

Writing a '0' to this bit disables the Least Recently Used Policy Supported.

Writing a '1' to this bit enables the Least Recently Used Policy Supported.

Bit 2 – RANDP Random Selection Policy Supported

Writing a '0' to this bit disables the Random Selection Policy Supported.

Writing a '1' to this bit enables the Random Selection Policy Supported.

Bit 1 – GCLK Dynamic Clock Gating

Writing a '0' to this bit disables the Dynamic Clock Gating feature.

Writing a '1' to this bit enables the Dynamic Clock Gating feature.

Bit 0 – AP Access Port Access Allowed

Writing a '0' to this bit disables the Access Port Access Allowed.

Writing a '1' to this bit enables the Access Port Access Allowed.

10.10.2 Cache Configuration

Name: CFG
Offset: 0x04
Reset: 0x00000020
Property: R/W

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W			R/W	R/W	
Reset	0	1	0			0	0	
CSIZESW[2:0]								

Bits 6:4 – CSIZESW[2:0] Cache Size Configured by Software

This field configures the cache size.

Value	Name	Description
0x0	CONF_CSIZE_1KB	The Cache Size is configured to 1KB
0x1	CONF_CSIZE_2KB	The Cache Size is configured to 2KB
0x2	CONF_CSIZE_4KB	The Cache Size is configured to 4KB
0x3	CONF_CSIZE_8KB	The Cache Size is configured to 8KB
0x4	CONF_CSIZE_16KB	The Cache Size is configured to 16KB
0x5	CONF_CSIZE_32KB	The Cache Size is configured to 32KB
0x6	CONF_CSIZE_64KB	The Cache Size is configured to 64KB
0x7	Reserved	

Bit 2 – DCDIS Data Cache Disable

Writing a '0' to this bit enables data caching.

Writing a '1' to this bit disables data caching.

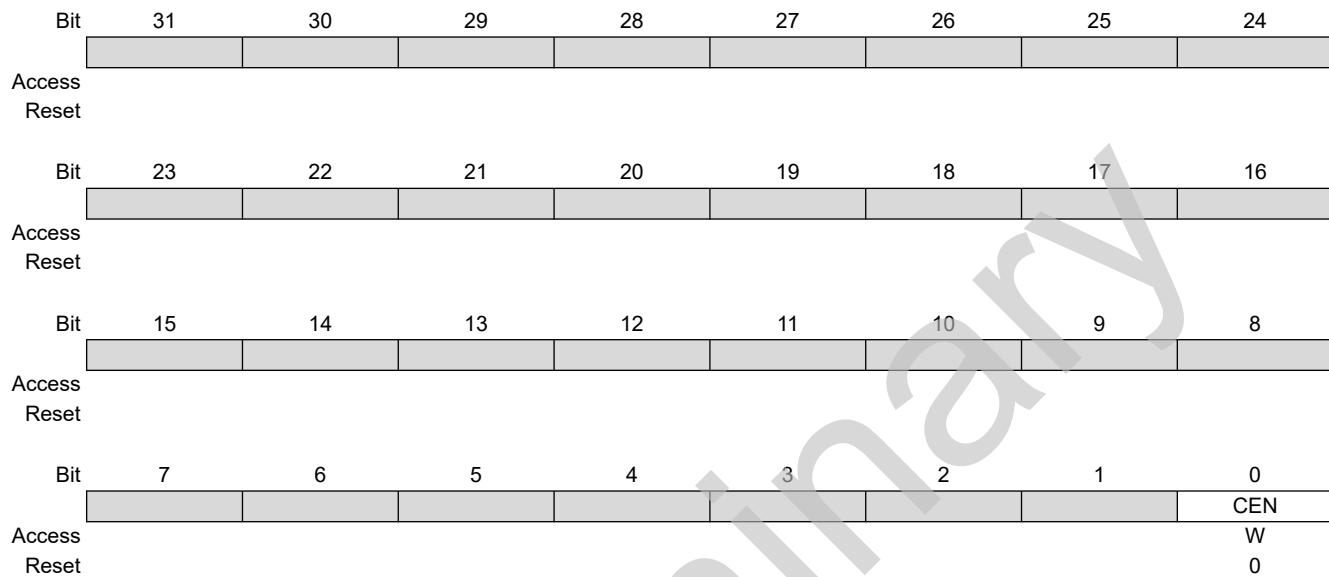
Bit 1 – ICDIS Instruction Cache Disable

Writing a '0' to this bit enables instruction caching.

Writing a '1' to this bit disables instruction caching.

10.10.3 Cache Control

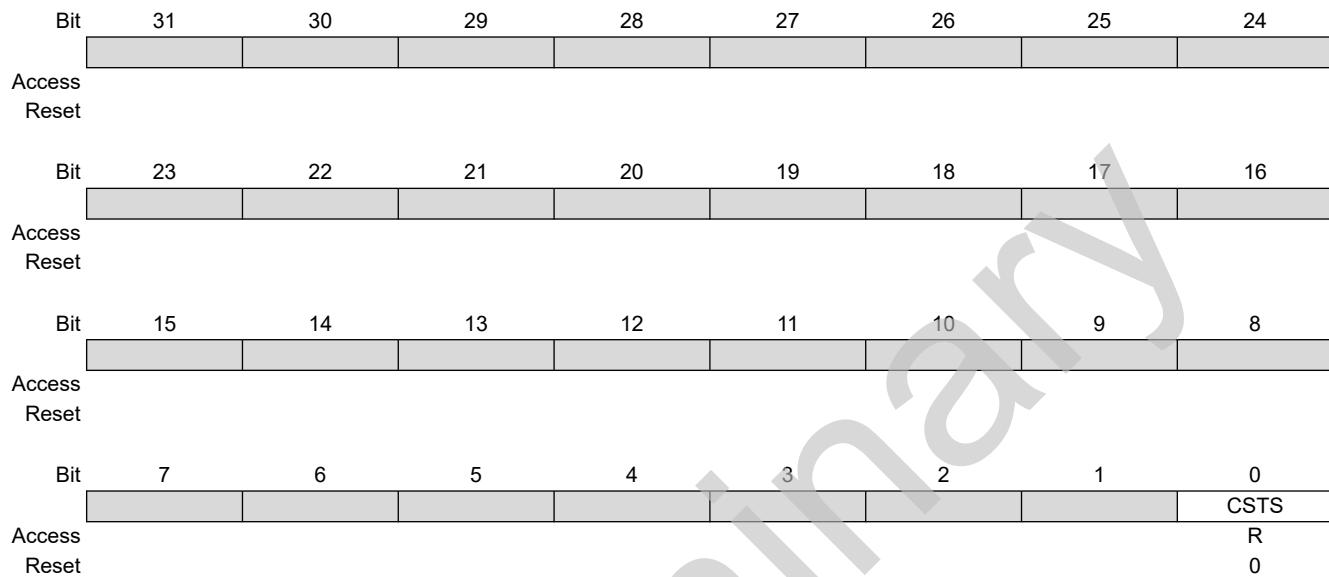
Name: CTRL
Offset: 0x08
Reset: 0x00000000
Property: Write-only



Bit 0 – CEN Cache Controller Enable
Writing a '0' to this bit disables the CMCC.
Writing a '1' to this bit enables the CMCC.

10.10.4 Cache Status

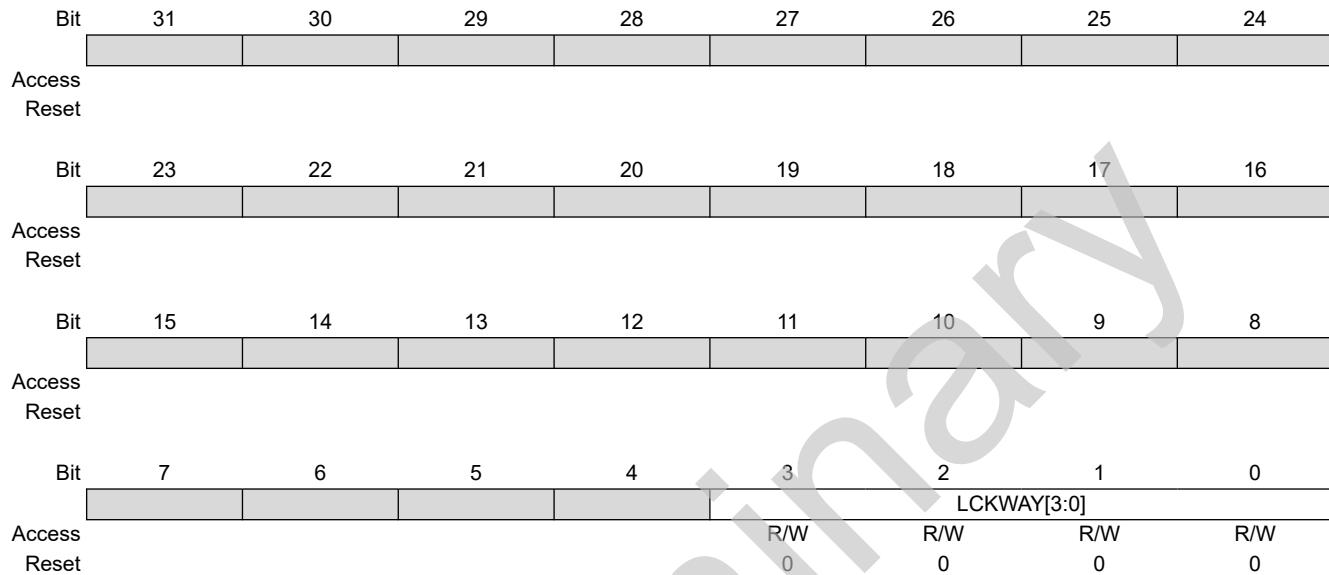
Name: SR
Offset: 0x0C
Reset: 0x00000000
Property: Read-only



Bit 0 – CSTS Cache Controller Status
Writing a '0' to this bit disables the CMCC.
Writing a '1' to this bit enables the CMCC.

10.10.5 Cache Lock per Way

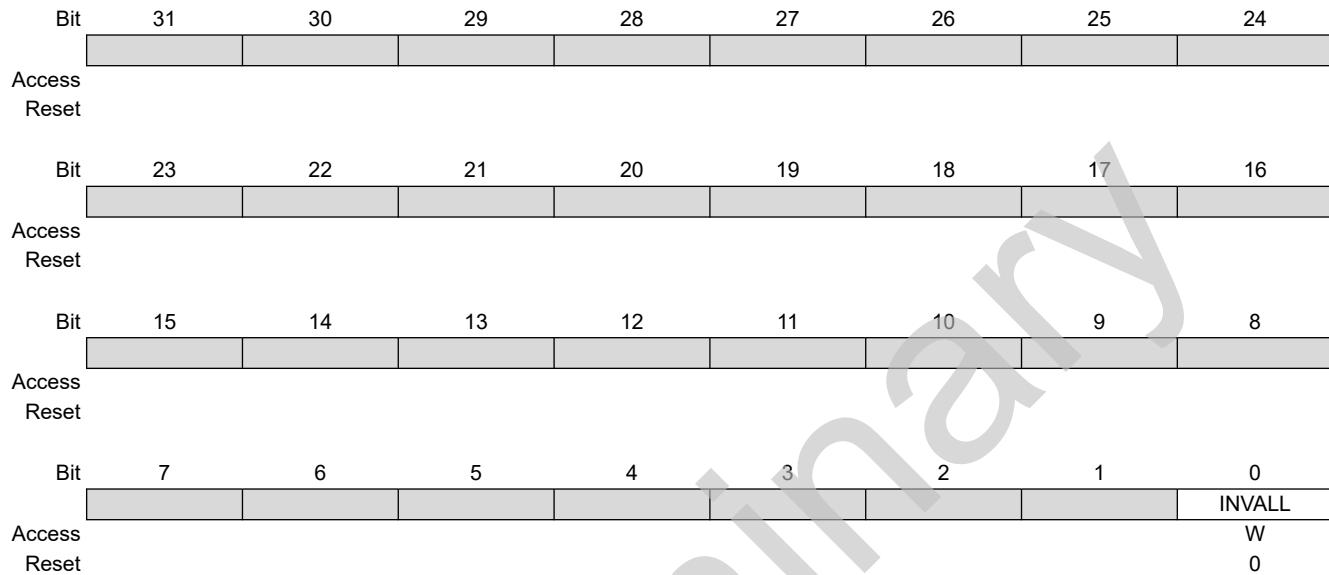
Name: LCKWAY
Offset: 0x10
Reset: 0x00000000
Property: Read/Write



Bits 3:0 – LCKWAY[3:0] Lockdown Way Register
This field selects which way is locked.

10.10.6 Cache Maintenance 0

Name: MAINT0
Offset: 0x20
Reset: 0x00000000
Property: Write-only



Bit 0 – INVALL Cache Controller Invalidate All
Writing a '0' to this bit has no effect.
Writing a '1' to this bit invalidates all cache entries.

10.10.7 Cache Maintenance 1

Name: MAINT1
Offset: 0x24
Reset: 0x00000000
Property: Write-only

Bit	31	30	29	28	27	26	25	24
WAY[3:0]								
Access	W	W	W	W				
Reset	0	0	0	0				
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
INDEX[7:4]								
Access					W	W	W	W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
INDEX[3:0]								
Access	W	W	W	W				
Reset	0	0	0	0				

Bits 31:28 – WAY[3:0] Invalidate Way

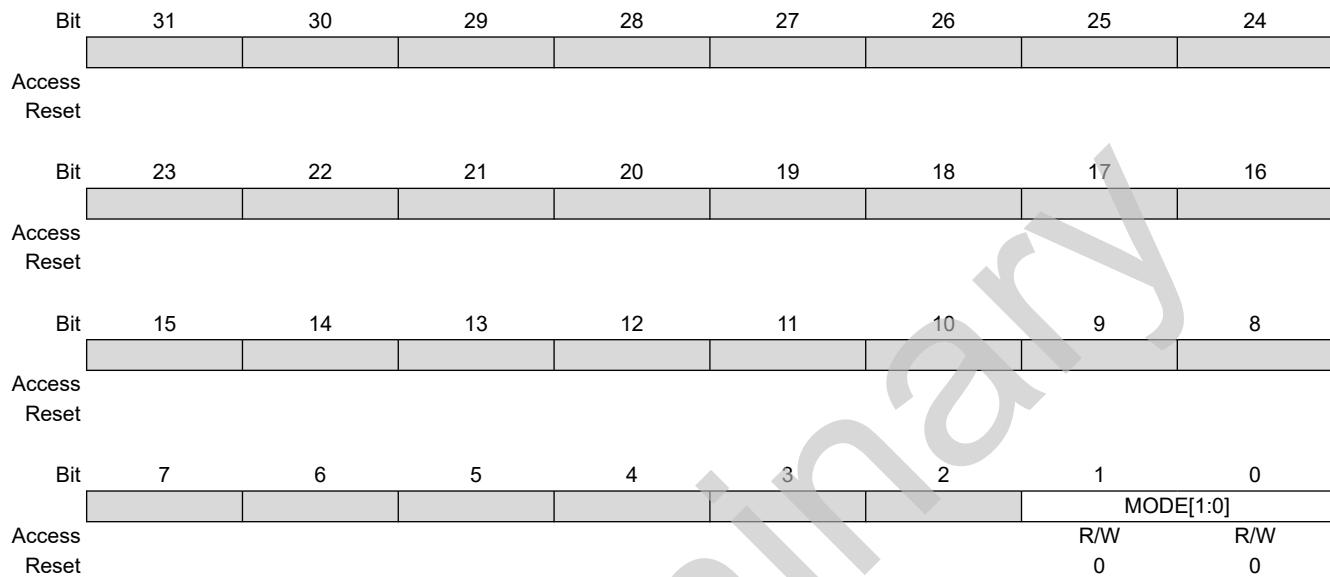
Value	Name	Description
0x0	WAY0	Way 0 is selection for index invalidation
0x1	WAY1	Way 1 is selection for index invalidation
0x2	WAY2	Way 2 is selection for index invalidation
0x3	WAY3	Way 3 is selection for index invalidation
0x4–0xF	Reserved	

Bits 11:4 – INDEX[7:0] Invalidate Index

This field selects the index value for invalidation

10.10.8 Cache Monitor Configuration

Name: MCFG
Offset: 0x28
Reset: 0x00000000
Property: Read/Write



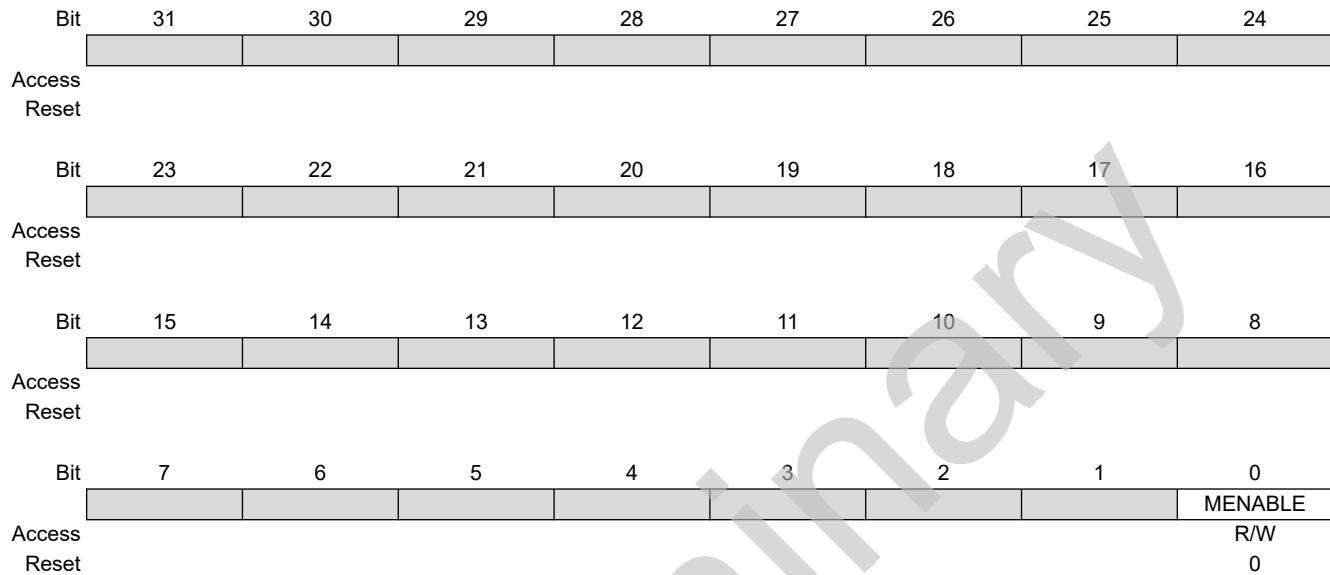
Bits 1:0 – MODE[1:0] Cache Controller Monitor Counter Mode

This field selects the type of data monitored.

Value	Name	Description
0x0	CYCLE_COUNT	Cycle counter
0x1	IHIT_COUNT	Instruction hit counter
0x2	DHIT_COUNT	Data hit counter
0x3		Reserved

10.10.9 Cache Monitor Enable

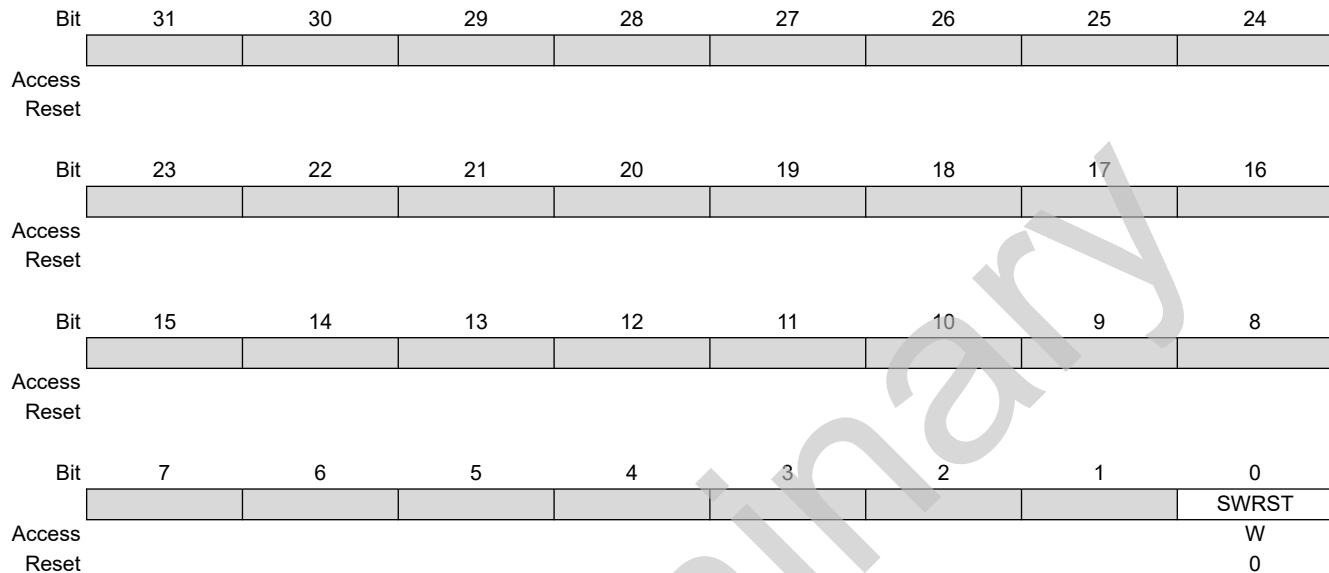
Name: MEN
Offset: 0x2C
Reset: 0x00000000
Property: Read/Write



Bit 0 – MENABLE Cache Controller Monitor Enable
Writing a '0' to this bit disables the monitor counter.
Writing a '1' to this bit enables the monitor counter.

10.10.10 Cache Monitor Control

Name: MCTRL
Offset: 0x30
Reset: 0x00000000
Property: Write-only



Bit 0 – SWRST Cache Controller Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the event counter register.

10.10.11 Cache Monitor Status

Name: MSR
Offset: 0x34
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
EVENT_CNT[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
EVENT_CNT[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
EVENT_CNT[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
EVENT_CNT[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – EVENT_CNT[31:0] Monitor Event Counter

This field indicates the Monitor Event Counter value.

11. Device Service Unit (DSU)

11.1 Overview

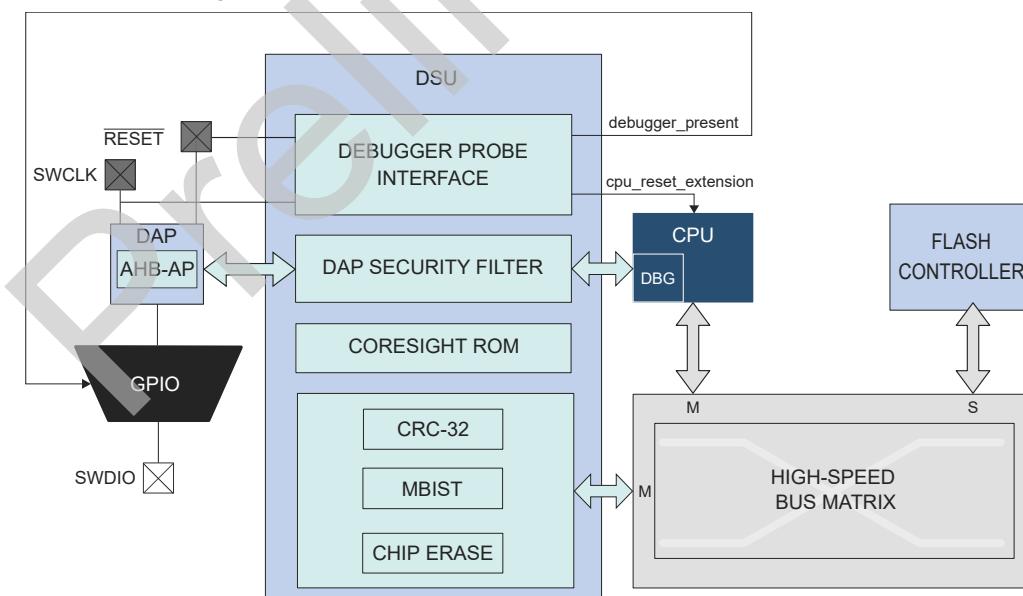
The Device Service Unit (DSU) provides a means of detecting debugger probes. It enables the ARM Debug Access Port (DAP) to have control over multiplexed debug pads and CPU Reset. The DSU also provides system-level services to debug adapters in an ARM debug system. It implements a CoreSight Debug ROM that provides device identification as well as identification of other debug components within the system. Hence, it complies with the ARM Peripheral Identification specification. The DSU also provides system services to applications that need memory testing, as required for IEC60730 Class B compliance, for example. The DSU can be accessed simultaneously by a debugger and the CPU, as it is connected on the High-Speed Bus Matrix. For security reasons, some of the DSU features will be limited or unavailable when the device is protected by the Code Protect bit.

11.2 Features

- CPU Reset Extension
- Debugger Probe Detection (Cold- and Hot-Plugging)
- Chip-Erase Command and Status
- 32-Bit Cyclic Redundancy Check (CRC32) of any Memory Accessible Through the Bus Matrix
- ARM® CoreSight™ Compliant Device Identification
- Two Debug Communications Channels
- Debug Access Port Security Filter

11.3 Block Diagram

Figure 11-1. DSU Block Diagram



11.4 Signal Description

The DSU uses three signals to function.

Signal Name	Type	Description
RESET	Digital Input	External Reset pin
SWCLK	Digital Input	SW clock pin
SWDIO	Digital I/O	SW bidirectional data pin

11.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

11.5.1 I/O Lines

The SWCLK pin is by default assigned to the DSU module to allow debugger probe detection and to stretch the CPU Reset phase, see *Debugger Probe Detection* from Related Links. The Hot-Plugging feature depends on the GPIO configuration. If the SWCLK pin function is changed in the port, the Hot-Plugging features is not disabled. Hot-Plugging is disabled with the CFGCON0.HPLUGDIS bit, which is enabled by default. Therefore to use the SWCLK pin for GPIO functions, it must be disabled by setting CFGCON0.HPLUGDIS = 1.

Related Links

[11.6.3. Debugger Probe Detection](#)

11.5.2 Power Management

The DSU will continue to operate in any sleep mode where the selected source clock is running.

11.5.3 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

[21. Direct Memory Access Controller \(DMAC\)](#)

11.5.4 Interrupts

Not applicable.

11.5.5 Events

Not applicable.

11.5.6 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Debug Communication Channel 0 register (DCC0)
- Debug Communication Channel 1 register (DCC1)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

11.5.7 Analog Connections

Not applicable.

11.6 Debug Operation

11.6.1 Principle of Operation

The DSU provides basic services to allow on-chip debug using the ARM Debug Access Port and the ARM processor debug resources:

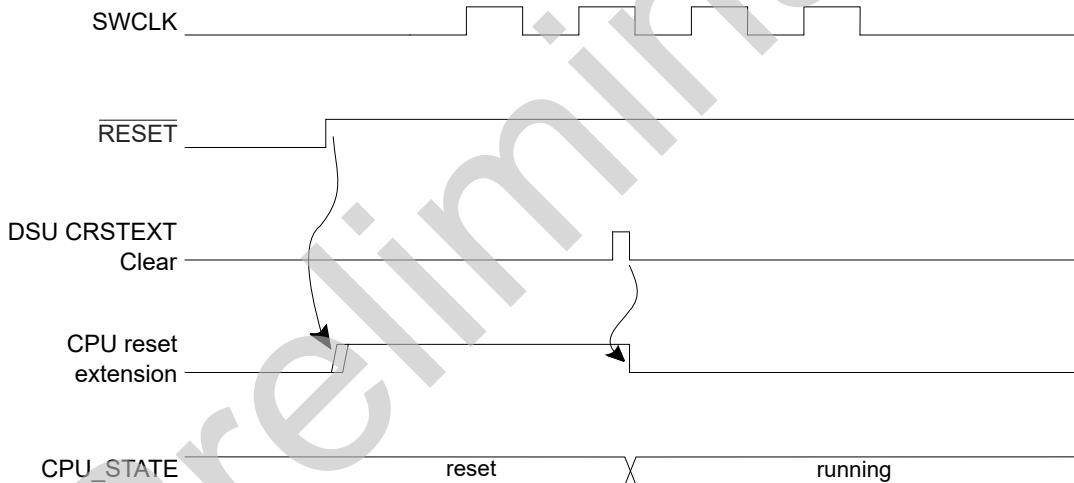
- CPU Reset extension
- Debugger probe detection

For more details on the ARM debug components, refer to the *ARM Debug Interface v5 Architecture Specification*.

11.6.2 CPU Reset Extension

“CPU Reset extension” refers to the extension of the Reset phase of the CPU core after the external Reset is released. This ensures that the CPU is not executing code at start-up while a debugger is connected to the system. The debugger is detected on a **RESET** release event when SWCLK is low. At start-up, SWCLK is internally pulled up to avoid false detection of a debugger if the SWCLK pin is left unconnected. When the CPU is held in the Reset extension phase, the CPU Reset Extension bit of the Status A register (STATUSA.CRSTEXT) is set. To release the CPU, write a ‘1’ to STATUSA.CRSTEXT. STATUSA.CRSTEXT will then be set to ‘0’. Writing a ‘0’ to STATUSA.CRSTEXT has no effect. For security reasons, it is not possible to release the CPU Reset extension when the device is protected by the Code Protect bit. Trying to do so sets the Protection Error bit (PERR) of the Status A register (STATUSA.PERR).

Figure 11-2. Typical CPU Reset Extension Set and Clear Timing Diagram



11.6.3 Debugger Probe Detection

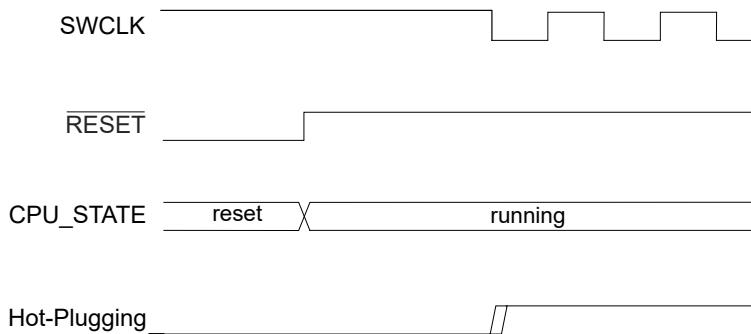
11.6.3.1 Cold Plugging

Cold-Plugging is the detection of a debugger when the system is in Reset. Cold-Plugging is detected when the CPU Reset extension is requested, as described above.

11.6.3.2 Hot Plugging

Hot-Plugging is the detection of a debugger probe when the system is not in Reset. Hot-Plugging is not possible under Reset because the detector is reset when POR or **RESET** are asserted. Hot-Plugging is active when a SWCLK falling edge is detected. The SWCLK pad is multiplexed with other functions and the user must ensure that its default function is assigned to the debug system. If the SWCLK pin function is changed in the port, the Hot-Plugging features is not disabled. Hot-Plugging is disabled with the CFGCON0.HPLUGDIS bit, which is enabled by default. Therefore to use the SWCLK pin for GPIO functions it must be Disabled by setting CFGCON0.HPLUGDIS=1. Availability of the Hot-Plugging feature can be read from the Hot-Plugging Enable bit of the Status B register (STATUSB.HPE).

Figure 11-3. Hot-Plugging Detection Timing Diagram



The presence of a debugger probe is detected when either Hot-Plugging or Cold-Plugging is detected. Once detected, the Debugger Present bit of the Status B register (STATUSB.DBGPRES) is set. For security reasons, Hot-Plugging is not available when the device is protected by the Code Protect bit.

This detection requires that pads are correctly powered. Thus, at cold start-up, this detection cannot be done until POR is released. If the device is protected, Cold-Plugging is the only way to detect a debugger probe, and so the external Reset timing must be longer than the POR timing. If external Reset is deasserted before POR release, the user must retry the procedure above until it gets connected to the device.

11.7 Chip Erase

Chip erase consists of removing all sensitive information stored in the chip and clearing the Code Protect bit. Therefore, all volatile memories and the Flash memory (including the EEPROM emulation area) will be erased. The Flash auxiliary rows, including the user row, will not be erased.

When the device is protected, the debugger must first reset the device in order to be detected. This ensures that internal registers are reset after the Protected state is removed. The chip erase operation is triggered by writing a '1' to the chip erase bit in the Control register (CTRL.CE). This command will be discarded if the DSU is protected by the Peripheral Access Controller (PAC). Once issued, the module clears volatile memories prior to erasing the Flash array. To ensure that the chip erase operation is completed, check the Done bit of the Status A register (STATUSA.DONE).

The chip erase operation depends on clocks and power management features that can be altered by the CPU. For that reason, it is recommended to issue a chip erase after a Cold-Plugging procedure to ensure that the device is in a known and Safe state.

The recommended sequence is as follows:

1. Issue the Cold-Plugging procedure (see *Cold Plugging* from Related Links). The device then:
 - a. Detects the debugger probe.
 - b. Holds the CPU in Reset.
2. Issue the chip erase command by writing a '1' to CTRL.CE. The device then:
 - a. Clears the system volatile memories.
 - b. Erases the whole Flash array (excluding OTP).
 - c. Erases the Code Protect bit protection.
3. Check for completion by polling STATUSA.DONE (read as '1' when completed).
4. Reset the device to let the Flash Controller update the fuses.

Related Links

[11.6.3.1. Cold Plugging](#)

11.8 Programming

Programming the Flash or RAM memories is only possible when the device is not protected by the Code Protect bit. The programming procedure is as follows:

1. At power-up, RESET is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold (see *Power-on Reset (POR)* from Related Links for the characteristics). The system continues to be held in this Static state until the internally regulated supplies have reached a safe Operating state.
2. The PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock and any Bus Clocks that do not have clock gate control). Internal Resets are maintained due to the external Reset.
3. The debugger maintains a low level on SWCLK. RESET is released, resulting in a debugger Cold-Plugging procedure.
4. The debugger generates a clock signal on the SWCLK pin, the Debug Access Port (DAP) receives a clock.
5. The CPU remains in Reset due to the Cold-Plugging procedure; meanwhile, the rest of the system is released.
6. A chip erase is issued to ensure that the Flash is fully erased prior to programming.
7. Programming is available through the AHB-AP. Refer to the *PIC32CX-BZ2 Programming Specification* for more details.
8. After the operation is completed, the chip can be restarted either by asserting RESET or toggling power. Make sure that the SWCLK pin is high when releasing RESET to prevent extending the CPU Reset.

Related Links

[12.18.4.2. Power-on Reset \(POR\)](#)

11.9 Intellectual Property Protection

Intellectual property protection consists of restricting access to internal memories from external tools when the device is protected, and this is accomplished by setting the Code Protect bit. This Protected state can be removed by issuing a chip erase (see *Chip Erase* from Related Links). When the device is protected, read/write accesses using the AHB-AP are limited to the DSU address range and DSU commands are restricted. When issuing a chip erase, sensitive information is erased from volatile memory and Flash.

The DSU implements a security filter that monitors the AHB transactions inside the DAP. If the device is protected, then AHB-AP read/write accesses outside the DSU external address range are discarded, causing an error response that sets the ARM AHB-AP sticky error bits (For more details, refer to the *ARM Debug Interface v5 Architecture Specification* on www.arm.com).

The DSU is intended to be accessed either:

- Internally from the CPU, without any limitation, even when the device is protected
- Externally from a debug adapter, with some restrictions when the device is protected

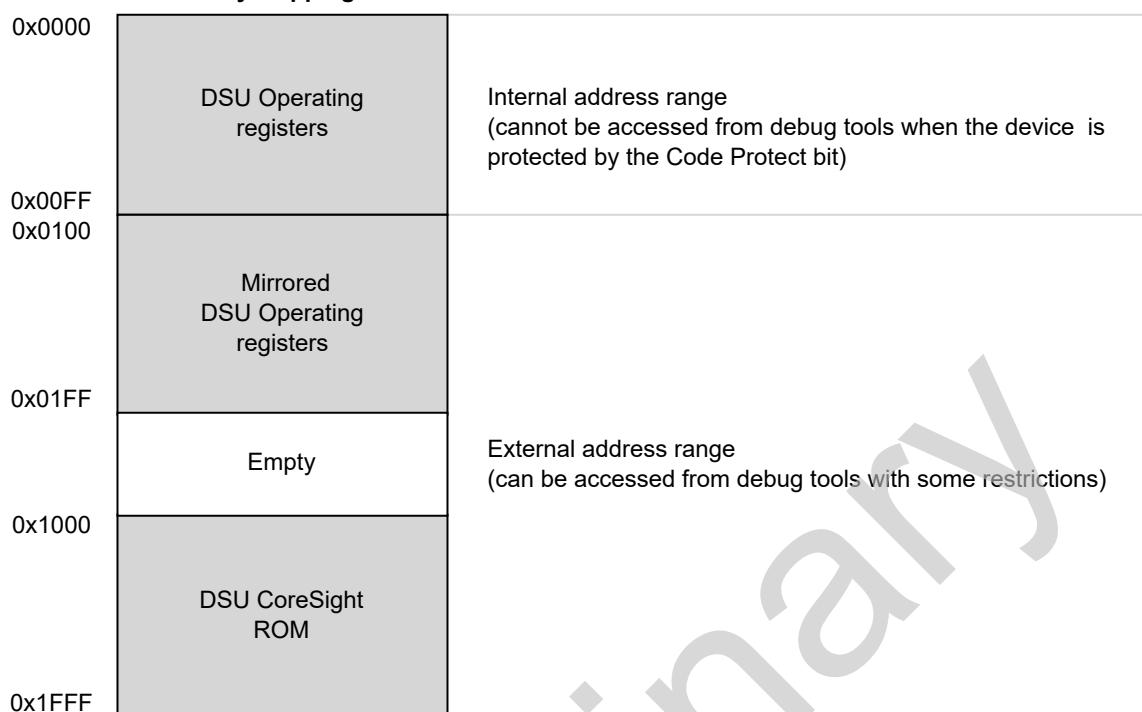
For security reasons, DSU features have limitations when used from a debug adapter. To differentiate external accesses from internal ones, the first 0x100 bytes of the DSU register map has been mirrored at offset 0x100:

- The first 0x100 bytes form the internal address range
- The next 0x100 bytes form the external address range

When the device is protected, the DAP can only issue MEM-AP accesses in the DSU range 0x0100-0x2000.

The DSU Operating registers are located in the 0x0000-0x00FF area and remapped in 0x0100-0x01FF to differentiate accesses coming from a debugger and the CPU. If the device is protected and an access is issued in the region 0x0100-0x01FF, it is subject to security restrictions. For more information, refer to the following table.

Figure 11-4. APB Memory Mapping



Some features not activated by APB transactions are not available when the device is protected:

Table 11-1. Feature Availability Under Protection

Features	Availability When the Device is Protected
CPU Reset Extension	Yes
Clear CPU Reset Extension	No
Debugger Cold-Plugging	Yes
Debugger Hot-Plugging	No

Related Links

[11.7. Chip Erase](#)

11.10 Device Identification

Device identification relies on the ARM CoreSight component identification scheme, which allows the chip to be identified as a SAM device implementing a DSU. The DSU contains identification registers to differentiate the device.

11.10.1 CoreSight Identification

A system-level ARM® CoreSight™ ROM table is present in the device to identify the vendor and the chip identification method. Its address is provided in the MEM-AP BASE register inside the ARM Debug Access Port. The CoreSight ROM implements a 64-bit conceptual ID composed as follows from the PID0 to PID7 CoreSight ROM Table registers:

Figure 11-5. Conceptual 64-bit Peripheral ID

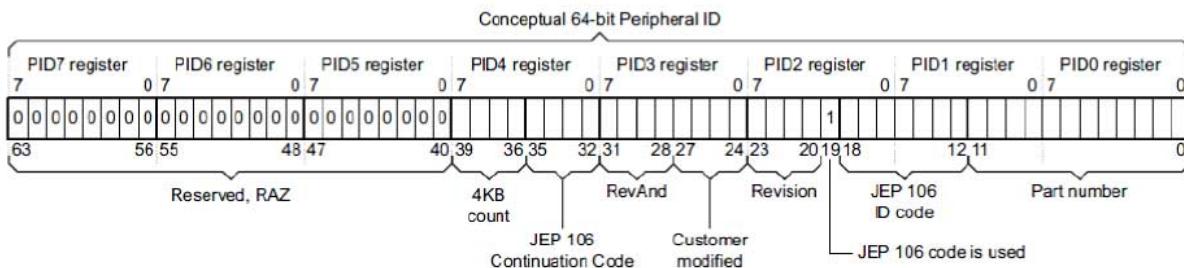


Table 11-2. Conceptual 64-Bit Peripheral ID Bit Descriptions

Field	Size	Description	Location
JEP-106 CC code	4	Microchip continuation code: 0x0	PID4
JEP-106 ID code	7	Microchip device ID: 0x29	PID1+PID2
4KB count	4	Indicates that the CoreSight component is a ROM: 0x0	PID4
RevAnd	4	Not used; read as 0	PID3
CUSMOD	4	Not used; read as 0	PID3
PARTNUM	12	Contains 0xCD0 to indicate that DSU is present	PID0+PID1
REVISION	4	DSU revision (starts at 0x0 and increments by 1 at both major and minor revisions). Identifies DSU identification method variants. If 0x0, this indicates that device identification can be completed by reading the Device Identification register (DID)	PID2

For more details, refer to the *ARM Debug Interface Version 5 Architecture Specification*.

11.10.2 Chip Identification Method

The DSU DID register identifies the device as shown in the following table:

Table 11-3. DSU DID Encoding

Field	Size	Value	Comments
Revision	4 bits	0x0	Immutable Field (0x0=Rev-A0)
Family	5 bits	0b00000	Family[4:0]
Series	6 bits	0b00000	Series[5:0]
Die	8 bits	0x9B	Immutable Field = Mask ID [7:0]
DEVSEL	8 bits	Flash Fuses	Determines variants of product {VSEL[7:0]} [0x8F 0x0B]

11.11 Functional Description

11.11.1 Principle of Operation

The DSU provides memory services, such as CRC32 that require almost the same interface. Hence, the Address, Length and Data registers (ADDR, LENGTH, DATA) are shared. These shared registers must be configured first; then a command can be issued by writing the Control register. When a command is ongoing, other commands are

discarded until the current operation is completed. Hence, the user must wait for the STATUSA.DONE bit to be set prior to issuing another one.

11.11.2 Basic Operation

11.11.2.1 Initialization

The module is enabled by enabling its clocks, see *Clock and Reset (CRU)* from Related Links. The DSU registers can be PAC write-protected, see *Peripheral Access Controller (PAC)* from Related Links.

Related Links

- [12. Clock and Reset Unit \(CRU\)](#)
- [25. Peripheral Access Controller \(PAC\)](#)

11.11.2.2 Operation From a Debug Adapter

Debug adapters should access the DSU registers in the external address range 0x100 – 0x2000. If the device is protected by the Code Protect bit, accessing the first 0x100 bytes causes the system to return an error. See *Intellectual Property Protection* from Related Links.

Related Links

- [11.9. Intellectual Property Protection](#)

11.11.2.3 Operation From the CPU

There are no restrictions when accessing DSU registers from the CPU. However, the user must access DSU registers in the internal address range (0x0–0x100) to avoid external security restrictions. See *Intellectual Property Protection* from Related Links.

Related Links

- [11.9. Intellectual Property Protection](#)

11.11.3 32-bit Cyclic Redundancy Check CRC32

The DSU unit provides support for calculating a cyclic redundancy check (CRC32) value for a memory area (including Flash and AHB RAM).

When the CRC32 command is issued from:

- The internal range, the CRC32 can be operated at any memory location
- The external range, the CRC32 operation is restricted; DATA, ADDR, and LENGTH values are forced (see below)

Table 11-4. AMOD Bit Descriptions when Operating CRC32

AMOD[1:0]	Short name	External range restrictions
0	ARRAY	CRC32 is restricted to the full Flash array area (EEPROM emulation area not included) DATA forced to 0xFFFFFFFF before calculation (no seed)
1	EEPROM	CRC32 of the whole EEPROM emulation area DATA forced to 0xFFFFFFFF before calculation (no seed)
2-3	Reserved	

The algorithm employed is the industry standard CRC32 algorithm using the generator polynomial 0xEDB88320 (reversed representation).

11.11.3.1 Starting CRC32 Calculation

CRC32 calculation for a memory range is started after writing the start address into the Address register (ADDR) and the size of the memory range into the Length register (LENGTH). Both must be word-aligned.

The initial value used for the CRC32 calculation must be written to the Data register (DATA). This value will usually be 0xFFFFFFFF, but can be, for example, the result of a previous CRC32 calculation if generating a common CRC32 of separate memory blocks.

Once completed, the calculated CRC32 value can be read out of the Data register. The read value must be complemented to match standard CRC32 implementations or kept noninverted if used as starting point for subsequent CRC32 calculations.

The actual test is started by writing a '1' in the 32-bit Cyclic Redundancy Check bit of the Control register (CTRL.CRC). A running CRC32 operation can be canceled by resetting the module (writing '1' to CTRL.SWRST).

11.11.3.2 Interpreting the Results

The user should monitor the Status A register. When the operation is completed, STATUSA.DONE is set. Then the Bus Error bit of the Status A register (STATUSA.BERR) must be read to ensure that no bus error occurred.

11.11.4 Debug Communication Channels

The Debug Communication Channels (DCC0 and DCC1) consist of a pair of registers with associated handshake logic, accessible by both CPU and debugger even if the device is protected by the Code Protect bit. The registers can be used to exchange data between the CPU and the debugger, during run time as well as in Debug mode. This enables the user to build a custom debug protocol using only these registers.

The DCC0 and DCC1 registers are accessible when the Protected state is active. When the device is protected, however, it is not possible to connect a debugger while the CPU is running (STATUSA.CRSTEXT is not writable and the CPU is held under Reset).

Two Debug Communication Channel status bits in the Status B registers (STATUS.DCCDx) indicate whether a new value has been written in DCC0 or DCC1. These bits, DCC0D and DCC1D, are located in the STATUSUSB registers. They are automatically set on write and cleared on read.

Note: The DCC0 and DCC1 registers are shared with the on-board memory testing logic (MBIST). Accordingly, DCC0 and DCC1 must not be used while performing MBIST operations.

11.11.5 System Services Availability when Accessed Externally and Device is Protected

External access: Access performed in the DSU address offset 0x200-0x1FFF range.

Internal access: Access performed in the DSU address offset 0x000-0x100 range.

Table 11-5. Available Features when Operated From The External Address Range and Device is Protected

Features	Availability From The External Address Range and Device is Protected
Chip erase command and status	Yes
CRC32	Yes, only full array or full EEPROM
CoreSight Compliant Device identification	Yes
Debug communication channels	Yes
STATUSA.CRSTEXT clearing	No (STATUSA.PERR is set when attempting to do so)

11.12 DSU Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRL	7:0				CE				SWRST
0x01	STATUSA	7:0				PERR	FAIL	BERR	CRSTEXT	DONE
0x02	STATUSB	7:0			CELCK	HPE	DCCD1	DCCD0	DBGPRES	PROT
0x03	Reserved									
0x04	ADDR	7:0				ADDR[5:0]				AMOD[1:0]
		15:8					ADDR[13:6]			
		23:16					ADDR[21:14]			
		31:24					ADDR[29:22]			
0x08	LENGTH	7:0				LENGTH[5:0]				
		15:8					LENGTH[13:6]			
		23:16					LENGTH[21:14]			
		31:24					LENGTH[29:22]			
0x0C	DATA	7:0					DATA[7:0]			
		15:8					DATA[15:8]			
		23:16					DATA[23:16]			
		31:24					DATA[31:24]			
0x10	DCC0	7:0					DATA[7:0]			
		15:8					DATA[15:8]			
		23:16					DATA[23:16]			
		31:24					DATA[31:24]			
0x14	DCC1	7:0					DATA[7:0]			
		15:8					DATA[15:8]			
		23:16					DATA[23:16]			
		31:24					DATA[31:24]			
0x18	DID	7:0					DEVSEL[7:0]			
		15:8					DIE[7:0]			
		23:16	FAMILY[0]					SERIES[5:0]		
		31:24		REVISION[3:0]					FAMILY[4:1]	
0x1C ... 0xFFFF	Reserved									
0x1000	ENTRY0	7:0							FMT	EPRES
		15:8			ADDOFF[3:0]					
		23:16					ADDOFF[11:4]			
		31:24					ADDOFF[19:12]			
0x1004	ENTRY1	7:0							FMT	EPRES
		15:8			ADDOFF[3:0]					
		23:16					ADDOFF[11:4]			
		31:24					ADDOFF[19:12]			
0x1008	END	7:0					END[7:0]			
		15:8					END[15:8]			
		23:16					END[23:16]			
		31:24					END[31:24]			
0x100C ... 0x1FCB	Reserved									
0x1FCC	MEMTYPE	7:0								SMEMP
		15:8								
		23:16								
		31:24								
0x1FD0	PID4	7:0			FKBC[3:0]			JEPCC[3:0]		
		15:8								
		23:16								
		31:24								

PIC32CX-BZ2 and WBZ45 Family Device Service Unit (DSU)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1FD4										
...										
0x1FDF	Reserved									
		7:0								
0x1FE0	PID0	15:8								
		23:16								
		31:24								
0x1FE4	PID1	7:0			JEPIDCL[3:0]					
		15:8								
		23:16								
		31:24								
0x1FE8	PID2	7:0			REVISION[3:0]			JEPU		JEPIDCH[2:0]
		15:8								
		23:16								
		31:24								
0x1FEC	PID3	7:0			REVAND[3:0]					CUSMOD[3:0]
		15:8								
		23:16								
		31:24								
0x1FF0	CID0	7:0						PREAMBLEB0[7:0]		
		15:8								
		23:16								
		31:24								
0x1FF4	CID1	7:0			CCLASS[3:0]					PREAMBLE[3:0]
		15:8								
		23:16								
		31:24								
0x1FF8	CID2	7:0						PREAMBLEB2[7:0]		
		15:8								
		23:16								
		31:24								
0x1FFC	CID3	7:0						PREAMBLEB3[7:0]		
		15:8								
		23:16								
		31:24								

11.13 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Related Links

[11.5.6. Register Access Protection](#)

11.13.1 Control

Name: CTRL
Offset: 0x0000
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				CE				SWRST
Access					W			W
Reset				0				0

Bit 4 – CE Chip-Erase

Writing a '0' to this bit has no effect.

Writing a '1' to this bit starts the Chip-Erase operation.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the module.

11.13.2 Status A

Name: STATUSA
Offset: 0x0001
Reset: 0x00
Property: PAC Write Protection

Bit	7	6	5	4	3	2	1	0
Access				PERR	FAIL	BERR	CRSTEXT	DONE
Reset				R/W	R/W	R/W	R/W	R/W

Bit 4 – PERR Protection Error

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Protection Error bit.

This bit is set when a command that is not allowed in Protected state is issued.

Bit 3 – FAIL Failure

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Failure bit.

This bit is set when a DSU operation failure is detected.

Bit 2 – BERR Bus Error

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Bus Error bit.

This bit is set when a bus error is detected.

Bit 1 – CRSTEXT CPU Reset Phase Extension

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the CPU Reset Phase Extension bit.

This bit is set when a debug adapter Cold-Plugging is detected, which extends the CPU Reset phase.

Bit 0 – DONE Done

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Done bit.

This bit is set when a DSU operation is completed.

11.13.3 Status B

Name: STATUSB
Offset: 0x0002
Reset: 0x0x
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access			CELCK	HPE	DCCD1	DCCD0	DBGRES	PROT
Reset			R	R	R	R	R	R

Bit 5 – CELCK Chip Erase Locked

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when Chip Erase is locked.

This bit is cleared when Chip Erase is unlocked.

Bit 4 – HPE Hot-Plugging Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when Hot-Plugging is enabled.

This bit is cleared when Hot-Plugging is disabled. This is the case when the SWCLK function is changed. Only a power-reset or a external reset can set it again.

Bits 2, 3 – DCCD Debug Communication Channel x Dirty

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when DCC is written.

This bit is cleared when DCC is read.

Bit 1 – DBGRES Debugger Present

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when a debugger probe is detected.

This bit is never cleared.

Bit 0 – PROT Protected

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set at power-up when the device is protected.

This bit is never cleared.

11.13.4 Address

Name: ADDR
Offset: 0x0004
Reset: 0x00000000
Property: PAC Write Protection

Bit	31	30	29	28	27	26	25	24
ADDR[29:22]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[21:14]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[13:6]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[5:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
AMOD[1:0]								

Bits 31:2 – ADDR[29:0] Address

Initial word start address needed for memory operations.

Bits 1:0 – AMOD[1:0] Access Mode

The functionality of these bits is dependent on the operation mode.

Bit description when operating CRC32, see *32-bit Cyclic Redundancy Check CRC32* from Related Links.

Related Links

[11.11.3. 32-bit Cyclic Redundancy Check CRC32](#)

11.13.5 Length

Name: LENGTH
Offset: 0x0008
Reset: 0x00000000
Property: PAC Write Protection

Bit	31	30	29	28	27	26	25	24
LENGTH[29:22]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
LENGTH[21:14]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
LENGTH[13:6]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
LENGTH[5:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:2 – LENGTH[29:0] Length

Length in words needed for memory operations.

11.13.6 Data

Name: DATA
Offset: 0x000C
Reset: 0x00000000
Property: PAC Write Protection

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data

Memory operation initial value or result value.

11.13.7 Debug Communication Channel x

Name: DCC
Offset: 0x10 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data
Data register.

11.13.8 Device Identification

Name: DID
Offset: 0x0018
Property: PAC Write Protection

Bit	31	30	29	28	27	26	25	24	
	REVISION[3:0]								
Access	R	R	R	R	R	R	R	R	
Reset	p	p	p	p	f	f	f	f	
Bit	23	22	21	20	19	18	17	16	
	FAMILY[0]		SERIES[5:0]						
Access	R		R	R	R	R	R	R	
Reset	f		s	s	s	s	s	s	
Bit	15	14	13	12	11	10	9	8	
	DIE[7:0]								
Access	R	R	R	R	R	R	R	R	
Reset	d	d	d	d	d	d	d	d	
Bit	7	6	5	4	3	2	1	0	
	DEVSEL[7:0]								
Access	R	R	R	R	R	R	R	R	
Reset	x	x	x	x	x	x	x	x	

Bits 31:28 – REVISION[3:0] Processor

The value of this field identifies the die revision number. 0x0=rev.A0.

Bits 27:23 – FAMILY[4:0] Product Family

The value of this field corresponds to the product family part of the ordering code. For this device, the value of this field is 0x0.

Bits 21:16 – SERIES[5:0] Product Series

The value of this field corresponds to the product series part of the ordering code. For this device, the value of this field is 0x01, corresponding to a product with the Cortex-M0+ processor with DMA and USB features.

Bits 15:8 – DIE[7:0] Die Number

Identifies the die family.

Bits 7:0 – DEVSEL[7:0] Device Selection

This bit field identifies a device within a product family and product series. The value corresponds to the Flash memory density, pin count and device variant parts of the ordering code.

11.13.9 CoreSight ROM Table Entry x

Name: ENTRY
Offset: 0x1000 + n*0x04 [n=0..1]
Reset: 0xxxxxx00x
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
ADDOFF[19:12]								
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x
ADDOFF[11:4]								
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x
ADDOFF[3:0]								
Access	R	R	R	R				
Reset	x	x	x	x				
FMT EPRES								
Access						R	R	
Reset						1	x	

Bits 31:12 – ADDOFF[19:0] Address Offset

The base address of the component, relative to the base address of this ROM table.

Bit 1 – FMT Format

Always reads as '1', indicating a 32-bit ROM table.

Bit 0 – EPRES Entry Present

This bit indicates whether an entry is present at this location in the ROM table.

This bit is set at power-up if the device is not protected indicating that the entry is not present.

This bit is cleared at power-up if the device is not protected indicating that the entry is present.

11.13.10 CoreSight ROM Table End

Name: END
Offset: 0x1008
Reset: 0x00000000
Property: -

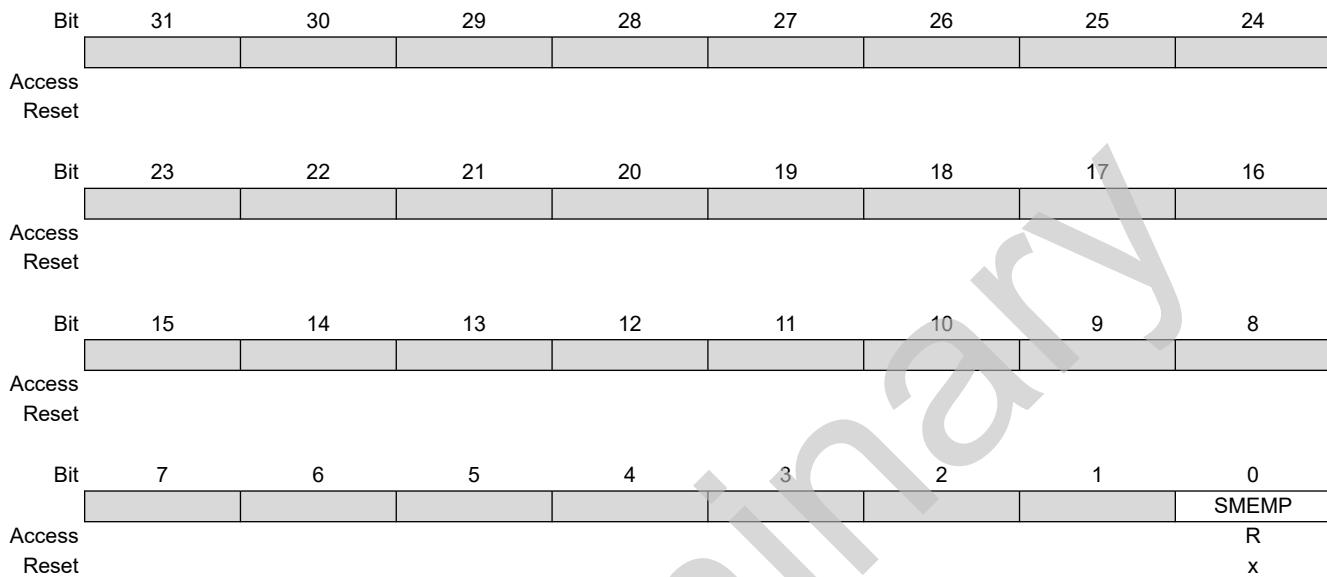
Bit	31	30	29	28	27	26	25	24
END[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
END[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
END[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
END[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – END[31:0] End Marker

Indicates the end of the CoreSight ROM table entries.

11.13.11 CoreSight ROM Table Memory Type

Name: MEMTYPE
Offset: 0x1FCC
Reset: 0x0000000X
Property: -



Bit 0 – SMEMP System Memory Present

This bit indicates whether system memory is present on the bus that connects to the ROM table.

This bit is set at power-up if the device is not protected, indicating that the system memory is accessible from a debug adapter.

This bit is cleared at power-up if the device is protected, indicating that the system memory is not accessible from a debug adapter.

11.13.12 Peripheral Identification 4

Name: PID4
Offset: 0x1FD0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	FKBC[3:0]				JEPCC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – FKBC[3:0] 4KB Count

These bits will always return zero when read, indicating that this debug component occupies one 4KB block.

Bits 3:0 – JEPCC[3:0] JEP-106 Continuation Code

These bits will always return zero when read.

11.13.13 Peripheral Identification 0

Name: PID0
Offset: 0x1FE0
Reset: 0x000000D0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				PARTNBL[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PARTNBL[7:0] Part Number Low

These bits will always return 0xD0 when read, indicating that this device implements a DSU module instance.

11.13.14 Peripheral Identification 1

Name: PID1
Offset: 0x1FE4
Reset: 0x000000FC
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	JEPIDCL[3:0]				PARTNBH[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	1	1	1	0	0

Bits 7:4 – JEPIDCL[3:0] Low Part of the JEP-106 Identity Code
 These bits will always return 0xF when read (JEP-106 identity code is 0x1F).

Bits 3:0 – PARTNBH[3:0] Part Number High
 These bits will always return 0xC when read, indicating that this device implements a DSU module instance.

11.13.15 Peripheral Identification 2

Name: PID2
Offset: 0x1FE8
Reset: 0x00000009
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
			REVISION[3:0]		JEPU		JEPIDCH[2:0]	
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	1	0	0	1

Bits 7:4 – REVISION[3:0] Revision Number

Revision of the peripheral. Starts at 0x0 and increments by one at both major and minor revisions.

Bit 3 – JEPU JEP-106 Identity Code is Used

This bit will always return one when read, indicating that JEP-106 code is used.

Bits 2:0 – JEPIDCH[2:0] JEP-106 Identity Code High

These bits will always return 0x1 when read, (JEP-106 identity code is 0x1F).

11.13.16 Peripheral Identification 3

Name: PID3
Offset: 0x1FEC
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	REVAND[3:0]				CUSMOD[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – REVAND[3:0] Revision Number
 These bits will always return 0x0 when read.

Bits 3:0 – CUSMOD[3:0] ARM CUSMOD
 These bits will always return 0x0 when read.

11.13.17 Component Identification 0

Name: CID0
Offset: 0x1FF0
Reset: 0x0000000D
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				PREAMBLEB0[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	1	1	0	1

Bits 7:0 – PREAMBLEB0[7:0] Preamble Byte 0
These bits will always return 0x0000000D when read.

11.13.18 Component Identification 1

Name: CID1
Offset: 0x1FF4
Reset: 0x00000010
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
			CCLASS[3:0]			PREAMBLE[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	1	0	0	0	0

Bits 7:4 – CCLASS[3:0] Component Class

These bits will always return 0x1 when read indicating that this ARM CoreSight component is ROM table (For more details, refer to the *ARM Debug Interface v5 Architecture Specification* at <http://www.arm.com>).

Bits 3:0 – PREAMBLE[3:0] Preamble

These bits will always return 0x00 when read.

11.13.19 Component Identification 2

Name: CID2
Offset: 0x1FF8
Reset: 0x00000005
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				PREAMBLEB2[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	0	1

Bits 7:0 – PREAMBLEB2[7:0] Preamble Byte 2
These bits will always return 0x00000005 when read.

11.13.20 Component Identification 3

Name: CID3
Offset: 0x1FFC
Reset: 0x000000B1
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				PREAMBLEB3[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	1	0	1	1	0	0	0	1

Bits 7:0 – PREAMBLEB3[7:0] Preamble Byte 3
These bits will always return 0x000000B1 when read.

12. Clock and Reset Unit (CRU)

12.1 Overview

The PIC32CX-BZ2 Clock System provides both clocking and reset functions. This chapter describes the clocking functionality, summarizes the clock distribution and terminology in the PIC32CX-BZ2 device. For more details on configuration, see the respective peripherals descriptions. Clock control is handled by the CRU to provide system clocks and interface peripheral clocks. CRU controls switching and synchronization of clock sources.

For details on Reset functionality, see *Resets* from Related Links.

Related Links

[12.18. Resets](#)

12.2 Features

The Clock and Reset Unit has the following features:

- Supports the following as system clock sources:
 - 16 MHz Primary Crystal Oscillator (POSC)
 - 8 MHz Fast RC Oscillator (FRC)
 - 32 kHz Low Power RC Oscillator (LPRC)
 - 32.768 kHz Secondary Crystal Oscillator (SOSC)
 - 96 MHz System PLL (RFPLL)
- Provides control registers for all PLLs
- Provides for glitch-free clock switching between various clock sources
- Post dividers on processor clock generator to slow down system clock for power save
- A fail safe clock monitor that detects clock failure and provides automatic switching to the FRC
- Provides control registers for user interface of clocks and resets
- Provides configuration bits for oscillator selection and calibration of on-chip oscillators
- Provides control registers to generate a reference clock output
- Provide resets for the system
- Provides NMI interrupts for the system
- Multiple PB clock dividers
- One System Clock, `cru_sys_clk`, from which almost all clocks used throughout the system are derived
- Three Peripheral Clocks, created by independent integer dividers of the `sys_clk`:
 - `pb1_clk`: PB-PIC and PB-Bridge-A Bus
 - `pb2_clk`: PB-Bridge-B and PB-Bridge-C
 - `pb3_clk`: DS/XDS Bus Clock.
- Six Reference Output Clocks (REFO1 - REFO6) with the following clock sources:
 - System Clock
 - PB1 Bus Clock
 - 16 MHz Primary Crystal Oscillator (POSC)
 - 8 MHz Fast RC Oscillator (FRC)
 - 32 kHz Low Power RC Oscillator (LPRC)
 - 32.768 kHz Secondary Crystal Oscillator (SOSC)
 - 96 MHz System PLL (RFPLL)
 - 64 MHz System PLL (RFPLL PGM MHz)
 - REFI Pin
 - Sleep Control, supporting Req/Ack signaling with the bus matrix to determine that no transactions are in flight when initiating Sleep.

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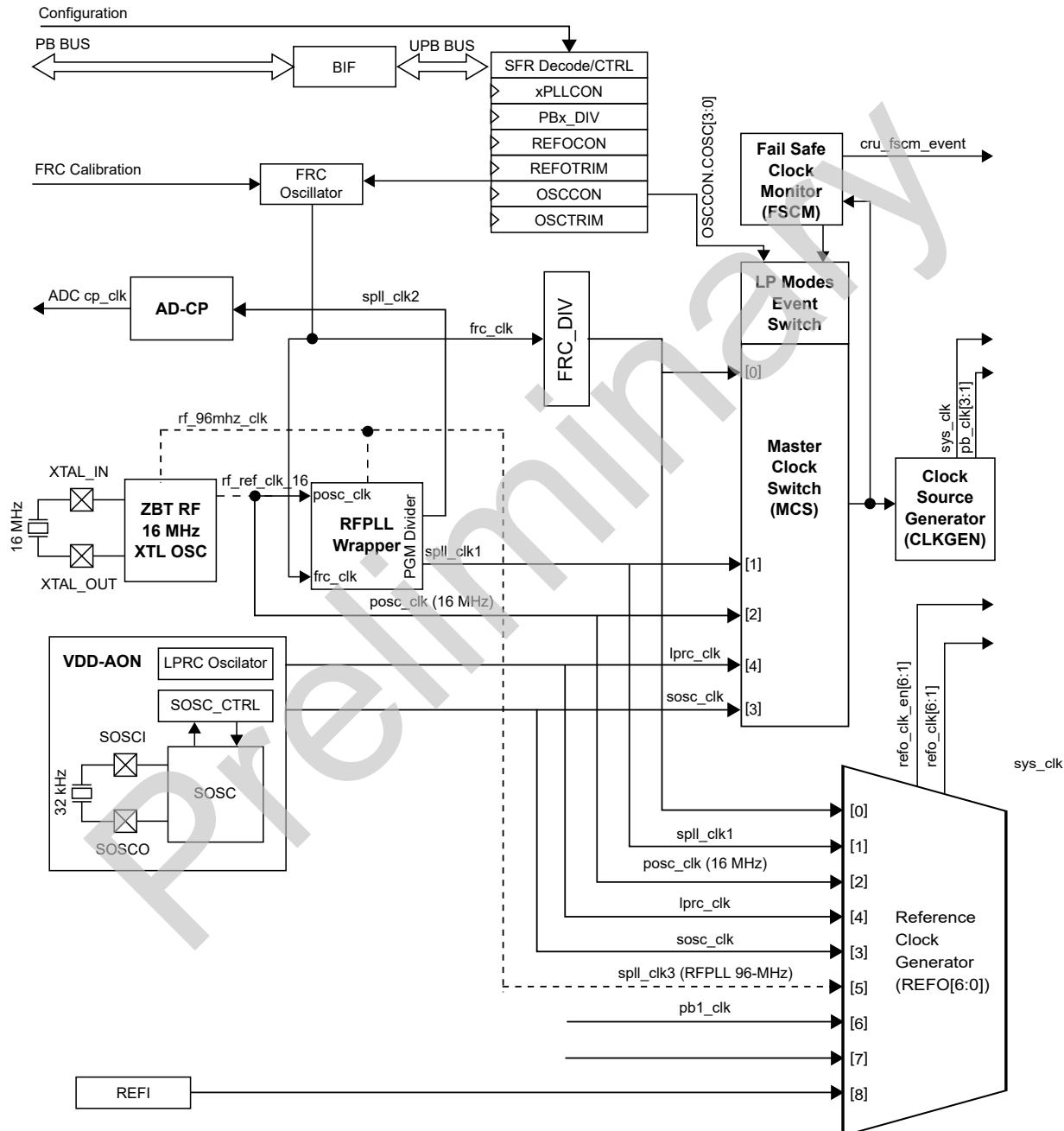
Clock and Reset Unit (CRU)

- JTAG TCK clock control

12.3 Block Diagram

The CRU along with the PMD provides gated clock output for all peripheral buses. The following figure shows the CRU block diagram.

Figure 12-1. Clock and Reset Unit Block Diagram



PIC32CX-BZ2 and WBZ45 Family Clock and Reset Unit (CRU)

Figure 12-2. RFPLL Wrapper

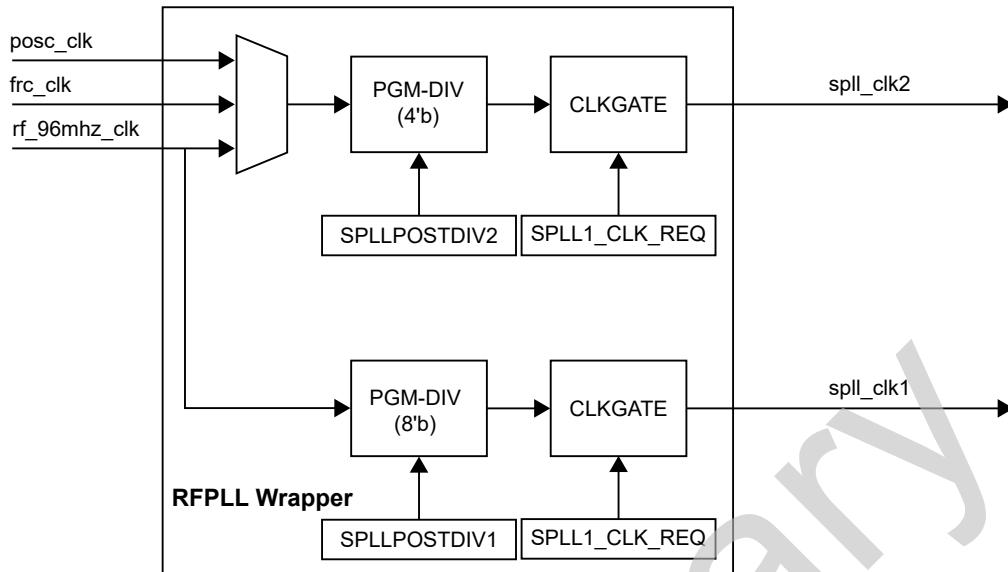
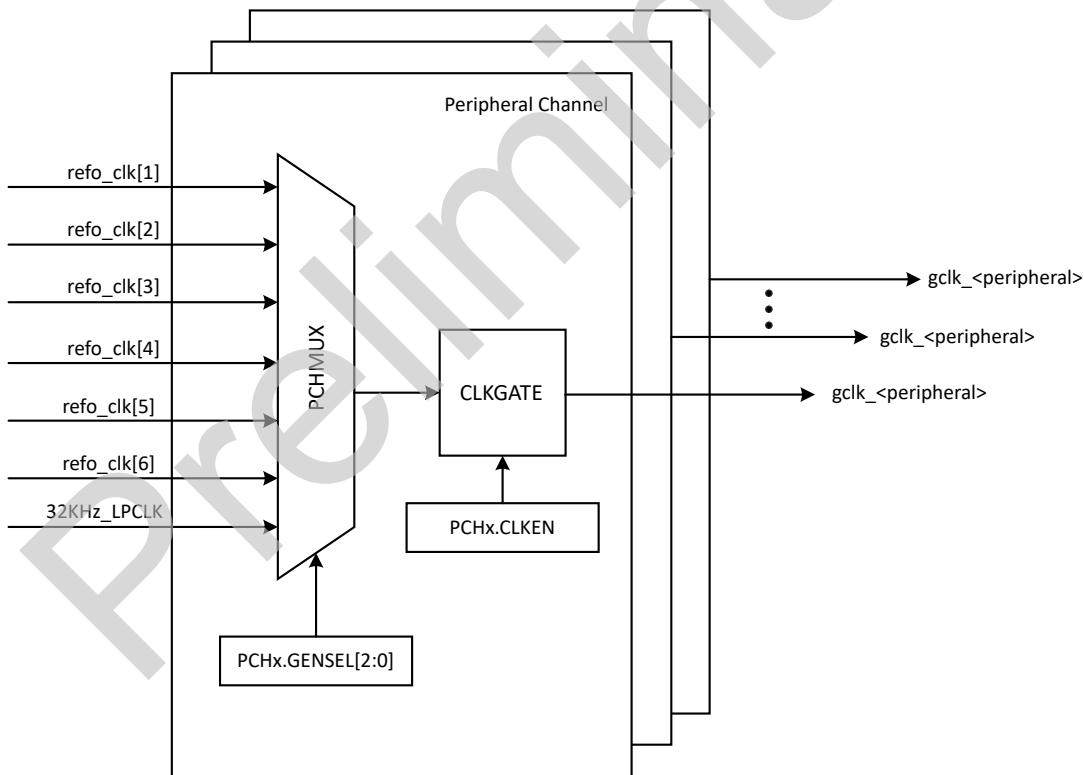


Figure 12-3. Peripheral Clock Generation



The CRU Master Clock Switch selects which input clock is fed to the CLKGEN Synchronous Clock Generator. The CLKGEN generates and controls the synchronous clocks on the system. This includes the CPU, bus clocks (APB and AHB) and the synchronous (to the CPU) user interfaces of the peripherals. It contains prescalers for the CPU and bus clocks.

12.4 System and Peripheral Clock Generation (CLKGEN)

This sub-module generates system clocks needed for the device from a single source clock. In addition, this module also shuts down these clocks during Sleep mode.

There are two types of clocks generated by this block, called core clocks and peripheral clocks. The system clock (`sys_clk`) is typically used by the CPU, it supports components such as memory subsystems, and fast peripherals. The peripheral bus clocks (`pb_clk`) are used to clock slow peripheral devices attached to the `pb_bus`. The `pb_clk[n]` outputs are based on the `sys_clk` frequency with a fixed divisor. The divisor is determined by the value of the `PBxDIV` registers.

The system and peripheral clocks are stopped when in Sleep mode. The clocks are restarted by disabling the sleep enable.

12.4.1 Sleep Mode

Sleep mode is entered when `DSCON[DSEN]` is clear and the `OSCCON[SLPEN]` bit is set and the `cpu` executes a `WFI` instruction.. This causes the device clocks to be held low ('0').

12.4.2 Sleep Mode Entry

Entry into the Sleep mode from any other mode does not require a clock switch. This is due to the fact that once in Sleep mode, no clocks are needed.

Note: If software writes to the CRU SFR's before going into Sleep mode, it is recommended a read be done of the SFR's in order to flush the write before executing the `WAIT` instruction that initiates Sleep mode.

12.4.3 Sleep Mode Exit

Unless the Two-Speed Start-up is enabled, there are no clock switching events when exiting a Sleep mode. With Two-Speed Start-up disabled, Sleep mode is effectively extended until the selected clock is ready. Once the clock is ready, the device enters the RUN mode.

If Two-Speed Start-up is enabled, the device will come out of Sleep running with the FRC as the clock source and perform an automatic clock switch to the selected clock source.

If Two-Speed Start-up is enabled, RUN mode is entered immediately using the Two-Speed Start-up clock source. A clock switch to the selected clock source occurs once the source is ready.

Note: Two-speed start-up is not permanently enabled and is software programmable.

12.4.4 Sleep Mode with Delayed Exit

In some low power Sleep modes, some of the on chip voltage regulators may be turned off in the system. If this is the case, Sleep mode cannot be exited immediately on a wake-up event. The wake from Sleep will be delayed until the system is ready to have clocks turned on again.

12.5 IDLE Mode

IDLE mode is entered when the `OSCCON[SLPEN]` bit is low and the `cpu` executes a `WFI` instruction.. Only the CPU's internal clock is stopped in this mode.

Note: When exiting from Sleep mode, the CRU will transition the system to IDLE mode before transitioning to RUN mode. This transition to IDLE is used to support DREAM mode and always occurs regardless of the CRU is transitioning to DREAM mode or RUN mode. Therefore, when exiting Sleep mode both the RCON bits [`SLEEP`] and [`IDLE`] will be set.

12.6 Dream Mode

When the `DRMEN` bit in the `OSCCON` register is set, it allows a DMA controller to switch between the IDLE mode and the Sleep mode. When the `OSCCON.SLPEN` bit is set and the `OSCCON.DRMEN` bit is set, the CRU monitors the DMAC to make sure all transfers are complete before going into Sleep mode.

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If OSCCON.SLPEN = 1, OSCCON.DRMEN = 1, and peripheral clock requests are active, the CRU goes into IDLE mode until all peripheral clock requests are non-active, at which time the CRU goes into Sleep mode.

If OSCCON.SLPEN is not set, the DRMEN bit has no affect as the DMA clocks are still running in IDLE mode.

If the CRU recognizes a wake/interrupt event whose priority will wake the DMA, but not the CPU, the CRU transitions to IDLE mode, so the DMA can perform the needed operations and when the DMA is finished, the CRU will go back to Sleep mode. During this time the CPU is still asleep.

If the wake event is such that the CPU must handle the event, the whole system will exit Sleep mode and transition back to RUN mode.

12.7 FRCDIV

The FRC can be divided and used as a system clock. The user controls the divider setting using the OSCCON.FRCDIV[2:0] register bits.. The divisor is configured for eight divider selections: /1, /2, /4, /8, /16, /32, /64, /256.

12.8 RFPLL Wrapper

The RFPLL wrapper generates two clocks:

- spll_clk1 (PGM MHz)
 - Clock frequencies = 96 MHz/(1-255) and 64 MHz frequency choices and optional clock disable option
 - Clock ready indication
- spll_clk2 (PGM MHz)
 - Clock frequencies = 96 MHz/(1-15) and optional clock disable option
 - Clock ready indication

Clocks are produced only when there is a request generated by the user; for clk1, it is CRU and for clk2, it is ADC charge-pump. Along with the clocks, individual clock ready is also generated which indicates that clocks are ready for consumption.

12.9 Start-Up Considerations

The presence of hardware NVR fuses on the PIC32CX-BZ2 device allows the system configuration fuses to be ready upon exiting reset. The following start-up conditions exist:

- On any device Reset, no start-up time is required to transfer configuration values from the NVR memory into the configuration holding registers.
- Once the device is active, the user may change the primary system clock source from FRC to SPPLL by using the OSCCON register.

12.10 Fail-Safe Clock Monitor

The Clock System includes a Fail-safe Clock Monitor (FSCM). The FSCM monitors the sys_clk for continuous operation. If it detects that the sys_clk has failed, it switches the sys_clk over to the FRC oscillator and triggers a NMI. The FRC is an untuned 8 MHz oscillator that drives the sys_clk during FSCM event. When the NMI is executed, software can restart the main oscillator or shut down the system.

In the Sleep mode both the sys_clk and the FSCM halt, prevents FSCM detection.

12.11 Fast RC Oscillator

The on-chip 8 MHz Fast RC Oscillator (FRC) is intended to be a fast with precise frequency internal RC oscillator. The FRC supports calibration to $\pm 0.25\%$ accuracy pre-package. However, package induced stress lowers the accuracy.

The FRC oscillator is accurate to provide the clock frequency necessary to maintain baud rate tolerance for serial data transmissions. FRC is enabled with conditions in 1.11.1 otherwise is not enabled. Power on reset sets NOSC[3:0]=0000 so its always "on" when powered up.

The oscillator module provides a 6-bit wide user tuning adjustment capability using the OSCTRM.TUN[5:0] bits.

12.11.1 Enabling the FRC

The FRC oscillator is powered when OSCCON.NOSC[3:0] = 4'b0000 or a Fail-safe clock monitor is enabled and a clock fail is detected, forcing a switch to FRC. It is also enabled whenever it gets requested by: ADC requesting for FRC, Configuring SPLL2 source as FRC, PMU Controller requesting for FRC, Flash Controller requesting for FRC, Configuring LPCLK (32 KHz) source to FRC.

12.11.2 Frequency Tuning in User Mode

In addition to the factory calibration, the base frequency can be tuned in the user's application. This frequency tuning capability allows the user to deviate from the factory calibrated frequency. The user can tune the frequency by writing to the OSCTRM register. The tuning range of the FRC oscillator is $\pm 1.5\%$ of nominal in 3.75 kHz steps.

12.12 Secondary Oscillator

The Secondary Oscillator (SOSC) is a low-power 32.768 kHz crystal oscillator which provides accurate time keeping.

The Secondary Oscillator has the following features:

- 32.768 kHz operation
- Provides system clock output
- Provided to CRU or LPCLKGEN on request
- Can be disabled to reduce power
- Ultra Low Power driver
- No calibration is required

12.13 Low Power RC Oscillator (LPRC)

The Low Power Internal RC Oscillator (LPRC) operates at a nominal frequency of 32.768 kHz ($\pm 2\%$). The oscillator variation over VDD and temperature must be less than $\pm 2\%$.

Note: The LPRC is not a 50% duty cycle clock, however it maintains an average frequency over number of base locks.

The LPRC can be used as both, a source for the system clock and a reference for Backup core modules. These modules include the deep sleep watchdog, clock monitor circuits, and other modules that require a 32 kHz reference clock.

12.14 Reference Clock Generator

The Reference Clock Generator provides the Generic Clocks (GCLK_<Peripherhal>) for system peripherals via Peripheral Channels. There are a total of 24 Peripheral Channels, with the mapping as shown in following table.

Table 12-1. Peripheral Clock Generation

Peripheral Clock	Pchannel Index
GCLK_EIC, GCLK_CCL	0
GCLK_FREQM_MSR	1
GCLK_FREQM_REF	2
GCLK_SERCOM0_CORE, GCLK_SERCOM1_CORE	3
GCLK_SERCOM2_CORE, GCLK_SERCOM3_CORE	4

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.....continued

Peripheral Clock	Pchannel Index
GCLK_TC0	5
GCLK_TC1	6
GCLK_TC2, GCLK_TC3	7
GCLK_EVSYS_CH_0	8
GCLK_EVSYS_CH_1	9
GCLK_EVSYS_CH_2	10
GCLK_EVSYS_CH_3	11
GCLK_EVSYS_CH_4	12
GCLK_EVSYS_CH_5	13
GCLK_EVSYS_CH_6	14
GCLK_EVSYS_CH_7	15
GCLK_EVSYS_CH_8	16
GCLK_EVSYS_CH_9	17
GCLK_EVSYS_CH_10	18
GCLK_EVSYS_CH_11	19
GCLK_TCC0	20
GCLK_TCC1, GCLK_TCC2	21
GCLK_AC	22
GCLK_CM4_TRACE	23

The mapping for the source of the clocks for both the CLKGEN generator and Reference clock generator are shown in following table.

Table 12-2. CRU Clock Mapping

clock_in[x]	MCS/COSC Mapping	REFO/ROSEL Mapping	FSCM Clock Source	Clock to Switch to on a FSCM Fail
0 - FRC	0000	0000	-	X
1 - SPLL_CLK1	0001	0001	-	-
2 - POSC (16 MHz)	0010	0010	-	-
3 - SOSC	0011	0011	-	-
4 - LPRC	0100	0100	X	-
5 - SPLL_CLK3 (RFPLL, 96 MHz)	-	0101	-	-
6 - pb1_clk	-	0110	-	-
7 - sys_clk	-	0111	-	-
8 - REFI Pin	-	1000	-	-

12.15 CRU Configuration Registers

The BASE address of the CRU registers is 0x4400_0A00. The Register Summary table shows the mapping of the registers in memory as well as the details of the bit fields in each register. Each register has an associated SET/CLR/INV function register with the suffix appended to the register name, for example: <reg>SET, <reg>CLR, <reg>INV.

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12.16 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	OSCCON	7:0	CLKLOCK			SLPEN	CF		SOSCEN	OSWEN
		15:8		COSC[3:0]				NOSC[3:0]		
		23:16	DRMEN		2SPDSLP					
		31:24						FRCDIV[2:0]		
0x04	OSCTRM	7:0		TUN[5:0]						
		15:8								
		23:16								
		31:24								
0x08	SPLLCON	7:0		SPLLRST	SPLLFLOCK	SPLLPWDN				
		15:8		SPLL1POSTDIV1[7:0]						
		23:16		SPLL2POSTDIV2[3:0]						
		31:24	SPLL_BYP[1:0]							
0x0C	RCON	7:0	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR
		15:8		[4:0]				DPSLP	CMR	
		23:16		[6:0]						VBAT
		31:24	POR_IO	POR_CORE	[1:0]		BCFGERR	BCFGFAIL	NVMLTA	NVMEOL
0x10	RSWRST	7:0		[6:0]						SWRST
		15:8		[14:7]						
		23:16		[22:15]						
		31:24		[30:23]						
0x14	RNMIICON	7:0		NMICNT[7:0]						
		15:8		NMICNT[15:8]						
		23:16	SWNMI	[2:0]			EXT	PLVD	CF	WDTS
		31:24		[5:0]					DMTO	WDTR
0x18 ... 0x1B	Reserved									
0x1C	REFO1CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
0x20	REFO1TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x24	REFO2CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
0x28	REFO2TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x2C	REFO3CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
0x30	REFO3TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x34	REFO4CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x38	REFO4TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x3C	REFO5CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
0x40	REFO5TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x44	REFO6CON	7:0					ROSEL3	ROSEL2	ROSEL1	ROSEL0
		15:8	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
		23:16	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
		31:24		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
0x48	REFO6TRIM	7:0								
		15:8								
		23:16	ROTRIM0							
		31:24	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
0x4C	PB1DIV	7:0				PB1DIV[6:0]				
		15:8	PB1DIVON				PB1DIVRDY			
		23:16								
		31:24								
0x50	PB2DIV	7:0			PB1DIV[6:0]					
		15:8	PB1DIVON				PB1DIVRDY			
		23:16								
		31:24								
0x54	PB3DIV	7:0			PB1DIV[6:0]					
		15:8	PB1DIVON				PB1DIVRDY			
		23:16								
		31:24								
0x58	SLEWCON	7:0					SLW_UP	SLW_DN	SLW_BUSY	
		15:8						SLW_DIV[2:0]		
		23:16						SYS_DIV[3:0]		
		31:24						SLW_DELAY[3:0]		
0x5C	CLKSTAT	7:0	SPLL3RDY			LPRCRDY	SOSCRDY	POSCRDY	SPLL1RDY	FRCRDY
		15:8								
		23:16								
		31:24								
0x60 ... 0x63	Reserved									
0x64	CLK_DIAG	7:0	SPLL3_STOP	SPLL2_STOP	SPLL1_STOP	LPRC_STOP	FRC_STOP	SOSC_STOP	POSC_STOP	
		15:8								
		23:16	NMICTR7	NMICTR6	NMICTR5	NMICTR4	NMICTR3	NMICTR2	NMICTR1	NMICTR0
		31:24	NMICTR15	NMICTR14	NMICTR13	NMICTR12	NMICTR11	NMICTR10	NMICTR9	NMICTR8

12.17 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

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Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

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12.17.1 CRU Oscillator Control

Name: OSCCON
Offset: 0x00
Reset: 0x00000000

Note: The system unlock sequence must be done before this register can be written.

Bit	31	30	29	28	27	26	25	24
	FRCDIV[2:0]							
Access					R/W/L	R/W/L	R/W/L	
Reset					0	0	0	
Bit	23	22	21	20	19	18	17	16
	DRMEN		2SPDSLP					
Access	R/W/L		R/W/L					
Reset	0		1					
Bit	15	14	13	12	11	10	9	8
	COSC[3:0]				NOSC[3:0]			
Access	R	R	R	R	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CLKLOCK			SLPEN	CF		SOSCEN	OSWEN
Access	R/W/L			R/W/L	R/W/HS/L		R/W/L	R/W/HC/L
Reset	0			0	0		1	1

Bits 26:24 – FRCDIV[2:0] Fast RC Clock Divider bits

Value	Description
000	FRC Divide by 1 (default value)
001	FRC Divide by 2
010	FRC Divide by 4
011	FRC Divide by 8
100	FRC Divide by 16
101	FRC Divide by 32
110	FRC Divide by 64
111	FRC Divide by 256

Bit 23 – DRMEN Enable Dream Mode bit

Value	Description
1	When the cpu_si_sleep input is asserted and SLPEN = 1, peripheral clock requests are NOT active causes SLEEP Mode to be entered
0	DMA transfer has no effect

Bit 21 – 2SPDSLP 2-Speed start-up enabled in Sleep mode bit

Note: Default Reset Value is specified by cfg_two_speed_startup_en input.

Value	Description
1	When the device EXITS Sleep Mode, the sys_clk will be from FRC until the selected clock is ready
0	When the device EXITS Sleep Mode, the sys_clk will be from the selected clock

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Bits 15:12 – COSC[3:0] Current Oscillator Selection bits (Read-only)

Notes:

- Default value on reset is 4'b0000, which ensures that a virgin die has frc_clk running for ICDJTAG or EJTAG to program the NVR.
- Loaded with NOSC[3:0] at the completion of a successful clock switch.
- Set to FRC value (0000) when FSCM detects a failure and switches clock to FRC.

Value	Description
0000	Fast RC Oscillator (FRC) divided by OSCCON.FRCDIV
0001	System PLL Clock-1 (SPLL1 Module) (input clock and divider set by SPLLCON)
0010	Primary Oscillator- POSC
0011	Secondary Oscillator (SOSC)
0100	Low Power RC Oscillator (LPRC)
0101-111	Reserved for future use
1	

Bits 11:8 – NOSC[3:0] New Oscillator Selection bits

Note: Default value on reset is 4'b0000, which ensures that a virgin die has frc_clk running for ICDJTAG or EJTAG to program the NVR.

Value	Description
0000	Fast RC Oscillator (FRC) divided by OSCCON.FRCDIV
0001	System PLL Clock-1 (SPLL1 Module) (input clock and divider set by SPLLCON)
0010	Primary Oscillator- POSC
0011	Secondary Oscillator (SOSC)
0100	Low Power RC Oscillator (LPRC)
0101-111	Reserved for future use
1	

Bit 7 – CLKLOCK Clock Lock Enabled bit

Notes:

- Once set, this bit can only be cleared via a Device Reset.
- When active, this bit prevents writes to the following registers: NOSC[3:0], and OSWEN.

Value	Description
1	All clock and PLL configuration registers are locked. These include OSCCON, OSCTRIM, SPLLCON, UPLLCON, PBxDIV
0	Clock and PLL selection registers are not locked, configurations may be modified.

Bit 4 – SLPEN Enable SLEEP Mode bit

Value	Description
1	When a WAIT Instruction is executed device will enter SLEEP Mode
0	When a WAIT instruction is executed device will enter IDLE Mode

Bit 3 – CF Clock Fail Detect bit (Read / writable / Clearable by application)

Notes:

- Writing a '1' to this bit will cause a clock switching sequence to be initiated by the clock switch state machine
- Reset when a valid clock switching sequence is initiated by the clock switch state machine
- This bit is Set when clock fail event detected

Value	Description
1	FSCM has detected clock failure
0	FSCM has not detected clock failure

Bit 1 – SOSCEN 32 kHz Secondary (LP) Oscillator Enable bit

Note: Set to value specified by SOSCEN configuration bits ("cfg_lposcen" input signal) on RESET

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Value	Description
1	Enable Secondary Oscillator
0	Disable Secondary Oscillator

Bit 0 – OSWEN Oscillator Switch Enable bit

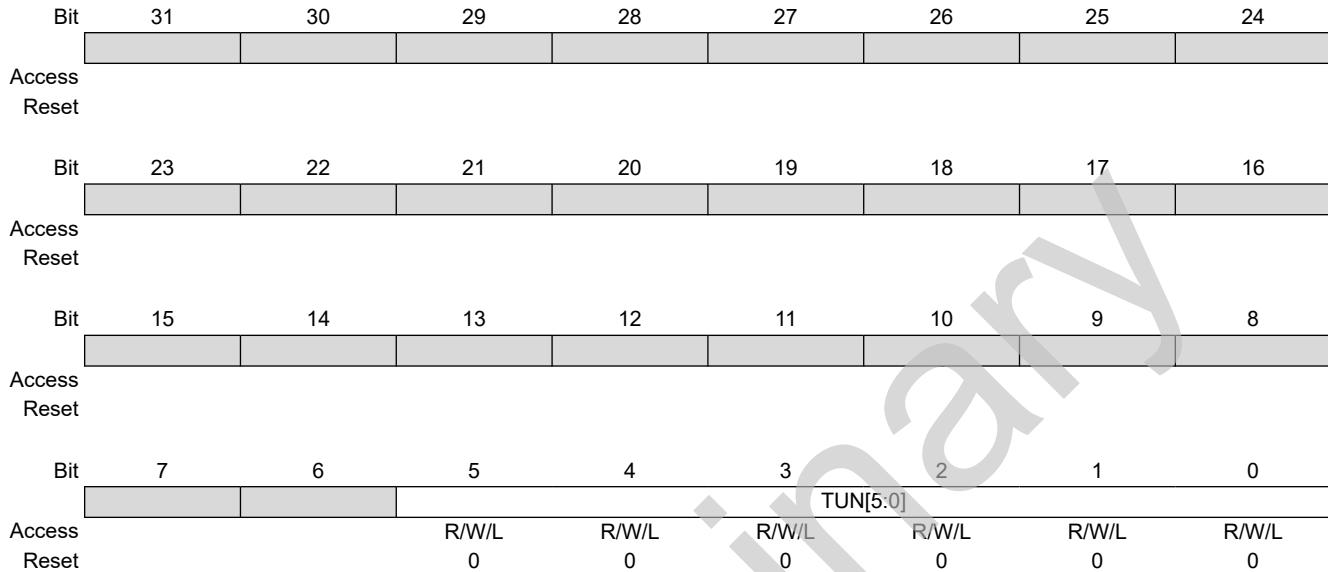
Notes:

- A Write of value ‘0’ has no effect.
- Cleared by hardware after a successful clock switch
- Cleared by hardware after a redundant clock switch (NOSC = COSC)
- Cleared by hardware after FSCM switches the oscillator to Fail-Safe Clock Source (FRC)

Value	Description
1	Request oscillator switch to selection specified by NOSC[3:0] bits
0	Oscillator switch is complete

12.17.2 CRU Oscillator Trimming

Name: OSCTRM
Offset: 0x04
Reset: 0x00000000



Bits 5:0 – TUN[5:0] Internal Fast RC (FRC) Oscillator Tuning bits

This bit field specifies the user tuning capability for the internal fast RC oscillator.

Note: The system unlock sequence must be done before this register can be written.

Value	Description
011111	Maximum Frequency
011110	
...	
000001	
000000	Center Frequency, oscillator is running at calibrated frequency
111111	
111110	
...	
100001	
100000	Minimum Frequency

12.17.3 SPLL (RFPLL/Wrapper) Control

Name: SPLLCON
Offset: 0x08
Reset: 0x00000000

Note: The system unlock sequence must be done before these registers can be written.

Bit	31	30	29	28	27	26	25	24
SPLL_BYP[1:0]								
Access	R/W/L	R/W/L						
Reset	1	1						
Bit	23	22	21	20	19	18	17	16
SPLL2POSTDIV2[3:0]								
Access				R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8
SPLL1POSTDIV1[7:0]								
Access	R/W/L							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
SPLLRST SPLLFLOCK SPLLPWDN								
Access		R/W/L	R/W/L	R/W/L				
Reset		1	0	1				

Bits 31:30 – SPLL_BYP[1:0] SPLL Bypass; when this bit is set, the input clock REF bypasses PLL to PLLOUTx.

Notes:

- Dictates clock source for ADC CP (Analog to Digital Converter Charge Pump) (SPLL2) Clock generation only
- Clock source must be preselected and kept ready before the need of ADC CP arrives. Failure to do so will result in loss of clock for one or two cycles when ADC CP is enabled.

Value	Description
00	RFPLL Clock is the clock source for ADC CP Clock Generation.
x1	FRC is used as clock source for ADC CP Clock Generation.
10	POSC is used as clock source for ADC CP Clock Generation.

Bits 19:16 – SPLL2POSTDIV2[3:0] ADC-CP Post Divide Value.

Value	Description
1 ≤ SPLLPOST DIV2 ≤ 15	Divide-by SPLLPOSTDIV2
0	No Clock; Clock disabled

Bits 15:8 – SPLL1POSTDIV1[7:0] First Post Divide Value.

Value	Description
2 ≤ SPLLPOST DIV ≤ 255	Divide-by SPLLPOSTDIV
0	Divide-by 1
1	Divide-by 1.5

Bit 5 – SPLLRST System PLL Reset

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Clock and Reset Unit (CRU)

Value	Description
1	Assert the reset to the SPLL
0	De-assert the reset to the SPLL

Bit 4 – SPLLFLOCK System PLL Force Lock

Value	Description
1	Force the SPLL lock signal to be asserted
0	Do not force the SPLL lock signal to be asserted

Bit 3 – SPLLPWDN PLL Power Down Register bit

Value	Description
1	PLL is powered down
0	PLL is active

12.17.4 Reference Oscillator x Control

Name: REFOxCON
Offset: 0x1C + (x-1)*0x08 [x=1..6]
Reset: 0x00000000

Notes:

- REFOCON.ROSEL should not be written while the REFOCON.ACTIVE bit is '1' - This will result in undefined behavior.
- REFOCON should not be written when REFOCON[ON] != REFOCON[ACTIVE] - This will result in undefined behavior.
- This register can always be accessed regardless of the cfg_sys_unlock value.

Bit	31	30	29	28	27	26	25	24
		RODIV14	RODIV13	RODIV12	RODIV11	RODIV10	RODIV9	RODIV8
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	RODIV7	RODIV6	RODIV5	RODIV4	RODIV3	RODIV2	RODIV1	RODIV0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ON	FRZ	SIDL	OE	RSLP		DIVSW_EN	ACTIVE
Access	R/W	R/W	R/W	R/W	R/W		HC/ R/W	HS/HC/ R
Reset	0	0	0	0	0		0	0
Bit	7	6	5	4	3	2	1	0
					ROSEL3	ROSEL2	ROSEL1	ROSEL0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30 – RODIV Reference Clock Divider bits
 Specifies 1/2 period of reference clock in the source clocks.

Example: Period of refo_clk = [Reference source * 2] * RODIV

Value	Description
1111111111111111	REFOx clock is Base clock frequency divided by 65,534 (32,767 *2)
1111111111111110	REFOx clock is Base clock frequency divided by 65,532 (32,766 * 2)
...	
...	
...	
0000000000000011	REFOx clock is Base clock frequency divided by 6 (3*2)
0000000000000010	REFOx clock is Base clock frequency divided by 4 (2*2)
0000000000000001	REFOx clock is Base clock frequency divided by 2 (1*2)
0000000000000000	REFOx clock is same frequency as Base clock (no divider)

Bit 15 – ON Output Enable bit

Value	Description
1	Reference Oscillator Module enabled
0	Reference Oscillator Module disabled

Bit 14 – FRZ Freeze in Debug mode bit

Value	Description
1	When emulator is in Debug mode, module freezes operation

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Value	Description
0	When emulator is in Debug mode, module continues operation

Bit 13 – SIDL Peripheral Stop in Idle Mode bit

Value	Description
1	Discontinue module operation when device enters Idle mode
0	Continue module operation in Idle mode

Bit 12 – OE Reference Clock Output Enable bit

Value	Description
1	Reference clock is driven out on REFOx pin
0	Reference clock is not driven out on REFOx pin

Bit 11 – RSLP Reference Oscillator Run in Sleep bit

Note: This bit is ignored when ROSEL[3:0] = (0000 or 0001).

Value	Description
1	Reference Oscillator output continues to run in Sleep
0	Reference Oscillator output is disabled in Sleep

Bit 9 – DIVSW_EN Clock RODIV/ROTRIM switch enabled

Value	Description
1	Clock Divider Switching currently in progress
0	Clock Divider Switch has completed

Bit 8 – ACTIVE Reference Clock Request Status bit

Value	Description
1	Reference clock request is active (User should not update this REFOCON register)
0	Reference clock request is not active (User can update this REFOCON register)

Bits 0, 1, 2, 3 – ROSEL Reference Clock Source Select bits

Select one of various clock sources to be used as the reference clock.

Value	Description
1001 –	Reserved
1111	
1000	REFI Pin
0111	System clock (reference clock reflects any device clock switching)
0110	Peripheral clock (reference clock reflects any peripheral clock switching)
0101	System PLL (Clock-3)
0100	LPRC
0011	SOSC
0010	POSC
0001	System PLL (Clock-1)
0000	FRC

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Clock and Reset Unit (CRU)

12.17.5 Reference Oscillator x Trim

Name: REFOxTRIM
Offset: 0x20 + (x-1)*0x08 [x=1..6]
Reset: 0x00000000

Notes:

- REFOxTRIM should not be written when REFOxCON[ON] != REFOxCON[ACTIVE] - This will result in undefined behavior.
- This register can always be accessed regardless of the cfg_sys_unlock value.

Bit	31	30	29	28	27	26	25	24
	ROTRIM8	ROTRIM7	ROTRIM6	ROTRIM5	ROTRIM4	ROTRIM3	ROTRIM2	ROTRIM1
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	ROTRIM0							
Access	R/W							
Reset	0							
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 23, 24, 25, 26, 27, 28, 29, 30, 31 – ROTRIM Trim bits - Provides fractional additive to RODIV value for 1/2 period of REFOx clock

Note: ROTRIM values greater than zero are only valid when RODIV values are greater than 0.

Value	Description
0000_0000_0	0/512 (0.0) divisor added to RODIV value
0000_0000_1	1/512 (0.001953125) divisor added to RODIV value
0000_0001_0	2/512 (0.00390625) divisor added to RODIV value
...	...
...	...
100000000	256/512 (0.5000) divisor added to RODIV value
...	...
...	...
1111_1111_0	510/512 (0.99609375) divisor added to RODIV value
1111_1111_1	511/512 (0.998046875) divisor added to RODIV value

12.17.6 PBx Clock Divisor Control

Name: PBxDIV
Offset: 0x4C + (x-1)*0x04 [x=1..3]
Reset: 0x00000000

Note: The system unlock sequence must be done before this register can be written. PBx registers include PB1DIV, PB2DIV and PB3DIV. Ensure the PB3DIV[6:0] value = 0x09 or greater if you are not using Microchip provided boot code.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R				R			
Reset	1				1			
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 15 – PB1DIVON Output Enable bit

Value	Description
1	PB1 Output clock is enabled
0	PB1 Output clock is disabled

Note: PB1DIV[PB1DIVON] bit cannot be written to a '0', as this clock is used by the system CLK_RST macro.

Bit 11 – PB1DIVRDY PB1 Peripheral Clock Divisor Ready

Value	Description
1	Indicates the PB clock divisor logic is not switching divisors and the PB1DIV may be written.
0	Indicates the PB clock divisor logic is currently switching values and the PB1DIV cannot be written.

Bits 6:0 – PB1DIV[6:0] PB1 Peripheral Clock Divisor Control value

Value	Description
000_0000	Divide by 1 PB1 Clock same frequency as sys_clk
000_0001	Divide by 2 PB1 Clock is 1/2 of sys_clk
000_0010	Divide by 3 PB1 Clock is 1/3 of sys_clk
000_0011	Divide by 4 PB1 Clock is 1/4 of sys_clk
...	...
...	...
000_1111	Divide by 16 PB1 Clock is 1/16 of sys_clk
001_0000	Divide by 17 PB1 Clock is 1/17 of sys_clk
...	...
...	...
111_1110	Divide by 127 PB1 Clock is 1/127 of sys_clk
111_1111	Divide by 128 PB1 Clock is 1/128 of sys_clk

12.17.7 Slew Rate Control for Clock Switching

Name: SLEWCON
Offset: 0x58
Reset: 0x00000000

Notes:

- The system unlock sequence must be done before this register can be written.
- Updates to this register do not take affect until OSCCON[OSWEN] is set.

Bit	31	30	29	28	27	26	25	24
SLW_DELAY[3:0]								
Access					R/W	R/W	R/W	R/W
Reset					c	c	c	c
Bit	23	22	21	20	19	18	17	16
SYS_DIV[3:0]								
Access					R/W	R/W	R/W	R/W
Reset					c	c	c	c
Bit	15	14	13	12	11	10	9	8
SLW_DIV[2:0]								
Access					R/W	R/W	R/W	R/W
Reset					c	c	c	c
Bit	7	6	5	4	3	2	1	0
SLW_UP SLW_DN SLW_BUSY								
Access					R/W	R/W	R/W	R/W
Reset					c	c	c	c

Bits 27:24 – SLW_DELAY[3:0] Number of clocks generated at each slew step for a clock switch

Note: The reset value of this register field is defined by the input cfg_slewcon_sel[].

Value	Description
0000	1 clock will be generated at each slew step
0001	2 clocks will be generated at each slew step
...	...
1111	16 clocks will be generated at each slew step

Bits 19:16 – SYS_DIV[3:0] PBx Peripheral Clock Divisor Control value

Value	Description
0000	Divide by 1 - sys_clk_out same frequency as sys_clk source - Default
0001	Divide by 2 - sys_clk_out is 1/2 of sys_clk source
0010	Divide by 3 - sys_clk_out is 1/3 of sys_clk source
...	...
1111	Divide by 16 - sys_clk_out is 1/16 of sys_clk source

Bits 10:8 – SLW_DIV[2:0] Divisor steps used when doing slewed clock switches

Note: Each Divisor step lasts 4 clocks

Value	Description
000	No Divisor used
001	Divide by 2 (2^1), then no divisor
010	Divide by 4 (2^2), then by 2, then no divisor
011	Divide by 8 (2^3), then by 4, then by 2, then no divisor
100	Divide by 16 (2^4), then by 8, then by 4, then by 2, then no divisor
...	...

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Value	Description
111	Divide by 128 (2^7), then by 64, then by 32, then by 16, then by 8, then by 4, then by 2, then no divisor

Bit 2 – SLW_UP Clock slew enable for switching up to faster clocks

Value	Description
0	Clock Slew disabled
1	Clock Slew enabled on a clock switch OR exit from SLEEP

Bit 1 – SLW_DN Clock slew enable for switching down to slower clocks

Value	Description
0	Clock Slew disabled
1	Clock Slew enabled on a clock switch

Bit 0 – SLW_BUSY Clock Switch Slew Active Status Bit - Read-Only

Value	Description
0	Clock Switch has reached its final value
1	Clock frequency is being actively Slewed

12.17.8 Clock Status

Name: CLKSTAT
Offset: 0x5C
Reset: 0x00000000

Note: The corresponding RDY bits are updated only after clock switch request is initiated via OSCCON.NOSC[3:0].

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	R/HS/HC							
Reset	0	0	0	0	0	0	0	0

Bit 6 – SPLL3RDY System PLL (Clock-3) Ready Status value

Value	Description
1	SPLL3 is stable and ready
0	SPLL3 is not stable and not ready

Bit 4 – LPRCRDY LPRC Ready Status value

Value	Description
1	LPRC is stable and ready
0	LPRC is not stable and not ready

Bit 3 – SOSCRDY SOSC Ready Status value

Value	Description
1	SOSC is stable and ready
0	SOSC is not stable and not ready

Bit 2 – POSCRDY Primary Oscillator Ready Status value

Value	Description
1	POSC is stable and ready
0	POSC is not stable and not ready

Bit 1 – SPLL1RDY System PLL (Clock-1) Ready Status value

Value	Description
1	SPLL1 is stable and ready
0	SPLL1 is not stable and not ready

Bit 0 – FRCRDY FRC Ready Status value

Value	Description
1	FRC is stable and ready
0	FRC is not stable and not ready

12.17.9 User Clock Diagnostics Control

Name: CLK_DIAG
Offset: 0x64
Reset: 0x00000000

Note: The system unlock sequence must be done before this register can be written.

Bit	31	30	29	28	27	26	25	24
	NMICTR15	NMICTR14	NMICTR13	NMICTR12	NMICTR11	NMICTR10	NMICTR9	NMICTR8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	NMICTR7	NMICTR6	NMICTR5	NMICTR4	NMICTR3	NMICTR2	NMICTR1	NMICTR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		SPLL3_STOP	SPLL2_STOP	SPLL1_STOP	LPRC_STOP	FRC_STOP	SOSC_STOP	POSC_STOP
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – NMICTR Internal value of internal NMI Counter
This field reflects the actual value of internal NMI counter

Bit 6 – SPLL3_STOP SPLL Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	SPLL3 clock source runs as normal
1	SPLL3 clock source is stopped

Bit 5 – SPLL2_STOP SPLL Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	SPLL2 clock source runs as normal
1	SPLL2 clock source is stopped

Bit 4 – SPLL1_STOP SPLL Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	SPLL1 clock source runs as normal
1	SPLL1 clock source is stopped

Bit 3 – LPRC_STOP LPRC Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	LPRC clock source runs as normal
1	LPRC clock source is stopped

Bit 2 – FRC_STOP FRC Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	FRC clock source runs as normal
1	FRC clock source is stopped

Bit 1 – SOSC_STOP SOSC Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	SOSC clock source runs as normal
1	SOSC clock source is stopped

Bit 0 – POSC_STOP POSC Clock Stop Control value

Note: Gating logic is outside of this macro

Value	Description
0	POSC clock source runs as normal
1	POSC clock source is stopped

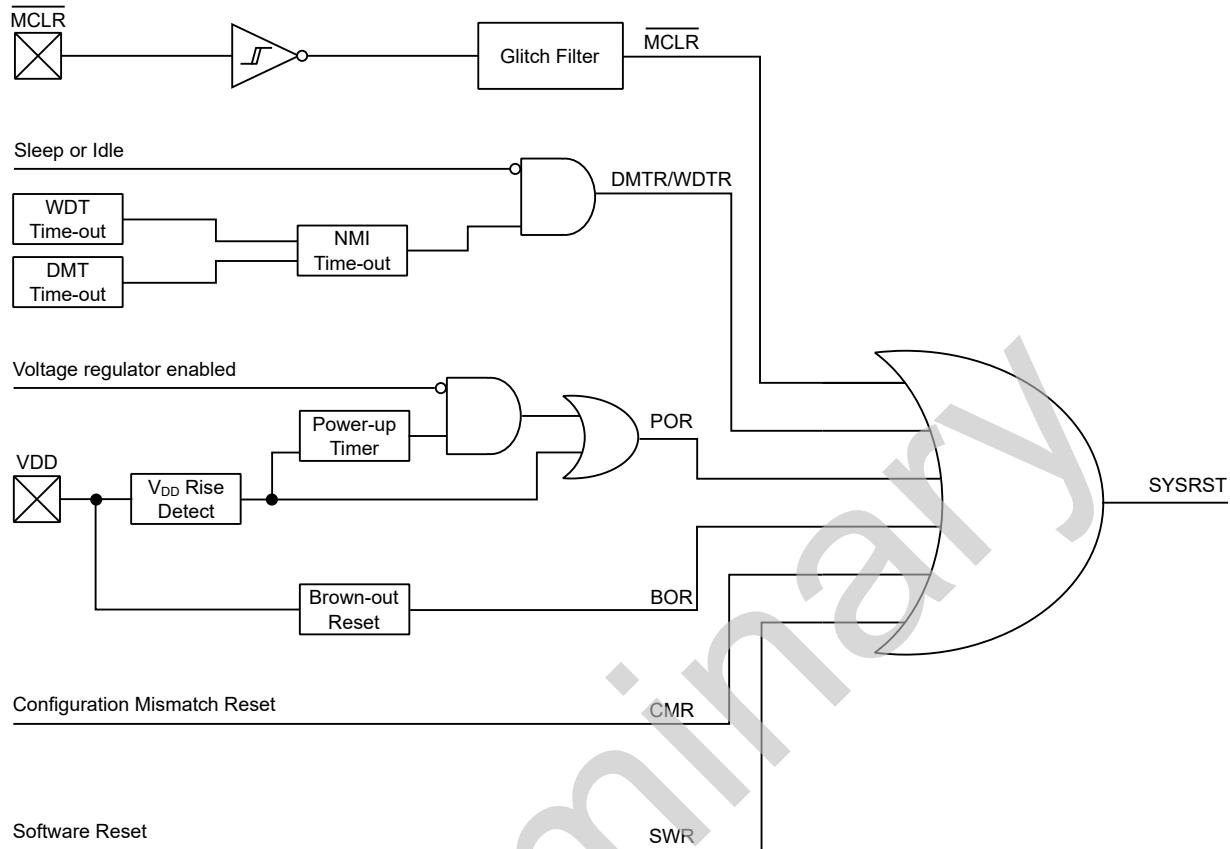
12.18 Resets

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (V_{dd} , IO, or POR)
- Brown-out Reset (BOR/ZPBOR)
- Master Clear Reset (MCLR)
- Watchdog Timer Reset (NMI Counter)
- Dead Man Timer Reset (NMI Counter)
- Software Reset (SWR)
- Test mode Entry and Exit
- JTAG Reset
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is shown in the following figure. Any active source of reset will make the system Reset signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state.

Figure 12-4. System Reset Block Diagram



12.18.1 Control Registers

Most types of device resets will set corresponding Status bits in the RCON register to indicate the type of Reset (see *RCONregister* from Related Links). The one exception is the Non-maskable Interrupt (NMI) time-out Reset. A Power-on Reset (POR) will clear all bits, except for the BOR and POR bits (RCON[1:0]), which are set. The user software may set or clear any of the bits at any time during code execution. The RCON bits serve only as Status bits. Setting a Reset status bit in software will not cause a system Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. For more information on the function of these bits, see *Using the RCON Status Bits* from Related Links.

The RSWRST control register has only one bit, SWRST. This bit is used to force a software Reset condition.

A delay equal to the duration of the number of NMICNT system clocks begins as it is decremented to zero. During this interval, the program can clear the WDT or DMT flag bits, if desired, to avoid a Reset. If the active flag is not cleared, the device will be reset at the end of the interval. The NMICNT value can be set to zero for no delay and up to 255 SYSCLK cycles.

The NMI interrupt can also be triggered by setting the SWNMI bit in software, or if the CF bit is set by the FSCM, but these do not begin the countdown and do not automatically lead to a reset.

The Resets module consists of the following Special Function Registers (SFRs):

- RCON: Reset Control Register
- RSWRST: Software Reset Register
- RNMICON: Non-Maskable Interrupt (NMI) Control Register

The base address of these registers is 0x4400_0A00. The offset for each register is shown in Reset Register Map (see *Reset Register Map* in the *Reset Control Registers* from Related Links). Multiply the address offset in the table by 4. The other three addresses represent the CLR/SET/INV bitwise registers.

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Related Links

- [12.18.2.1. RCON](#)
- [12.18.3. Reset Control Registers](#)
- [12.18.5.3. Using the RCON Status Bits](#)

Preliminary

12.18.2 Reset Register Summary

Following registers provides a brief summary of the Reset Control registers.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0B	Reserved									
0x0C	RCON	7:0	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR
		15:8		[4:0]				DPSLP	CMR	
		23:16			[6:0]					VBAT
		31:24	POR_IO	POR_CORE	[1:0]		BCFGERR	BCFGFAIL	NVMLTA	NVMEOL
0x10	RSWRST	7:0			[6:0]					SWRST
		15:8				[14:7]				
		23:16				[22:15]				
		31:24				[30:23]				
0x14	RNMICON	7:0				NMICNT[7:0]				
		15:8				NMICNT[15:8]				
		23:16	SWNMI		[2:0]		EXT	PLVD	CF	WDTS
		31:24			[5:0]				DMTO	WDTR

12.18.2.1 Reset Control Register

Name: RCON
Offset: 0xC
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	POR_IO	POR_CORE	[1:0]		BCFGERR	BCFGFAIL	NVMLTA	NVMEOL
Access	R/W/HS	R/W/HS	R	R	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
				[6:0]				VBAT
Access	R	R	R	R	R	R	R	R/W/HS
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
			[4:0]			DPSLP	CMR	
Access	R	R	R	R	R	R/W/HS	R/W/HS	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR
Access	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset	0	0	0	0	0	0	0	0

Bit 31 – POR_IO IO Voltage POR Flag bit

- '1' = A Power-on Reset has occurred due to IO voltage.
- '0' = A Power-on Reset has not occurred due to IO voltage.

Set by hardware at detection of an IO POR event. User software must clear this bit to view next detection.

Note: User may write this bit to '1'. Does not cause a POR_IO.

Bit 30 – POR_CORE Core Voltage POR Flag bit

- '1' = A Power-on Reset has occurred due to core voltage.
- '0' = A Power-on Reset has not occurred due to core voltage.

Set by hardware at detection of a core POR event. User software must clear this bit to view next detection.

Note: User may write this bit to '1'. Does not cause a POR_CORE.

Bits 29:28 – [1:0]

Unimplemented: Read as '0'.

Bit 27 – BCFGERR BCFG Error Flag bit

- '0' = A BCFG error has not occurred.
- '1' = A BCFG error has occurred.

A primary BCFG value had an error but the secondary BCFG value was valid and used.

Bit 26 – BCFGFAIL BCFG Failure Flag bit

- '0' = A BCFG failure has not occurred.
- '1' = A BCFG failure has occurred.

Both the Primary and Secondary BCFG values had an unrecoverable error – Default values are in effect.

Bit 25 – NVMLTA NVM Life Time Alert Flag bit

- '0' = A NVM LTA error has not occurred.
- '1' = A NVM LTA error has occurred.

NVM Life Time Alert – due to charge leakage, the NVM is nearing EOL.

Bit 24 – NVMEOL NVM End of Life Flag bit

- '0' = A NVM EOL failure has not occurred.
- '1' = A NVM EOL failure has occurred.

NVM End of Life – may not be visible to user, because the part will not come out of Reset if the bit is asserted.

Bits 23:17 – [6:0]

Unimplemented: Read as '0'.

Bit 16 – VBAT VBAT Mode Flag bit

- '1' = A POR exit from VBAT has occurred. A true POR must be established with the valid VBAT voltage level on the VBAT pin.
- '0' = A POR exit from VBAT has not occurred.

Bits 15:11 – [4:0]

Unimplemnted: Read as '0'.

Bit 10 – DPSLP Deep Sleep Mode Flag bit

- '1' = Deep Sleep mode has occurred.
- '0' = Deep Sleep mode has not occurred.

Set by hardware at time of entry into Deep Sleep mode. User software must clear this bit to view next detection.

Bit 9 – CMR Configuration Mismatch Reset Flag bit

- '1' = A CMR event has occurred.
- '0' = A CMR event has not occurred.

Note: User may write this bit to '1'. Does not cause a Mismatch Reset.

Bit 8 –

Unimplemented: Read as '0'.

Bit 7 – EXTR External Reset (MCLR) Status bit

- '1' = A Master Clear (pin) Reset has occurred.
- '0' = A Master Clear (pin) Reset has not occurred.

Note: User may write this bit to '1'. Does not cause a (MCLR).

Bit 6 – SWR Software Reset Flag bit

- '1' = A SWR has occurred.
- '0' = A SWR has not occurred.

Note: User may write this bit to '1'. Does not cause SWR.

Bit 5 – DMT0 Deadman Timer Time-out Flag bit

- '1' = DMT Time-out has occurred and caused a Reset.
- '0' = DMT Time-out has not occurred.

Note: User may write this bit to '1'. Does not cause DMT Reset.

Bit 4 – WDTO Watchdog Timer Time-out Flag bit

- ‘1’ = WDT Time-out has occurred and caused a Reset.
- ‘0’ = WDT Time-out has not occurred.

Note: User may write this bit to ‘1’. Does not cause WDT Reset.

Bit 3 – SLEEP Wake from Sleep Flag bit

- ‘1’ = Device has been in Sleep mode.
- ‘0’ = Device has not been in Sleep mode.

Note: User may write this bit to ‘1’. Does not invoke Sleep mode.

Bit 2 – IDLE Wake from Idle Flag bit

- ‘1’ = Device was in Idle mode.
- ‘0’ = Device was not in Idle mode.

Note: User may write this bit to ‘1’. Does not invoke Idle mode.

Bit 1 – BOR BOR Flag bit

- ‘1’ = A BOR has occurred.
- ‘0’ = A BOR has not occurred.

Set by hardware at detection of a BOR event. User software must clear this bit to view next detection.

Note: User may write this bit to ‘1’. Does not cause a BOR.

Bit 0 – POR POR Flag bit

- ‘1’ = A Power-on Reset has occurred.
- ‘0’ = A Power-on Reset has not occurred.

Set by hardware at detection of a POR event. User software must clear this bit to view next detection.

Note: User may write this bit to ‘1’. Does not cause a POR.

12.18.2.2 Software Reset Register

Name: RSWRST
Offset: 0x10
Reset: 0x00000000
Property: -

Note: The system unlock sequence must be done before this register can be written.

Bit	31	30	29	28	27	26	25	24
[30:23]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[22:15]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[14:7]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
[6:0]								
Access	R	R	R	R	R	R	R	W/HC
Reset	0	0	0	0	0	0	0	0

Bits 31:1 – [30:0]

Unimplemented: Read as '0'.

Bit 0 – SWRST Software Reset Trigger bit

'1' = Enable SWR event. A subsequent read of this register triggers the system Reset sequence. The system unlock sequence must be done before the bit can be written. This bit always reads a value of logic '0'.

12.18.2.3 NMI Control Register

Name: RNMICON
Offset: 0x14
Reset: 0x00000000
Property: -

Note: The system unlock sequence must be done before this register can be written.

[registerDescription]

Bit	31	30	29	28	27	26	25	24
[5:0]								
Access	R	R	R	R	R	R	DMTO	WDTR
Reset	0	0	0	0	0	0	0	0
[2:0]								
Bit	23	22	21	20	19	18	17	16
Access	SWNMI		[2:0]		EXT	PLVD	CF	WDTs
Reset	0	0	0	0	0	0	0	0
NMICNT[15:8]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
NMICNT[7:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:26 – [5:0]

Unimplemented: Read as '0'.

Bit 25 – DMTO Deadman Timer Time-out Flag bit (this will cause a Reset when NMICNT expires)

- '1' = DMT Time-out has occurred and caused a NMI.
- '0' = DMT Time-out has not occurred.

Note: User may write this bit to '1'. Does cause a user initiated DMT NMI event and NMICNT start.

Bit 24 – WDTR Watchdog Timer Time-out in Run Flag bit

- '1' = WDT Time-out has occurred and caused a NMI (this may cause a Reset if NMICNT expires).
- '0' = WDT Time-out has not occurred.

Note: User may write this bit to '1'. Does cause a user initiated WDT NMI event and NMICNT start.

Bit 23 – SWNMI Software NMI Trigger bit

- '1' = Writing a '1' to this bit will cause an NMI to be generated.
- '0' = Writing a '0' to this bit will have no effect.

Bits 22:20 – [2:0]

Unimplemented: Read as '0'.

Bit 19 – EXT External / Generic NMI Event bit

- '1' = A general NMI event has been detected and caused an NMI. Writing '0' to this bit will clear the NMI event
- '0' = A general NMI event has not been detected.

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Note: User may write this bit to '1'. Does cause a user initiated EXT NMI event.

Bit 18 – PLVD Programmable Low Voltage Detect Event bit

- '1' = PLVD has detected a low voltage condition and caused an NMI
- '0' = PLVD has not detected a low voltage condition

Note: User may write this bit to '1'. Does cause a user initiated PLVD NMI event.

Bit 17 – CF Clock Fail Detect bit (Read/Clear-able by application)

- '1' = FSCM has detected clock failure and caused an NMI
- '0' = FSCM has not detected clock failure

Note: Writing a '1' to the CF bit will cause a user-initiated clock failure NMI event, but will not actually cause a clock switch.

Bit 16 – WDTS Watch-Dog Timer Time-out in Sleep Flag bit

- '1' = WDT Time-out has occurred during Sleep mode and caused a wake-up from sleep.
- '0' = WDT Time-out has not occurred during Sleep mode.

Note: User may write this bit to '1'. Does cause a user initiated WDT NMI event.

Bits 15:0 – NMICNT[15:0] NMI Reset counter value bit

This bit field specifies the reload value used by the NMI Reset counter.

0000_0000_0000_0000 = No delay between NMI assertion and device Reset event
0000_0000_0000_0001
0000_0000_0000_0010

.....
.....
.....

1111_1111_1111_1110

1111_1111_1111_1111 = Number of SYSCLK cycles that Software has to clear the NMI event before a device Reset is performed. If the NMI event is cleared before the counter reached zero, then NO device Reset is asserted.

Note: When a WDT NMI event (when not in Sleep mode), the NMICNT starts incrementing from 0 NMICNT value. When a DMT NMI event is triggered, the NMICNT starts decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

12.18.3 Reset Control Registers

Table 12-3. Reset Register Map

	Register	Bit Range	Bits																		All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
0XC	RCON	31:16	POR_IO	POR_CORE	—	—	BCFGERR	BCFGFAIL	NVMLTA	NVMEOL	—	—	—	—	—	—	—	VBAT	0000		
		15:0	—	—	—	—	—	DPSLP	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0000		
0X10	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000		
0X14	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTR	SWNMI	—	—	—	EXT	PLVD	CF	WDTS	0000		
		15:0	NMICNT[15:0]																0000		

12.18.4 Modes of Operation

12.18.4.1 System Reset (SYSRST)

The internal System Reset (SYSRST) can be generated from multiple Reset sources, such as:

- Power-on Reset (POR)
- Brown-out Reset (BOR/ZPBOR)
- Master Clear Reset ($\overline{\text{MCLR}}$)
- Watchdog Time-out Reset (WDTO)
- Deadman Timer Reset (DMTR)
- Software Reset (SWR)
- Configuration Mismatch Reset (CMR)
- Test Mode Entry and Exit Reset
- JTAG Reset

A system Reset is active at the first POR and asserted until device configuration settings are loaded, and the oscillator clock sources become stable. The system Reset is then de-asserted allowing the CPU to start fetching code after eight system clock cycles (SYSCLK). On any device Reset, no start-up time is required to transfer configuration values from the NVR memory into the configuration holding registers. Once the device is active, the user may change the primary system clock source from FRC to SPLL by using the OSCCON register.

12.18.4.2 Power-on Reset (POR)

A power-on event generates an internal POR pulse when a VDD rise is detected above VPOR. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise-rate specifications, refer to the Electrical Specifications.

This device has on-chip internal voltage regulator and its power-on delay is designated as TPU. For more information on the TPU specification, refer to the Electrical Specifications.

At this point the POR event has expired, but the device Reset is still asserted while device configuration settings are loaded, and the clock oscillator sources are configured. The clock monitoring circuitry waits for the oscillator source to become stable. The clock source of this device when exiting from Reset, is always FRC (NOSC[3:0] bits (OSCCON[11:8])).

After these delays expire, the system Reset, SYSRST, is de-asserted. Before allowing the CPU to start code execution, eight system clock cycles are required before the synchronized Reset to the CPU core is de-asserted.

The power-on event sets the BOR and POR status bits (RCON[1:0]).

For more information on the values of the delay parameters, refer to the Electrical Specifications.

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user software must ensure that the delay between the time power is first applied and the time the system Reset is released is adequate to get all operating parameters within the specification.

12.18.4.3 Master Clear Reset

Whenever the master clear pin ($\overline{\text{MCLR}}$) is driven low, the Reset event is synchronized with the system clock, SYSCLK, before asserting the system Reset, SYSRST, provided the input pulse on $\overline{\text{MCLR}}$ is longer than a certain minimum width, as specified in the Electrical Specifications.

The $\overline{\text{MCLR}}$ pin provides a filter to minimize the effects of noise and to avoid unwanted Reset events. The status bit, EXTR (RCON[7]), is set to indicate the $\overline{\text{MCLR}}$ Reset.

The $\overline{\text{MCLR}}$ pin can be configured to generate a POR event, rather than a normal SYSRST event. This is configured through the SMCLR bit (CFGCON1[14]).

12.18.4.4 Software Reset (SWR)

This device does not provide a specific RESET instruction; however, a hardware Reset can be performed in software (software Reset) by executing a software Reset command sequence. The software Reset acts like a $\overline{\text{MCLR}}$ Reset. The software Reset sequence requires the system unlock sequence to be executed before the SWRST bit (RSWRST[0]) can be written.

A software Reset is performed as follows:

1. Write the system unlock sequence.
2. Set the SWRST bit (RSWRST[0]) = 1.
3. Read the RSWRST register.

Setting the SWRST bit (RSWRST[0]) will arm the software Reset. The subsequent read of the RSWRST register triggers the software Reset, which should occur on the next clock cycle following the read operation. To ensure no other user code is executed before the Reset event occurs, it is recommended that four NOP instructions or a while (1); statement is placed after the READ instruction.

The SWR Status bit (RCON[6]) is set to indicate the software Reset.

12.18.4.5 Watchdog Timer Reset (WDTR)

A Watchdog Timer (WDT) Reset event is synchronized with the system clock (SYSCLK), before asserting the system Reset.

Note: A WDT time-out during Sleep or Idle mode will wake-up the processor and branch to the reset vector, but, it does not Reset the processor.

The only bits affected are WDTO, and SLEEP or IDLE in the RCON register. See *Clock and Reset Unit (CRU)* from Related Links for more information on the WDT Reset.

Related Links

[12. Clock and Reset Unit \(CRU\)](#)

12.18.4.6 Brown-out Reset (BOR)

This device has a simple Brown-out Reset (BOR) capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a BOR event, which is synchronized with the system clock, SYSCLK, before asserting the system Reset. This event is captured by the BOR flag bit (RCON[1]). For more information, refer to the Electrical Specifications.

12.18.4.7 Configuration Mismatch Reset (CMR)

To maintain the integrity of the stored configuration values, all device Configuration bits are loaded and implemented as a complementary set of bits. As the Configuration Words are being loaded, for each bit loaded as '1', a complementary value of '0' is stored into its corresponding background word location and vice versa. The bit pairs are compared every time the Configuration Words are loaded, including Sleep mode. During this comparison, if the Configuration bit values are not found opposite to each other, a configuration mismatch event is generated, which causes a device Reset.

If a device Reset occurs as a result of a configuration mismatch, the CMR Status bit (RCON[9]) is set.

12.18.4.8 Deadman Timer Reset (DMTR)

A Deadman Timer (DMT) Reset is generated when the DMT count has expired.

The primary function of the DMT is to Reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT[4:0] bits in the CFGCON2 Configuration register.

A DMT is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected. For more information on the DMT reset, see *Deadman Timer (DMT)* from Related Links.

Related Links

[16. Deadman Timer \(DMT\)](#)

12.18.4.9 Non-maskable Interrupt (NMI) Timer

The NMI timer provides a delay between DMT or WDT events and a device Reset. Set the delay in System Clock counts from 0 to 255 in the NMICNT[15:0] bits (RNMICON[15:0]). If these bits are set to zero, there will be no delay between the DMTO or WDTO flag and a device Reset. If set to a non-zero value, the NMI interrupt has that number of system clocks to clear flags or save data for debugging purposes.

If the corresponding NMI flag is not cleared in RNMICON before the counter reaches zero, then a device Reset will be issued. If the corresponding NMI flag in RNMICON is cleared before the counter reaches zero, then the counter is stopped, then reloaded with the NMICNT value again and waits for another NMI event to occur. A device reset will not be asserted in this case and software will be able to return from this interrupt.

The DMTO flag will be set if there is a DMT event. The device will be Reset after the NMI counter expires.

The WDTO flag will be set if there is a WDT event. The device will be Reset after the NMI counter expires.

The WDTS flag will be set if there is a WDT event during Sleep mode. The WDTS flag will trigger the NMI interrupt, but will not start the NMI counter, nor cause a Reset.

The CF bit (RNMICON[17]) may be set by the Fail-Safe Clock Monitor (FSCM) if there a clock failure is detected. The CF flag will trigger the NMI interrupt, but will not start the timer, nor cause a Reset.

The SWNMI bit (RNMICON[23]) can be set in software to cause a NMI interrupt, but will not start the NMI counter, nor cause a Reset.

12.18.4.10 Determining the Source of Device Reset

After a device Reset, the RCON register can be examined to confirm the source of the reset. All reset status bits in the RCON register should be cleared after reading them to ensure the RCON value will provide meaningful results after the next device Reset.

12.18.5 Effects of Various Resets

The Reset value for the Reset Control register, RCON, will depend on the type of device Reset, as indicated in the following table.

Table 12-4. Status Bits, Their Significance and the Initialization Condition for RCON Register⁽¹⁾

Condition	Program Counter	EXTR	SWR	WDTO	DMTO	SLEEP ⁽²⁾	IDLE (2)	CMR	BOR	POR
Power-on Reset or MCLR set as POR		0	0	0	0	0	0	0	1	1
Brown-out Reset		0	0	0	0	0	0	0	1	u
MCLR Reset during Run Mode		1	u	u	u	u	u	u	u	u
MCLR Reset during Idle Mode		1	u	u	u	u	1	u	u	u
MCLR Reset during Sleep Mode		1	u	u	u	1	u	u	u	u
Software Reset Command		u	1	u	u	u	u	u	u	u
Configuration Word Mismatch Reset		u	u	u	u	u	u	1	u	u
WDT Time-out Reset during Run Mode		u	u	1	u	u	u	u	u	u
WDT Time-out Reset during Idle Mode		u	u	1	u	u	1	u	u	u
WDT Time-out Reset during Sleep Mode		u	u	1	u	1	u	u	u	u
DMT Time-out Reset		u	u	u	1	u	u	u	u	u
Interrupt Exit from Idle Mode	Vector	u	u	u	u	u	1	u	u	u
Interrupt Exit from Sleep Mode		u	u	u	u	1	u	u	u	u

- Legends:

- u = unchanged

- SLEEP or IDLE states are entered when the correct sequence plus WAIT instruction is executed.

12.18.5.1 Special Function Register (SFR) Reset States

Most of the SFRs associated with the CPU and peripherals are reset to a particular value at a device Reset. This also applies to a WDT/DMT NMI condition, which is treated as a full device Reset by the CPU and peripherals.

The reset value for the Reset Control register, RCON, is depending on the type of device reset, as described in [Table 12-4](#).

12.18.5.2 Configuration Word Register Reset States

All Reset conditions force the configuration settings to be reloaded. The POR and BOR resets all the Configuration Word registers before loading the configuration settings. For all other Reset conditions, the Configuration Word registers are not reset prior to being reloaded.

12.18.5.3 Using the RCON Status Bits

The user software can read the RCON register after any system Reset to determine the cause of the reset. The following table provides a summary of the reset flag bit operation.

Note: The status bits in the RCON register should be cleared after they are read, so that the next RCON register value after a device Reset will be meaningful.

Table 12-5. Reset Flag Bit Operation

Flag Bit	Set by	Cleared by
POR (RCON[0])	POR	User Software
BOR (RCON[1])	POR, BOR	User Software
IDLE (RCON[2])	WAIT Instruction	User Software, POR, BOR
SLEEP (RCON[3])	WAIT Instruction	User Software, POR, BOR
WDTO (RCON[4])	WDT Time-out	User Software, POR, BOR
DMTO (RCON[5])	DMT Time-out	User Software, POR, BOR
SWR (RCON[6])	Software Reset Command	User Software, POR, BOR
EXTR (RCON[7])	MCLR Reset	User Software, POR, BOR
CMR (RCON[9])	Configuration Mismatch Reset	User Software, POR, BOR
BCFGFAIL (RCON[26])	Non-recoverable error in Primary and Alternate configuration words	User Software, POR, BOR
BCFGERR (RCON[27])	Recoverable error in primary configuration words	User Software, POR, BOR

12.18.5.4 Device Reset to Code Execution Start Time

The delay between the end of a Reset event and when the device actually begins to execute code is determined by two main factors: the type of Reset, and the system clock source coming out of the Reset. The code execution start time for various types of device Resets are summarized in the following table. Individual delays are characterized in the Electrical Specifications.

Table 12-6. Code Execution Start Time for Various Device Resets

Reset Type	Clock Source	Power-up Delay	System Clock Delay	FSCM Delay
POR	TBD	TBD	TBD	TBD
BOR	TBD	TBD	TBD	TBD
MCLR	TBD	TBD	TBD	TBD
CMR	TBD	TBD	TBD	TBD
SWR	TBD	TBD	TBD	TBD

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.....continued

Reset Type	Clock Source	Power-up Delay	System Clock Delay	FSCM Delay
WDTO	TBD	TBD	TBD	TBD
DMTO	TBD	TBD	TBD	TBD

Preliminary

13. RAMECC – RAM Error Correction Code (ECC)

13.1 Overview

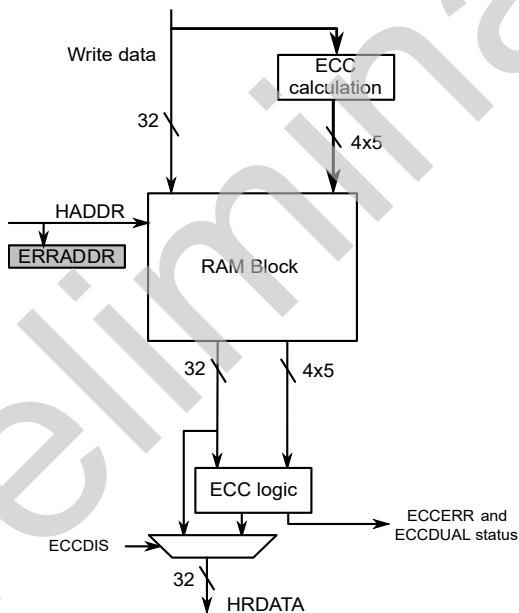
Single bit error correction and dual bit error detection is available for RAM.

13.2 Features

- Single bit correction and dual bit detection.
- Error Interrupt.
- Operates in any Sleep mode.
- Interrupts generated by RAMECC can be used to wake up the device from sleep modes.

13.3 Block Diagram

Figure 13-1. RAMECC Block Diagram



13.4 Signal Description

Not applicable.

13.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

13.5.1 I/O Lines

Not applicable.

13.5.2 Power Management

The RAMECC will continue to operate in any sleep mode where the selected source clock is running. The RAMECC's interrupts can be used to wake up the device from sleep modes. See *Power Management Unit (PMU)* from Related Links for details on the different sleep modes.

Related Links

[14. Power Management Unit \(PMU\)](#)

13.5.3 DMA

Not applicable.

13.5.4 Interrupts

The interrupt request line is connected to the interrupt controller. Using the RAMECC interrupt(s) requires the interrupt controller to be configured first.

13.5.5 Events

Not applicable.

Related Links

[27. Event System \(EVSYS\)](#)

13.5.6 Debug Operation

When the CPU is halted in debug mode the RAMECC will correct and log ECC errors based on the table below.

Table 13-1. ECC Debug Operation

DBGCTRL.ECCELOG	DBGCTRL.ECCDIS	Description
0	0	ECC errors from debugger reads are corrected but not logged in INTFLAG.
1	0	ECC errors from debugger reads are corrected and logged in INTFLAG.
X	1	ECC errors from debugger reads are not corrected or logged in INTFLAG.

If the RAMECC is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

13.5.7 Register Access Protection

All registers with write-access are optionally write-protected by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Flag Status and Clear (INTFLAG) register
- Status (STATUS) register.

Write-protection is denoted by the Write-Protected property in the register description.

Write-protection does not apply to accesses through an external debugger, see *Peripheral Access Controller (PAC)* from Related Links.

Related Links

[25. Peripheral Access Controller \(PAC\)](#)

13.5.8 Analog Connections

Not applicable.

13.6 Functional Description

13.6.1 Principle of Operation

Error Correcting Code (ECC) is implemented to detect and correct errors that may arise in the RAM arrays. The ECC logic is capable of double error detection and single error correction per 8-bit byte.

Upon single bit error detection, the Single Bit Error interrupt flag is raised (INTFLAG.SINGLEE). If a dual error is detected, the Dual Error interrupt flag (INTFLAG.DUALE) is raised. When the first error is detected, the ERRADDR register is frozen with the failing address and remains frozen until INTFLAG.DUALE and INTFLAG.SINGLEE are cleared. If a dual bit error occurs while INTFLAG.SINGLEE is set, the ERRADDR register is updated with the dual bit error information and INTFLAG.DUALE is also set.

The INTFLAG.SINGLEE and INTFLAG.DUALE bits are both cleared on ERRADDR read.

The block diagram shows the ECC interface. When ECC is disabled (CTRLA.ECCDIS=1), the ECC field in RAM is left unchanged on writes. On reads, ECC errors are not corrected or flagged.

Related Links

[13.3. Block Diagram](#)

13.6.2 Interrupts

The RAMECC has the following interrupt sources:

- Dual Bit Error (DUALE): Indicates that a dual bit error has been detected.
- Single Bit Error (SINGLEE): Indicates that a single bit error has been detected.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the ERRADDR register is read, the interrupt is disabled, or the RAMECC is reset.

All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

Related Links

[13.8.3. INTFLAG](#)

13.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	INTENCLR	7:0							DUALE	SINGLEE
0x01	INTENSET	7:0							DUALE	SINGLEE
0x02	INTFLAG	7:0							DUALE	SINGLEE
0x03	STATUS	7:0								ECCDIS
0x04	ERRADDR	7:0	ERRADDR[7:0]							
		15:8	ERRADDR[15:8]							
		23:16								ERRADDR[16]
		31:24								
0x08 ...	Reserved									
0x0F	DBGCTRL	7:0							ECCELOG	ECCDIS

13.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description, see *Register Access Protection* from Related Links.

Related Links

[13.5.7. Register Access Protection](#)

13.8.1 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	7	6	5	4	3	2	1	0
Access							DUALE	SINGLEE
Reset							R/W 0	R/W 0

Bit 1 – DUALE Dual Bit Error Interrupt Enable Clear

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Dual Bit Error Interrupt Enable bit, which disables the Dual Bit Error interrupt.

Value	Description
0	The Dual Bit Error interrupt is disabled.
1	The Dual Bit Error interrupt is enabled.

Bit 0 – SINGLEE Single Bit Error Interrupt Enable Clear

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Single Bit Error Interrupt Enable bit, which disables the Single Bit Error interrupt.

Value	Description
0	The Single Bit Error interrupt is disabled.
1	The Single Bit Error interrupt is enabled.

13.8.2 Interrupt Enable Set

Name: INTENSET
Offset: 0x01
Reset: 0x00
Property: Write-Protected

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	7	6	5	4	3	2	1	0
Access							DUALE	SINGLEE
Reset							R/W 0	R/W 0

Bit 1 – DUALE Dual Bit Error Interrupt Enable Set

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Dual Bit Error Interrupt Enable bit, which enables the Dual Bit Error interrupt.

Value	Description
0	The Dual Bit Error interrupt is disabled.
1	The Dual Bit Error interrupt is enabled.

Bit 0 – SINGLEE Single Bit Error Interrupt Enable Set

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Single Bit Error Interrupt Enable bit, which disables the Single Bit Error interrupt.

Value	Description
0	The Single Bit Error interrupt is disabled.
1	The Single Bit Error interrupt is enabled.

13.8.3 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x02
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
Access							DUALE	SINGLEE
Reset							R/W	R/W

Bit 1 – DUALE Dual Bit ECC Error Interrupt

This flag is set on the occurrence of a dual bit ECC error.

Writing a '0' to this bit has no effect.

Reading the ECCADDR register will clear the Dual Bit Error interrupt flag.

Value	Description
0	No dual bit errors have been received since the last clear.
1	At least one dual bit error has occurred since the last clear.

Bit 0 – SINGLEE Single Bit ECC Error Interrupt

This flag is set on the occurrence of a single bit ECC error.

Writing a '0' to this bit has no effect.

Reading the ECCADDR register will clear the Single Bit Error interrupt flag.

Value	Description
0	No errors have been received since the last clear.
1	At least one single bit error has occurred since the last clear.

13.8.4 Status

Name: STATUS
Offset: 0x03
Reset: 0x00
Property: Read Only, Write-Protected

Bit	7	6	5	4	3	2	1	0	ECCDIS
Access									R
Reset									0

Bit 0 – ECCDIS ECC Disable

This bit is fuse updated at startup. When enabled, the calculated ECC is written to RAM along with data. ECC correction and detection is enabled for reads.

Value	Description
0	ECC detection and correction is enabled.
1	ECC detection and correction is disabled.

13.8.5 Error Address

Name: ERRADDR
Offset: 0x04
Reset: 0x00000000
Property: R

Bit	31	30	29	28	27	26	25	24	
Access									
Reset									
Bit	23	22	21	20	19	18	17	16	ERRADDR[16]
Access									R
Reset									0
Bit	15	14	13	12	11	10	9	8	
Access	R	R	R	R	R	R	R	R	ERRADDR[15:8]
Reset	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	ERRADDR[7:0]
Access	R	R	R	R	R	R	R	R	
Reset	0	0	0	0	0	0	0	0	

Bits 16:0 – ERRADDR[16:0] ECC Error Address

The RAM address offset from RAM start that caused an ECC error. If a single bit error is followed by a dual bit error, this register will be updated with the address of the dual bit error, otherwise it stalls on the first error occurrence. This register will read as zero unless INTFLAG.SINGLE and/or INTFLAG.DUALE are 1.

13.8.6 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access							ECCELOG	ECCDIS
Reset							R/W	R/W
							0	0

Bit 1 – ECCELOG ECC Error Log

When DBGCTRL.ECCDIS=0, This bit controls whether ECC errors are logged in the INTFLAG register. When DBGCTRL.ECCDIS=1, this bit has no meaning.

Value	Description
0	ECC errors for debugger reads are not logged.
1	ECC errors for debugger reads are logged if DBGCTRL.ECCDIS=0.

Bit 0 – ECCDIS ECC Disable

By default, ECC errors during debugger reads are corrected and logged based on DBGCTRL.ECCELOG. Setting this bit will disable ECC correction and logging.

Value	Description
0	ECC errors are corrected for debugger reads and logged based on DBGCTRL.ECCELOG.
1	ECC errors are masked for debugger reads.

14. Power Management Unit (PMU)

14.1 Introduction

This chapter describes the Power Management Unit (PMU) in the PIC32CX-BZ2 wireless microcontroller with the various modes it provides. Its is for information purposes only.

Note:

The PMU is a complex power controller that requires specific configuration and handling by the software for correct, safe operation of the SOC. The software SDK and operational stacks provided by Microchip handles the startup and operation of the PMU. Therefore, Microchip highly recommends using this software framework for all application development on the device.

14.2 Power Modes

To minimize power consumption, the PIC32CX-BZ2 incorporates a PMU that provides both DC-DC (Buck) and LDO power conversion. The input voltage range to the PMU is 1.9V to 3.6V – VDD (main). On power-up, the PIC32CX-BZ2 operates in LDO mode, software must enable the DC-DC Buck converter.

Refer to Electrical Specifications for detailed electrical information.

The power modes and power management features provided by the PMU are shown in the following table.

Table 14-1. Power Modes and Power Management Features

Functions	Device Power Modes					
	Run	Idle	Dream ¹	Sleep(Standby)	Deep Sleep(Backup)	eXtreme Deep Sleep(Off)
CPU	On	Clock Gated	Clock Gated	Clock Gated	Off	Off
Peripherals	On	Idle	On Demand	Clock Gated	Off	Off
Flash	On	Idle	On Demand	Clock Gated	Off	Off
Core System Memory	On	Idle	On Demand	Retention Mode	Off	Off
Radio	On	Idle	On Demand	Clock Gated	Off	Off
DSWDT	On	On	On	On	On	Off
RTCC	On	On	On	On	On	Off
Backup RAM	On	Idle	On Demand	Retention Mode	Retention Mode	Off
XTAL(16 MHz)	On	On	On	On	Off	Off
SPLL	On	On	On Demand	Off	Off	Off
ADC	On	Idle	On Demand	Disabled	Disabled	Disabled
Analog Comp	On	Idle	On Demand	Disabled	Disabled	Disabled
FRC	On	On	On Demand	Off	Disabled	Disabled
LPRC	On	On	On	On	On	On

Note:

1. Dream (Sleep Walking) is not a mode by itself but is a companion mode to Sleep mode. This mode cannot be entered directly through a SW command.

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All transitions from **RUN** state to any of the low power states is simply initiated by WFI command from the CPU. However, prior to initiating the WFI command.

SW performs the following actions:

- Disabling all interrupts
- Setting up the DSCON[DSEN], OSCCON[SLPEN], OSCCON[DRMEN], and Wireless Subsystem Sleep Mode Controls
- Set the Wireless Subsystem into low power mode
- Enable the appropriate wake-up events
- Checking for any pending interrupts and if present, abort deep sleep and service the interrupt
- If no pending interrupts then, issue a SLEEP/WAIT command from the CPU to get into appropriate low power mode

In **Run** mode, the CPU is actively executing code. Run mode provides normal operation of the processor and all peripherals that are currently enabled.

In **Idle** mode, all active peripherals can be clocked, but the CPU core is clock gated off and no code is executed.

In **Dream** mode (or Sleep Walking mode), the CPU is clock gated but peripherals can be turned on on-demand by events related to those peripherals. No code is executed.

In the **Sleep** and **Deep Sleep** modes, the backup RAM is in retention mode, while the CPU and most peripherals are clock gated off and no code is executed.

In **eXtreme Deep Sleep** mode, only the Low Power RC oscillator is enabled. Exiting Deep sleep/XDS is equivalent to Power-on Reset. RCON register provides status whether its a normal power up or exiting from deep sleep/XDS.

The low power mode entry and exit commands and wake up resources are shown in the following table.

Table 14-2. Low Power Mode Entry and Exit commands and Wake up Resources

Device Power Modes	Entry Commands	Wake up Resources
Run	-	-
Idle	WFI Instruction + ~OSCCON[SLPEN]	IRQ, Reset, Others ¹
Dream	OSCCON[DREAM] + Event + Sleep mode	IRQ, Reset, Others
Sleep	~DSCON[DSEN]+OSCCON[SLPEN]+Wireless Sleep followed by WFI	IRQ, Reset, Others
Deep Sleep	DSCON[DSEN]+ {RTCC (Enabled) or DSWDT (Enabled)} + Wireless Sleep followed by WFI	INT0, RTCC, DSWDT, Reset
eXtreme Deep Sleep	DSCON[DSEN]+ {RTCC (Disabled) and DSWDT (Disabled)} + Wireless Sleep followed by WFI	INT0, Reset

Note:

1. Others = System wake-up (Dream), WDT (Timeout Event), DMT (Timeout Event), PLVD Event, PMU Event, External NMI/INT, DSU/ICD Debug Event, CPU Debug Event.

15. WDT - Watchdog Timer

15.1 Overview

The Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. The user can configure the WDT in Windowed mode or non-Windowed mode. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

15.1.1 Features

The key features of the WDT module are:

- Configuration using Fuses (DEVCFG) or Software controlled
- Up to 32 Configurable Time-Out Periods
- Can wake the Device from Sleep or Idle mode
- Independent Run and Sleep mode Counters
- WDT may use alternate Clock source and Postscaler for Run mode Counter
- Independent 5-bit Postscalers for Run and Sleep mode Counters
- Hardware and Software enabled
- Two Clock sources
- Windowed WDT

Note: When the CPU is running on the same clock or clock frequency as the WDT, the lowest pre-scale values may not allow the CPU to have enough time to reset the WDT before it expires.

15.2 Applications

The WDT is a free-running timer with a configurable postscaler. The counter is clocked with an external reference clock until the counter value exceeds the selected WDT period. If enabled, the WDT will continue to operate even if the main processor clock (for example, the crystal oscillator) fails.

The WDT uses separate internal counters for use in Run mode and Sleep/Idle modes. One counter operates only in Run mode; the count value of this counter is frozen when the device is in Sleep or Idle modes.

The second counter operates only in Sleep and Idle modes; it is reset when entering Sleep or Idle. This provides the following benefits:

- A different WDT clock source can be used in Run mode(PB1_CLK or LPRC) vs. Sleep/Idle modes (LPRC only).
- A different post-scale value may be used in Run mode vs. Sleep/Idle modes.
- The Run mode WDT count is preserved while in Sleep or Idle modes, which makes it easier to manage the WDT while in windowed mode.

The WDT can have two modes of operation, Windowed and non-Windowed. In Windowed mode, software can clear the WDT only when the counter is in its final window before a period match occurs. There are four window size options (25%, 37.5%, 50% and 75% of the total WDT period). This window is active when the timer counter is greater than a predetermined value for each option. The window size is determined by the WDTWINSZ configuration fuses, see *System Configuration Registers (CFG)* from Related Links. Any attempts to clear the WDT when the window is not active would cause a device Reset. In non-Windowed configuration, software can clear the WDT anytime before the period match occurs.

Note: Windowed WDT operation is not applicable in Sleep or Idle modes.

Related Links

[17. System Configuration and Locking \(CFG\)](#)

15.2.1 Enabling the WDT

The WDT can be enabled through hardware or software control. The WDT is enabled if WDTEN=1 in DEVCFG2 fuse register. If WDTEN=0, the WDT is disabled, and can be controlled through using the ON bit (WDTCON[15]).

15.2.2 Selecting WDT Clock Source

The Sleep Mode Counter always uses the 32 kHz LPRC clock source. The Run Mode Counter will use the clock source selected by the WDTRMCS bit in fuses Configuration Bits register DEVCFG2 to be either the 32 kHz LPRC clock or the PB1_CLK bus clock (sysclk). See *WDTRMCS[1:0]* bits in the *CFGCON2(L)* register from Related Links.

Related Links

[17.4.3. CFGCON2\(L\)](#)

15.2.3 Clearing the Watch Dog Timer

To clear the WDT, software must write to the WDTKEY register with the value 16'h5743 before the timer expires. The upper two bytes of WDTCON must be written simultaneously, as a 16-bit write. Any other write with a different value or byte size will NOT clear the timer.

15.2.4 Selecting WDT Period

The WDT can be configured for various time-out periods by controlling the WDT postscaler value. The settings are chosen using the WDTPSR[4:0] inputs for the Run Mode Counter and the WDTPSS[4:0] inputs for the Sleep Mode Counter. These values range from 1 to 2²⁰ and allow for time-out periods of from 1ms to over 17 minutes when using the 21 kHz LPRC clock.

15.2.5 Events that Reset both WDT Counters

The following events will reset both internal WDT counters:

- A generic device reset
- Disabling the WDT via the ON bit

15.2.6 Events that Reset only the Run Mode Counter

The following events reset the Run Mode Counter:

- Any counter value greater than the selected WDT period
- Detecting a correct write value to WDTCON.WDTKEY within the correct time window

15.2.7 Events that Reset only the Sleep Mode Counter

The following events reset the Sleep Mode Counter:

- Entry into Sleep or Idle modes
- Any counter value greater than the selected WDT period

15.2.8 Run Mode WDT Event

Once the WDT period is exceeded, or if a correct write value to the WDTCON.WDTKEY is executed in a Windowed mode when the window is not yet active, the WDT event is activated. The event remains active for one clock period.

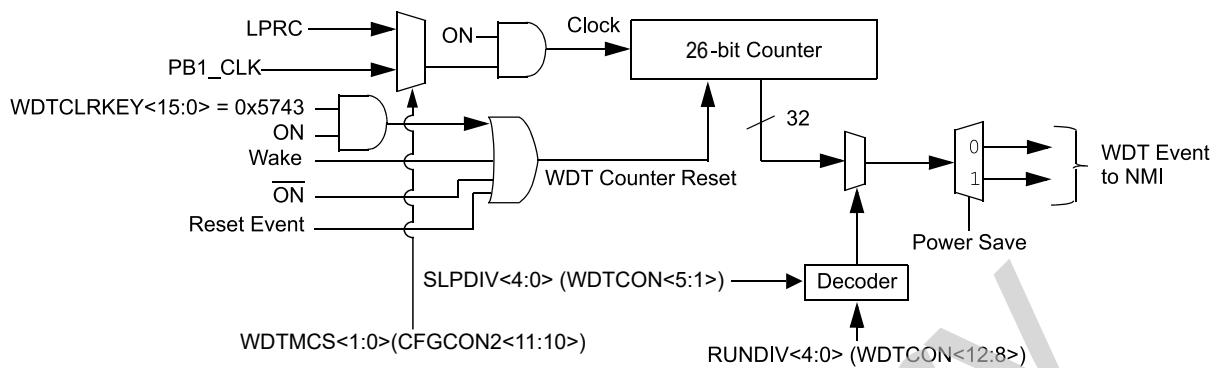
The WDT is reset after the count is exceeded and continues to run.

15.2.9 Sleep Mode WDT Event

Once the WDT period is exceeded, the WDT event is activated. The event remains active for one clock period. The WDT is reset after the count is exceeded.

15.3 Block Diagram

Figure 15-1. Watchdog Timer Block Diagram



15.4 Configuration

The WDT is configured using the following config register bits/fields:

- Window size (CFGCON2.FWINSZ[1:0])
- Windowing disable (CFGCON2.WINDIS)
- Post-scaler selection (CFGCON2.WDTPS[4:0])
- Run Mode Counter clock source (CFGCON2.WDTRMCS[1:0])

15.5 Register Summary - WDT

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	WDTCON	7:0					SLPDIV[4:0]			WDTWINEN
		15:8	ON					RUNDIV[4:0]		
		23:16					WDTCLRKEY[7:0]			
		31:24					WDTCLRKEY[15:8]			

15.6 Register Description

All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Following conventions are used in the following tables:

- R = Readable bit
- W = Writable bit
- — = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
- y = Values set from Configuration bits on POR
- Reset values are shown in hexadecimal.

Related Links

[5.1.9. CLR, SET, and INV Registers](#)

15.6.1 WDTCON - Watchdog Timer Control Register

Name: WDTCON
Offset: 0x00
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
WDTCRKEY[15:8]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
WDTCRKEY[7:0]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
RUNDIV[4:0]								
Access	R/W			R	R	R	R	R
Reset	y			y	y	y	y	y
SLPDIV[4:0] WDTWINEN								
Access			R	R	R	R	R	R/W
Reset			y	y	y	y	y	0

Bits 31:16 – WDTCRKEY[15:0] Watchdog Timer Clear Key bits

To clear the WDT to prevent a time-out, software must write the value 0x5743 to this location using a single 16-bit write. Anything other than a 16-bit write will not reset the WDT. You must use a 16-bit write for the WDTCRKEY[15:0] bits.

Bit 15 – ON Watchdog Timer Enable bit

Note:

1. This bit only has control when the WDTEN bit (DEVCFG2/CFGCON2[23]) = 0.

Value	Description
1	WDT is enabled
0	WDT is disabled

Bits 12:8 – RUNDIV[4:0] Watchdog Timer Postscaler Run Counter Value bits

On Reset, these bits are set to the values of the WDTPSR[4:0] Configuration bits in CFGCON2.

Bits 5:1 – SLPDIV[4:0] Watchdog Timer Postscaler Sleep Counter Value bits

On Reset, these bits are set to the values of the WDTPSS[4:0] Configuration bits in CFGCON1.

Bit 0 – WDTWINEN Watchdog Timer Window Enable bit

Value	Description
1	Enable windowed WDT
0	Disable windowed WDT

16. Deadman Timer (DMT)

16.1 Overview

The Deadman Timer (DMT) module is designed to enable users to monitor the health of their application software by requiring periodic timer interrupts within a user-specified timing window. The DMT module is a synchronous counter and when enabled, counts instruction fetches, and cause a system reset if the DMT counter is not cleared within a set number of instructions. The DMT is typically connected to the system clock that drives the processor. The user specifies the timer time-out value and a mask value that specifies the range of the window, which is the range of counts that is not considered for the comparison event.

16.2 Features

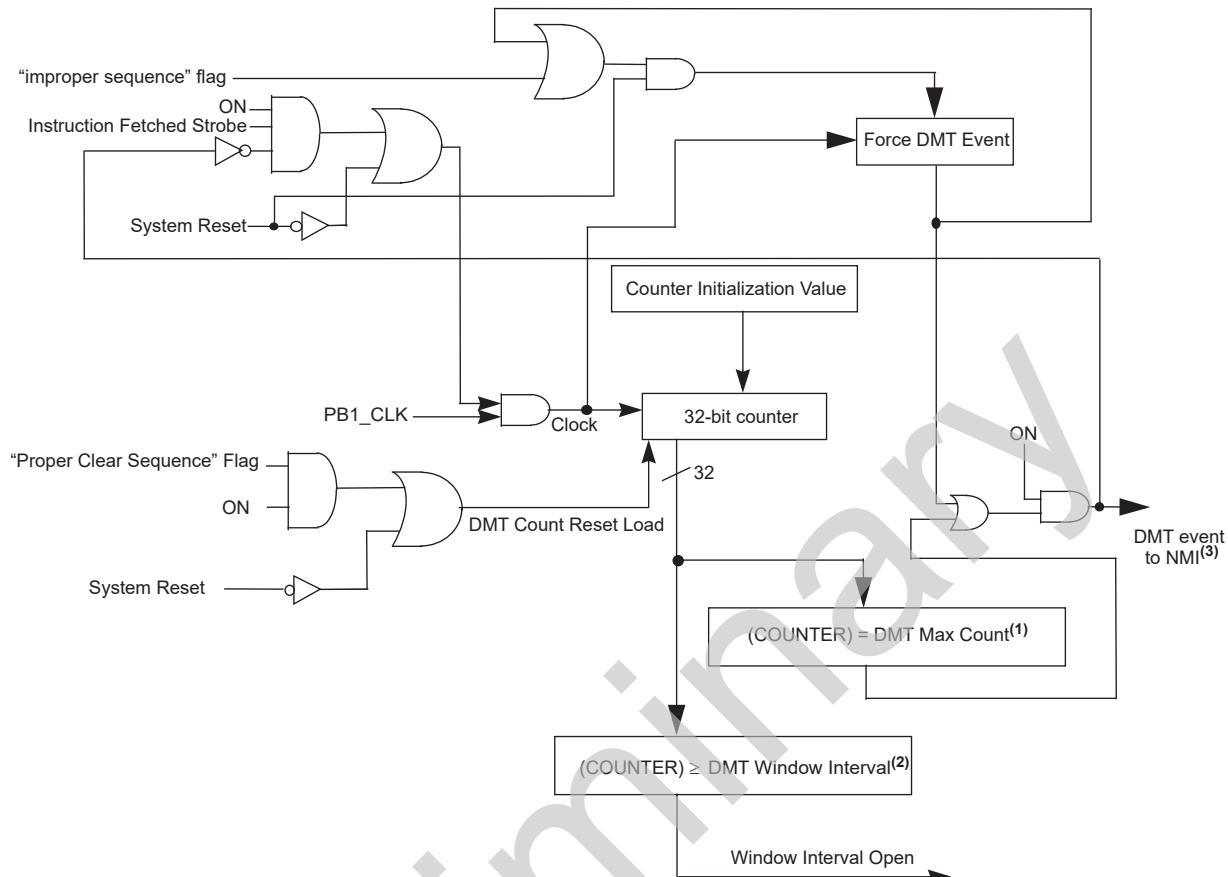
Some of the key features of this module are:

- 32-bit configurable count-limit based on counting instructions fetched
- Hardware or software enable control
- User-configurable time-out period or instruction count
- Two instruction sequence to clear timer
- 32-bit configurable window to clear timer

16.3 Block Diagram

The following figure shows the block diagram of the Deadman Timer.

Figure 16-1. Deadman Timer Block Diagram



Notes:

1. DMT Max Count is controlled by the DMTCNT[4:0] bits in the CFGCON2 register "Maximum = 2^31".
2. DMT Window Interval is controlled by the DMTINTV[2:0] bits in the CFGCON2 register.
3. For more details, see *Resets* from Related Links.

Related Links

[12.18. Resets](#)

16.4 DMT Operation

16.4.1 Mode of Operation

The primary function of the Deadman Timer (DMT) module is to reset the processor in the event of a software malfunction. The DMT module, which works on the system clock, is a free running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. The instructions are not fetched when the processor is in the Sleep mode.

The DMT module consists of a 32-bit counter, the read-only DMTCNT register with a time-out count match value as specified by the 32-bit DMT count configuration fuse bits CFGCON2.DMTCNT[4:0]. Whenever the count match occurs, a DMT reset event will occur and the DMTEVENT bit in DMTSTAT register will be set.

A DMT module is typically used in mission critical and safety critical applications, where any failure of the software functionality and sequencing must be detected.

16.4.2 Enabling and Disabling the DMT Module

Because of the nature of the Deadman Timer, PMD register bit is not provided to enable/disable the module. The DMT module can be enabled or disabled by the DMT enable (DMTEN) bit in Configuration Control Register 2 (CFGCON2) fuse register or it can be enabled through software by writing to the Deadman Timer Control (DMTCON) register. Once the DMT is enabled, it may not be disabled without a device reset.

If the DMTEN configuration bit in the CFGCON2 fuse register is set, the DMT is always enabled. The ON control bit (DMTCON[15]) in DMTCON register will reflect this by reading a '1'. In this mode, the ON bit (DMTCON[15]) cannot be cleared in software. To disable the DMT, the DMTEN configuration bit must be cleared in CFGCON2 fuse register. When DMTEN is cleared to '0' in the CFGCON2, the DMT is disabled in hardware.

Software can enable the DMT by setting the ON bit in the DMTCON register. However, for software control, the DMTEN configuration bit in the CFGCON2 fuse register should be set to '0'.

16.4.3 DMT Count Windowed Interval

The DMT module has the Windowed Operation mode. The DMT interval (DMTINV[2:0]) bits in Configuration Control Register 2 (CFGCON2) fuse register sets the window interval value. The PSINTV[31:0] bits in DMT interval post status register (DMTPSINTV) allows the software to read the DMT window interval value. That means this register reads the value which is written to the DMT interval (DMTINV[2:0]) bits in Configuration Control Register 2 (CFGCON2) fuse register.

In the Windowed mode, software can clear the DMT only when the counter is in its final window before a count match occurs. That is, if the DMT counter value is greater than or equal to the value written to the window interval value, only then the DMT clear sequence can be executed in the DMT module. If the DMT is cleared before the allowed window, a DMT reset event is immediately generated.

16.4.4 DMT Count Selection

The Deadman Timer count is set by the DMT count configuration (DMTCNT[4:0]) bits in Configuration Control Register 2 (CFGCON2) fuse register. The current DMT count value can be obtained by reading the DMT count register DMTCNT.

The PSCNT[31:0] bits in the DMT count post status register (DMTPSCNT) allows the software to read the maximum count selected for the DMT. The PSCNT_x bit values are the values that are initially written to the DMTCNT_x bits in the CFGCON2 fuse register. Whenever the DMT event occurs, the user can always compare to see whether the current counter value in the DMTCNT register is equal to the value of the DMTPSCNT register, which hold the maximum count value.

Whenever the DMT current counter value in DMTCNT reaches the value of the DMTPSINTV register, the window interval opens therefore the user can execute the DMT clear sequence. Window interval open is indicated by the WINOPN bit in DMTSTAT register.

The UPRCNT[15:0] bits in the DMT hold register (DMTHOLDREG) holds the value of the last read DMT upper count values whenever DMTCNT is last read.

16.4.5 DMT Operation in Power-Saving Modes

As the DMT module is only incremented by instruction fetches, the count value will not change when the core is inactive. The DMT module remains inactive in the Sleep and Idle modes. As soon as the device wakes-up from Sleep or Idle, the DMT counter starts incrementing again for every instruction fetch.

16.4.6 Resetting the DMT

The DMT can be reset in two ways: one way is after a system reset and another way is by writing an ordered sequence to the DMT pre-clear register (DMTPRECLR) and DMT clear register (DMTCLR) in a specific two step sequence.

Clearing the DMT counter value requires the following sequence of operations:

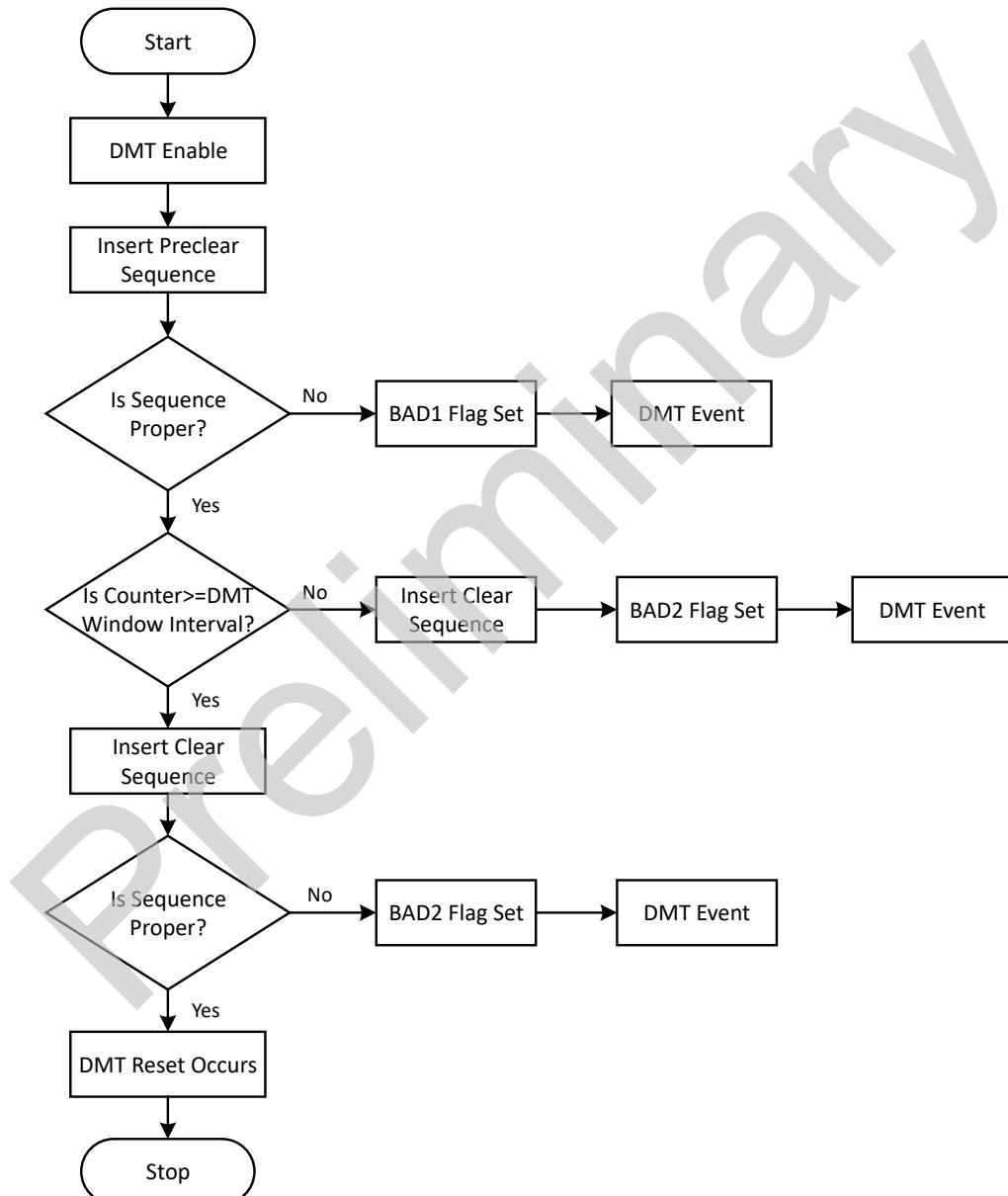
1. The STEP1[7:0] bits in the DMTPRECLR register must be written as '01000000' (0x40). This action sets "enable for clearing" state which enables the DMT to be cleared by step 2.
2. The STEP2[7:0] bits in the DMTCLR register must be written as '00001000' (0x08). This can only be done if preceded by Step 1 and the DMT is in the open window interval.

Once these values are written, following are cleared to zero:

- DMTCNT counter
- DMTPRECLR register
- DMTCLR register
- DMTSTAT register

If any value other than 0x40 is written to the STEP1x bits, the BAD1 bit in the DMTSTAT register will be set and it causes a DMT event to occur. Any value other than 0x08, written to the STEP2x bits, will cause the BAD2 bit to be set in the DMTSTAT register. Also, if Step 2 is not preceded by Step 1 or Step 2 is not carried out in the open window interval, it causes the BAD2 flag to be set. Immediately, a DMT event will occur. In both these cases the DMTEVENT bit in DMTSTAT register will be set. Refer to the flowchart as shown in the following figure.

Figure 16-2. Flowchart for Clearing the DMT



16.5 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	DMTCON	7:0								
		15:8	ON							
		23:16								
		31:24								
0x04 ... 0x0F	Reserved									
0x10	DMTPRECLR	7:0								
		15:8					STEP1[7:0]			
		23:16								
		31:24								
0x14 ... 0x1F	Reserved									
0x20	DMTCLR	7:0				STEP2[7:0]				
		15:8								
		23:16								
		31:24								
0x24 ... 0x2F	Reserved									
0x30	DMTSTAT	7:0	BAD1	BAD2	DMT_EVENT					WINOPN
		15:8								
		23:16								
		31:24								
0x34 ... 0x3F	Reserved									
0x40	DMTCNT	7:0			COUNTER[7:0]					
		15:8			COUNTER[15:8]					
		23:16			COUNTER[23:16]					
		31:24			COUNTER[31:24]					
0x44 ... 0x4F	Reserved									
0x50	DMTHOLDREG	7:0			UPRCNT[7:0]					
		15:8			UPRCNT[15:8]					
		23:16								
		31:24								
0x54 ... 0x5F	Reserved									
0x60	DMTPSCNT	7:0			PSCNT[7:0]					
		15:8			PSCNT[15:8]					
		23:16			PSCNT[23:16]					
		31:24			PSCNT[31:24]					
0x64 ... 0x6F	Reserved									
0x70	DMTPSINTV	7:0			PSINTV[7:0]					
		15:8			PSINTV[15:8]					
		23:16			PSINTV[23:16]					
		31:24			PSINTV[31:24]					

16.6 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

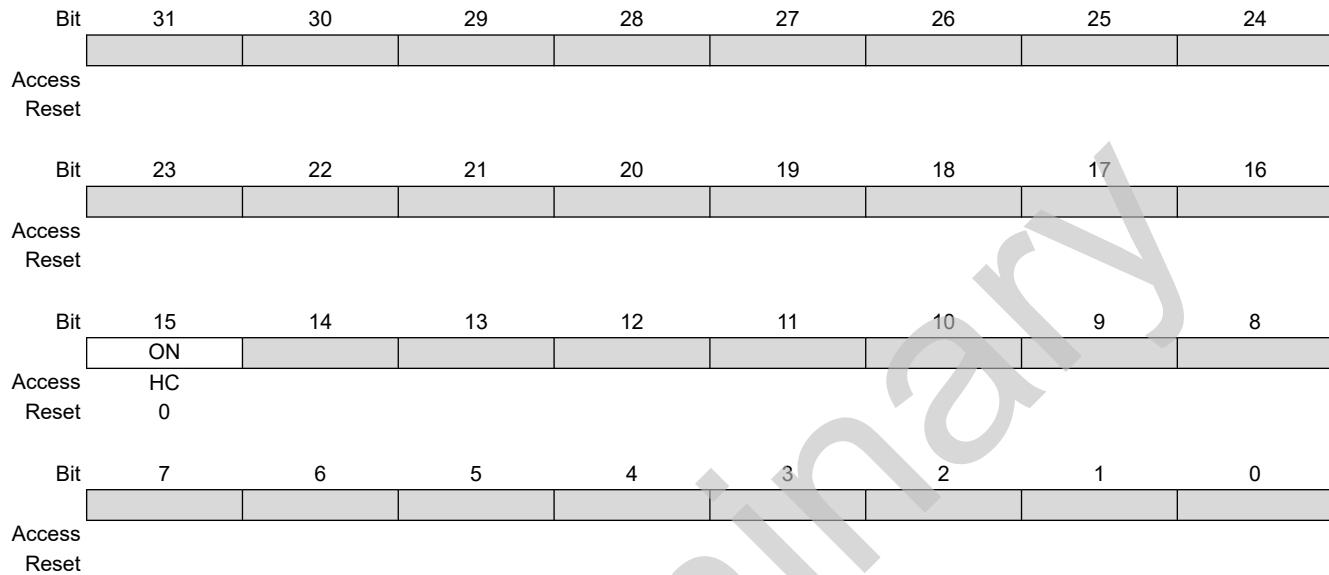
Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

All registers in the Register Summary table have corresponding CLR, SET and INV registers with the suffix appended to the register name, for example: <reg>SET, <reg>CLR, <reg>INV at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

Preliminary

16.6.1 Deadman Timer Control

Name: DMTCON
Offset: 0x00
Reset: 0x00
Property: -



Bit 15 – ON On bit

The ON bit reflects the status of the configuration fuse CFGCON2.DMTEN, if the fuse is set.

Value	Description
1	Enables the Deadman Timer if the event configuration fuse is not enabled.
0	The DMT disabled.

16.6.2 Deadman Timer Preclear

Name: DMTPRECLR
Offset: 0x10
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	STEP1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – STEP1[7:0] Pre-Clear Enable bit when write pattern is:

Value	Description
01000000	Enables the Deadman Timer Pre-Clear (STEP 1).
all other write patterns	Sets DMTSTAT.BAD1 flag to '1'. Note: Bits 15:8 are cleared when a DMT reset event occurs. STEP1 is also cleared if DMTCLR.STEP2 is loaded with the correct value in the correct sequence.

16.6.3 Deadman Timer Clear

Name: DMTCLR
Offset: 0x20
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				STEP2[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – STEP2[7:0] Clear Timer bit when write pattern is:

Value	Description
00001000	Clears DMTPRECLR.STEP1, DMTCLR.STEP2 and the Dead Man Timer if, and only if, preceded by correct loading of Pre-Clear Enable (STEP1) in the correct sequence. The write to DMTCLR.STEP2 field may be verified by reading DMTCNT and observing the counter being reset.
all other write patterns	DMTSTAT.BAD2 flag is set to '1', the value in the DMTPRECLR.STEP1 will remain unchanged, and the new value being written DMTCLR.STEP2 will be captured. Note: These bits 7:0 are also cleared when a DMT reset event occurs.

16.6.4 Deadman Timer Status

Name: DMTSTAT
Offset: 0x30
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R					R
Reset	0	0	0					0

Bit 7 – BAD1 When incorrect DMTPRECLR.STEP1 value is detected, this bit is set. It is cleared by a Reset.

Bit 6 – BAD2 When incorrect value of DMTCLR.STEP2 is detected, this bit is set. It is cleared by a Reset.

Bit 5 – DMT_EVENT This bit is set when Deadman timer event is detected (counter expired or bad STEP1[7:0] or STEP2[7:0] value is entered prior to counter increment). This bit remains set and is cleared by only by a Reset.

Bit 0 – WINOPN Deadman Timer Clear Window bit.

A value of ‘1’ indicates that a STEP2 “clear” action can take place and if this “clearing” action occurs as part of a correct sequence of actions, the DMT counter will be cleared.

16.6.5 Deadman Timer Count

Name: DMTCNT
Offset: 0x40
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
COUNTER[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNTER[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNTER[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNTER[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNTER[31:0] Read current contents of DMT Counter.

16.6.6 Deadman Timer Count Holding Register

Name: DMTHOLDREG
Offset: 0x50
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	UPRCNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	UPRCNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – UPRCNT[15:0]

It is the content of DMTCNT.COUNTER[31:16] when counter was last read to ensure a synchronous snapshot of counter. This register is initialized to '0' on reset and is only loaded when the DMTCNT register is read.

16.6.7 Post Status Configure DMT Count Status Register

Name: DMTPSCNT
Offset: 0x60
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
PSCNT[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSCNT[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSCNT[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSCNT[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSCNT[31:0]

DMT Instruction Count Value Configuration Fuse Status bits. This bit always reflects the value of CFGCON2.DMTCNT.

16.6.8 Post Status Configure DMT Interval Status Register

Name: DMTPSINTV
Offset: 0x70
Reset: 0x00
Property: -

Bit	31	30	29	28	27	26	25	24
PSINTV[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSINTV[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSINTV[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
PSINTV[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSINTV[31:0] DMT Window Interval Configuration Status bits.

This bit reflects the value of CFGCON2.DMTINTV.

17. System Configuration and Locking (CFG)

17.1 Overview

This device provides several user writable configuration registers related to the configuration and operation of the system. The registers marked with (L) are loadable from Flash via their corresponding FBCFG* registers in the following table. The user must program these FBCFG* registers, which then loads the appropriate register after reset.

This device provides a single user writable configuration register related to boot configuration of the device. BCFG0 register provides control, selection and locking for various features of the device, including Flash BCFG7-0 valid, Flash Signature Bit (read only), Code Protect Status (read only). BCFG0 is a read-only register, loaded from Flash register FBCFG0 in the following table.

Table 17-1. Writable Configuration Registers

Register	Address	Destination
FBCFG0	0x0004_5F9C	BCFG0 (0x4400_0200)
FBCFG1/DEVCFG0	0x0004_5F98	CFGCON0(L) (0x4400_0000)
FBCFG2/DEVCFG1	0x0004_5F94	CFGCON1(L) (0x4400_0010)
FBCFG3/DEVCFG2	0x0004_5F90	CFGCON2(L) (0x4400_0020)
FBCFG4/DEVCFG4	0x0004_5F8C	CFGCON4(L) (0x4400_0040)
FBCFG5/FUSERID	0x0004_5F88	USERID(L) (0x4400_00A0)

CFGCON0(L) – Provides control, selection and locking for various features of the device.

- PPS register locking
- PMD register locking
- CFGPG register locking
- Config register locking
- JTAG port enable and configuration
- Trace port enable
- Flash ECC control

CFGCON1(L) – Provides control, selection and locking for various features of the device.

- Debug port and feature configuration CFGCON0 locking control
- Class B functionality enable

CFGCON2(L) – Provides control, selection and locking for various features of the device.

- Deadman timer enable and configuration
- Watchdog timer enable and configuration
- Clock monitoring and control
- Oscillator enable and configuration
- 2-Speed start-up enabled in the Sleep mode bit

CFGCON4(L) – Provides control, selection and locking for various features of the device.

- Deep sleep modules control
- SOSC configuration control

CFGPGQOS – The CFGPGQOS register defines the permission group settings for various bus masters on the device bus matrix.

USER_ID(L) – The USER_ID register is used to provide the end user with a 16-bit ID field that may be read out directly through the JTAG interface via the USER_ID JTAG instruction.

BCFG0 - Used to set Code Protect, Sign Bit, and control PCHE cache mode.

17.2 Applications

17.2.1 Loading User/Device Configuration Registers

The non BCFG system configuration registers (CFGCON* and CFGCON(L)*) are available in memory mapped area under software based locking control.

There are registers which do not have permanent storage e.g. WiFi (RF, BBP, PHY) System Configurations and Calibration values, System PLLs, CRU clock switching, and Analog calibration values. For these registers, the firmware (boot code and/or application code) must allocate nonvolatile storage of system configuration values and load them into the memory mapped system configuration registers during a device boot. The recommended non volatile storage space in NVR boot memory is shown in the Flash Memory Organization table, see *Flash Memory Organization* from Related Links.

In general, if the reset value or flash loaded value of a system configuration register is the value that is required, then it is not necessary to load the system configuration register during a device boot.

Related Links

[23.4.2. Flash Memory Organization](#)

17.2.2 Locking and Unlocking the System Configuration Registers

Write access to the system configuration registers is controlled via the CFGCON0.CFGLOCK[1:0] register bits.

17.2.3 NMI Events

The only system configuration register that gets reset on an NMI event is CFGPGQOS. Resetting the CFGPGQOS register on an NMI allows application firmware to pass control back to the boot-loader and re-enable reads of all configuration words from Boot Flash NVR pages if reads of the NVR pages were disabled using group permissions.

17.2.4 Alternate System Configuration

In order to provide better data retention for the configuration data (compared to the data retention of the rest of the device Flash), each set of DEVCFGx, FBCFG0 registers are duplicated in an alternate set. As time passes, this improves the chances of correct system configuration out of reset. In the event of an uncorrectable error in a word (ECC DED), the flash controller uses the alternate set to obtain the correct data.

Table 17-2. Alternate Register

Register	Alternate Register
FBCFG0	ALTFBCFG0(0004_5E9C)
DEVCFG0	ALTDEVCFG0(0004_5E98)
DEVCFG1	ALTDEVCFG1(0004_5E94)
DEVCFG2	ALTDEVCFG2(0004_5E90)
DEVCFG4	ALTDEVCFG4(0004_5E8C)
FUSERID	ALTFUSERID(0004_5E88)

PIC32CX-BZ2 and WBZ45 Family

System Configuration and Locking (CFG)

17.3 CFG Register Summary

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CFGCON0(L)	7:0	CPENFILT	ACCMPP1_ALT EN	GPSOSCE*	ADCOPVR	JTAGEN	TROEN	SWOEN	TDOEN
		15:8	CFGLOCK[1:0]		IOLOCK	PMDLOCK	PGLOCK	PMULOCK	RTCOUT_ALT EN	RTCIN0_ALT EN
		23:16	SLRTEN2	SLRTEN1	SLRTENO	HPLUGDIS	SMBUSEN2	SMBUSEN1	SMBUSEN0	VBCMODE
		31:24		FRECCDIS	FECCCON/ECCCTL[1:0]	ADFCEN	INT0P	INT0E	PCM	
0x04 ... 0x0F	Reserved									
0x10	CFGCON1(L)	7:0	ZBTWKSYS		TRCEN	ICESEL[1:0]			DEBUG[1:0]	
		15:8	QSCHE_EN	SMCLR	SLRCTRL2	SLRCTRL1	SLRCTRL0	CLASSBDIS	CMP1_OE	CMP0_OE
		23:16	I2CDSEL2	I2CDSEL1	I2CDSEL0	CCL_OE		SCOM_HSEN[2:0]		QSPI_HSEN
		31:24		CLKZBREF	QSPIDDRM			WDTPSS[4:0]		
0x14 ... 0x1F	Reserved									
0x20	CFGCON2(L)	7:0	PMUTEST_V DD_EN		DMTINTV[2:0]			ACMP_CYCLE[2:0]		
		15:8	FSCMEN	CKSWEN	WAKE2SPD	SOSCSEL	WDTRMC[1:0]	POSCMD[1:0]		
		23:16	WDTEN	WINDIS	WDTSPGM		WDTPSR[4:0]			
		31:24	DMTEN		DMTCNT[4:0]			WINSZ[1:0]		
0x24 ... 0x3F	Reserved									
0x40	CFGCON4(L)	7:0			SOSC_CFG[7:0]					
		15:8	MLPCLK_MO D	VBKP_DIVSE L	VBKP_32KCSEL[1:0]	VBKP_1KCSE L	RTCEVENT_ EN	RTCEVENTSEL[1:0]		
		23:16		DSWDTPS[2:0]	DSZPBOREN		CPEN_DLY[2:0]		RTCEVTYPE	
		31:24	RTCNMT_CS EL	LPOSSEN	UVREGROVR	DSBITEN	DSWDTEN	DSWDTLPRC		DSWDTPS[4:3]
0x44 ... 0x4F	Reserved									
0x50	CFGPGQOS	7:0	ICDJQOS[1:0]		ICDJPG[1:0]		CPUQOS[1:0]	CPUPG[1:0]		
		15:8						DMAPG[1:0]		
		23:16	ICMQOS[1:0]		ICMPG[1:0]		ADCQOS[1:0]	ADCPG[1:0]		
		31:24	WISIBQOS[1:0]		FCQOS[1:0]			DSUPG[1:0]		
0x54 ... 0x5F	Reserved									
0x60	CFGPCLKGEN1	7:0	RCD		FREQMRCSEL[2:0]	EICCD		EICCSEL[2:0]		
		15:8	S01D		SERCOM01CSEL[2:0]	MCD		FREQMMCSEL[2:0]		
		23:16	TCC12CD		TCC12CSEL[2:0]	S23D		SERCOM23CSEL[2:0]		
		31:24	CM4TD		CM4TCSEL[2:0]	TC23CD		TC23CSEL[2:0]		
0x64 ... 0x6F	Reserved									
0x70	CFGPCLKGEN2	7:0	C2D		EVSYS2SEL[2:0]	C1D		EVSYS1SEL[2:0]		
		15:8	C4D		EVSYS4SEL[2:0]	C3D		EVSYS3SEL[2:0]		
		23:16	C6D		EVSYS6SEL[2:0]	C5D		EVSYS5SEL[2:0]		
		31:24	C8D		EVSYS8SEL[2:0]	C7D		EVSYS7SEL[2:0]		
0x74 ... 0x7F	Reserved									

PIC32CX-BZ2 and WBZ45 Family System Configuration and Locking (CFG)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x80	CFGPCLKGEN3	7:0	C10D	EVSYSC10SEL[2:0]			C9D	EVSYSC9SEL[2:0]		
		15:8	C12D	EVSYSC12SEL[2:0]			C11D	EVSYSC11SEL[2:0]		
		23:16	TCC0CD	TCC0CSEL[2:0]			ACCD	ACCLKSEL[2:0]		
		31:24	TC1CD	TC1CSEL[2:0]			TC0CD	TC0CSEL[2:0]		
0x84 ... 0x9F	Reserved									
0xA0	USER_ID	7:0		USER_ID[7:0]						
		15:8		USER_ID[15:8]						
		23:16								
		31:24								
0xA4 ... 0x01FF	Reserved									
0x0200	BCFG0	7:0								PCSCMODE
		15:8								
		23:16								
		31:24	BINFOVALID0	SIGN	CP					

17.4 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

PIC32CX-BZ2 and WBZ45 Family

System Configuration and Locking (CFG)

17.4.1 Configuration Control Register 0

Name: CFGCON0(L)
Offset: 0x00
Reset: 0x7100000b
Property: -

The CFGLOCK[1:0] register bits are writable only when CFGLOCK[0] = 1'b0.

The IOLOCK, PMDLOCK and PGLOCK register bits can only be cleared on a system reset. Thereafter, it is controlled as described above.

This register is loaded with trusted data from FBCFG1 during pre-boot period. Trusted data from Flash means when there is no BCFG* fail status and BINFOVALID = 0 during Flash configuration word reads. If accompanied by fail status or blank/erase indication then reset values (described in the register description below) are retained and new values from FBCFG1 are not loaded.

Under all conditions Flash loading is omitted for following bits in CFGCON0 and HPLUGDIS register:

- IOLOCK
- CFGLOCK[1:0]
- PMDLOCK
- PGLOCK
- PMULOCK
- JTAGEN

Bit	31	30	29	28	27	26	25	24
		FRECCDIS	FECCCON/ECCCTL[1:0]		ADCFCEN	INT0P	INT0E	PCM
Access		R/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset		1	1	1	0	0	0	1
Bit	23	22	21	20	19	18	17	16
	SLRTEN2	SLRTEN1	SLRTEN0	HPLUGDIS	SMBUSEN2	SMBUSEN1	SMBUSEN0	VBCMODE
Access	R/W/L	R/W/L	R/W/L	R/W	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CFGLOCK[1:0]	IOLOCK	PMDLOCK	PGLOCK	PMULOCK	RTCOUT_ALTE_N	RTCIN0_ALTE_N	
Access	R/W/L	R/W/L	R/S/L	R/S/L	R/S/L	R/S/L	R/W/L	R/W/L
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CPENFILT	ACCMPI_ALTE_N	GPSOSCE*	ADCOPVR	JTAGEN	TROEN	SWOEN	TDOEN
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	1	0	1	1

Bit 30 – FRECCDIS Flex RAM ECC Control

Notes:

- This bit is only writable when CFGLOCK[1:0] is '00'.
- Only a read-only fuse bit, sets the initialization value of RAMECC Control. "True" RAMECC override is available in RAMECC module.

Value	Description
1	ECC is disabled
0	ECC is enabled

PIC32CX-BZ2 and WBZ45 Family

System Configuration and Locking (CFG)

Bits 29:28 – FECCCON/ECCCTL[1:0] Flash ECC Control

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
11	ECC and dynamically ECC are disabled
10	ECC and dynamically ECC are disabled
01	Dynamically ECC is enabled
00	ECC is enabled (NVMOP = Word Programming disabled)

Bit 27 – ADCFCEN ADC FC Channel Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Exclusive ADC FC Channel Enable (Disables all second/third class channels)
0	ADC FC Channel Disable (Only second/third class channels are enabled)

Bit 26 – INT0P INT0P Polarity

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	INT0 Polarity (Positive)
0	INT0 Polarity (Negative)

Bit 25 – INT0E INT0 Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	INT0 Enabled
0	INT0 Disabled

Bit 24 – PCM PCHE I/D Cacheable Mode

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Always enabled from outside. Can be further enabled/disabled by PCHE SFR registers.
0	The cache-ability is controlled by the CPU via HPROT[3]. This feature is not available on all the ARM cores.

Bit 23 – SLRTEN2 SLRT Enable for SERCOM2

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate enabled
0	Slew rate disabled

Bit 22 – SLRTEN1 SLRT Enable for SERCOM1

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate enabled
0	Slew rate disabled

Bit 21 – SLRTEN0 SLRT Enable for SERCOM0

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate enabled
0	Slew rate disabled

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Bit 20 – HPLUGDIS Hot Plugging Disable (outside fuse loading)

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Disabled
0	Enabled

Bit 19 – SMBUSEN2 SMBus Enable for SERCOM2

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	SMBus enabled
0	SMBus disabled

Bit 18 – SMBUSEN1 SMBus Enable for SERCOM1

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	SMBus enabled
0	SMBus disabled

Bit 17 – SMBUSEN0 SMBus Enable for SERCOM0

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	SMBus enabled
0	SMBus disabled

Bit 16 – VBCMODE VBC Operating Mode

Notes:

- This bit is only writable when CFGLOCK[1:0] is ‘00’.
- Do not change this field if there are pending accesses to VDDBKUPCORE memory map. Failing to do so may result in unexpected data.

Value	Description
1	Indirect addressing. The VDDBKUPCORE IO mapped using PMU Controller.
0	Direct addressing. The VDDBKUPCORE memory mapped on PB-Bridge-B.

Bits 15:14 – CFGLOCK[1:0] Configuration Register Lock

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’ or ‘10’.

Value	Description
11	All NVR memory self-writes, Boot Configuration (BCFG0) and System Configuration registers (CFG* and USER_ID) are locked and cannot be written - CFGLOCK value cannot be changed.
10	All NVR memory self-writes, Boot Configuration (BCFG0) and System Configuration registers (CFG* and USER_ID) are locked and cannot be written - CFGLOCK value can be changed.
01	Reserved for future use
00	All NVR memory self-writes, Boot Configuration (BCFG0) and System Configuration registers (CFG* and USER_ID) are not locked and can be written - CFGLOCK value can be changed.

Bit 13 – IOLOCK IO Lock

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	IO Remap SFR bits are locked and cannot be modified
0	IO Remap SFR are not locked and can be modified

Bit 12 – PMDLOCK Peripheral Module Disable (PMD) Lock

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

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Value	Description
1	PMDx SFR bits are locked and cannot be modified
0	PMDx SFR bits are not locked and can be modified

Bit 11 – PGLOCK Permission Group Lock

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	CFGPG SFR bits are locked and cannot be modified
0	CFGPG SFR bits are not locked and can be modified

Bit 10 – PMULOCK PMU Controller Register Lock

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	PMU* SFR bits are locked and cannot be modified
0	PMU* SFR bits are not locked and can be modified

Bit 9 – RTCOUT_ALTEN RTCOUT Alternate Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	RTC/OUT is available on PA10
0	RTC/OUT is available on PA4

Bit 8 – RTCIN0_ALTEN RTCIN0 Alternate Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	RTC/IN0 is available on PA9
0	RTC/IN0 is available on PA3

Bit 7 – CPENFILT ADC CP Filter Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	ADC CP Filter Enabled
0	ADC CP Filter Disabled

Bit 6 – ACCMP1_ALTEN AC CMP1 Alternate Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	AC/CMP1 Out is available on PA6
0	AC/CMP1 Out is available on PA1

Bit 5 – GPSOSCE* GPIO/SOSC Enable* This bit is not applicable to 48-pin devices PIC32CX1012BZ25048.

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	SOSC Selected
0	GPIO Selected

Bit 4 – ADCOPVR ADC Charge Pump Override

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Overriden (SW Controlled)
0	HW Controlled

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System Configuration and Locking (CFG)

Bit 3 – JTAGEN JTAG Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	JTAG Port Enabled
0	JTAG Port Disabled

Bit 2 – TROEN Trace Output Enable

Notes:

- When CFGCON1.TRCEN=0, the value of this bit is ignored but has the effect of being ‘0’.
- This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Start Trace Clock and enable Trace Outputs (Trace probe must be present)
0	Stop Trace Clock and disable Trace Outputs

Bit 1 – SWOEN SWO enable on 2-wire debug interface

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	SWO Enabled
0	SWO Disabled

Bit 0 – TDOEN TDO enable for 2-wire JTAG

Implementing the JTAG protocol over the 2-wire interface requires four 2-wire clocks for each TCK if TDO is required. However, if the values shifted out TDO are predetermined, then TDO can be disabled saving two 2-wire clocks.

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	2-wire JTAG protocol uses TDO (Four phase (Full Duplex) Protocol)
0	2-wire JTAG protocol does not use TDO (Two phase (Half Duplex) Protocol)

PIC32CX-BZ2 and WBZ45 Family

System Configuration and Locking (CFG)

17.4.2 Configuration Control Register 1

Name: CFGCON1(L)
Offset: 0x10
Reset: 0x1f00443b
Property: -

This register is loaded with trusted data from FBCFG2 during pre-boot period. Thereafter, it is controlled as described above.

Trusted data from Flash means when there is no BCFG* fail status during Flash configuration word reads. If accompanied by fail status or blank/erase indication then reset values (described in the register description below) are retained and new values from FBCFG2 are not loaded.

Under all conditions Flash loading is omitted for following bits in CFGCON1 register:

- DEBUG[1:0]

Bit	31	30	29	28	27	26	25	24
		CLKZBREF	QSPIIDDRM	WDTPSS[4:0]				
Access		R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset		0	0	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
	I2CDSEL2	I2CDSEL1	I2CDSEL0	CCL_OE	SCOM_HSEN[2:0]			QSPI_HSEN
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	QSCHE_EN	SMCLR	SLRCTRL2	SLRCTRL1	SLRCTRL0	CLASSBDIS	CMP1_OE	CMP0_OE
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	0	0	0	1	0	0
Bit	7	6	5	4	3	2	1	0
	ZBTWKSYS		TRCEN	ICESEL[1:0]			DEBUG[1:0]	
Access	R/W/L		R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0		1	1	1	1	1	1

Bit 30 – CLKZBREF External Reference Clock ZB Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Enable clk_zb_to_ext on PPS.REFO1
0	No clk_zb_to_ext on PPS.REFO1, PPS.REFO1 is unchanged

Bit 29 – QSPIIDDRM QSPI DDR Mode Clock Enable

Notes:

- When using the QSPI DDR Mode, System Clock (sys_clk) should be <= 48 MHz.
- This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	QSPI DDR Mode Clock Enable
0	Disabled

Bits 28:24 – WDTPSS[4:0] Watchdog Timer Post-scale Select Sleep bits

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
10100	1:1048576
10011	1:524288

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Value	Description
10010	1:262144
10001	1:131072
10000	1:65536
01111	1:32768
01110	1:16384
01101	1:8192
01100	1:4096
01011	1:2048
01010	1:1024
01001	1:512
01000	1:256
00111	1:128
00110	1:64
00101	1:32
00100	1:16
00011	1:8
00010	1:4
00001	1:2
00000	1:1

Bit 23 – I2CDSEL2 I2C Delay Select for SERCOM2

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	I2C Delay Enabled
0	I2C Delay Disabled

Bit 22 – I2CDSEL1 I2C Delay Select for SERCOM1

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	I2C Delay Enabled
0	I2C Delay Disabled

Bit 21 – I2CDSEL0 I2C Delay Select for SERCOM0

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	I2C Delay Enabled
0	I2C Delay Disabled

Bit 20 – CCL_OE CCL Pads (via PPS) Output Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Enable
0	Disable

Bits 19:17 – SCOM_HSEN[2:0] SCOM (Direct) Enable, 17=SCOM0, 18=SCOM1, 19=SCOM2

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Direct Mode (High-Speed)
0	via PPS

Bit 16 – QSPI_HSEN QSPI (Direct) Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

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System Configuration and Locking (CFG)

Value	Description
1	Direct Mode (High-Speed)
0	via PPS

Bit 15 – QSCHE_EN QSPI Address Space Cache Attribute

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Cache attribute enabled
0	Caching disabled

Bit 14 – SMCLR Selects CRU handling of MCLR Control

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’ or ‘10’.

Value	Description
1	Legacy mode (system clear does not reset all state of device)
0	MCLR causes a faux POR

Bit 13 – SLRCTRL2 I2C Delay Select for SERCOM2

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate control configured via SERCOM configuration
0	Slew rate control configured via GPIO configuration

Bit 12 – SLRCTRL1 I2C Delay Select for SERCOM1

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate control configured via SERCOM configuration
0	Slew rate control configured via GPIO configuration

Bit 11 – SLRCTRL0 I2C Delay Select for SERCOM0

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Slew rate control configured via SERCOM configuration
0	Slew rate control configured via GPIO configuration

Bit 10 – CLASSBDIS Disable CLASSB Device Functionality

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	CLASSB functions disabled
0	CLASSB functions enabled

Bit 9 – CMP1_OE Analog Comparator-1 Output Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	AC1 Output enabled
0	AC1 Output disabled

Bit 8 – CMP0_OE Analog Comparator-0 Output Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	AC0 Output enabled
0	AC0 Output disabled

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System Configuration and Locking (CFG)

Bit 7 – ZBTWKSYS ZBT Subsystem External Wake-up source

Notes:

- Write only bit, with read-as zero; when written to ‘1’, creates one clk_lp_cycle wide pulse on ZBT Subsystem.external_NMI0 pin. This enables external system wake-up to Bluetooth subsystem. This allows CPU and Bluetooth subsystem wake-up/sleep to be independent of each other.
- Flash fuse loading is excluded for this bit.

Bit 5 – TRCEN Trace Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Trace features in the CPU are enabled
0	Trace features in the CPU are disabled

Bits 4:3 – ICESEL[1:0] EMUC/EMUD Communication Channel Select

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
11	ICE EMUC1/EMUD1 pins are shared with PGC1/PGD1
10	ICE EMUC2/EMUD2 pins are shared with PGC2/PGD2
01	ICE EMUC3/EMUD3 pins are shared with PGC3/PGD3 (Not used on this device)
00	ICE EMUC4/EMUD4 pins are shared with PGC4/PGD4

Bits 1:0 – DEBUG[1:0] Background Debugger Access Selection

Notes:

1. JTAGEN = 0 prevents 4-wire JTAG Debugging, but not EMUC/EMUD debugging.
2. If CPN = 0, then the JTAG TAP controller denies access to the EJTAG TAP Controller (i.e. the SWTAP command is ignored), and therefore external access to debugging features is denied.
3. This bit is only writable when CFGLOCK[1:0] = ‘00’.

Value	Description
11	4-wire JTAG I/F Enabled - EMUC/EMUD Disabled - ICD Module Disabled
10	4-wire JTAG I/F Enabled - EMUC/EMUD Disabled - ICD Module Enabled
01	EMUC/EMUD Enabled - 4-wire JTAG I/F Disabled - ICD Module Disabled
00	EMUC/EMUD Enabled - 4-wire JTAG I/F Disabled - ICD Module Enabled

PIC32CX-BZ2 and WBZ45 Family

System Configuration and Locking (CFG)

17.4.3 Configuration Control Register 2

Name: CFGCON2(L)
Offset: 0x20
Reset: 0x00
Property: -

This register is loaded with trusted data from FBCFG3 during pre-boot period. Thereafter, it is controlled as described above.

Trusted data from Flash means when there is no BCFG* fail status during Flash configuration word reads. If accompanied by fail status or blank/erase indication then reset values (described in the register description below) are retained and new values from FBCFG3 are not loaded.

Bit	31	30	29	28	27	26	25	24
	DMTEN		DMTCNT[4:0]				WINSZ[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	1	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
	WDTEN	WINDIS	WDTSPGM		WDTPSR[4:0]			
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
	FSCMEN	CKSWEN	WAKE2SPD	SOSCSEL	WDTRMC[1:0]		POSCMD[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
	PMUTEST_VD D_EN		DMTINTV[2:0]			ACMP_CYCLE[2:0]		
Access	R/W/L		R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0		1	1	1	0	0	0

Bit 31 – DMTEN Dead Man Timer Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	DMT enabled
0	DMT disabled (control is placed on the DMTCON.ON bit)

Bits 30:26 – DMTCNT[4:0] Dead Man Timer Count Select bits

Notes:

- This bit is only writable when CFGLOCK[1:0] is ‘00’.
- On devices where the DMTCNT[4:0] configuration field is loaded.

Value	Description
00000	Counter value is 2^8 for cfg_dmt_cnt[31:0]
00001	Counter value is 2^9 for cfg_dmt_cnt[31:0]
...	...
10100	Counter value is 2^{28} for cfg_dmt_cnt[31:0]
10101	Counter value is 2^{29} for cfg_dmt_cnt[31:0]
10110	Counter value is 2^{30} for cfg_dmt_cnt[31:0]
10111	Counter value is 2^{31} for cfg_dmt_cnt[31:0]
11000 – 11111	Reserved

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Bits 25:24 – WINSZ[1:0] Watchdog Timer Window Size bits

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
00	Window size is 75%
01	Window size is 50%
10	Window size is 37.5%
11	Window size is 25%

Bit 23 – WDTEN Watchdog Timer Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	WDT enabled
0	WDT disabled (control is placed on the SWDTEN bit)

Bit 22 – WINDIS Windowed Watchdog Timer Disable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Standard WDT selected; windowed WDT disabled
0	Windowed WDT enabled

Bit 21 – WDTSPGM Watchdog Timer Stop during Flash Programming bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	The WDT stops during NVR programming (legacy)
0	The WDT runs during NVR programming (for read/execute while programming flash systems)

Bits 20:16 – WDTPSR[4:0] Watchdog Timer Post-scale Select Run bits

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
10100	1:1048576
10011	1:524288
10010	1:262144
10001	1:131072
10000	1:65536
01111	1:32768
01110	1:16384
01101	1:8192
01100	1:4096
01011	1:2048
01010	1:1024
01001	1:512
01000	1:256
00111	1:128
00110	1:64
00101	1:32
00100	1:16
00011	1:8
00010	1:4
00001	1:2
00000	1:1

Bit 15 – FSCMEN Fail-Safe Clock Monitor Enable

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

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System Configuration and Locking (CFG)

Value	Description
1	FSCM enabled
0	FSCM disabled

Bit 14 – CKSWEN Software Clock Switching Enable

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Software clock switching enabled
0	Software clock switching disabled

Bit 13 – WAKE2SPD 2-Speed startup enabled in Sleep mode bit

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	When the device EXITS Sleep Mode, the sys_clk will be from FRC until the selected clock is ready.
0	When the device EXITS Sleep Mode, the sys_clk will be from the selected clock.

Bit 12 – SOSCSEL SOSC Selection Configuration bit

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Crystal (SOSCI/SOSCO) mode
0	Digital (SCLKI) mode

Bits 11:10 – WDTRMCS[1:0] WDT RUN Mode Clock Select

Note: This bit is only writable when CFGLOCK[1:0] is '00' or '10'.

Value	Description
11	LPRC
10	Do not use
01	Do not use
00	Module PB Clock

Bits 9:8 – POSCMD[1:0] Primary Oscillator Configuration bits

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
11	Primary oscillator disabled
10	HS oscillator mode selected
01	HS oscillator mode selected
00	HS oscillator mode selected

Bit 7 – PMUTEST_VDD_EN PMU Test Output or VDD/2 Enable via ADC IE12

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	PMU test output monitor enable
0	VDD/2 monitor enable

Bits 5:3 – DMTINTV[2:0] Dead Man Timer Count Window Interval bits

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
000	Window/Interval value is zero for cfg_dmt_intv[31:0] - windowed mode is disabled
001	Window/Interval value is 1/2 Counter value for cfg_dmt_intv[31:0]
010	Window/Interval value is 3/4 Counter value for cfg_dmt_intv[31:0]
011	Window/Interval value is 7/8 Counter value for cfg_dmt_intv[31:0]
100	Window/Interval value is 15/16 Counter value for cfg_dmt_intv[31:0]
101	Window/Interval value is 31/32 Counter value for cfg_dmt_intv[31:0]

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Value	Description
110	Window/Interval value is 63/64 Counter value for cfg_dmt_intv[31:0]
111	Window/Interval value is 127/128 Counter value for cfg_dmt_intv[31:0]

Bits 2:0 – ACMP_CYCLE[2:0] AC SIB Comparator Result Wait Cycles

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
n	Wait for 32us* ACMP_CYCLE+1 cycles to generate comparator done indication

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System Configuration and Locking (CFG)

17.4.4 Configuration Control Register 4

Name: CFGCON4(L)
Offset: 0x40
Reset: 0x840e4000
Property: -

This register is loaded with trusted data from FBCFG4/DEVCFG4 during pre-boot period.

Trusted data from Flash means when there is no BCFG* fail status during Flash configuration word reads. If accompanied by fail status BCFGFAIL (RCON[26]) or blank/erase indication then reset values (described in the following register description) are retained and new values from FBCFG4 are not loaded.

Bit	31	30	29	28	27	26	25	24
	RTCNTM_CSEL	LPOSCEN	UVREGROVR	DSBITEN	DSWDTEN	DSWDTLPRC	DSWDTPS[4:3]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	1	0	0	0	0	1	0	0
Bit	23	22	21	20	19	18	17	16
	DSWDTPS[2:0]		DSZPBOREN	CPEN_DLY[2:0]			RTCEVTYPE	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8
	MLPCLK_MOD	VBKP_DIVSEL	VBKP_32KCSEL[1:0]		VBKP_1KCSEL	RTCEVENT_EN	RTCEVENTSEL[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SOSC_CFG[7:0]							
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0	0	0	0	0	0	0

Bit 31 – RTCNTM_CSEL RTC Counter Mode Clock Select

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Raw 32 KHz clock
0	Processed 32 KHz clock

Bit 30 – LPOSCEN Low Power (Secondary) Oscillator Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Enable Low Power (Secondary) Oscillator, also at reset
0	Disable Low Power (Secondary) Oscillator

Bit 29 – UVREGROVR ULPVREG Retention Mode Override

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	ULPVREG forced in the Retention mode
0	ULPVREG controlled by XDS/DS FSM

Bit 28 – DSBITEN Deep Sleep Bit Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

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Value	Description
1	Enable DS bit in DSCON
0	Disable DS bit in DSCON

Bit 27 – DSWDTEN Deep Sleep Watchdog Timer Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Enable DSWDT during deep sleep
0	Disable DSWDT during deep sleep

Bit 26 – DSWDTLPRC Deep Sleep Watchdog Timer Reference Clock Select bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
1	Select LPRC as DSWDT reference clock
0	Select SOSC as DSWDT reference clock

Bits 25:21 – DSWDTPS[4:0] Deep Sleep Watchdog Timer Postscale Select bits

The DS WDT prescaler is 32; this creates an approximate base time unit of 1 ms.

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

Value	Description
11111	1:2 ³⁶ (25.7 days)
11110	1:2 ³⁵ (12.8 days)
11101	1:2 ³⁴ (6.4 days)
11100	1:2 ³³ (77.0 hours)
11011	1:2 ³² (38.5 hours)
11010	1:2 ³¹ (19.2 hours)
11001	1:2 ³⁰ (9.6 hours)
11000	1:2 ²⁹ (4.8 hours)
10111	1:2 ²⁸ (2.4 hours)
10110	1:2 ²⁷ (72.2 minutes)
10101	1:2 ²⁶ (36.1 minutes)
10100	1:2 ²⁵ (18.0 minutes)
10011	1:2 ²⁴ (9.0 minutes)
10010	1:2 ²³ (4.5 minutes)
10001	1:2 ²² (135.3 s)
10000	1:2 ²¹ (67.7 s)
01111	1:2 ²⁰ (33.825 s)
01110	1:2 ¹⁹ (16.912 s)
01101	1:2 ¹⁸ (8.456 s)
01100	1:2 ¹⁷ (4.228 s)
01011	1:65536 (2.114 s)
01010	1:32768 (1.057 s)
01001	1:16384 (528.5 ms)
01000	1:8192 (264.3 ms)
00111	1:4096 (132.1 ms)
00110	1:2048 (66.1 ms)
00101	1:1024 (33 ms)
00100	1:512 (16.5 ms)
00011	1:256 (8.3 ms)
00010	1:128 (4.1 ms)
00001	1:64 (2.1 ms)
00000	1:32 (1 ms)

Bit 20 – DSZPBOREN Deep Sleep Zero-Power BOR Enable bit

Note: This bit is only writable when CFGLOCK[1:0] is ‘00’.

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Value	Description
1	Enable ZPBOR during deep sleep
0	Disable ZPBOR during deep sleep

Bits 19:17 – CPEN_DLY[2:0] Charge-pump Ready Digital Delay (Safety delay to Analog CP Ready)
 $n = (n+1)$ LPRC Clock Cycle Delay

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Bit 16 – RTCEVTYPE RTC Event Type

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	RTC_EVENT
0	RTC_OUT

Bit 15 – MLPCLK_MOD LPCLK Modifier in Counter/Delay Mode

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Divide-by 1.024 (Recommended when LPCLK = 32.768 KHz)
0	Divide-by 1 (Recommended when LPCLK = 32 KHz)

Bit 14 – VBKP_DIVSEL VDDBUKPCORE LPCLK Clock Divider Selection

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Divide by 31.25 (Recommended when LPCLK = 32 KHz)
0	Divide-by 32 (Recommended when LPCLK = 32.768 KHz)

Bits 13:12 – VBKP_32KCSEL[1:0] VDDBUKPCORE 32 KHz Clock Source Selection

Notes:

- When '00' or '01'; the DS mode entry, falls back to '11'. Any change of clock source will result in gaps in LPCLK output.
- This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
11	LPRC
10	SOSC
01	POSC
00	FRC

Bit 11 – VBKP_1KCSEL VDDBUKPCORE LPCLK Clock Selection

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Divide by 32 or 31.25 clock depending on VBKP_DIVSEL
0	32 KHz low power clock

Bit 10 – RTCEVENT_EN Output Enable for RTC Event Output

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
1	Enables RTC-Event output
0	Disables RTC-Event output

Bits 9:8 – RTCEVENTSEL[1:0] RTC Event Selection

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Value	Description
00	1-Second clock

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Value	Description
01	Alarm pulse
1x	32 KHz clock

Bits 7:0 – SOSC_CFG[7:0] SOSC Configuration Bits

Note: This bit is only writable when CFGLOCK[1:0] is '00'.

Preliminary

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17.4.5 Permission Group Configuration

Name: CFGPGQOS
Offset: 0x50
Reset: 0xe040004c
Property: -

All bits in this register are writable only when CFGCON0.PGLOCK = '0'.

There is no Flash location for this register because the purpose of this register to provide SW based protection mechanism to device memory mapped region which is typically handled by trusted boot/OScode.

Note: Ensure this register is programmed to the values shown: 0xE040_004C if you are not using Microchip provided boot code.

Bit	31	30	29	28	27	26	25	24
	WISIBQOS[1:0]		FCQOS[1:0]				DSUPG[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L			R/W/L	R/W/L
Reset	1	1	1	0			0	0
Bit	23	22	21	20	19	18	17	16
	ICMQOS[1:0]		ICMPG[1:0]		ADCQOS[1:0]		ADCPG[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
							DMAPG[1:0]	
Access							R/W/L	R/W/L
Reset							0	0
Bit	7	6	5	4	3	2	1	0
	ICDJQOS[1:0]		ICDJPG[1:0]		CPUQOS[1:0]		CPUPG[1:0]	
Access	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	1	0	0	1	1	0	0

Bits 31:30 – WISIBQOS[1:0] Wireless SIB QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 29:28 – FCQOS[1:0] FC Controller QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 25:24 – DSUPG[1:0] DSU Permission Group, drive directly the inputs cfg_dsu_pg[1:0] to the SSX

The DSU bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- DSUPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- DSUPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)

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- DSUPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- DSUPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Bits 23:22 – ICMQOS[1:0] ICM QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 21:20 – ICMPG[1:0] ICM Permission Group, drive directly the inputs cfg_icm_pg[1:0] to the SSX

The ICM bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- ICMPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- ICMPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)
- ICMPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- ICMPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Note: This field is only writable when CFGCON0.PGLOCK = 0

Bits 19:18 – ADCQOS[1:0] ADC Controller QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 17:16 – ADCPG[1:0] ADC Controller Permission Group, drive directly the inputs cfg_adc_pg[1:0] to the SSX

The ADC bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- ADCPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- ADCPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)
- ADCPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- ADCPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Bits 9:8 – DMAPG[1:0] DMA (Rd/Wr) Permission Group, drive directly the inputs cfg_dma_pg[1:0] to the SSX

The DMA bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- DMAPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- DMAPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)
- DMAPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- DMAPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Note: This field is only writable when CFGCON0.PGLOCK = 0

Bits 7:6 – ICDJQOS[1:0] ICD-JTAG Bus QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

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Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 5:4 – ICDJPG[1:0] ICD-JTAG Permission Group, drive directly the inputs cfg_icdj_pg[1:0] to the SSX
The ICD-JTAG bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- ICDJPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- ICDJPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)
- ICDJPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- ICDJPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Bits 3:2 – CPUQOS[1:0] CPU I/D and System Bus QOS Control bits

Note: This field is only writable when CFGCON0.PGLOCK = '0'.

Value	Description
00	Disable; Background
01	Low; Sensitive bandwidth
10	Medium; Sensitive latency
11	High; Critical latency

Bits 1:0 – CPUPG[1:0] CPU (Code) Permission Group, drive directly the inputs cfg_cpu_pg[1:0] to the SSX
The CPU Bus master has access to Access Controlled memory regions as defined by the bit-fields RDPER[3:0] and WRPER[3:0] in the Bus Structure's Permission Groups SFRs for these memory regions. The encoding works as follows:

- CPUPG[1:0] == 2'b11 : Read Access if RDPER[3]==1, Write Access if WRPER[3]==1 (Perm. Grp. 3)
- CPUPG[1:0] == 2'b10 : Read Access if RDPER[2]==1, Write Access if WRPER[2]==1 (Perm. Grp. 2)
- CPUPG[1:0] == 2'b01 : Read Access if RDPER[1]==1, Write Access if WRPER[1]==1 (Perm. Grp. 1)
- CPUPG[1:0] == 2'b00 : Read Access if RDPER[0]==1, Write Access if WRPER[0]==1 (Perm. Grp. 0)

Notes:

- CPUPG[1:0] automatically reverts to 2'b00 when the CPU acknowledges entering into an NMI exception as indicated by its STAUS[NMI] bit, which is carried by the cpu1_si_nmitaken system signal.
- This field is only writable when CFGCON0.PGLOCK = '0'.

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17.4.6 Peripheral Clock Generator 1

Name: CFGPCLKGEN1
Offset: 0x60
Reset: 0x00
Property: -

The CFGPCLKGEN1 dictates the peripheral clock selection described in *Clock System* chapter.

There is no Flash location for this register because the purpose of this register to provide application based peripheral clocking selection. This is best handled in the application SW drivers.

Bit	31	30	29	28	27	26	25	24
	CM4TD	CM4TCSEL[2:0]			TC23CD	TC23CSEL[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	TCC12CD	TCC12CSEL[2:0]			S23D	SERCOM23CSEL[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	S01D	SERCOM01CSEL[2:0]			MCD	FREQMMCSEL[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RCD	FREQMRCSEL[2:0]			EICCD	EICCSEL[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – CM4TD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 30:28 – CM4TCSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REFO1-6 clock selected
7	Low power clock selected

Bit 27 – TC23CD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 26:24 – TC23CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected

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Value	Description
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 23 – TCC12CD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 22:20 – TCC12CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 19 – S23D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 18:16 – SERCOM23CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 15 – S01D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 14:12 – SERCOM01CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 11 – MCD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 10:8 – FREQMMCSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

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Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 7 – RCD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 6:4 – FREQMRCSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 3 – EICCD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 2:0 – EICCSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

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17.4.7 Peripheral Clock Generator 2

Name: CFGPCLKGEN2
Offset: 0x70
Reset: 0x00
Property: -

The CFGPCLKGEN2 dictates the peripheral clock selection described in *Clock System* chapter.

There is no Flash location for this register because the purpose of this register to provide application based peripheral clocking selection. This is best handled in the application SW drivers.

Bit	31	30	29	28	27	26	25	24
C8D EVSYSC8SEL[2:0] C7D EVSYSC7SEL[2:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
C6D EVSYSC6SEL[2:0] C5D EVSYSC5SEL[2:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
C4D EVSYSC4SEL[2:0] C3D EVSYSC3SEL[2:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
C2D EVSYSC2SEL[2:0] C1D EVSYSC1SEL[2:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 31 – C8D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 30:28 – EVSYSC8SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 27 – C7D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 26:24 – EVSYSC7SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected

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Value	Description
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 23 – C6D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 22:20 – EVSYSC6SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 19 – C5D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 18:16 – EVSYSC5SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 15 – C4D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 14:12 – EVSYSC4SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 11 – C3D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 10:8 – EVSYSC3SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

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Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 7 – C2D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 6:4 – EVSYSC2SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 3 – C1D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 2:0 – EVSYSC1SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

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System Configuration and Locking (CFG)

17.4.8 Peripheral Clock Generator 3

Name: CFGPCLKGEN3
Offset: 0x80
Reset: 0x00
Property: -

The CFGPCLKGEN3 dictates the peripheral clock selection described in *Clock System* chapter.

There is no Flash location for this register because the purpose of this register to provide application based peripheral clocking selection. This is best handled in the application SW drivers.

Bit	31	30	29	28	27	26	25	24
	TC1CD	TC1CSEL[2:0]				TC0CD	TC0CSEL[2:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	TCC0CD	TCC0CSEL[2:0]				ACCD	ACCLKSEL[2:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	C12D	EVSYSC12SEL[2:0]				C11D	EVSYSC11SEL[2:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	C10D	EVSYSC10SEL[2:0]				C9D	EVSYSC9SEL[2:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – TC1CD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 30:28 – TC1CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REFO1-6 clock selected
7	Low power clock selected

Bit 27 – TC0CD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 26:24 – TC0CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected

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Value	Description
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 23 – TCC0CD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 22:20 – TCC0CSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 19 – ACCD Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 18:16 – ACCLKSEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 15 – C12D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 14:12 – EVSYSC12SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1–6	REF01-6 clock selected
7	Low power clock selected

Bit 11 – C11D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 10:8 – EVSYSC11SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

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Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 7 – C10D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 6:4 – EVSYSC10SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

Bit 3 – C9D Peripheral Clock Disable

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	Clock disabled
1	Clock enabled

Bits 2:0 – EVSYSC9SEL[2:0] Peripheral Clock Selection

Note: This field is only writable when CFGLOCK[1:0] = '00'.

Value	Description
0	No clock selected
1 – 6	REF01-6 clock selected
7	Low power clock selected

PIC32CX-BZ2 and WBZ45 Family System Configuration and Locking (CFG)

17.4.9 User Unique ID

Name: USER_ID
Offset: 0xA0
Reset: 0x00
Property: -

The User ID is a 16-bit ID that may be programmed to differentiate products that use the same device. The User ID value may be read directly out of the USER_ID register or through the JTAG interface via the MCHP_CMD.USER_ID command.

There is no dedicated JTAG status bit to indicate when the User ID value is loaded into the USER_ID register, and is ready to be read from JTAG. It is assumed that a non-zero value for the User ID will be used to indicate that the User ID is loaded.

The USER_ID register is reset on power-up then is loaded with trusted data from FBCFG5 during pre-boot period and it is controlled.

Trusted data from Flash means when there is no BCFG* fail status during Flash configuration word reads. If accompanied by fail status or blank/erase indication then reset values (described in the register description below) are retained and new values from FBCFG5 are not loaded.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/W/L							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W/L							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – USER_ID[15:0] User unique ID, readable using the JTAG USER_ID instruction

Note: This field is only writable when CFGLOCK[1:0] = '00'.

17.4.10 Boot Configuration 0

Name: BCFG0
Offset: 0x200
Reset: 0x00
Property: -

Note: Safe value of BCFG0 is 0xFFFF_FFFF as applicable only to the implemented bits.

Bit	31	30	29	28	27	26	25	24
	BINFOVALID0		SIGN	CP				
Access	R		R	R				
Reset	c		c	c				
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
							PCSCMODE	
Access							R	
Reset							c	

Bit 31 – BINFOVALID0 First 256-bit BCFG information is valid

Notes:

1. This bit is added to provide a mechanism to know if information coming from Flash is valid or invalid. The BCFG area is critical to device boot up.
2. Trusted FBCFG* data = (BINFOVALID=0) and (BCFGFAIL=0).
3. It is recommended for application to program this bit to zero for proper operation.

Value	Description
1	FBCFG0 to FBCFG5 is not valid (Untrusted, flash values are ignored and safe values are used)
0	FBCFG0 to FBCFG5 is valid (Trusted and loaded from Flash)

Bit 29 – SIGN Flash SIGN bit

Value	Description
1	Unsigned
0	Signed

Bit 28 – CP Boot Code Protect (~FCPN0.CPN && ~FSIGN0.SIGN).

Value	Description
1	Protection enabled
0	Protection disabled

Bit 1 – PCSCMODE PCHE Single cache mode

Value	Description
1	PCHE ICache Only. CPU Instructions (code, data) go to PCHE ICache only.
0	PCHE ICache and DCache. CPU opcodes go to PCEHE ICache port and data goes to PCHE DCache port.

18. Register Locking

This device provides several different types of register level locking:

Locking using the System Lock Register - This mechanism, described in System Lock Register (see *System Lock Register* from Related Links), provides for a 2-way (locking and unlocking) write lock of system critical registers. It includes protection for the following registers:

- CRU.OSCCON
- CRU.OSCTRM
- CRU.SPLLCON
- CRU.RSWRST
- CRU.RNMICON
- CRU.PB1DIV
- CRU.PB2DIV
- CRU.PB3DIV
- CRU.SLEWCON
- CRU.CLK_DIAG

Locking using the CFGCON0.IOLOCK, CFGCON0.PMDLOCK, CFGCON0.PMULOCK, and

CFGCON0.PGLOCK register bits - This mechanism provides for a 1-way lock (once locked, only a reset can unlock) of the following registers:

- All PPS registers (IOLOCK bit)
- All PMD registers (PMDLOCK bit)
- CFGPG register (PGLOCK bit)
- All PMU registers (PMULOCK bit)

Locking using the CFGCON0.CFGLOCK[1:0] register bits - This mechanism provides for a 1-way or 2-way lock (software selectable). It applies to the following registers and memories:

- BCFG0
- CFGCON0
- CFGCON1
- CFGCON2
- CFGCON3
- USER_ID
- CFGCON4
- CFGPCLKGENx

Related Links

[18.1. System Lock Register](#)

18.1 System Lock Register

Several modules contain registers that are protected from errant code causing unwanted changes by the system lock feature. When the system lock is in effect, which is the default state, registers protected by it are not writable. The system lock feature protects registers that are system critical such as boot time option.

Each module that uses the system lock feature describes which register bits and functions it affects. A specific sequence of writes to the SYSKEY register unlock the access to those register bits and features.

18.1.1 Unlock Requirements

The unlock sequence must be atomic. If any other peripheral bus access occurs on the same peripheral bus on which SYSKEY resides during the unlock attempt sequence, the unlock fails. Therefore, turn off all bus initiators like DMA, USB, etc; and disable interrupts.

18.1.2 Unlock Sequence

It is recommended that application code performs steps 2 and 3 before steps 5 and 6. The unlock sequencer, however, only looks for steps 5 and 6 to be atomic. For this sequence, atomic means that there is no other activity on the peripheral bus between steps 5 and 6. Step 4 is only needed to ensure that the sequence starts from a known locked state.

1. Suspend all other Peripheral Bus accesses.
2. Load 0xAA996655 to CPU register X.
3. Load 0x556699AA to CPU register Y.
4. Store CPU register r0 to SYSKEY.
5. Store CPU register X to SYSKEY.
6. Store CPU register Y to SYSKEY.

18.1.3 Lock Sequence

When the system is unlocked, any write to the SYSKEY register causes system lock to become active.

18.1.4 Lock/Unlock Indication

The SYSKEY register read value indicates the status of the unlock sequence. A value of 0x00000000 indicates the system is still locked. A value of 0x00000001 indicates the sequence succeeded and the system is unlocked.

Related Links

- [7. Product Memory Mapping Overview](#)
- [18.3.1. SYSKEY](#)

18.2 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0xAF	Reserved									
0xB0	SYSKEY	7:0	SYSKEY7	SYSKEY6	SYSKEY5	SYSKEY4	SYSKEY3	SYSKEY2	SYSKEY1	SYSKEY0
		15:8	SYSKEY15	SYSKEY14	SYSKEY13	SYSKEY12	SYSKEY11	SYSKEY10	SYSKEY9	SYSKEY8
		23:16	SYSKEY23	SYSKEY22	SYSKEY21	SYSKEY20	SYSKEY19	SYSKEY18	SYSKEY17	SYSKEY16
		31:24	SYSKEY31	SYSKEY30	SYSKEY29	SYSKEY28	SYSKEY27	SYSKEY26	SYSKEY25	SYSKEY24

18.3 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

PIC32CX-BZ2 and WBZ45 Family

Register Locking

18.3.1 System Key Register

Name: SYSKEY
Offset: 0xB0
Reset: 0x0

Bit	31	30	29	28	27	26	25	24
	SYSKEY31	SYSKEY30	SYSKEY29	SYSKEY28	SYSKEY27	SYSKEY26	SYSKEY25	SYSKEY24
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	SYSKEY23	SYSKEY22	SYSKEY21	SYSKEY20	SYSKEY19	SYSKEY18	SYSKEY17	SYSKEY16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	SYSKEY15	SYSKEY14	SYSKEY13	SYSKEY12	SYSKEY11	SYSKEY10	SYSKEY9	SYSKEY8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SYSKEY7	SYSKEY6	SYSKEY5	SYSKEY4	SYSKEY3	SYSKEY2	SYSKEY1	SYSKEY0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

**Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 –
SYSKEY System Key**

Keys are written to this register as part of a sequence to unlock system critical registers. A successful key write to this register will set the system signal.

19. Peripheral Module Disable Register (PMD)

This section describes the following peripheral module disable functions:

- Device Peripheral Configuration
- Configuration defined by product variants
- Peripheral disable for power conservation

19.1 Enabling Peripherals

Peripheral Module Disable (PMD) register bits control the operation of individual peripherals on the device. When a peripheral's associated PMD bit is zero (0), the peripheral is enabled and operates as programmed. However, when the associated PMD bit is one (1), the peripheral logic, memory map and SFR bits are completely removed from visibility and the peripheral is held in reset. This disabled state provides for the lowest power state of the peripheral.

Before a peripheral may be configured or used, it must be enabled by clearing the corresponding PMD register bit.

There are some caveats to using PMD bits. The following should be observed:

1. Disabling a peripheral while its ON bit is zero (0) results in undefined behavior of the external interface.
2. For bus initiators, software must verify the module is not busy after setting the ON bit to zero (0) before disabling it.
3. Setting the PMD bit when there is a pending interrupt results in undefined behavior. Therefore, all Interrupt Flags must be cleared prior to setting the associated PMD.

Finally, setting the PMD bit when there is a pending interrupt results in undefined behavior. Therefore, all Interrupt Flags must be cleared prior to setting the associated PMD.

19.2 Registers and Bits

Note: PMD registers may be write-locked using the CFGCON0.PMDLOCK register bit. If this bit is set, then writing of PMD registers have no effects.

See *PMD1*, *PMD2*, and *PMD3* in the *PMD Register Summary* from Related Links for a description of the PMD registers and to identify the location of the register, see *Device Configuration Map* in the *Product Memory Mapping Overview* from Related Links

Related Links

7. Product Memory Mapping Overview
- 19.3.1. PMD Register Summary

19.3 PMD Register

PIC32CX-BZ2 and WBZ45 Family

Peripheral Module Disable Register (PMD)

19.3.1 PMD Register Summary

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0xBF	Reserved									
0xC0	PMD1	7:0	ADCMD	ACMD		PLVDM	LPAMD	MPAMD	BTMD	ZBMD
		15:8								ADCSARMD
		23:16								RTCCMD
		31:24			SQIMD					

19.3.2 Register Description

Some peripherals include module enable bits internally. The PMD bit is used for clock gating of the PBx_CLK and GCLK for all peripherals. If the peripheral also includes the internal enable bit, the PMD bit and internal enable configuration bit must be configured by software for that peripheral.

The following table summarizes each peripherals enable and disable controls. For more details on the internal enable/disable control, see *Peripheral Access Controller (PAC)* from Related Links.

Table 19-1. Module Enable/Disable Controls

Module	PMD control	Module control	Enable/Disable Strategy
AC	Present	Present	Disable at PMD or Module
AES	Present	Present	Disable at PMD or Module
CCL	NA	Present	Disable at Module
CMCC	NA	Present	Disable at Module
DMAC	NA	Present	Disable at Module
DSU	NA	NA	Always Enabled (Dynamic On/Off)
EIC	NA	Present	Disable at Module
EVSYS	NA	NA	Always Enabled (Dynamic On/Off)
FREQM	NA	Present	Disable at Module
ICM	Present	Present	Enable both/Disable at PMD or Module
PAC	NA	NA	Always Enabled (Dynamic On/Off)
PUKCC	Present	NA	Disable at PMD
QSPI	Present	Present	Enable both/Disable at PMD or Module
RAMECC	NA	NA	Disable using fuse bit
RTCC	Present	Present	Enable both/Disable at PMD or Module
SERCOM	Present	Present	Enable both/Disable at PMD or Module
TC	Present	Present	Enable both/Disable at PMD or Module
TCC	Present	Present	Enable both/Disable at PMD or Module
TRNG	Present	Present	Enable both/Disable at PMD or Module

Note: For Modules with both PMD control and Module control, Enable = PMDx=0 AND Module Enable=1, Disable =PMIx=1 OR Module Enable=0.

PIC32CX-BZ2 and WBZ45 Family

Peripheral Module Disable Register (PMD)

Related Links

- 25. Peripheral Access Controller (PAC)

Preliminary

PIC32CX-BZ2 and WBZ45 Family

Peripheral Module Disable Register (PMD)

19.3.3 PMD1 - Peripheral Module Disable 1 Register

Name: PMD1
Offset: 0x00C0
Reset: 0x00000000
Property: -

Note: This bit is only writable when CFGCON0.PMDLOCK = 0.

Bit	31	30	29	28	27	26	25	24
Access			SQIMD					
Reset			R/W/L					
Bit	23	22	21	20	19	18	17	16
Access							RTCCMD	
Reset							R/W/L	0
Bit	15	14	13	12	11	10	9	8
Access							ADCSARMD	
Reset							R/W/L	0
Bit	7	6	5	4	3	2	1	0
Access	ADCMD	ACMD		PLVDMD	LPAMD	MPAMD	BTMD	ZBMD
Reset	R/W/L	R/W/L		R/W/L	R/W/L	R/W/L	R/W/L	R/W/L
Reset	0	0		0	0	0	0	0

Bit 29 – SQIMD SQI Module Disable

Value	Description
1	Disabled
0	Enabled

Bit 16 – RTCCMD RTCC Module Disable (Unused at top level, part of XDS controller SFR)

Value	Description
1	Disabled
0	Enabled

Bit 8 – ADCSARMD SharedADC SAR Core Module Disable bit

Value	Description
1	Disabled, When disabled, the corresponding ADC SAR SHARED will be disabled.
0	Enabled

Bit 7 – ADCMD ADC Controller Module Disable

Value	Description
1	Disabled
0	Enabled

Bit 6 – ACMD AC Module Disable

Value	Description
1	Disabled
0	Enabled

Bit 4 – PLVDMD PLVD Module Disable bit

Value	Description
1	Disabled, When disabled, the corresponding PLVD will be disabled.

PIC32CX-BZ2 and WBZ45 Family Peripheral Module Disable Register (PMD)

Bit 3 – LPAMD RF LPA Module Disable bit

Value	Description
1	Disabled
0	Enabled

Bit 2 – MPAMD RF MPA Module Disable bit

Value	Description
1	Disabled
0	Enabled

Bit 1 – BTMD Bluetooth Module Disable bit

Value	Description
1	Disabled
0	Enabled

Bit 0 – ZBMD ZigBee Module Disable bit

Value	Description
1	Disabled
0	Enabled

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Related Links

[5.1.9. CLR, SET, and INV Registers](#)

19.4

PMDx Initialization Values by Variant Name

Table 19-2. PMDx Initialization Values

PartName	31				24	23				16	15					8	7					0	Hex
PMD1																							
PIC32CX1 012BZ250 48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000 0_0 000 1	
PIC32CX1 012BZ240 32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000 0_0 000 1	
PartName	31				24	23				16	15					8	7					0	Hex
PMD2																							
PIC32CX1 012BZ250 48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000 0_0 000 1	
PIC32CX1 012BZ240 32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000 0_0 000 1	

PIC32CX-BZ2 and WBZ45 Family Peripheral Module Disable Register (PMD)

PartName	31	PMD3																7	0	Hex	
		24	23	16	5																
						TCC2MD	TCC1MD	TCC0MD	TC3MD	TC2MD	TC1MD	TC0MD	AESMD	RNGMD	PUKCCMD	ICMMD	SER3MD	SER2MD	SER1MD	SER0MD	
PIC32CX1 012BZ250 48	0	0	0	0	0	0	0	0	0	0	0	0	0 ¹	000 0_0 000 1							
PIC32CX1 012BZ240 32	0	0	0	0	0	0	0	0	0	0	0	0	0 ¹	0 ¹	0 ¹	0 ¹	1 ¹	1 ¹	0 ¹	0 ¹	000 0_0 00C 1

Notes:

1. Value depends on the specific Device Variant, as specified in Configuration Summary, see *Configuration Summary* from Related Links.
2. 32 and 48 pin package differences that varies module sub-parameters like ADC channels are not visible in this table.

20. RTC – Real-Time Counter

20.1 Overview

The Real-Time Counter (RTC) is a 32-bit counter with a 10-bit programmable prescaler that typically runs continuously to keep track of time. The RTC can wake up the device from sleep modes using the alarm/compare wake up, periodic wake up, or overflow wake up mechanisms, or from the wake inputs.

The RTC can generate periodic peripheral events from outputs of the prescaler, as well as alarm/compare interrupts and peripheral events, which can trigger at any counter value. Additionally, the timer can trigger an overflow interrupt and peripheral event, and can be reset on the occurrence of an alarm/compare match. This allows periodic interrupts and peripheral events at very long and accurate intervals.

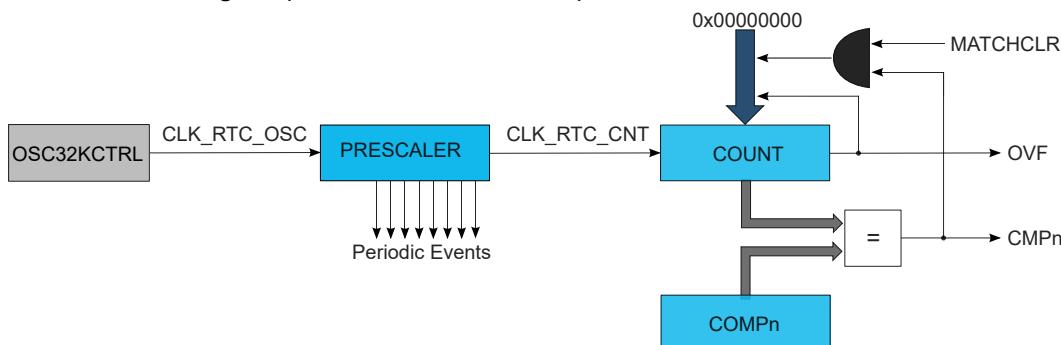
The 10-bit programmable prescaler can scale down the clock source. By this, a wide range of resolutions and time-out periods can be configured. With a 32.768 kHz clock source, the minimum counter tick interval is 30.5 μ s, and time-out periods can range up to 36 hours. For a counter tick interval of 1s, the maximum time-out period is more than 136 years.

20.2 Features

- 32-bit counter with 10-bit prescaler
- Multiple clock sources
- 32-bit or 16-bit counter mode
- Two 32-bit or four 16-bit compare values
- Clock/Calendar mode
 - Time in seconds, minutes, and hours (12/24)
 - Date in day of month, month, and year
 - Leap year correction
- Digital prescaler correction/tuning for increased accuracy
- Overflow, alarm/compare match and prescaler interrupts and events
 - Optional clear on alarm/compare match
- 4 general purpose registers
- 1 backup register with retention capability
- Tamper Detection
 - Timestamp on event or up to 4 inputs with debouncing
 - Active layer protection

20.3 Block Diagram

Figure 20-1. RTC Block Diagram (Mode 0 — 32-Bit Counter)



PIC32CX-BZ2 and WBZ45 Family

RTC – Real-Time Counter

Figure 20-2. RTC Block Diagram (Mode 1 — 16-Bit Counter)

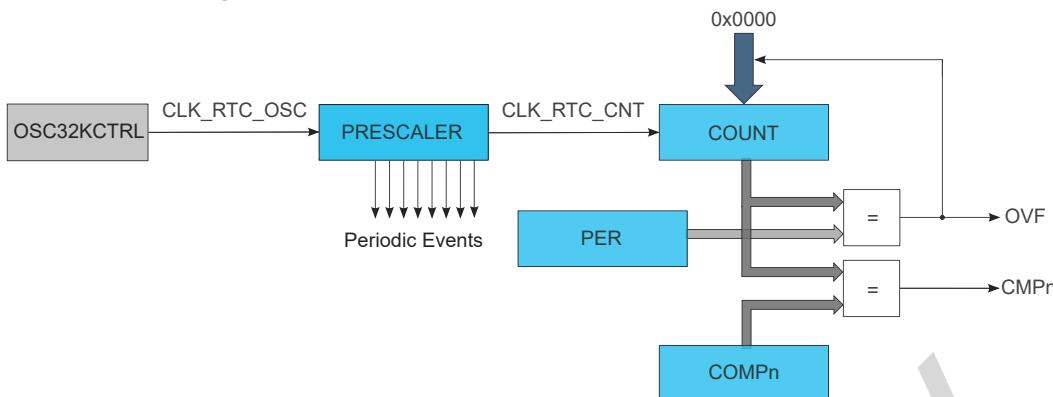


Figure 20-3. RTC Block Diagram (Mode 2 — Clock/Calendar)

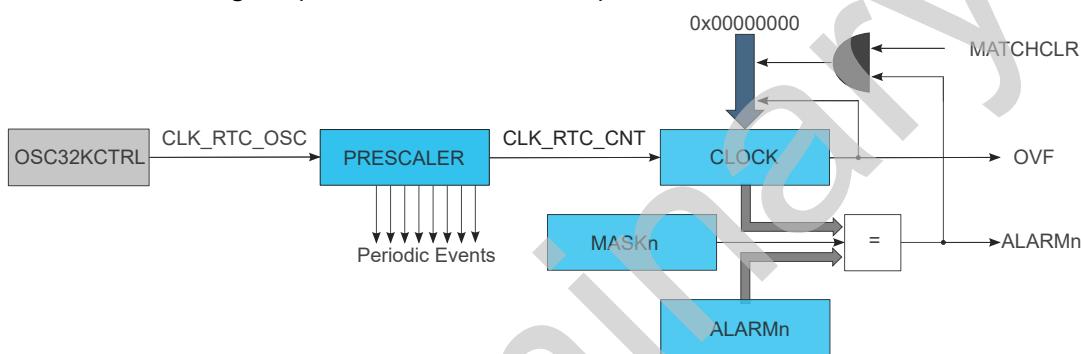
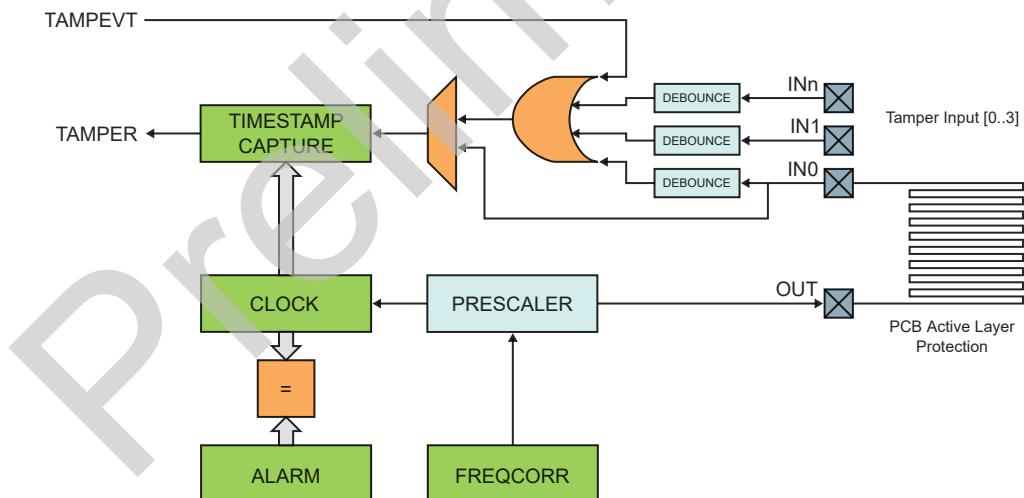


Figure 20-4. RTC Block Diagram (Tamper Detection)



20.4 Signal Description

Table 20-1. Signal Description

Signal	Description	Type
INn [n=0..3]	Tamper Detection Input	Digital input
OUTn [n=0]	Tamper Detection Output	Digital output

.....continued

Signal	Description	Type
RTC_EVENT	RTC Event Output	Digital output

20.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

20.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the RTC must be enabled and no higher priority peripherals for the RTC pins can be enabled. See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.

Related Links

[5. I/O Ports and Peripheral Pin Select \(PPS\)](#)

20.5.2 Power Management

The RTC will continue to operate in any sleep modes where the selected source clock is running. The RTC interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes. See *Power Management Unit (PMU)* from Related Links for details on the different sleep modes.

The RTC can only be reset by a power on reset (POR) or by setting the Software Reset bit in the Control A register (CTRLA.SWRST=1).

Related Links

[14. Power Management Unit \(PMU\)](#)

20.5.3 Clocks

A 32 KHz or 1 KHz oscillator clock (CLK_RTC_OSC) is required to clock the RTC. The 32 KHz clock source can be FRC, POSC, SOSC or LPRC based on the mux selection controlled by the CFG.CFGCON4.VBKP_32KCSEL bit. The 1 KHz clock source is based on the mux selection controlled by the CFG.CFGCON4.VBKP_1KCSEL bit.

This oscillator clock is asynchronous to the bus clock (CLK_RTC_APB). Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains.

20.5.4 DMA

The DMA request lines (or line if only one request) are connected to the DMA Controller (DMAC). Using the RTC DMA requests requires the DMA Controller to be configured first.

20.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the RTC interrupt requires the Interrupt Controller to be configured first.

20.5.6 Events

The events are connected to the *Event System*. For more information refer to the Related Links.

20.5.7 Debug Operation

When the CPU is halted in debug mode the RTC will halt normal operation. The RTC can be forced to continue operation during debugging. See *DBGCTRL* from Related Links.

Related Links

[20.8.7. DBGCTRL](#)

20.6 Functional Description

20.6.1 Principle of Operation

The RTC keeps track of time in the system and enables periodic events, as well as interrupts and events at a specified time. The RTC consists of a 10-bit prescaler that feeds a 32-bit counter. The actual format of the 32-bit counter depends on the RTC operating mode.

The RTC can function in one of these modes:

- Mode 0 - COUNT32: RTC serves as 32-bit counter
- Mode 1 - COUNT16: RTC serves as 16-bit counter
- Mode 2 - CLOCK: RTC serves as clock/calendar with alarm functionality

20.6.2 Basic Operation

20.6.2.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the RTC is disabled (CTRLA.ENABLE=0):

- Operating Mode bits in the Control A register (CTRLA.MODE)
- Prescaler bits in the Control A register (CTRLA.PRESCALER)
- Clear on Match bit in the Control A register (CTRLA.MATCHCLR)
- Clock Representation bit in the Control A register (CTRLA.CLKREP)

The following registers are enable-protected:

- Event Control register (EVCTRL)
- Tamper Control register (TAMPCTRL)

Enable-protected bits and registers can be changed only when the RTC is disabled (CTRLA.ENABLE=0). If the RTC is enabled (CTRLA.ENABLE=1), these operations are necessary: first write CTRLA.ENABLE=0 and check whether the write synchronization has finished, then change the desired bit field value. Enable-protected bits in CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

The RTC prescaler divides the source clock for the RTC counter.

Note: In Clock/Calendar mode, the prescaler must be configured to provide a 1 Hz clock to the counter for correct operation.

The frequency of the RTC clock (CLK_RTC_CNT) is given by the following formula:

$$f_{\text{CLK_RTC_CNT}} = \frac{f_{\text{CLK_RTC_OSC}}}{2^{\text{PRESCALER}}}$$

The frequency of the oscillator clock, CLK_RTC_OSC, is given by $f_{\text{CLK_RTC_OSC}}$, and $f_{\text{CLK_RTC_CNT}}$ is the frequency of the internal prescaled RTC clock, CLK_RTC_CNT.

20.6.2.2 Enabling, Disabling, and Resetting

The RTC is enabled by setting the Enable bit in the Control A register (CTRLA.ENABLE=1). The RTC is disabled by writing CTRLA.ENABLE=0.

The RTC is reset by setting the Software Reset bit in the Control A register (CTRLA.SWRST=1). All registers in the RTC, except DEBUG, will be reset to their initial state, and the RTC will be disabled. The RTC must be disabled before resetting it.

20.6.2.3 32-Bit Counter (Mode 0)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x0, the counter operates in 32-bit Counter mode. See *RTC Block Diagram (Mode 0 — 32-Bit Counter)* figure in the *Block Diagram* from Related Links. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT.

The counter will increment until it reaches the top value of 0xFFFFFFFF, and then wrap to 0x00000000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 32-bit format.

The counter value is continuously compared with the 32-bit Compare registers (COMPn, n=0–1). When a compare match occurs, the Compare n Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next 0-to-1 transition of CLK_RTC_CNT.

If the Clear on Match bit in the Control A register (CTRLA.MATCHCLR) is '1', the counter is cleared on the next counter cycle when a compare match with COMPn occurs. This allows the RTC to generate periodic interrupts or events with longer periods than the prescaler events. Note that when CTRLA.MATCHCLR is '1', INTFLAG.CMPn and INTFLAG.OVF will both be set simultaneously on a compare match with COMPn.

Related Links

[20.3. Block Diagram](#)

20.6.2.4 16-Bit Counter (Mode 1)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x1, the counter operates in 16-bit Counter mode. See *RTC Block Diagram (Mode 1 — 16-Bit Counter)* figure in the *Block Diagram* from Related Links. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. In 16-bit Counter mode, the 16-bit Period register (PER) holds the maximum value of the counter. The counter will increment until it reaches the PER value, and then wrap to 0x0000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 16-bit format.

The counter value is continuously compared with the 16-bit Compare registers (COMPn, n=0..). When a compare match occurs, the Compare n Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn, n=0..) is set on the next 0-to-1 transition of CLK_RTC_CNT.

Related Links

[20.3. Block Diagram](#)

20.6.2.5 Clock/Calendar (Mode 2)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x2, the counter operates in Clock/Calendar mode. See *RTC Block Diagram (Mode 2 — Clock/Calendar)* figure in the *Block Diagram* from Related Links. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The selected clock source and RTC prescaler must be configured to provide a 1Hz clock to the counter for correct operation in this mode.

The time and date can be read from or written to the Clock Value register (CLOCK) in a 32-bit time/date format. Time is represented as:

- Seconds
- Minutes
- Hours

Hours can be represented in either 12- or 24-hour format, selected by the Clock Representation bit in the Control A register (CTRLA.CLKREP). This bit can be changed only while the RTC is disabled.

The date is represented in this form:

- Day as the numeric day of the month (starting at 1)
- Month as the numeric month of the year (1 = January, 2 = February, etc.)
- Year as a value from 0x00 to 0x3F. This value must be added to a user-defined reference year. The reference year must be a leap year (2016, 2020 etc). Example: the year value 0x2D, added to a reference year 2016, represents the year 2061.

The RTC will increment until it reaches the top value of 23:59:59 December 31 of year value 0x3F, and then wrap to 00:00:00 January 1 of year value 0x00. This will set the Overflow Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.OVF).

The clock value is continuously compared with the 32-bit Alarm registers (ALARM n , $n=0..1$). When an alarm match occurs, the Alarm n Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.ALARM n , $n=0..1$) is set on the next 0-to-1 transition of CLK_RTC_CNT. E.g. For a 1Hz clock counter, it means the Alarm 0 Interrupt flag is set with a delay of 1s after the occurrence of alarm match.

A valid alarm match depends on the setting of the Alarm Mask Selection bits in the Alarm n Mask register (MASK n .SEL). These bits determine which time/date fields of the clock and alarm values are valid for comparison and which are ignored.

If the Clear on Match bit in the Control A register (CTRLA.MATCHCLR) is set, the counter is cleared on the next counter cycle when an alarm match with ALARM n occurs. This allows the RTC to generate periodic interrupts or events with longer periods than it would be possible with the prescaler events only (see *Periodic Intervals* from Related Links).

Note: When CTRLA.MATCHCLR is 1, INTFLAG.ALARM0 and INTFLAG.OVF will both be set simultaneously on an alarm match with ALARM n .

Related Links

[20.3. Block Diagram](#)

[20.6.8.1. Periodic Intervals](#)

20.6.3 DMA Operation

The RTC generates the following DMA request:

- Tamper (TAMPER): The request is set on capture of the timestamp. The request is cleared when the Timestamp register is read.

If the CPU accesses the registers which are source for DMA request set/clear condition, the DMA request can be lost or the DMA transfer can be corrupted, if enabled.

20.6.4 Interrupts

The RTC has the following interrupt sources:

- Overflow (OVF): Indicates that the counter has reached its top value and wrapped to zero.
- Tamper (TAMPER): Indicates detection of valid signal on a tamper input pin or tamper event input.
- Compare (CMP n): Indicates a match between the counter value and the compare register.
- Alarm (ALARM n): Indicates a match between the clock value and the alarm register.
- Period n (PER n): The corresponding bit in the prescaler has toggled, see *Periodic Intervals* from Related Links.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by setting the corresponding bit in the Interrupt Enable Set register (INTENSET=1), and disabled by setting the corresponding bit in the Interrupt Enable Clear register (INTENCLR=1). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is raised and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled or the RTC is reset. See the description of the INTFLAG registers for details on how to clear interrupt flags.

All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC, see *Nested Vector Interrupt Controller* from Related Links. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated, see *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

[20.6.8.1. Periodic Intervals](#)

20.6.5 Events

The RTC can generate the following output events and these events can be used by EVSYS module:

- Overflow (OVF): Generated when the counter has reached its top value and wrapped to zero.
- Tamper (TAMPER): Generated on detection of valid signal on a tamper input pin or tamper event input.
- Compare (CMP0-1): Indicates a match between the counter value and the compare register.
- Alarm (ALARM0): Indicates a match between the clock value and the alarm register.
- Period n (PER0-7): The corresponding bit in the prescaler has toggled, see *Periodic Intervals* from Related Links.
- Periodic Daily (PERD): Generated when the COUNT/CLOCK has incremented at a fixed period of time.
- RTC Event (RTC_EVENT): Refer to CFG.CFGCON4.RTCEVENTSEL[1:0] bits for functionality description. Note that for 48-pin devices, the RTC_OUT for tamper detect and the legacy RTC_EVENT signals can be brought out to separate pin so that both can be used simultaneously. For 32-pin devices only 1 function is available and is selected by the CFG.CFGCON4.RTCEVTYPE bit.

Setting the Event Output bit in the Event Control Register (EVCTRL.xxxEO=1) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. See *Event System (EVSYS)* from Related Links for more details on configuring the event system.

The RTC can take the following actions on an input event:

- Tamper (TAMPEVT): Capture the RTC counter to the timestamp register. See *Tamper Detection* from Related Links.

Writing a one to an Event Input bit into the Event Control register (EVCTRL.xxxEI) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event.

RTC Event (RTC_EVENT): Other than the above events, which are mapped to the EVSYS module, the following events can generate specific external signal on the RTC EVENT I/O pin.

- 32 KHz clock
- Alarm pulse
- 1-second clock

These event signals are configured using CFGCON4.RTCEVENTSEL[1:0] bits.

Note: The RTC_OUT and RTC_EVENT signals are multiplexed and any one of the signal can be out at a time in pin limited variants.

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links. The selection between RTC_OUT and RTC_EVENT is configurable through CFGCON4.RTCEVTYPE bit.

Related Links

- 20.6.8.1. Periodic Intervals
- 27. Event System (EVSYS)
- 20.6.8.5. Tamper Detection
- 5. I/O Ports and Peripheral Pin Select (PPS)

20.6.6 Sleep Mode Operation

The RTC will continue to operate in any sleep mode where the source clock is active. The RTC *interrupts* can be used to wake up the device from a sleep mode. RTC *events* can trigger other operations in the system without exiting the sleep mode.

An interrupt request will be generated after the wake-up if the Interrupt Controller is configured accordingly. Otherwise the CPU will wake up directly, without triggering any interrupt. In this case, the CPU continues executing right from the first instruction that followed the entry into sleep.

The periodic events can also wake up the CPU through the interrupt function of the Event System. In this case, the event must be enabled and connected to an event channel with its interrupt enabled. See *Event System (EVSYS)* from Related Links.

Related Links

- 27. Event System (EVSYS)

20.6.7 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in Control A register, CTRLA.SWRST
- Enable bit in Control A register, CTRLA.ENABLE
- Count Read Synchronization bit in Control A register (CTRLA.COUNTSYNC)
- Clock Read Synchronization bit in Control A register (CTRLA.COUNTSYNC)

The following registers are synchronized when written:

- Counter Value register, COUNT
- Clock Value register, CLOCK
- Counter Period register, PER
- Compare n Value registers, COMPn
- Alarm n Value registers, ALARMn
- Frequency Correction register, FREQCORR
- Alarm n Mask register, MASKn
- The General Purpose n registers (GPn)

The following registers are synchronized when read:

- The Counter Value register, COUNT, if the Counter Read Sync Enable bit in CTRLA (CTRLA.COUNTSYNC) is '1'
- The Clock Value register, CLOCK, if the Clock Read Sync Enable bit in CTRLA (CTRLA.CLOCKSYNC) is '1'
- The Timestamp Value register (TIMESTAMP)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

20.6.8 Additional Features

20.6.8.1 Periodic Intervals

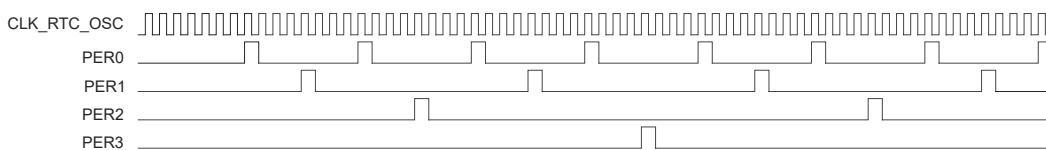
The RTC prescaler can generate interrupts and events at periodic intervals, allowing flexible system tick creation. Any of the upper eight bits of the prescaler (bits 2 to 9) can be the source of an interrupt/event. When one of the eight Periodic Event Output bits in the Event Control register (EVCTRL.PEREO[n=0..7]) is '1', an event is generated on the 0-to-1 transition of the related bit in the prescaler, resulting in a periodic event frequency of:

$$f_{\text{PERIODIC}(n)} = \frac{f_{\text{CLK_RTC_OSC}}}{2^{n+3}}$$

$f_{\text{CLK_RTC_OSC}}$ is the frequency of the internal prescaler clock CLK_RTC_OSC, and n is the position of the EVCTRL.PEREO_n bit. For example, PER0 will generate an event every eight CLK_RTC_OSC cycles, PER1 every 16 cycles, etc. This is shown in the figure below.

Periodic events are independent of the prescaler setting used by the RTC counter, except if CTRLA.PRESCALER is zero. Then, no periodic events will be generated.

Figure 20-5. Example Periodic Events



Note: The same applies for interrupts enabled in INTENSET/CLR.

20.6.8.2 Frequency Correction

The RTC Frequency Correction module employs periodic counter corrections to compensate for a too-slow or too-fast oscillator. Frequency correction requires that **CTRLA.PRESCALER** is greater than 1.

The digital correction circuit adds or subtracts cycles from the RTC prescaler to adjust the frequency in approximately 1ppm steps. Digital correction is achieved by adding or skipping a single count in the prescaler once every 8192 CLK_RTC_OSC cycles. The Value bit group in the Frequency Correction register (FREQCORR.VALUE) determines the number of times the adjustment is applied over 128 of these periods. The resulting correction is as follows:

$$\text{Correction in ppm} = \frac{\text{FREQCORR.VALUE}}{8192 \cdot 128} \cdot 10^6 \text{ppm}$$

This results in a resolution of 0.95367ppm.

The Sign bit in the Frequency Correction register (FREQCORR.SIGN) determines the direction of the correction. A positive value will add counts and increase the period (reducing the frequency), and a negative value will reduce counts per period (speeding up the frequency).

Digital correction also affects the generation of the periodic events from the prescaler. When the correction is applied at the end of the correction cycle period, the interval between the previous periodic event and the next occurrence may also be shortened or lengthened depending on the correction value.

20.6.8.3 Backup Registers

The RTC includes one Backup register (BKUP0). This register maintains its content in Backup sleep mode. It can be used to store user-defined values.

If more user-defined data must be stored than the Backup register can hold, the General Purpose registers (GPn) can be used.

20.6.8.4 General Purpose Registers

The RTC includes four General Purpose registers (GPn). These registers are reset only when the RTC is reset or when tamper detection occurs while **CTRLA.GPTRST=1**, and remain powered while the RTC is powered. They can be used to store user-defined values while other parts of the system are powered off.

The general purpose registers 2^n and 2^n+1 are enabled by writing a '1' to the General Purpose Enable bit n in the Control B register (CTRLB.GPnEN).

The GP registers share internal resources with the COMPARE/ALARM features. Each COMPARE/ALARM register has a separate read buffer and write buffer. When the general purpose feature is enabled the even GP uses the read buffer while the odd GP uses the write buffer.

When the COMPARE/ALARM register is written, the write buffer holds temporarily the COMPARE/ALARM value until the synchronisation is complete (bit SYNCBUSY.COMPn going to 0). After the write is completed the write buffer can be used as an odd general purpose register without affecting the COMPARE/ALARM function.

If the COMPARE/ALARM function is not used, the read buffer can be used as an even general purpose register. In this case, writing the even GP will temporarily use the write buffer until the synchronisation is complete (bit SYNCBUSY.GPn going to 0). Thus an even GP must be written before writing the odd GP. Changing or writing an even GP needs to temporarily save the value of the odd GP.

Before using an even GP, the associated COMPARE/ALARM feature must be disabled by writing a '1' to the General Purpose Enable bit in the Control B register (CTRLB.GPnEN). To re-enable the compare/alarm, CTRLB.GPnEN must be written to zero and the associated COMPn/ALARMn must be written with the correct value.

It is recommended to use the Backup register (BKUPn) first to store user-defined values, and use the GPn only when the user-defined values exceed the capacity of the provided BKUPn.

An example procedure to write the general purpose registers GP0 and GP1 is:

1. Wait for any ongoing write to COMP0 to complete (SYNCBUSY.COMP0 = 0). If the RTC is operating in Mode 1, wait for any ongoing write to COMP1 to complete as well (SYNCBUSY.COMP1 = 0).
2. Write **CTRLB.GP0EN = 1** if GP0 is needed.
3. Write GP0 if needed.
4. Wait for any ongoing write to GP0 to complete (SYNCBUSY.GP0 = 0). Note that GP1 will also show as busy when GP0 is busy.

5. Write GP1 if needed.

The following table provides the correspondence of General Purpose Registers and the COMPARE/ALARM read or write buffer in all RTC modes.

Table 20-2. General Purpose Registers Versus Compare/Alarm Registers: n in 0, 2, 4, 6...

Register	Mode 0	Mode 1	Mode 2	Write Before
GPn	COMPn/2 write buffer	(COMPn , COMPn+1) write buffer	ALARM0 write buffer	GPn+1
GPn+1	COMPn/2 read buffer	(COMPn , COMPn+1) read buffer	ALARM0 read buffer	-

20.6.8.5 Tamper Detection

The RTC provides four tamper channels that can be used for tamper detection.

The action of each tamper channel is configured using the Input n Action bits in the Tamper Control register (TAMPCTRL.INnACT):

- Off: Detection for tamper channel n is disabled.
- Wake: A transition on INn input (tamper channel n) matching TAMPCTRL.TAMPLVLn will be detected and the tamper interrupt flag (INTFLAG.TAMPER) will be set. The RTC value will not be captured in the TIMESTAMP register.
- Capture: A transition on INn input (tamper channel n) matching TAMPCTRL.TAMPLVLn will be detected and the tamper interrupt flag (INTFLAG.TAMPER) will be set. The RTC value will be captured in the TIMESTAMP register.
- Active Layer Protection: A mismatch of an internal RTC signal routed between INn and OUTn pins will be detected and the tamper interrupt flag (INTFLAG.TAMPER) will be set. The RTC value will be captured in the TIMESTAMP register.

In order to determine which tamper source caused a tamper event, the Tamper ID register (TAMPID) provides the detection status of each tamper channel. These bits remain active until cleared by software.

A single interrupt request (TAMPER) is available for all tamper channels.

The RTC also supports an input event (TAMPEVT) for generating a tamper condition within the Event System.

The tamper input event is enabled by the Tamper Input Event Enable bit in the Event Control register (EVCTRL.TAMPEVTEI).

Up to four polarity external inputs (INn) can be used for tamper detection. The polarity for each input is selected with the Tamper Level bits in the Tamper Control register (TAMPCTRL.TAMPLVLn).

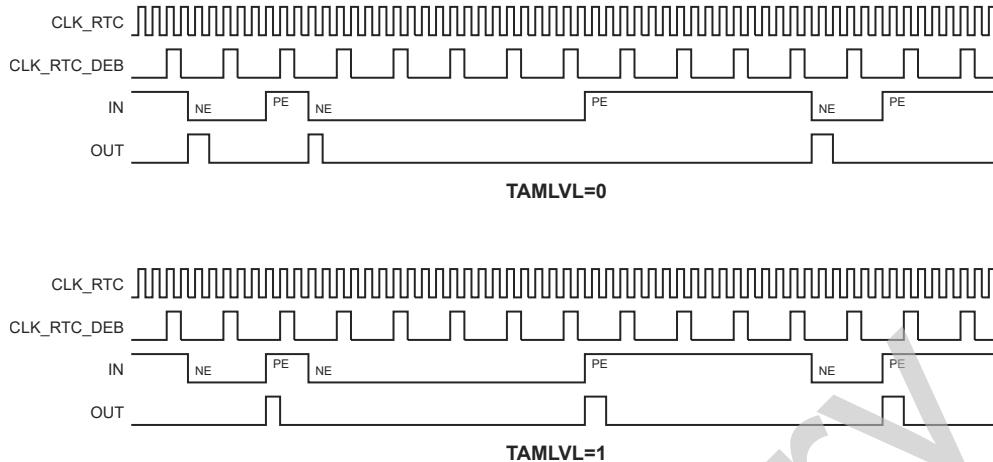
Separate debouncers are embedded for each external input. The debouncer for each input is enabled/disabled with the Debounce Enable bits in the Tamper Control register (TAMPCTRL.DEBNCn). The debouncer configuration is fixed for all inputs as set by the Control B register (CTRLB). The debouncing period duration is configurable using the Debounce Frequency field in the Control B register (CTRLB.DEBF). The period is set for all debouncers (i.e., the duration cannot be adjusted separately for each debouncer).

When TAMPCTRL.DEBNCn = 0, INn is detected asynchronously. See the following figure for an example.

PIC32CX-BZ2 and WBZ45 Family

RTC – Real-Time Counter

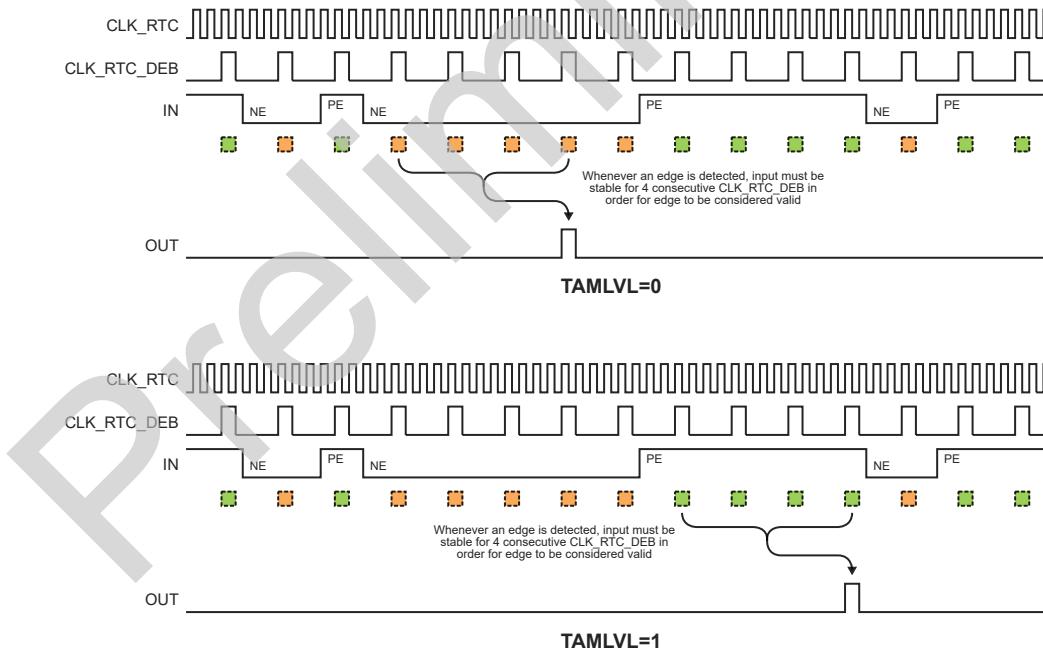
Figure 20-6. Edge Detection with Debouncer Disabled



When TAMPCTRL.DEBNCn = 1, the detection time depends on whether the debouncer operates synchronously or asynchronously, and whether majority detection is enabled or not. For more details, refer to the following table. Synchronous versus asynchronous stability debouncing is configured by the Debounce Asynchronous Enable bit in the Control B register (CTRLB.DEBASYNC):

- Synchronous (CTRLB.DEBASYNC = 0): INn is synchronized in two CLK_RTC periods and then must remain stable for four CLK_RTC_DEB periods before a valid detection occurs. See the following figure for an example.

Figure 20-7. Edge Detection with Synchronous Stability Debouncing

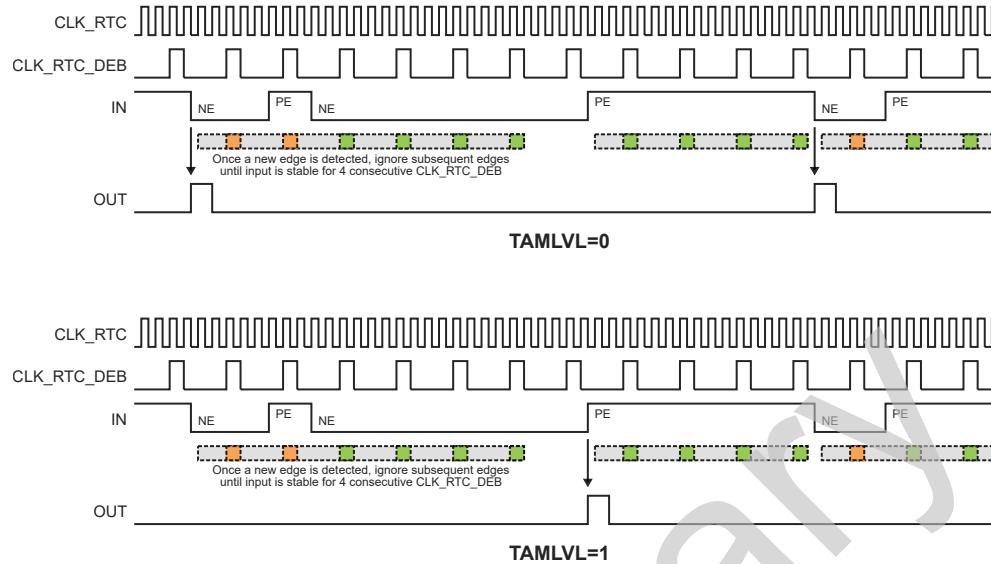


- Asynchronous (CTRLB.DEBASYNC = 1): The first edge on INn is detected. Further detection is blanked until INn remains stable for four CLK_RTC_DEB periods. See the following figure for an example.

PIC32CX-BZ2 and WBZ45 Family

RTC – Real-Time Counter

Figure 20-8. Edge Detection with Asynchronous Stability Debouncing



Majority debouncing is configured by the Debounce Majority Enable bit in the Control B register (CTRLB.DEBMAJ). INn must be valid for two out of three CLK_RTC_DEB periods. See the following figure for an example.

PIC32CX-BZ2 and WBZ45 Family

RTC – Real-Time Counter

Figure 20-9. Edge Detection with Majority Debouncing

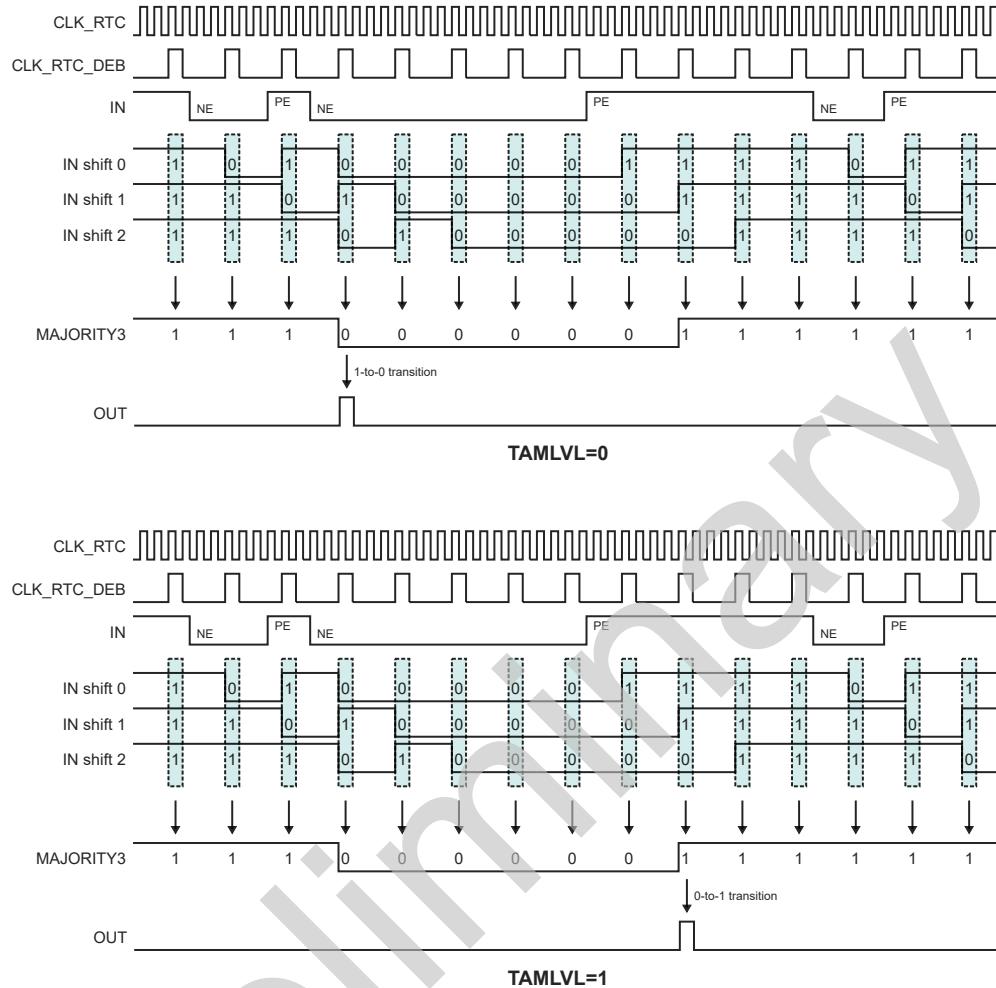


Table 20-3. Debouncer Configuration

TAMPCTRL. DEBNcN	CTRLB. DEBMAJ	CTRLB. DEBASYNC	Description
0	X	X	Detect edge on INn with no debouncing. Every edge detected is immediately triggered.
1	0	0	Detect edge on INn with synchronous stability debouncing. Edge detected is only triggered when INn is stable for 4 consecutive CLK_RTC_DEB periods.
1	0	1	Detect edge on INn with asynchronous stability debouncing. First detected edge is triggered immediately. All subsequent detected edges are ignored until INn is stable for 4 consecutive CLK_RTC_DEB periods.
1	1	X	Detect edge on INn with majority debouncing. Pin INn is sampled for 3 consecutive CLK_RTC_DEB periods. Signal level is determined by majority-rule (LLL, LLH, LHL, HLL = '0' and LHH, HLH, HHL, HHH = '1').

20.6.8.5.1 Timestamp

As part of tamper detection the RTC can capture the counter value (COUNT/CLOCK) into the TIMESTAMP register. Three CLK_RTC periods are required to detect the tampering condition and capture the value. The TIMESTAMP value can be read once the Tamper flag in the Interrupt Flag register (INTFLAG.TAMPER) is set. If the DMA Enable bit in the Control B register (CTRLB.DMAEN) is '1', a DMA request will be triggered by the timestamp. In order to determine which tamper source caused a capture, the Tamper ID register (TAMPID) provides the detection status of each tamper channel and the tamper input event. A DMA transfer can then read both TIMESTAMP and TAMPID in succession.

A new timestamp value cannot be captured until the Tamper flag is cleared, either by reading the timestamp or by writing a '1' to INTFLAG.TAMPER. If several tamper conditions occur in a short window before the flag is cleared, only the first timestamp may be logged. However, the detection of each tamper will still be recorded in TAMPID.

The Tamper Input Event (TAMPEVT) will always perform a timestamp capture. To capture on the external inputs (INn), the corresponding Input Action field in the Tamper Control register (TAMPCTRL.INnACT) must be written to '1'. If an input is set for wake functionality it does not capture the timestamp; however the Tamper flag and TAMPID will still be updated.

Note: Once the value from the TIMESTAMP register is read, the INTFLAG.TAMPER bit must be cleared. The next value from this register should be read only after the INTFLAG.TAMPER bit is set again.

20.6.8.5.2 Active Layer Protection

The RTC provides a mean of detecting broken traces on the PCB, also known as Active layer Protection. In this mode, a generated internal RTC signal can be directly routed over critical components on the board using the RTC_OUT output pin to one RTC INn input pin. A tamper condition is detected if there is a mismatch on the generated RTC signal.

The Active Layer Protection mode and the generation of the RTC signal is enabled by setting the RTCOUT bit in the Control B register (CTRLB.RTCOUT).

Note: The Active Layer Protection works with one output pin (RTC_OUT) and multiple input pin INn. This is achieved by clearing the Separate Tamper Output bit CTRLB.SEPTO.

Enabling active layer protection requires the following steps:

- Enable the RTC prescaler output by writing a one to the RTC Out bit in the Control B register (CTRLB.RTCOUT). The I/O pins must also be configured to correctly route the signal to the external pins.
 - Select the frequency of the output signal by configuring the RTC Active Layer Frequency field in the Control B register (CTRLB.ACTF).
- $$GCLK_{RTC_OUT} = \frac{CLK_{RTC}}{2^{CTRLB.ACTF+1}}$$
- Enable the tamper input n (INn) in active layer mode by writing 3 to the corresponding Input Action field in the Tamper Control register (TAMPCTRL.INnACT). When active layer protection is enabled and INn and OUTn pin are used, the value of INn is sampled on the falling edge of CLK_RTC and compared to the expected value of OUTn. Therefore up to one half of a CLK_RTC period is available for propagation delay through the trace.
 - Enable Acitive Layer Protection by setting CTRLB.RTCOUT bit.

20.7 Register Summary - Mode 0 - 32-Bit Counter

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	MATCHCLR				MODE[1:0]	ENABLE	SWRST	
		15:8	COUNTSYNC	GPTRST	BKTRST			PRESCALER[3:0]		
0x02	CTRLB	7:0	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
		15:8			ACTF[2:0]				DEBF[2:0]	
0x04	EVCTRL	7:0	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
		15:8	OVFEO	TAMPEREO					CMPEOn[1:0]	
		23:16								TAMPEVEI
		31:24								
0x08	INTENCLR	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					CMP1	CMP0
0x0A	INTENSET	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					CMP1	CMP0
0x0C	INTFLAG	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					CMP1	CMP0
0x0E	DBGCTRL	7:0								DBGRUN
0x0F	Reserved									
0x10	SYNCBUSY	7:0		COMP1	COMP0		COUNT	FREQCORR	ENABLE	SWRST
		15:8	COUNTSYNC							
		23:16					GP3	GP2	GP1	GP0
		31:24								
0x14	FREQCORR	7:0	SIGN				VALUE[6:0]			
0x15 ... 0x17	Reserved									
0x18	COUNT	7:0					COUNT[7:0]			
		15:8					COUNT[15:8]			
		23:16					COUNT[23:16]			
		31:24					COUNT[31:24]			
0x1C ... 0x1F	Reserved									
0x20	COMP0	7:0					COMP[7:0]			
		15:8					COMP[15:8]			
		23:16					COMP[23:16]			
		31:24					COMP[31:24]			
0x24	COMP1	7:0					COMP[7:0]			
		15:8					COMP[15:8]			
		23:16					COMP[23:16]			
		31:24					COMP[31:24]			
0x28 ... 0x3F	Reserved									
0x40	GP0	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x44	GP1	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x48	GP2	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x4C	GP3	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x50 ...	Reserved									
0x60	TAMPCTRL	7:0	IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]	
		15:8							IN4ACT[1:0]	
		23:16			TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0	
		31:24			DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0	
0x64	TIMESTAMP	7:0			COUNT[7:0]					
		15:8			COUNT[15:8]					
		23:16			COUNT[23:16]					
		31:24			COUNT[31:24]					
0x68	TAMPID	7:0			TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0	
		15:8								
		23:16								
		31:24	TAMPEVT							
0x6C ...	Reserved									
0x80	BKUP0	7:0			BKUP[7:0]					
		15:8			BKUP[15:8]					
		23:16			BKUP[23:16]					
		31:24			BKUP[31:24]					

20.8 Register Description - Mode 0 - 32-Bit Counter

This Register Description section is valid if the RTC is in COUNT32 mode (CTRLA.MODE=0).

20.8.1 Control A in COUNT32 mode (CTRLA.MODE=0)

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	COUNTSYNC	GPTRST	BKTRST					
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MATCHCLR				MODE[1:0]	ENABLE	SWRST	
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 15 – COUNTSYNC COUNT Read Synchronization Enable

The COUNT register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the COUNT register.

This bit is not enable-protected.

Value	Description
0	COUNT read synchronization is disabled
1	COUNT read synchronization is enabled

Bit 14 – GPTRST GP Registers Reset On Tamper Enable

Only GP registers enabled by the CTRLB.GPnEN bits are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Bit 13 – BKTRST BKUP Registers Reset On Tamper Enable

All BKUPn registers are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Value	Description
0	BKUPn registers will not reset when a tamper condition occurs.
1	BKUPn registers will reset when a tamper condition occurs.

Bits 11:8 – PRESCALER[3:0] Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0xA	DIV512	CLK_RTC_CNT = GCLK_RTC/512
0xB	DIV1024	CLK_RTC_CNT = GCLK_RTC/1024
0xC–0xF	-	Reserved

Bit 7 – MATCHCLR Clear on Match

This bit defines if the counter is cleared or not on a match.

This bit is not synchronized.

Value	Description
0	The counter is not cleared on a Compare/Alarm 0 match
1	The counter is cleared on a Compare/Alarm 0 match

Bits 3:2 – MODE[1:0] Operating Mode

This bit group defines the operating mode of the RTC.

This bit is not synchronized.

Value	Name	Description
0x0	COUNT32	Mode 0: 32-bit counter
0x1	COUNT16	Mode 1: 16-bit counter
0x2	CLOCK	Mode 2: Clock/calendar
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization there is a delay between writing CTRLA.ENABLE and until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the RTC (except DBGCTRL) to their initial state, and the RTC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay between writing CTRLA.SWRST and until the reset is complete.

CTRLA.SWRST will be cleared when the reset is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is not reset operation ongoing
1	The reset operation is ongoing

20.8.2 Control B in COUNT32 mode (CTRLA.MODE=0)

Name: CTRLB
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	ACTF[2:0]					DEBF[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bits 14:12 – ACTF[2:0] Active Layer Frequency

These bits define the prescaling factor for the RTC clock output (OUT) used during active layer protection in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_OUT = CLK_RTC / 2
0x1	DIV4	CLK_RTC_OUT = CLK_RTC / 4
0x2	DIV8	CLK_RTC_OUT = CLK_RTC / 8
0x3	DIV16	CLK_RTC_OUT = CLK_RTC / 16
0x4	DIV32	CLK_RTC_OUT = CLK_RTC / 32
0x5	DIV64	CLK_RTC_OUT = CLK_RTC / 64
0x6	DIV128	CLK_RTC_OUT = CLK_RTC / 128
0x7	DIV256	CLK_RTC_OUT = CLK_RTC / 256

Bits 10:8 – DEBF[2:0] Debounce Frequency

These bits define the prescaling factor for the input debouncers in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_DEB = CLK_RTC / 2
0x1	DIV4	CLK_RTC_DEB = CLK_RTC / 4
0x2	DIV8	CLK_RTC_DEB = CLK_RTC / 8
0x3	DIV16	CLK_RTC_DEB = CLK_RTC / 16
0x4	DIV32	CLK_RTC_DEB = CLK_RTC / 32
0x5	DIV64	CLK_RTC_DEB = CLK_RTC / 64
0x6	DIV128	CLK_RTC_DEB = CLK_RTC / 128
0x7	DIV256	CLK_RTC_DEB = CLK_RTC / 256

Bit 7 – DMAEN DMA Enable

The RTC can trigger a DMA request when the timestamp is ready in the TIMESTAMP register.

Value	Description
0	Tamper DMA request is disabled. Reading TIMESTAMP has no effect on INTFLAG.TAMPER.
1	Tamper DMA request is enabled. Reading TIMESTAMP will clear INTFLAG.TAMPER.

Bit 6 – RTCOUT RTC Output Enable

Value	Description
0	The RTC active layer output is disabled.
1	The RTC active layer output is enabled.

Bit 5 – DEBASYNC Debouncer Asynchronous Enable

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Value	Description
0	The tamper input debouncers operate synchronously.
1	The tamper input debouncers operate asynchronously.

Bit 4 – DEBMAJ Debouncer Majority Enable

Value	Description
0	The tamper input debouncers match three equal values.
1	The tamper input debouncers match majority two of three values.

Bit 1 – GP2EN General Purpose 2 Enable

Value	Description
0	COMP1 compare function enabled. GP2/GP3 disabled.
1	COMP1 compare function disabled. GP2/GP3 enabled.

Bit 0 – GP0EN General Purpose 0 Enable

Value	Description
0	COMP0 compare function enabled. GP0/GP1 disabled.
1	COMP0 compare function disabled. GP0/GP1 enabled.

20.8.3 Event Control in COUNT32 mode (CTRLA.MODE=0)

Name: EVCTRL
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								R/W
Reset								0
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 16 – TAMPEVEI Tamper Event Input Enable

Value	Description
0	Tamper event input is disabled and incoming events will be ignored.
1	Tamper event input is enabled and incoming events will capture the COUNT value.

Bit 15 – OVFE0 Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 14 – TAMPEROE Tamper Event Output Enable

Value	Description
0	Tamper event output is disabled and will not be generated.
1	Tamper event output is enabled and will be generated for every tamper input.

Bits 9:8 – CMPEOn[1:0] Compare n Event Output Enable [n = 1..0]

Value	Description
0	Compare n event is disabled and will not be generated.
1	Compare n event is enabled and will be generated for every compare match.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PEREOOn Periodic Interval n Event Output Enable [n = 7..0]

Value	Description
0	Periodic Interval n event is disabled and will not be generated.
1	Periodic Interval n event is enabled and will be generated.

20.8.4 Interrupt Enable Clear in COUNT32 mode (CTRLA.MODE=0)

Name: INTENCLR
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					CMP1	CMP0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Tamper Interrupt Enable bit, which disables the Tamper interrupt.

Value	Description
0	The Tamper interrupt is disabled.
1	The Tamper interrupt is enabled.

Bits 8, 9 – CMPn Compare n Interrupt Enable [n = 1..0]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Compare n Interrupt Enable bit, which disables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Periodic Interval n Interrupt Enable bit, which disables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.8.5 Interrupt Enable Set in COUNT32 mode (CTRLA.MODE=0)

Name: INTENSET
Offset: 0x0A
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					CMP1	CMP0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Tamper Interrupt Enable bit, which enables the Tamper interrupt.

Value	Description
0	The Tamper interrupt is disabled.
1	The Tamper interrupt is enabled.

Bits 8, 9 – CMPn Compare n Interrupt Enable [n = 1..0]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Compare n Interrupt Enable bit, which enables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.8.6 Interrupt Flag Status and Clear in COUNT32 mode (CTRLA.MODE=0)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					CMP1	CMP0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

Bit 14 – TAMPER Tamper event

This flag is set after a damper condition occurs, and an interrupt request will be generated if INTENCLR.TAMPER/INTENSET.TAMPER is '1'. Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the Tamper interrupt flag.

Bits 8, 9 – CMPn Compare n [n = 1..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after a match with the compare condition, and an interrupt request will be generated if INTENCLR/SET.COMPn is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Compare n interrupt flag.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n [n = 7..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the 0-to-1 transition of prescaler bit [n+2], and an interrupt request will be generated if INTENCLR/SET.PERn is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Periodic Interval n interrupt flag.

20.8.7 Debug Control

Name: DBGCTRL
Offset: 0x0E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGRUN 0

Bit 0 – DBGRUN Debug Run

This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The RTC is halted when the CPU is halted by an external debugger.
1	The RTC continues normal operation when the CPU is halted by an external debugger.

20.8.8 Synchronization Busy in COUNT32 mode (CTRLA.MODE=0)

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					GP3	GP2	GP1	GP0
Reset					R	R	R	R
Bit	15	14	13	12	11	10	9	8
Access	R							
Reset	0							
Bit	7	6	5	4	3	2	1	0
Access		COMP1	COMP0		COUNT	FREQCORR	ENABLE	SWRST
Reset		R	R		R	R	R	R
	0	0	0		0	0	0	0

Bits 16, 17, 18, 19 – GPn General Purpose n Synchronization Busy Status

Value	Description
0	Write synchronization for GPn register is complete.
1	Write synchronization for GPn register is ongoing.

Bit 15 – COUNTSYNC Count Read Sync Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.COUNTSYNC bit is complete.
1	Write synchronization for CTRLA.COUNTSYNC bit is ongoing.

Bits 5, 6 – COMPn Compare n Synchronization Busy Status [n = 1..0]

Value	Description
0	Write synchronization for COMPx register is complete.
1	Write synchronization for COMPx register is ongoing.

Bit 3 – COUNT Count Value Synchronization Busy Status

Value	Description
0	Read/write synchronization for COUNT register is complete.
1	Read/write synchronization for COUNT register is ongoing.

Bit 2 – FREQCORR Frequency Correction Synchronization Busy Status

Value	Description
0	Write synchronization for FREQCORR register is complete.
1	Write synchronization for FREQCORR register is ongoing.

Bit 1 – ENABLE Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.

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Value	Description
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST Software Reset Synchronization Busy Status

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

20.8.9 Frequency Correction

Name: FREQCORR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0	
	SIGN	VALUE[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Bit 7 – SIGN Correction Sign

Value	Description
0	The correction value is positive, i.e., frequency will be decreased.
1	The correction value is negative, i.e., frequency will be increased.

Bits 6:0 – VALUE[6:0] Correction Value

These bits define the amount of correction applied to the RTC prescaler.

Value	Description
0	Correction is disabled and the RTC frequency is unchanged.
1 – 127	The RTC frequency is adjusted according to the value.

20.8.10 Counter Value in COUNT32 mode (CTRLA.MODE=0)

Name: COUNT
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
COUNT[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0] Counter Value

These bits define the value of the 32-bit RTC counter in mode 0.

20.8.11 Compare 0 Value in COUNT32 mode (CTRLA.MODE=0)

Name: COMP0
Offset: 0x20
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
COMP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COMP[31:0] Compare Value

The 32-bit value of COMPn is continuously compared with the 32-bit COUNT value. When a match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next counter cycle, and the counter value is cleared if CTRLA.MATCHCLR is one.

20.8.12 Compare 1 Value in COUNT32 mode (CTRLA.MODE=1)

Name: COMP1
Offset: 0x24
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
COMP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COMP[31:0] Compare Value

The 32-bit value of COMPn is continuously compared with the 32-bit COUNT value. When a match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next counter cycle, and the counter value is cleared if CTRLA.MATCHCLR is one.

20.8.13 General Purpose n

Name: GPn
Offset: 0x40 + n*0x04 [n=0..3]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
GP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GP[31:0] General Purpose

These bits are for user-defined general purpose use, see *General Purpose Registers* from Related Links.

Related Links

[20.6.8.4. General Purpose Registers](#)

20.8.14 Tamper Control

Name: TAMPCTRL
Offset: 0x60
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access				DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0
Reset				0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access				TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0
Reset				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access							IN4ACT[1:0]	
Reset							0	0
Bit	7	6	5	4	3	2	1	0
Access		IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]
Reset	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27, 28 – DEBNCn Debounce Enable of Tamper Input INn [n=0..3]

Note: Debounce feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	Debouncing is disabled for Tamper input INn
1	Debouncing is enabled for Tamper input INn

Bits 16, 17, 18, 19, 20 – TAMLVLn Tamper Level Select of Tamper Input INn [n=0..3]

Note: Tamper Level feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	A falling edge condition will be detected on Tamper input INn.
1	A rising edge condition will be detected on Tamper input INn.

Bits 0:1, 2:3, 4:5, 6:7, 8:9 – INnACT Tamper Channel n Action [n=0..3]

These bits determine the action taken by Tamper Channel n.

Value	Name	Description
0x0	OFF	Off (Disabled)
0x1	WAKE	Wake and set Tamper flag
0x2	CAPTURE	Capture timestamp and set Tamper flag
0x3	ACTL	Compare RTC signal routed between INn and OUT pins . When a mismatch occurs, capture timestamp and set Tamper flag

20.8.15 Timestamp

Name: TIMESTAMP
Offset: 0x64
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
COUNT[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNT[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNT[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
COUNT[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0] Count Timestamp Value

The 32-bit value of COUNT is captured by the TIMESTAMP when a tamper condition occurs

20.8.16 Tamper ID

Name: TAMPID
Offset: 0x68
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24	
	TAMPEVT								
Access	R/W								
Reset	0								
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0
Access				R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0

Bit 31 – TAMPEVT Tamper Event Detected

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper input event has not been detected
1	A tamper input event has been detected

Bits 0, 1, 2, 3, 4 – TAMPIDn Tamper on Channel n Detected [n=0..3]

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper condition has not been detected on Channel n
1	A tamper condition has been detected on Channel n

20.8.17 Backup0

Name: BKUP0
Offset: 0x80
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
BKUP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BKUP[31:0] Backup

These bits are user-defined for general purpose use in the Backup domain.

20.9 Register Summary - Mode 1 - 16-Bit Counter

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0					MODE[1:0]	ENABLE	SWRST	
		15:8	COUNTSYNC	GPTRST	BKTRST			PRESCALER[3:0]		
0x02	CTRLB	7:0	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
		15:8			ACTF[2:0]				DEBF[2:0]	
0x04	EVCTRL	7:0	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
		15:8	OVFEO	TAMPEREO					CMPEOn[3:0]	
		23:16								TAMPEVEI
		31:24								
0x08	INTENCLR	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
0x0A	INTENSET	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
0x0C	INTFLAG	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
0x0E	DBGCTRL	7:0								DBGRUN
0x0F	Reserved									
0x10	SYNCBUSY	7:0	COMP2	COMP1	COMP0	PER	COUNT	FREQCORR	ENABLE	SWRST
		15:8	COUNTSYNC							COMP3
		23:16					GP3	GP2	GP1	GP0
		31:24								
0x14	FREQCORR	7:0	SIGN				VALUE[6:0]			
0x15	Reserved									
0x17										
0x18	COUNT	7:0					COUNT[7:0]			
		15:8					COUNT[15:8]			
0x1A	Reserved									
0x1B										
0x1C	PER	7:0					PER[7:0]			
		15:8					PER[15:8]			
0x1E	Reserved									
0x1F										
0x20	COMP0	7:0					COMP[7:0]			
		15:8					COMP[15:8]			
0x22	Reserved									
0x23										
0x24	COMP1	7:0					COMP[7:0]			
		15:8					COMP[15:8]			
0x26	Reserved									
0x3F										
0x40	GP0	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x44	GP1	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x48	GP2	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x4C	GP3	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x50 ...	Reserved									
0x60	TAMPCTRL	7:0	IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]	
		15:8							IN4ACT[1:0]	
		23:16			TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0	
		31:24			DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0	
0x64	TIMESTAMP	7:0			COUNT[7:0]					
		15:8			COUNT[15:8]					
		23:16								
		31:24								
0x68	TAMPID	7:0			TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0	
		15:8								
		23:16								
		31:24	TAMPEVT							
0x6C ...	Reserved									
0x80	BKUP0	7:0			BKUP[7:0]					
		15:8			BKUP[15:8]					
		23:16			BKUP[23:16]					
		31:24			BKUP[31:24]					

20.10 Register Description - Mode 1 - 16-Bit Counter

This Register Description section is valid if the RTC is in COUNT16 mode (CTRLA.MODE=1).

20.10.1 Control A in COUNT16 mode (CTRLA.MODE=1)

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	COUNTSYNC	GPTRST	BKTRST				PRESCALER[3:0]	
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0
Bit	7	6	5	4	3	2	1	0
					MODE[1:0]		ENABLE	SWRST
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – COUNTSYNC COUNT Read Synchronization Enable

The COUNT register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the COUNT register.

This bit is not enable-protected.

Value	Description
0	COUNT read synchronization is disabled
1	COUNT read synchronization is enabled

Bit 14 – GPTRST GP Registers Reset On Tamper Enable

Only GP registers enabled by the CTRLB.GPnEN bits are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Value	Description
0	GPn registers will not reset when a tamper condition occurs.
1	GPn registers will reset when a tamper condition occurs.

Bit 13 – BKTRST BKUP Registers Reset On Tamper Enable

All BKUPn registers are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Value	Description
0	BKUPn registers will not reset when a tamper condition occurs.
1	BKUPn registers will reset when a tamper condition occurs.

Bits 11:8 – PRESCALER[3:0] Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0xA	DIV512	CLK_RTC_CNT = GCLK_RTC/512

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Value	Name	Description
0xB	DIV1024	CLK_RTC_CNT = GCLK_RTC/1024
0xC–0xF	-	Reserved

Bits 3:2 – MODE[1:0] Operating Mode

This field defines the operating mode of the RTC. This bit is not synchronized.

Value	Name	Description
0x0	COUNT32	Mode 0: 32-bit counter
0x1	COUNT16	Mode 1: 16-bit counter
0x2	CLOCK	Mode 2: Clock/calendar
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the RTC (except DBGCTRL) to their initial state, and the RTC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST will be cleared when the reset is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is not reset operation ongoing
1	The reset operation is ongoing

20.10.2 Control B in COUNT16 mode (CTRLA.MODE=1)

Name: CTRLB
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	ACTF[2:0]					DEBF[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bits 14:12 – ACTF[2:0] Active Layer Frequency

These bits define the prescaling factor for the RTC clock output (OUT) used during active layer protection in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_OUT = CLK_RTC / 2
0x1	DIV4	CLK_RTC_OUT = CLK_RTC / 4
0x2	DIV8	CLK_RTC_OUT = CLK_RTC / 8
0x3	DIV16	CLK_RTC_OUT = CLK_RTC / 16
0x4	DIV32	CLK_RTC_OUT = CLK_RTC / 32
0x5	DIV64	CLK_RTC_OUT = CLK_RTC / 64
0x6	DIV128	CLK_RTC_OUT = CLK_RTC / 128
0x7	DIV256	CLK_RTC_OUT = CLK_RTC / 256

Bits 10:8 – DEBF[2:0] Debounce Frequency

These bits define the prescaling factor for the input debouncers in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_DEB = CLK_RTC / 2
0x1	DIV4	CLK_RTC_DEB = CLK_RTC / 4
0x2	DIV8	CLK_RTC_DEB = CLK_RTC / 8
0x3	DIV16	CLK_RTC_DEB = CLK_RTC / 16
0x4	DIV32	CLK_RTC_DEB = CLK_RTC / 32
0x5	DIV64	CLK_RTC_DEB = CLK_RTC / 64
0x6	DIV128	CLK_RTC_DEB = CLK_RTC / 128
0x7	DIV256	CLK_RTC_DEB = CLK_RTC / 256

Bit 7 – DMAEN DMA Enable

The RTC can trigger a DMA request when the timestamp is ready in the TIMESTAMP register.

Value	Description
0	Tamper DMA request is disabled. Reading TIMESTAMP has no effect on INTFLAG.TAMPER.
1	Tamper DMA request is enabled. Reading TIMESTAMP will clear INTFLAG.TAMPER.

Bit 6 – RTCOUT RTC Output Enable

Value	Description
0	The RTC active layer output is disabled.
1	The RTC active layer output is enabled.

Bit 5 – DEBASYNC Debouncer Asynchronous Enable

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Value	Description
0	The tamper input debouncers operate synchronously.
1	The tamper input debouncers operate asynchronously.

Bit 4 – DEBMAJ Debouncer Majority Enable

Value	Description
0	The tamper input debouncers match three equal values.
1	The tamper input debouncers match majority two of three values.

Bit 1 – GP2EN General Purpose 2 Enable

Value	Description
0	COMP1 compare function enabled. GP2/GP3 disabled.
1	COMP1 compare function disabled. GP2/GP3 enabled.

Bit 0 – GP0EN General Purpose 0 Enable

Value	Description
0	COMP0 compare function enabled. GP0/GP1 disabled.
1	COMP0 compare function disabled. GP0/GP1 enabled.

20.10.3 Event Control in COUNT16 mode (CTRLA.MODE=1)

Name: EVCTRL
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								R/W
Reset								0
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 16 – TAMPEVEI Tamper Event Input Enable

Value	Description
0	Tamper event input is disabled, and incoming events will be ignored
1	Tamper event input is enabled, and incoming events will capture the COUNT value

Bit 15 – OVFE0 Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 14 – TAMPEROE Tamper Event Output Enable

Value	Description
0	Tamper event output is disabled, and will not be generated.
1	Tamper event output is enabled, and will be generated for every tamper input.

Bits 11:8 – CMPEOn[3:0] Compare n Event Output Enable [n = 3..0]

Value	Description
0	Compare n event is disabled and will not be generated.
1	Compare n event is enabled and will be generated for every compare match.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PEREOOn Periodic Interval n Event Output Enable [n = 7..0]

Value	Description
0	Periodic Interval n event is disabled and will not be generated.
1	Periodic Interval n event is enabled and will be generated.

20.10.4 Interrupt Enable Clear in COUNT16 mode (CTRLA.MODE=1)

Name: INTENCLR
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Tamper Interrupt Enable bit, which disables the Tamper interrupt.

Value	Description
0	The Tamper interrupt is disabled.
1	The Tamper interrupt is enabled.

Bits 8, 9, 10, 11 – CMPn Compare n Interrupt Enable [n = 3..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Compare n Interrupt Enable bit, which disables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Periodic Interval n Interrupt Enable bit, which disables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.10.5 Interrupt Enable Set in COUNT16 mode (CTRLA.MODE=1)

Name: INTENSET
Offset: 0x0A
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Tamper Interrupt Enable bit, which enables the Tamper interrupt.

Value	Description
0	The Tamper interrupt is disabled.
1	The Tamper interrupt is enabled.

Bits 8, 9, 10, 11 – CMPn Compare n Interrupt Enable [n = 3..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Compare n Interrupt Enable bit, which enables the Compare n interrupt.

Value	Description
0	The Compare n interrupt is disabled.
1	The Compare n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.10.6 Interrupt Flag Status and Clear in COUNT16 mode (CTRLA.MODE=1)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER			CMP3	CMP2	CMP1	CMP0
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

Bit 14 – TAMPER Tamper

This flag is set after a tamper condition occurs, and an interrupt request will be generated if INTENCLR.TAMPER/INTENSET.TAMPER is one.

Writing a '0' to this bit has no effect.

Writing a one to this bit clears the Tamper interrupt flag.

Bits 8, 9, 10, 11 – CMPn Compare n [n = 3..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after a match with the compare condition, and an interrupt request will be generated if INTENCLR/SET.COMPn is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Compare n interrupt flag.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n [n = 7..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the 0-to-1 transition of prescaler bit [n+2], and an interrupt request will be generated if INTENCLR/SET.PERx is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Periodic Interval n interrupt flag.

20.10.7 Debug Control

Name: DBGCTRL
Offset: 0x0E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGRUN 0

Bit 0 – DBGRUN Debug Run

This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The RTC is halted when the CPU is halted by an external debugger.
1	The RTC continues normal operation when the CPU is halted by an external debugger.

20.10.8 Synchronization Busy in COUNT16 mode (CTRLA.MODE=1)

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					GP3	GP2	GP1	GP0
Reset					R	R	R	R
Bit	15	14	13	12	11	10	9	8
Access	R							R
Reset	0							0
Bit	7	6	5	4	3	2	1	0
Access	COMP2	COMP1	COMP0	PER	COUNT	FREQCORR	ENABLE	SWRST
Reset	0	0	0	0	0	0	0	0

Bits 16, 17, 18, 19 – GPn General Purpose n Synchronization Busy Status

Value	Description
0	Write synchronization for GPn register is complete.
1	Write synchronization for GPn register is ongoing.

Bit 15 – COUNTSYNC Count Read Sync Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.COUNTSYNC bit is complete.
1	Write synchronization for CTRLA.COUNTSYNC bit is ongoing.

Bits 5, 6, 7, 8 – COMPn Compare n Synchronization Busy Status [n = 3..0]

Value	Description
0	Write synchronization for COMPn register is complete.
1	Write synchronization for COMPn register is ongoing.

Bit 4 – PER Period Synchronization Busy Status

Value	Description
0	Write synchronization for PER register is complete.
1	Write synchronization for PER register is ongoing.

Bit 3 – COUNT Count Value Synchronization Busy Status

Value	Description
0	Read/write synchronization for COUNT register is complete.
1	Read/write synchronization for COUNT register is ongoing.

Bit 2 – FREQCORR Frequency Correction Synchronization Busy Status

Value	Description
0	Write synchronization for FREQCORR register is complete.

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Value	Description
1	Write synchronization for FREQCORR register is ongoing.

Bit 1 – ENABLE Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST Software Reset Synchronization Busy Status

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

20.10.9 Frequency Correction

Name: FREQCORR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0	
	SIGN	VALUE[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Bit 7 – SIGN Correction Sign

Value	Description
0	The correction value is positive, i.e., frequency will be decreased.
1	The correction value is negative, i.e., frequency will be increased.

Bits 6:0 – VALUE[6:0] Correction Value

These bits define the amount of correction applied to the RTC prescaler.

Value	Description
0	Correction is disabled and the RTC frequency is unchanged.
1 – 127	The RTC frequency is adjusted according to the value.

20.10.10 Counter Value in COUNT16 mode (CTRLA.MODE=1)

Name: COUNT
Offset: 0x18
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
COUNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Counter Value

These bits define the value of the 16-bit RTC counter in COUNT16 mode (CTRLA.MODE=1).

20.10.11 Counter Period in COUNT16 mode (CTRLA.MODE=1)

Name: PER
Offset: 0x1C
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
PER[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
PER[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PER[15:0] Counter Period

These bits define the value of the 16-bit RTC period in COUNT16 mode (CTRLA.MODE=1).

20.10.12 Compare 0 Value in COUNT16 mode (CTRLA.MODE=1)

Name: COMP0
Offset: 0x20
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
COMP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COMP[15:0] Compare Value

The 16-bit value of COMPn is continuously compared with the 16-bit COUNT value. When a match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next counter cycle.

20.10.13 Compare 1 Value in COUNT16 mode (CTRLA.MODE=1)

Name: COMP1
Offset: 0x24
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
COMP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COMP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COMP[15:0] Compare Value

The 16-bit value of COMPn is continuously compared with the 16-bit COUNT value. When a match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next counter cycle.

20.10.14 General Purpose n

Name: GPn
Offset: 0x40 + n*0x04 [n=0..3]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
GP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GP[31:0] General Purpose

These bits are for user-defined general purpose use, see *General Purpose Registers* from Related Links.

Related Links

[20.6.8.4. General Purpose Registers](#)

20.10.15 Tamper Control

Name: TAMPCTRL
Offset: 0x60
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access				DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0
Reset				0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access				TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0
Reset				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access							IN4ACT[1:0]	
Reset							0	0
Bit	7	6	5	4	3	2	1	0
Access		IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]
Reset	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27, 28 – DEBNCn Debounce Enable of Tamper Input INn [n=0..3]

Note: Debounce feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	Debouncing is disabled for Tamper input INn
1	Debouncing is enabled for Tamper input INn

Bits 16, 17, 18, 19, 20 – TAMLVLn Tamper Level Select of Tamper Input INn [n=0..3]

Note: Tamper Level feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	A falling edge condition will be detected on Tamper input INn.
1	A rising edge condition will be detected on Tamper input INn.

Bits 0:1, 2:3, 4:5, 6:7, 8:9 – INnACT Tamper Channel n Action [n=0..3]

These bits determine the action taken by Tamper Channel n.

Value	Name	Description
0x0	OFF	Off (Disabled)
0x1	WAKE	Wake and set Tamper flag
0x2	CAPTURE	Capture timestamp and set Tamper flag
0x3	ACTL	Compare RTC signal routed between INn and OUT pins . When a mismatch occurs, capture timestamp and set Tamper flag

20.10.16 Timestamp

Name: TIMESTAMP
Offset: 0x64
Reset: 0x0000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Count Timestamp Value

The 16-bit value of COUNT is captured by the TIMESTAMP when a tamper condition occurs.

20.10.17 Tamper ID

Name: TAMPID
Offset: 0x68
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24	
	TAMPEVT								
Access	R/W								
Reset	0								
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0
Access				R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0

Bit 31 – TAMPEVT Tamper Event Detected

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper input event has not been detected
1	A tamper input event has been detected

Bits 0, 1, 2, 3, 4 – TAMPIDn Tamper on Channel n Detected [n=0..3]

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper condition has not been detected on Channel n
1	A tamper condition has been detected on Channel n

20.10.18 Backup0

Name: BKUP0
Offset: 0x80
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
BKUP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BKUP[31:0] Backup

These bits are user-defined for general purpose use in the Backup domain.

20.11 Register Summary - Mode 2 - Clock/Calendar

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	MATCHCLR	CLKREP			MODE[1:0]	ENABLE	SWRST	
		15:8	CLOCKSYNC	GPTRST	BKTRST			PRESCALER[3:0]		
0x02	CTRLB	7:0	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
		15:8			ACTF[2:0]				DEBF[2:0]	
0x04	EVCTRL	7:0	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
		15:8	OVFEO	TAMPEREO					ALARMEOn[1:0]	
		23:16								TAMPEVEI
		31:24								
0x08	INTENCLR	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					ALARM1	ALARM0
0x0A	INTENSET	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					ALARM1	ALARM0
0x0C	INTFLAG	7:0	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
		15:8	OVF	TAMPER					ALARM1	ALARM0
0x0E	DBGCTRL	7:0								DBGRUN
0x0F	Reserved									
0x10	SYNCBUSY	7:0		ALARM1	ALARM0		CLOCK	FREQCORR	ENABLE	SWRST
		15:8	CLOCKSYNC			MASK1	MASK0			
		23:16					GP3	GP2	GP1	GP0
		31:24								
0x14	FREQCORR	7:0	SIGN				VALUE[6:0]			
0x15 ...	Reserved									
0x18	CLOCK	7:0	MINUTE[1:0]				SECOND[5:0]			
		15:8		HOUR[3:0]				MINUTE[5:2]		
		23:16	MONTH[1:0]				DAY[4:0]			HOUR[4]
		31:24			YEAR[5:0]				MONTH[3:2]	
0x1C ...	Reserved									
0x20	ALARM0	7:0	MINUTE[1:0]				SECOND[5:0]			
		15:8		HOUR[3:0]				MINUTE[5:2]		
		23:16	MONTH[1:0]				DAY[4:0]			HOUR[4]
		31:24			YEAR[5:0]				MONTH[3:2]	
0x24	MASK0	7:0						SEL[2:0]		
0x25 ...	Reserved									
0x28	ALARM1	7:0	MINUTE[1:0]				SECOND[5:0]			
		15:8		HOUR[3:0]				MINUTE[5:2]		
		23:16	MONTH[1:0]				DAY[4:0]			HOUR[4]
		31:24			YEAR[5:0]				MONTH[3:2]	
0x2C	MASK1	7:0						SEL[2:0]		
0x2D ...	Reserved									
0x40	GP0	7:0				GP[7:0]				
		15:8				GP[15:8]				
		23:16				GP[23:16]				
		31:24				GP[31:24]				
0x44	GP1	7:0			GP[7:0]					
		15:8			GP[15:8]					
		23:16			GP[23:16]					
		31:24			GP[31:24]					

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x48	GP2	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x4C	GP3	7:0					GP[7:0]			
		15:8					GP[15:8]			
		23:16					GP[23:16]			
		31:24					GP[31:24]			
0x50 ... 0x5F	Reserved									
0x60	TAMPCTRL	7:0	IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]	
		15:8							IN4ACT[1:0]	
		23:16			TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0	
		31:24			DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0	
0x64	TIMESTAMP	7:0	MINUTE[1:0]				SECOND[5:0]			
		15:8		HOUR[3:0]				MINUTE[5:2]		
		23:16	MONTH[1:0]			DAY[4:0]			HOUR[4]	
		31:24		YEAR[5:0]				MONTH[3:2]		
0x68	TAMPID	7:0			TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0	
		15:8								
		23:16								
		31:24	TAMPEVT							
0x6C ... 0x7F	Reserved									
0x80	BKUP0	7:0			BKUP[7:0]					
		15:8			BKUP[15:8]					
		23:16			BKUP[23:16]					
		31:24			BKUP[31:24]					

20.12 Register Description - Mode 2 - Clock/Calendar

This Register Description section is valid if the RTC is in Clock/Calendar mode (CTRLA.MODE=2).

20.12.1 Control A in Clock/Calendar mode (CTRLA.MODE=2)

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CLOCKSYNC	GPTRST	BKTRST					
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MATCHCLR	CLKREP				MODE[1:0]	ENABLE	SWRST
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit 15 – CLOCKSYNC CLOCK Read Synchronization Enable

The CLOCK register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the CLOCK register.

This bit is not enable-protected.

Value	Description
0	CLOCK read synchronization is disabled
1	CLOCK read synchronization is enabled

Bit 14 – GPTRST GP Registers Reset On Tamper Enable

Only GP registers enabled by the CTRLB.GPnEN bits are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Bit 13 – BKTRST BKUP Registers Reset On Tamper Enable

All BKUPn registers are affected. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Value	Description
0	BKUPn registers will not reset when a tamper condition occurs.
1	BKUPn registers will reset when a tamper condition occurs.

Bits 11:8 – PRESCALER[3:0] Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0xA	DIV512	CLK_RTC_CNT = GCLK_RTC/512
0xB	DIV1024	CLK_RTC_CNT = GCLK_RTC/1024
0xC–0xF	-	Reserved

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Bit 7 – MATCHCLR Clear on Match

This bit is valid only in Mode 0 (COUNT32) and Mode 2 (CLOCK). This bit can be written only when the peripheral is disabled. This bit is not synchronized.

Value	Description
0	The counter is not cleared on a Compare/Alarm 0 match
1	The counter is cleared on a Compare/Alarm 0 match

Bit 6 – CLKREP Clock Representation

This bit is valid only in Mode 2 and determines how the hours are represented in the Clock Value (CLOCK) register. This bit can be written only when the peripheral is disabled. This bit is not synchronized.

Value	Description
0	24 Hour
1	12 Hour (AM/PM)

Bits 3:2 – MODE[1:0] Operating Mode

This field defines the operating mode of the RTC. This bit is not synchronized.

Value	Name	Description
0x0	COUNT32	Mode 0: 32-bit counter
0x1	COUNT16	Mode 1: 16-bit counter
0x2	CLOCK	Mode 2: Clock/calendar
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the RTC, except DBGCTRL, to their initial state, and the RTC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST will be cleared when the reset is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is not reset operation ongoing
1	The reset operation is ongoing

20.12.2 Control B in Clock/Calendar mode (CTRLA.MODE=2)

Name: CTRLB
Offset: 0x2
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	ACTF[2:0]					DEBF[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
Access	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
Reset	0	0	0	0			0	0

Bits 14:12 – ACTF[2:0] Active Layer Frequency

These bits define the prescaling factor for the RTC clock output (OUT) used during active layer protection in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_OUT = CLK_RTC / 2
0x1	DIV4	CLK_RTC_OUT = CLK_RTC / 4
0x2	DIV8	CLK_RTC_OUT = CLK_RTC / 8
0x3	DIV16	CLK_RTC_OUT = CLK_RTC / 16
0x4	DIV32	CLK_RTC_OUT = CLK_RTC / 32
0x5	DIV64	CLK_RTC_OUT = CLK_RTC / 64
0x6	DIV128	CLK_RTC_OUT = CLK_RTC / 128
0x7	DIV256	CLK_RTC_OUT = CLK_RTC / 256

Bits 10:8 – DEBF[2:0] Debounce Frequency

These bits define the prescaling factor for the input debouncers in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_DEB = CLK_RTC / 2
0x1	DIV4	CLK_RTC_DEB = CLK_RTC / 4
0x2	DIV8	CLK_RTC_DEB = CLK_RTC / 8
0x3	DIV16	CLK_RTC_DEB = CLK_RTC / 16
0x4	DIV32	CLK_RTC_DEB = CLK_RTC / 32
0x5	DIV64	CLK_RTC_DEB = CLK_RTC / 64
0x6	DIV128	CLK_RTC_DEB = CLK_RTC / 128
0x7	DIV256	CLK_RTC_DEB = CLK_RTC / 256

Bit 7 – DMAEN DMA Enable

The RTC can trigger a DMA request when the timestamp is ready in the TIMESTAMP register.

Value	Description
0	Tamper DMA request is disabled. Reading TIMESTAMP has no effect on INTFLAG.TAMPER.
1	Tamper DMA request is enabled. Reading TIMESTAMP will clear INTFLAG.TAMPER.

Bit 6 – RTCOUT RTC Out Enable

Value	Description
0	The RTC active layer output is disabled.
1	The RTC active layer output is enabled.

Bit 5 – DEBASYNC Debouncer Asynchronous Enable

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Value	Description
0	The tamper input debouncers operate synchronously.
1	The tamper input debouncers operate asynchronously.

Bit 4 – DEBMAJ Debouncer Majority Enable

Value	Description
0	The tamper input debouncers match three equal values.
1	The tamper input debouncers match majority two of three values.

Bit 1 – GP2EN General Purpose 2 Enable

Value	Description
0	COMP1 compare function enabled. GP2/GP3 disabled.
1	COMP1 compare function disabled. GP2/GP3 enabled.

Bit 0 – GP0EN General Purpose 0 Enable

Value	Description
0	COMP0 compare function enabled. GP0 disabled.
1	COMP0 compare function disabled. GP0 enabled.

20.12.3 Event Control in Clock/Calendar mode (CTRLA.MODE=2)

Name: EVCTRL
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24	
Access									
Reset									
Bit	23	22	21	20	19	18	17	16	TAMPEVEI
Access									R/W
Reset									0
Bit	15	14	13	12	11	10	9	8	ALARMEOn[1:0]
Access	R/W	R/W					R/W	R/W	
Reset	0	0					0	0	
Bit	7	6	5	4	3	2	1	0	
Access	R/W								
Reset	0	0	0	0	0	0	0	0	

Bit 16 – TAMPEVEI Tamper Event Input Enable

Value	Description
0	Tamper event input is disabled, and incoming events will be ignored.
1	Tamper event input is enabled, and all incoming events will capture the CLOCK value.

Bit 15 – OVFE0 Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 14 – TAMPEROE Tamper Event Output Enable

Value	Description
0	Tamper event output is disabled, and will not be generated
1	Tamper event output is enabled, and will be generated for every tamper input.

Bits 9:8 – ALARMEOn[1:0] Alarm n Event Output Enable [n = 1..0]

Value	Description
0	Alarm n event is disabled and will not be generated.
1	Alarm n event is enabled and will be generated for every compare match.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PEREOOn Periodic Interval n Event Output Enable [n = 7..0]

Value	Description
0	Periodic Interval n event is disabled and will not be generated.
1	Periodic Interval n event is enabled and will be generated.

20.12.4 Interrupt Enable Clear in Clock/Calendar mode (CTRLA.MODE=2)

Name: INTENCLR
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					ALARM1	ALARM0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Bits 8, 9 – ALARMn Alarm n Interrupt Enable [n = 1..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Alarm n Interrupt Enable bit, which disables the Alarm n interrupt.

Value	Description
0	The Alarm n interrupt is disabled.
1	The Alarm n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Periodic Interval n Interrupt Enable bit, which disables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.12.5 Interrupt Enable Set in Clock/Calendar mode (CTRLA.MODE=2)

Name: INTENSET
Offset: 0x0A
Reset: 0x0000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					ALARM1	ALARM0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Bit 14 – TAMPER Tamper Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Tamper Interrupt Enable bit, which enables the Tamper interrupt.

Value	Description
0	The Tamper interrupt is disabled.
1	The Tamper interrupt is enabled.

Bits 8, 9 – ALARMn Alarm n Interrupt Enable [n = 1..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Alarm n Interrupt Enable bit, which enables the Alarm n interrupt.

Value	Description
0	The Alarm n interrupt is disabled.
1	The Alarm n interrupt is enabled.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n Interrupt Enable [n = 7..0]

Writing a '0' to this bit has no effect. Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

Value	Description
0	Periodic Interval n interrupt is disabled.
1	Periodic Interval n interrupt is enabled.

20.12.6 Interrupt Flag Status and Clear in Clock/Calendar mode (CTRLA.MODE=2)

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
	OVF	TAMPER					ALARM1	ALARM0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF Overflow

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

Bit 14 – TAMPER Tamper

This flag is set after a tamper condition occurs, and an interrupt request will be generated if INTENCLR.TAMPER/INTENSET.TAMPER is '1'. Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the Tamper interrupt flag.

Bits 8, 9 – ALARMn Alarm n [n = 1..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after a match with the compare condition, and an interrupt request will be generated if INTENCLR/SET.ALARMn is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Alarm n interrupt flag.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PERn Periodic Interval n [n = 7..0]

This flag is cleared by writing a '1' to the flag.

This flag is set on the 0-to-1 transition of prescaler bit [n+2], and an interrupt request will be generated if INTENCLR/SET.PERx is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Periodic Interval n interrupt flag.

20.12.7 Debug Control

Name: DBGCTRL
Offset: 0x0E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGRUN 0

Bit 0 – DBGRUN Debug Run

This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The RTC is halted when the CPU is halted by an external debugger.
1	The RTC continues normal operation when the CPU is halted by an external debugger.

20.12.8 Synchronization Busy in Clock/Calendar mode (CTRLA.MODE=2)

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					GP3	GP2	GP1	GP0
Reset					R	R	R	R
Bit	15	14	13	12	11	10	9	8
Access	R			R	R			
Reset	0			0	0			
Bit	7	6	5	4	3	2	1	0
Access		ALARM1	ALARM0		CLOCK	FREQCORR	ENABLE	SWRST
Reset		R	R		R	R	R	R
Reset	0	0	0		0	0	0	0

Bits 16, 17, 18, 19 – GPn General Purpose n Synchronization Busy Status

Value	Description
0	Write synchronization for GPn register is complete.
1	Write synchronization for GPn register is ongoing.

Bit 15 – CLOCKSYNC Clock Read Sync Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.CLOCKSYNC bit is complete.
1	Write synchronization for CTRLA.CLOCKSYNC bit is ongoing.

Bits 11, 12 – MASKn Mask n Synchronization Busy Status [n = 1..0]

Value	Description
0	Write synchronization for MASKx register is complete.
1	Write synchronization for MASKx register is ongoing.

Bits 5, 6 – ALARMn Alarm n Synchronization Busy Status [n = 1..0]

Value	Description
0	Write synchronization for ALARMx register is complete.
1	Write synchronization for ALARMx register is ongoing.

Bit 3 – CLOCK Clock Register Synchronization Busy Status

Value	Description
0	Read/write synchronization for CLOCK register is complete.
1	Read/write synchronization for CLOCK register is ongoing.

Bit 2 – FREQCORR Frequency Correction Synchronization Busy Status

Value	Description
0	Write synchronization for FREQCORR register is complete.

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Value	Description
1	Write synchronization for FREQCORR register is ongoing.

Bit 1 – ENABLE Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

Bit 0 – SWRST Software Reset Synchronization Busy Status

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

20.12.9 Frequency Correction

Name: FREQCORR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0	
	SIGN	VALUE[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Bit 7 – SIGN Correction Sign

Value	Description
0	The correction value is positive, i.e., frequency will be decreased.
1	The correction value is negative, i.e., frequency will be increased.

Bits 6:0 – VALUE[6:0] Correction Value

These bits define the amount of correction applied to the RTC prescaler.

Value	Description
0	Correction is disabled and the RTC frequency is unchanged.
1 – 127	The RTC frequency is adjusted according to the value.

20.12.10 Clock Value in Clock/Calendar mode (CTRLA.MODE=2)

Name: CLOCK
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	YEAR[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
	MONTH[1:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
	DAY[4:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
	HOUR[3:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
	MINUTE[5:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
	SECOND[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:26 – YEAR[5:0] Year

The year offset with respect to the reference year (defined in software).
The year is considered a leap year if YEAR[1:0] is zero.

Bits 25:22 – MONTH[3:0] Month

- 1 – January
- 2 – February
- ...
- 12 – December

Bits 21:17 – DAY[4:0] Day

Day starts at 1 and ends at 28, 29, 30, or 31, depending on the month and year.

Bits 16:12 – HOUR[4:0] Hour

When CTRLA.CLKREP=0, the Hour bit group is in 24-hour format, with values 0-23. When CTRLA.CLKREP=1, HOUR[3:0] has values 1-12, and HOUR[4] represents AM (0) or PM (1).

Bits 11:6 – MINUTE[5:0] Minute

0 – 59

Bits 5:0 – SECOND[5:0] Second

0 – 59

20.12.11 Alarm n Value in Clock/Calendar mode (CTRLA.MODE=2)

Name: ALARM
Offset: 0x20 + n*0x08 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized

The 32-bit value of ALARM_n is continuously compared with the 32-bit CLOCK value, based on the masking set by MASK_n.SEL. When a match occurs, the Alarm n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.ALARM_n) is set on the next counter cycle, and the counter is cleared if CTRLA.MATCHCLR is '1'.

Bit	31	30	29	28	27	26	25	24
YEAR[5:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
MONTH[1:0]								
Bit	23	22	21	20	19	18	17	16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DAY[4:0]								
Bit	15	14	13	12	11	10	9	8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
HOUR[3:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0
MINUTE[5:0]								
Bit	11	10	9	8	7	6	5	4
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:26 – YEAR[5:0] Year

The alarm year. Years are only matched if MASK_n.SEL is 6

Bits 25:22 – MONTH[3:0] Month

The alarm month. Months are matched only if MASK_n.SEL is greater than 4.

Bits 21:17 – DAY[4:0] Day

The alarm day. Days are matched only if MASK_n.SEL is greater than 3.

Bits 16:12 – HOUR[4:0] Hour

The alarm hour. Hours are matched only if MASK_n.SEL is greater than 2.

Bits 11:6 – MINUTE[5:0] Minute

The alarm minute. Minutes are matched only if MASK_n.SEL is greater than 1.

Bits 5:0 – SECOND[5:0] Second

The alarm second. Seconds are matched only if MASK_n.SEL is greater than 0.

20.12.12 Alarm n Mask in Clock/Calendar mode (CTRLA.MODE=2)

Name: MASK
Offset: 0x24 + n*0x08 [n=0..1]
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	SEL[2:0]							
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – SEL[2:0] Alarm Mask Selection

These bits define which bit groups of Alarm n are valid.

Value	Name	Description
0x0	OFF	Alarm Disabled
0x1	SS	Match seconds only
0x2	MMSS	Match seconds and minutes only
0x3	HHMMSS	Match seconds, minutes, and hours only
0x4	DDHHMMSS	Match seconds, minutes, hours, and days only
0x5	MMDDHHMMSS	Match seconds, minutes, hours, days, and months only
0x6	YYMMDDHHMMSS	Match seconds, minutes, hours, days, months, and years
0x7	-	Reserved

20.12.13 General Purpose n

Name: GPn
Offset: 0x40 + n*0x04 [n=0..3]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
GP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GP[31:0] General Purpose

These bits are for user-defined general purpose use, see *General Purpose Registers* from Related Links.

Related Links

[20.6.8.4. General Purpose Registers](#)

20.12.14 Tamper Control

Name: TAMPCTRL
Offset: 0x60
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access				DEBNC4	DEBNC3	DEBNC2	DEBNC1	DEBNC0
Reset				0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access				TAMLVL4	TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0
Reset				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access							IN4ACT[1:0]	
Reset							0	0
Bit	7	6	5	4	3	2	1	0
Access		IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]
Reset	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27, 28 – DEBNCn Debounce Enable of Tamper Input INn [n=0..3]

Note: Debounce feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	Debouncing is disabled for Tamper input INn
1	Debouncing is enabled for Tamper input INn

Bits 16, 17, 18, 19, 20 – TAMLVLn Tamper Level Select of Tamper Input INn [n=0..3]

Note: Tamper Level feature does not apply to the Active Layer Protection mode (TAMPCTRL.INACT = ACTL).

Value	Description
0	A falling edge condition will be detected on Tamper input INn.
1	A rising edge condition will be detected on Tamper input INn.

Bits 0:1, 2:3, 4:5, 6:7, 8:9 – INnACT Tamper Channel n Action [n=0..3]

These bits determine the action taken by Tamper Channel n.

Value	Name	Description
0x0	OFF	Off (Disabled)
0x1	WAKE	Wake and set Tamper flag
0x2	CAPTURE	Capture timestamp and set Tamper flag
0x3	ACTL	Compare RTC signal routed between INn and OUT pins . When a mismatch occurs, capture timestamp and set Tamper flag

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20.12.15 Timestamp Value

Name: TIMESTAMP
Offset: 0x64
Reset: 0
Property: -

Bit	31	30	29	28	27	26	25	24
	YEAR[5:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
	MONTH[1:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
	DAY[4:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
	HOUR[3:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
	MINUTE[5:2]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
	SECOND[5:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:26 – YEAR[5:0] Year

The year value is captured by the TIMESTAMP when a tamper condition occurs.

Bits 25:22 – MONTH[3:0] Month

The month value is captured by the TIMESTAMP when a tamper condition occurs.

Bits 21:17 – DAY[4:0] Day

The day value is captured by the TIMESTAMP when a tamper condition occurs.

Bits 16:12 – HOUR[4:0] Hour

The hour value is captured by the TIMESTAMP when a tamper condition occurs.

Bits 11:6 – MINUTE[5:0] Minute

The minute value is captured by the TIMESTAMP when a tamper condition occurs.

Bits 5:0 – SECOND[5:0] Second

The second value is captured by the TIMESTAMP when a tamper condition occurs.

20.12.16 Tamper ID

Name: TAMPID
Offset: 0x68
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24	
	TAMPEVT								
Access	R/W								
Reset	0								
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	TAMPID4	TAMPID3	TAMPID2	TAMPID1	TAMPID0
Access				R/W	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0	0

Bit 31 – TAMPEVT Tamper Event Detected

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper input event has not been detected
1	A tamper input event has been detected

Bits 0, 1, 2, 3, 4 – TAMPIDn Tamper on Channel n Detected [n=0..3]

Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper condition has not been detected on Channel n
1	A tamper condition has been detected on Channel n

20.12.17 Backup0

Name: BKUP0
Offset: 0x80
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
BKUP[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BKUP[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BKUP[31:0] Backup

These bits are user-defined for general purpose use in the Backup domain.

21. Direct Memory Access Controller (DMAC)

21.1 Overview

The Direct Memory Access Controller (DMAC) contains both a Direct Memory Access engine and a Cyclic Redundancy Check (CRC) engine. The DMAC can transfer data between memories and peripherals, and thus off-load these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. With access to all peripherals, the DMAC can handle automatic transfer of data between communication modules.

The DMA part of the DMAC has several DMA channels which all can receive different types of transfer triggers to generate transfer requests from the DMA channels to the arbiter, see *DMAC Block Diagram* in the *Block Diagram* from Related Links. The arbiter will grant one DMA channel at a time to act as the active channel. When an active channel has been granted, the fetch engine of the DMAC will fetch a transfer descriptor from the SRAM and store it in the internal memory of the active channel, which will execute the data transmission.

An ongoing data transfer of an active channel can be interrupted by a higher prioritized DMA channel. The DMAC will write back the updated transfer descriptor from the internal memory of the *active* channel to SRAM, and grant the higher prioritized channel to start transfer as the new active channel. Once a DMA channel is done with its transfer, interrupts and events can be generated optionally.

The DMAC has four bus interfaces:

- The *data transfer bus* is used for performing the actual DMA transfer.
- The *AHB/APB Bridge bus* is used when writing and reading the I/O registers of the DMAC.
- The *descriptor fetch bus* is used by the fetch engine to fetch transfer descriptors before data transfer can be started or continued.
- The *write-back bus* is used to write the transfer descriptor back to SRAM.

All buses are AHB Master interfaces but the AHB/APB Bridge bus, which is an APB Slave interface.

Burst transfer options, buffered active channel to pre-fetch descriptors and advance quality of service features ensure low-latency transfers for high-speed peripherals or high-speed operations.

The CRC engine can be used by software to detect an accidental error in the transferred data and to take corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Related Links

[21.3. Block Diagram](#)

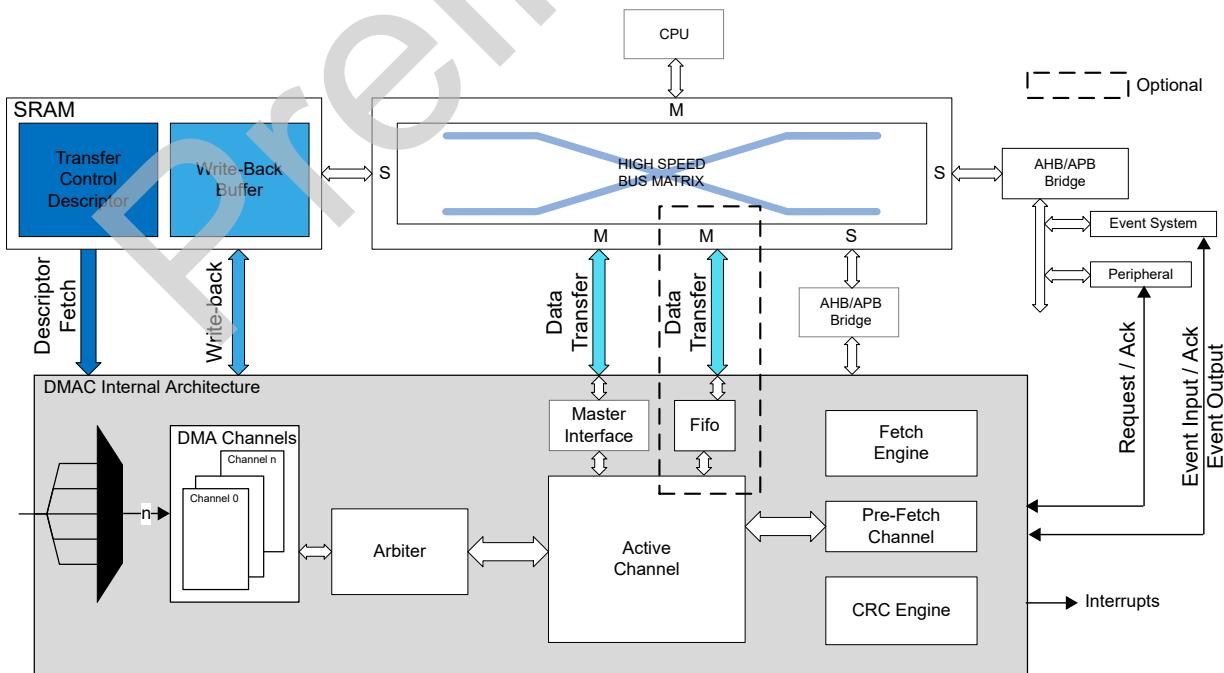
21.2 Features

- Data transfer from:
 - Peripheral to peripheral
 - Peripheral to memory
 - Memory to peripheral
 - Memory to memory
- Transfer trigger sources
 - Software
 - Events from Event System
 - Dedicated requests from peripherals
- SRAM based transfer descriptors
 - Single transfer using one descriptor
 - Multi-buffer or circular buffer modes by linking multiple descriptors
- Up to 16 channels
 - Enable 16 independent transfers

- Automatic descriptor fetch for each channel
- Suspend/resume operation support for each channel
- Flexible arbitration scheme
 - 4 configurable priority levels for each channel
 - Fixed or round-robin priority scheme within each priority level
- From 1 to 256KB data transfer in a single block transfer
- Multiple addressing modes
 - Static
 - Configurable increment scheme
- Optional interrupt generation
 - On block transfer complete
 - On error detection
 - On channel suspend
- 8 event inputs
 - One event input for each of the 8 least significant DMA channels
 - Can be selected to trigger normal transfers, periodic transfers or conditional transfers
 - Can be selected to suspend or resume channel operation
- 4 event outputs
 - One output event for each of the 4 least significant DMA channels
 - Selectable generation on AHB, block, or transaction transfer complete
- Error management supported by write-back function
 - Dedicated Write-Back memory section for each channel to store ongoing descriptor transfer
- CRC polynomial software selectable to
 - CRC-16 (CRC-CCITT)
 - CRC-32 (IEEE® 802.3)

21.3 Block Diagram

Figure 21-1. DMAC Block Diagram



21.4 Signal Description

Not applicable.

21.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

21.5.1 I/O Lines

Not applicable.

21.5.2 Power Management

The DMAC will continue to operate in any Sleep mode where the selected source clock is running. The DMAC's interrupts can be used to wake-up the device from Sleep modes. Events connected to the event system can trigger other operations in the system without exiting Sleep modes. On hardware or software Reset, all registers are set to their Reset value.

21.5.3 DMA

Not applicable.

21.5.4 Interrupts

The interrupt request line is connected to the interrupt controller. Using the DMAC interrupt requires the interrupt controller to be configured first.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

21.5.5 Events

The events are connected to the event system.

21.5.6 Debug Operation

When the CPU is halted in Debug mode the DMAC will halt normal operation. The DMAC can be forced to continue operation during debugging. See [DBGCTRL](#) from Related Links.

Related Links

[21.8.6. DBGCTRL](#)

21.5.7 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Pending register (INTPEND)
- Channel Interrupt Flag Status and Clear register (CHINTFLAG)

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

PAC write protection does not apply to accesses through an external debugger.

21.5.8 Analog Connections

Not applicable.

21.6 Functional Description

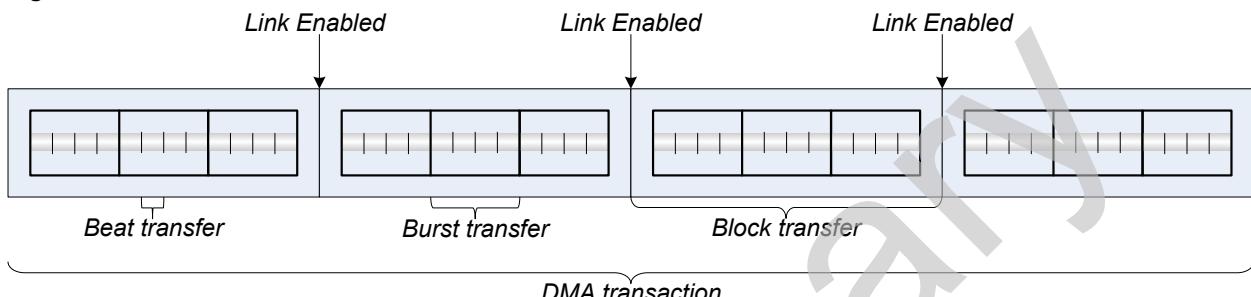
21.6.1 Principle of Operation

The DMAC consists of a DMA module and a CRC module.

21.6.1.1 DMA

The DMAC can transfer data between memories and peripherals without interaction from the CPU. The data transferred by the DMAC are called transactions, and these transactions can be split into smaller data transfers. The following figure shows the relationship between the different transfer sizes:

Figure 21-2. DMA Transfer Sizes



- Beat transfer: The size of one data transfer bus access, and the size is selected by writing the Beat Size bit group in the Block Transfer Control register (BTCTRL.BEATSIZE)
- Block transfer: The amount of data one transfer descriptor can transfer, and the amount can range from 1 to 64k beats. A block transfer can be interrupted.
- Transaction: The DMAC can link several transfer descriptors by having the first descriptor pointing to the second and so forth, as shown in the figure above. A DMA transaction is the complete transfer of all blocks within a linked list.

A transfer descriptor describes how a block transfer should be carried out by the DMAC, and it must remain in SRAM, see *Transfer Descriptors* from Related Links.

The figure above shows several block transfers linked together, which are called linked descriptors, see *Linked Descriptors* from Related Links.

A DMA transfer is initiated by an incoming transfer trigger on one of the DMA channels. This trigger can be configured to be either a software trigger, an event trigger, or one of the dedicated peripheral triggers. The transfer trigger will result in a DMA transfer request from the specific channel to the arbiter. If there are several DMA channels with pending transfer requests, the arbiter chooses which channel is granted access to become the active channel. The DMA channel granted access as the active channel will carry out the transaction as configured in the transfer descriptor. A current transaction can be interrupted by a higher prioritized channel, but will resume the block transfer when the according DMA channel is granted access as the active channel again.

For each beat transfer, an optional output event can be generated. For each block transfer, optional interrupts and an optional output event can be generated. When a transaction is completed, depending on the configuration, the DMA channel will either be suspended or disabled.

Related Links

[21.6.2.3. Transfer Descriptors](#)

[21.6.3.1. Linked Descriptors](#)

21.6.1.2 CRC

The internal CRC engine supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). It can be used on a selectable DMA channel, or on the I/O interface. See *CRC Operation* from Related Links.

Related Links

[21.6.3.8. CRC Operation](#)

21.6.2 Basic Operation

21.6.2.1 Initialization

DMAC Initialization

Before DMAC is enabled, it must be configured as defined below:

- The SRAM address of where the descriptor memory section is located must be written to the Description Base Address (BASEADDR) register.
- The SRAM address of where the write-back section should be located must be written to the Write-Back Memory Base Address (WRBADDR) register.
- Priority level x of the arbiter can be enabled by setting the Priority Level x Enable bit in the Control register (CTRL.LVLEN x =1)

DMA Channel Initialization

Before a DMA channel is enabled, the DMA channel and the corresponding first transfer descriptor must be configured, as defined below:

- DMA Channel Configuration:
 - The channel number of the DMA channel to configure must be written to the Channel Control A (CHCTRLA) register.
 - Trigger action must be selected by writing the Trigger Action bit field in the Channel Control A (CHCTRLA.TRIGACT) register.
 - Trigger source must be selected by writing the Trigger Source bit field in the Channel Control A (CHCTRLA.TRIGSRC) register.
- Transfer Descriptor
 - The size of each access of the data transfer bus must be selected by writing the Beat Size bit group in the Block Transfer Control (BTCTRL.BEATSIZE) register.
 - The transfer descriptor must be made valid by writing a one to the Valid bit in the Block Transfer Control (BTCTRL.VALID) register.
 - Number of beats in the block transfer must be selected by writing the Block Transfer Count (BTCNT) register.
 - Source address for the block transfer must be selected by writing the Block Transfer Source Address (SRCADDR) register.
 - Destination address for the block transfer must be selected by writing the Block Transfer Destination Address (DSTADDR) register.

CRC Calculation

If CRC calculation is needed, the CRC engine must be configured before it is enabled, as described below:

- The CRC input source must be selected by writing the CRC Input Source bit group in the CRC Control (CRCCTRL.CRCSRC) register.
- The type of CRC calculation must be selected by writing the CRC Polynomial Type bit group in the CRC Control (CRCCTRL.CRPCPOLY) register.
- If I/O is selected as input source, the beat size must be selected by writing the CRC Beat Size bit group in the CRC Control (CRCCTRL.CRCBEATSIZE) register.

Register Properties

The following DMAC registers are enable-protected, that is, they can only be written when the DMAC is disabled (CTRL.DMAENABLE=0):

- The Descriptor Base Memory Address (BASEADDR) register
- The Write-Back Memory Base Address (WRBADDR) register

The following DMAC bit is enable-protected, that is, it can only be written when the DMAC and CRC are disabled (CTRL.DMAENABLE=0 and CRCCTRL.CRCSRC=0):

- The Software Reset bit in the Control (CTRL.SWRST) register

The following DMA channel bit is enable-protected, meaning that it can only be written when the corresponding DMA channel is disabled:

- The Channel Software Reset bit in the Channel Control A (CHCTRLA.SWRST) register

The following CRC registers are enable-protected, that is, they can only be written when the CRC is disabled (CRCCTRL.CRCSRC=0):

- The CRC Control (CRCCTRL) register
- CRC Checksum (CRCCHKSUM) register

Enable-protection is denoted by the 'Enable-Protected' property in the register description.

21.6.2.2 Enabling, Disabling, and Resetting

The DMAC is enabled by writing the DMA Enable bit in the Control (CTRL.DMAENABLE) register to '1'. The DMAC is disabled by writing a '0' to the CTRL.DMAENABLE register.

A DMA channel is enabled by writing the Enable bit in the Channel Control A register (CHCTRLA.ENABLE) to '1', after the corresponding channel ID to the channel is configured. A DMA channel is disabled by writing a '0' to CHCTRLAn.ENABLE.

The CRC is enabled by writing a value to the CRC Source bits in the Control register (CRCCTRL.CRCSRC). The CRC is disabled by writing a '0' to CRCCTRL.CRCSRC.

The DMAC is reset by writing a '1' to the Software Reset bit in the Control register (CTRL.SWRST) while the DMAC and CRC are disabled. All registers in the DMAC except DBGCTRL will be reset to their initial state.

A DMA channel is reset by writing a '1' to the Software Reset bit in the Channel Control A register (CHCTRLAn.SWRST), after the corresponding channel is configured. The channel registers will be reset to their initial state. The corresponding DMA channel must be disabled in order for the Reset to take effect.

21.6.2.3 Transfer Descriptors

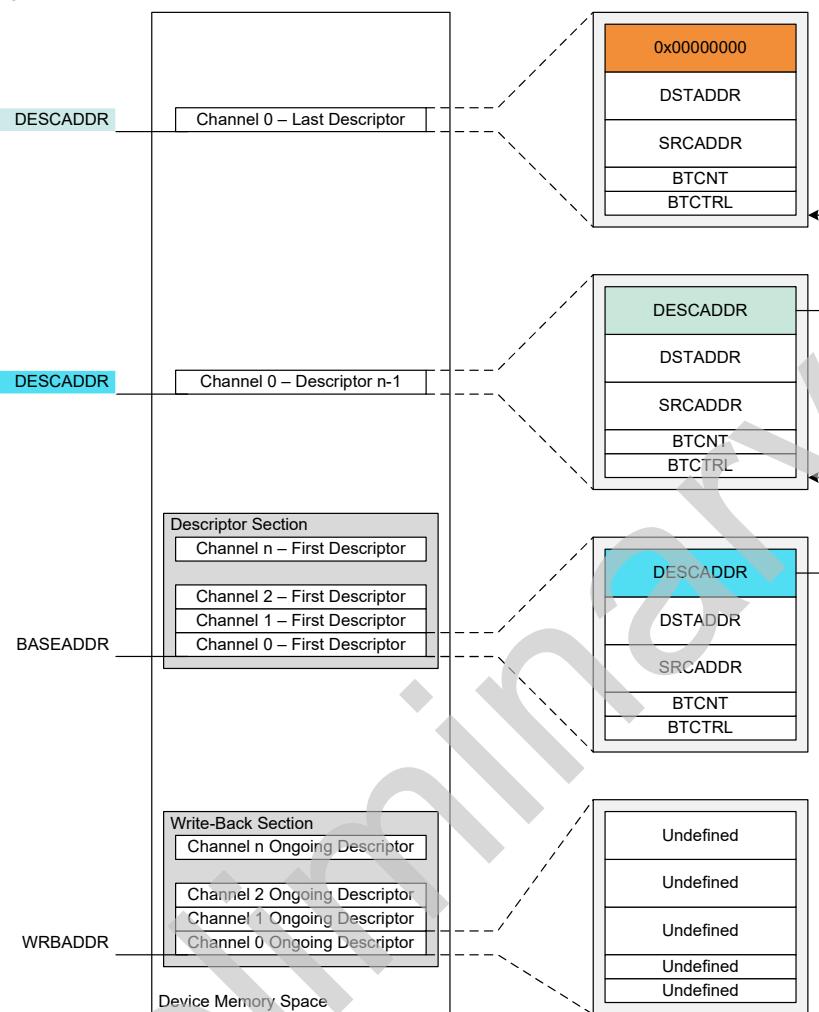
The transfer descriptors, together with the channel configurations, decide how a block transfer should be executed. Before a DMA channel is enabled (CHCTRLA.ENABLE is written to one) and receives a transfer trigger, its first transfer descriptor must be initialized and valid (BTCTRL.VALID). The first transfer descriptor describes the first block transfer of a transaction.

All transfer descriptors must reside in SRAM. The addresses stored in the Descriptor Memory Section Base Address (BASEADDR) and Write-Back Memory Section Base Address (WRBADDR) registers tell the DMAC where to find the descriptor memory section and the write-back memory section.

The descriptor memory section is where the DMAC expects to find the first transfer descriptors for all DMA channels. As BASEADDR points only to the first transfer descriptor of channel '0' (see the following figure). All first transfer descriptors must be stored in a contiguous memory section, where the transfer descriptors must be ordered according to their channel number, see *Linked Descriptors* from Related Links.

The write-back memory section is where the DMAC stores the transfer descriptors for the ongoing block transfers. WRBADDR points to the ongoing transfer descriptor of channel '0'. All ongoing transfer descriptors are stored in a contiguous memory section where the transfer descriptors are ordered according to their channel number. The figure below shows an example of linked descriptors on DMA channel '0', see *Linked Descriptors* from Related Links.

Figure 21-3. Memory Sections



The size of the descriptor and write-back memory sections are dependent on the number of the most significant enabled DMA channel m , as shown below:

$$\text{Size} = 128\text{bits} \cdot (m + 1)$$

For memory optimization, it is recommended to use the less significant DMA channels, if not all channels are required.

The descriptor and write-back memory sections can either be two separate memory sections, or they can share a memory section ($\text{BASEADDR}=\text{WRBADDR}$). The benefit of having them in two separate sections, is that the same transaction for a channel can be repeated without having to modify the first transfer descriptor.

Related Links

[21.6.3.1. Linked Descriptors](#)

21.6.2.4 Arbitration

If a DMA channel is enabled and not suspended when it receives a transfer trigger, it will send a transfer request to the arbiter. When the arbiter receives the transfer request it will include the DMA channel in the queue of channels having pending transfers, and the corresponding Pending Channel x bit in the Pending Channels registers (PENDCH.PENDCH x) will be set. Depending on the arbitration scheme, the arbiter will choose which DMA channel will be the next active channel. The next transfer descriptor will be fetched from SRAM memory and stored internally in the Pre-Fetch Channel. The active channel is the DMA channel being granted access to perform its next burst transfer. When the Active Channel has completed a burst transfer, the descriptor stored in the Pre-Fetch Channel is transferred to the Active Channel and a new burst will take place.

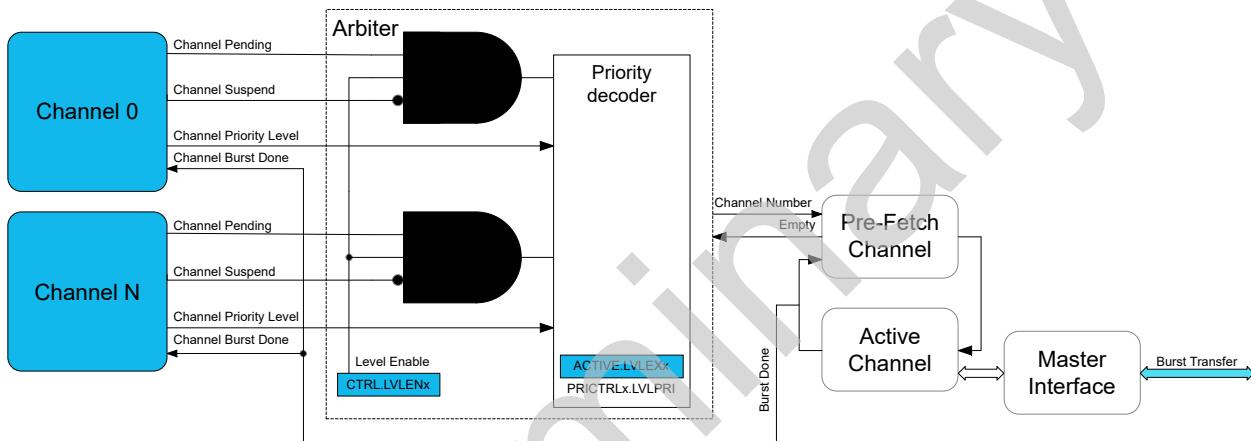
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When the descriptor stored in the Pre-Fetch Channel is transferred to the Active Channel, the corresponding PENDCH.PENDCHx will be cleared. In the same way, depending on trigger action settings and if the upcoming burst transfer is the first for the transfer request or not, the corresponding Busy Channel x bit in the Busy Channels register (BUSYCH.BUSYCHx), will either be set or remain '1'. When the channel has performed its granted burst transfer(s) it will be either fed into the queue of channels with pending transfers, set to be waiting for a new transfer trigger, suspended, or disabled. This depends on the channel and block transfer configuration. If the DMA channel is set to wait for a new transfer trigger, suspended or disabled, the corresponding BUSYCH.BUSYCHx will be cleared.

If a DMA channel is suspended while it has a pending transfer, it will be removed from the queue of pending channels, but the corresponding PENDCH.PENDCHx will remain set. The status will also be indicated in CHINTFLAGn.SUSP. When the same DMA channel is resumed, it will be added to the queue of pending channels again.

If a DMA channel gets disabled (CHCTRLA.ENABLE=0) while it has a pending transfer, it will be removed from the queue of pending channels, and the corresponding PENDCH.PENDCHx will be cleared.

Figure 21-4. Arbiter Overview



Priority Levels

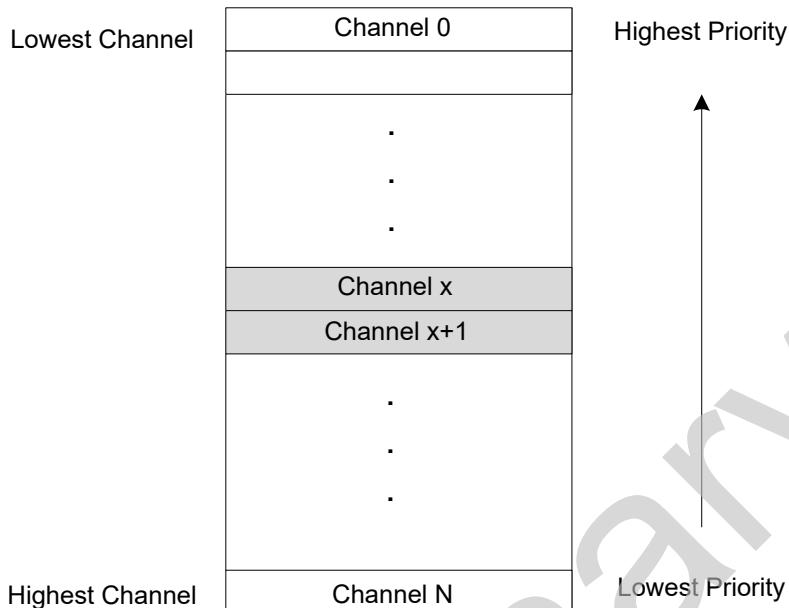
When a channel level is pending or the channel is transferring data, the corresponding Level Executing bit is set in the Active Channel and Levels register (ACTIVE.LVLEXx).

Each DMA channel supports up to 4-level priority scheme. The number of supported priority levels will differ from one device family to another.

The priority level for a channel is configured by writing to the Channel Arbitration Level bit group in the Channel Priority Level register (CHPRILVL.PRILVL). As long as all priority levels are enabled, a channel with a higher priority level number will have priority over a channel with a lower priority level number. A priority level is enabled by writing the Priority Level x Enable bit in the Control register (CTRL.LVLENx) to '1', for the corresponding level.

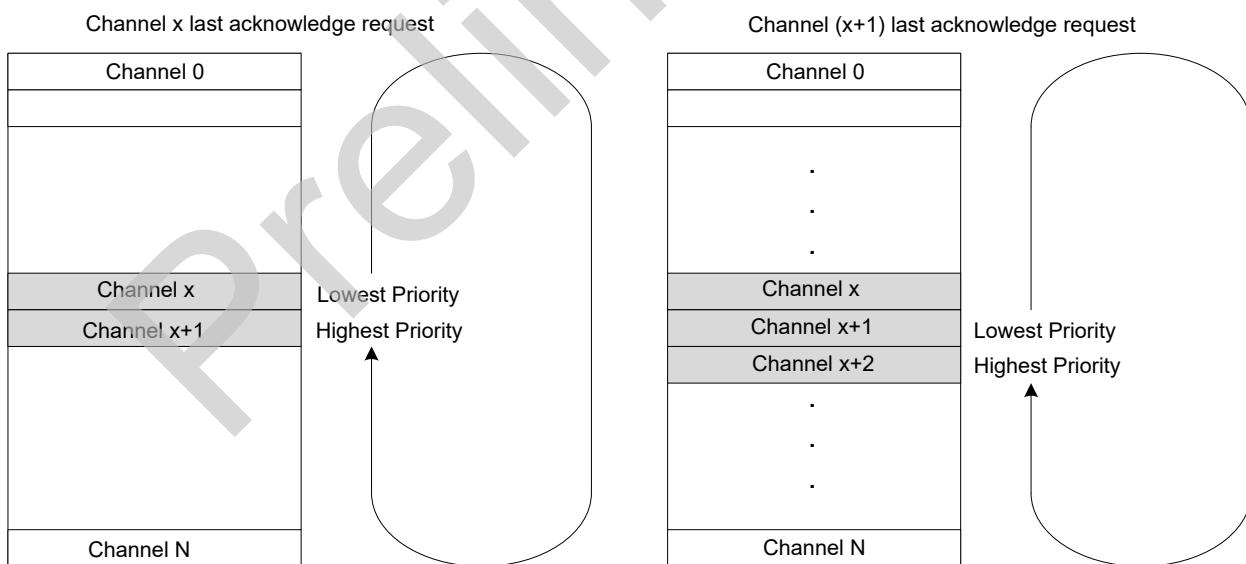
Within each priority level, the DMAC's arbiter can be configured to prioritize statically or dynamically. For the arbiter to perform static arbitration within a priority level, the Level X Round-Robin Scheduling Enable bit in the Priority Control x register (PRICTRL0.RRLVLENx) has to be written to '0'. When static arbitration is enabled (PRICTRL0.RRLVLENx is '0'), the arbiter will prioritize a low channel number over a high channel number as shown in the following figure. When using the static scheme, there is a risk of high channel numbers never being granted access as the active channel. This can be avoided using a dynamic arbitration scheme.

Figure 21-5. Static Priority Scheduling



The dynamic arbitration scheme in the DMAC is round-robin. Round-robin arbitration is enabled by writing PRICTRL0.RRLVLEN to '1', for a given priority level x . With the round-robin scheme, the channel number of the last channel being granted access will have the lowest priority the next time the arbiter has to grant access to a channel within the same priority level, as shown in the following figure. The channel number of the last channel being granted access as the active channel is stored in the Level x Channel Priority Number bit group in the Priority Control 0 register (PRICTRL0.LVLPRI x) for the corresponding priority level.

Figure 21-6. Dynamic (Round-Robin) Priority Scheduling



21.6.2.5 Data Transmission

Before the DMAC can perform a data transmission, a DMA channel has to be configured and enabled, its corresponding transfer descriptor has to be initialized, and the arbiter has to grant the DMA channel access as the active channel.

Once the arbiter has granted a DMA channel access as the active channel (see *DMAC Block Diagram* in the *Block Diagram* from Related Links) the transfer descriptor for the DMA channel will be fetched from SRAM using the fetch

bus, and stored in the internal memory for the active channel. For a new block transfer, the transfer descriptor will be fetched from the descriptor memory section (BASEADDR); For an ongoing block transfer, the descriptor will be fetched from the write-back memory section (WRBADDR). By using the data transfer bus, the DMAC will read the data from the current source address and write it to the current destination address. For further details on how the current source and destination addresses are calculated, see *Addressing* from the Related Links.

The arbitration procedure is performed after each transfer. If the current DMA channel is granted access again, the block transfer counter (BTCNT) of the internal transfer descriptor will be decremented by the number of beats in a transfer, the optional output event Beat will be generated if configured and enabled, and the active channel will perform a new transfer. If a different DMA channel than the current active channel is granted access, the block transfer counter value will be written to the write-back section before the transfer descriptor of the newly granted DMA channel is fetched into the internal memory of the active channel.

When a block transfer has come to its end (BTCNT is zero), the Valid bit in the Block Transfer Control register will be cleared (BTCTRL.VALID=0) before the entire transfer descriptor is written to the write-back memory. The optional interrupts, Channel Transfer Complete and Channel Suspend, and the optional output event Block, will be generated if configured and enabled. After the last block transfer in a transaction, the Next Descriptor Address register (DESCADDR) will hold the value 0x00000000, and the DMA channel will either be suspended or disabled, depending on the configuration in the Block Action bit group in the Block Transfer Control register (BTCTRL.BLOCKACT). If the transaction has further block transfers pending, DESCADDR will hold the SRAM address to the next transfer descriptor to be fetched. The DMAC will fetch the next descriptor into the internal memory of the active channel and write its content to the write-back section for the channel, before the arbiter gets to choose the next active channel.

Related Links

- [21.6.2.7. Addressing](#)
- [21.3. Block Diagram](#)

21.6.2.6 Transfer Triggers and Actions

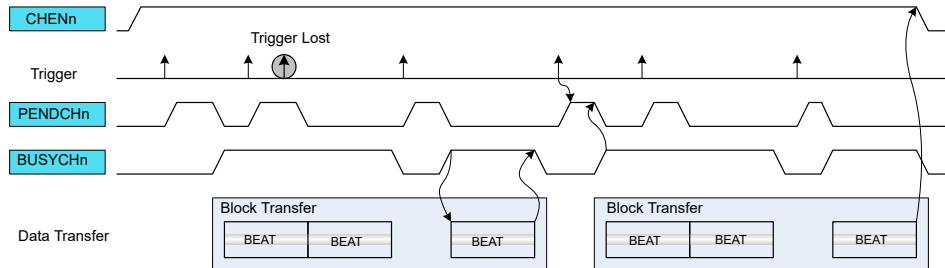
A DMA transfer through a DMA channel can be started *only* when a DMA transfer request is detected, and the DMA channel has been granted access to the DMA. A transfer request can be triggered from software, from a peripheral, or from an event. There are dedicated Trigger Source selections for each DMA Channel n Control A (CHCTRLAn.TRIGSRC).

The trigger actions are available in the Trigger Action bit group in the Channel n Control A register (CHCTRLAn.TRIGACT). By default, a trigger generates a request for a block transfer operation. If a single descriptor is defined for a channel, the channel is automatically disabled when a block transfer has been completed. If a list of linked descriptors is defined for a channel, the channel is automatically disabled when the last descriptor in the list is executed. As long as the list still has descriptors to execute, the channel will be waiting for the next block transfer trigger. When enabled again, the channel will wait for the next block transfer trigger. The trigger actions can also be configured to generate a request for a burst transfer (CHCTRLAn.TRIGACT=0x2) or transaction transfer (CHCTRLAn.TRIGACT=0x3) instead of a block transfer (CHCTRLAn.TRIGACT=0x0).

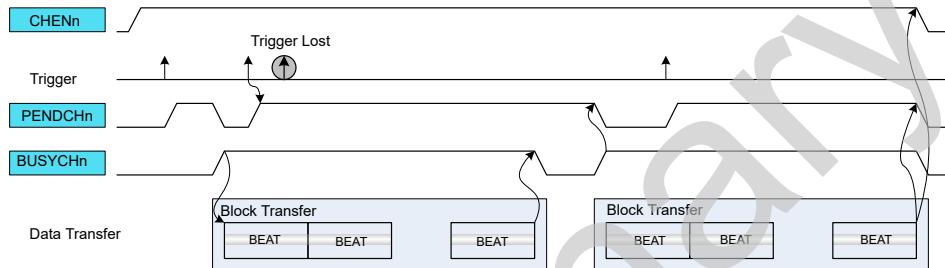
The following figure shows an example where triggers are used with two linked block descriptors.

Figure 21-7. Trigger Action and Transfers

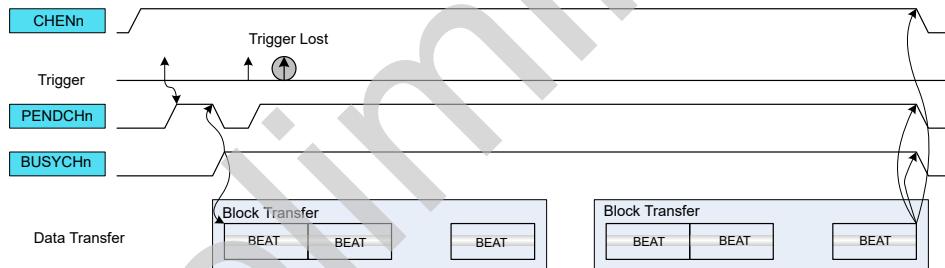
Beat Trigger Action



Block Trigger Action



Transaction Trigger Action



If the trigger source generates a transfer request for a channel during an ongoing transfer, the new transfer request will be kept pending (CHSTATUS_n.PEND=1), and the new transfer can start after the ongoing one is done. Only one pending transfer can be kept per channel. If the trigger source generates more transfer requests while one is already pending, the additional ones will be lost. All channels pending status flags are also available in the Pending Channels register (PENDCH).

When the transfer starts, the corresponding Channel Busy status flag is set in Channel _n Status register (CHSTATUS_n.BUSY). When the trigger action is complete, the Channel Busy status flag is cleared. All channel busy status flags are also available in the Busy Channels register (BUSYCH) in DMAC.

21.6.2.7 Addressing

Each block transfer needs to have both a source address and a destination address defined. The source address is set by writing the Transfer Source Address (SRCADDR) register, the destination address is set by writing the Transfer Destination Address (SRCADDR) register.

The addressing of this DMAC module can be static or incremental, for either source or destination of a block transfer, or both.

Incrementation for the source address of a block transfer is enabled by writing the Source Address Incrementation Enable bit in the Block Transfer Control register (BTCTRL.SRCINC=1). The step size of the incrementation is configurable and can be chosen by writing the Step Selection bit in the Block Transfer Control register (BTCTRL.STEPSEL=1) and writing the desired step size in the Address Increment Step Size bit group in the Block Transfer Control register (BTCTRL.STEPSIZE). If BTCTRL.STEPSEL=0, the step size for the source incrementation will be the size of one beat.

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When source address incrementation is configured (BTCTRL.SRCINC=1), SRCADDR is calculated as follows:

If BTCTRL.STEPSEL=1:

$$\text{SRCADDR} = \text{SRCADDR}_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1) \cdot 2^{\text{STEPSIZE}}$$

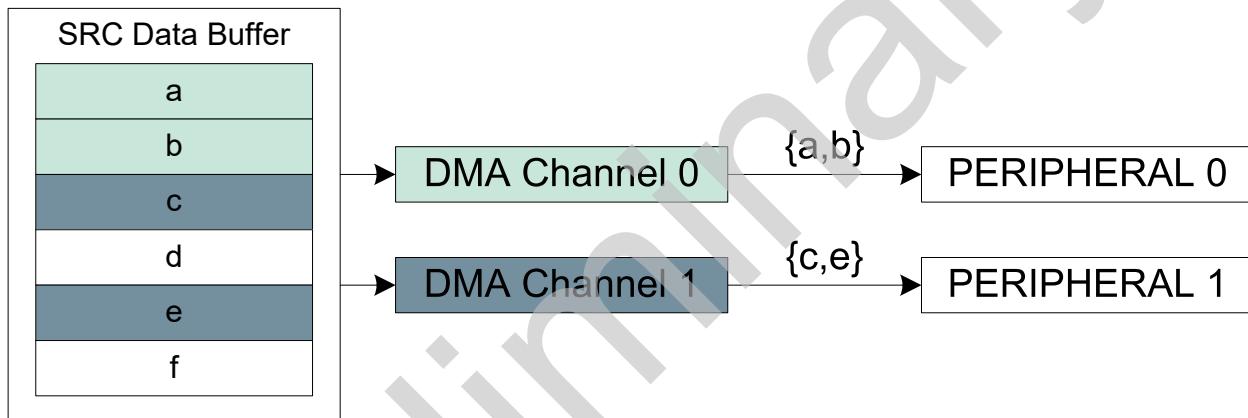
If BTCTRL.STEPSEL=0:

$$\text{SRCADDR} = \text{SRCADDR}_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1)$$

- $\text{SRCADDR}_{\text{START}}$ is the source address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

The following figure shows an example where DMA channel 0 is configured to increment the source address by one beat after each beat transfer (BTCTRL.SRCINC=1), and DMA channel 1 is configured to increment the source address by two beats (BTCTRL.SRCINC=1, BTCTRL.STEPSEL=1, and BTCTRL.STEPSIZE=0x1). As the destination address for both channels are peripherals, destination incrementation is disabled (BTCTRL.DSTINC=0).

Figure 21-8. Source Address Increment



Incrementation for the destination address of a block transfer is enabled by setting the Destination Address Incrementation Enable bit in the Block Transfer Control register (BTCTRL.DSTINC=1). The step size of the incrementation is configurable by clearing BTCTRL.STEPSEL=0 and writing BTCTRL.STEPSIZE to the desired step size. If BTCTRL.STEPSEL=1, the step size for the destination incrementation will be the size of one beat.

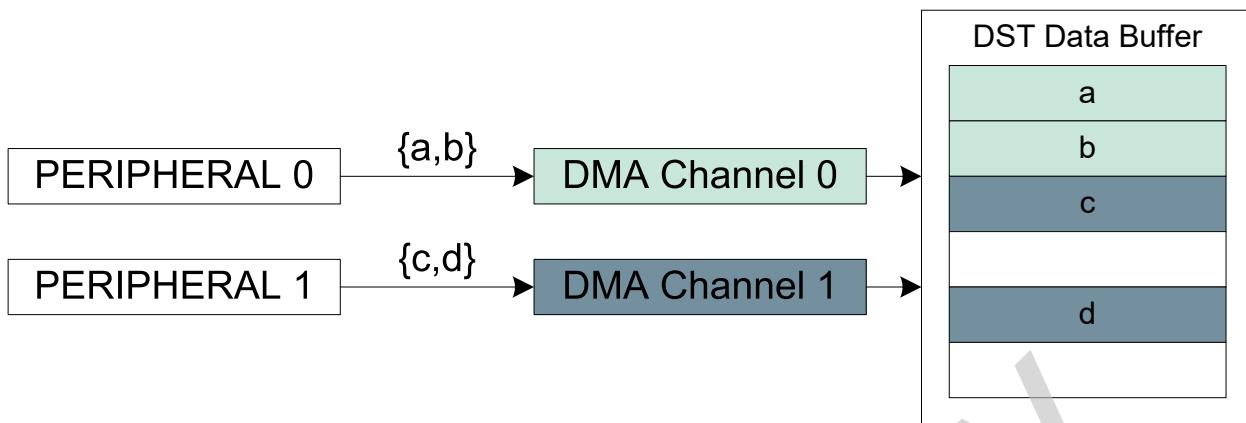
When the destination address incrementation is configured (BTCTRL.DSTINC=1), DSTADDR must be set and calculated as follows:

$DSTADDR = DSTADDR_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1) \cdot 2^{\text{STEPSIZE}}$	where BTCTRL.STEPSEL is zero
$DSTADDR = DSTADDR_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1)$	where BTCTRL.STEPSEL is one

- $\text{DSTADDR}_{\text{START}}$ is the destination address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

The following figure shows an example where DMA channel 0 is configured to increment destination address by one beat (BTCTRL.DSTINC=1) and DMA channel 1 is configured to increment destination address by two beats (BTCTRL.DSTINC=1, BTCTRL.STEPSEL=0, and BTCTRL.STEPSIZE=0x1). As the source address for both channels are peripherals, source incrementation is disabled (BTCTRL.SRCINC=0).

Figure 21-9. Destination Address Increment



21.6.2.8 Internal FIFO

To improve the bandwidth, the DMAC can support FIFO operation. When single-beat burst configuration is selected (CHCTRLx.BURSTLEN = SINGLE), the channel waits until the FIFO can transmit or accept a single beat transfer before it requests a bus access to write to the destination address. In all other cases, the channel waits until the FIFO threshold is reached before it requests a bus access to write to the destination address. The threshold is configurable and can be set by writing the THRESHOLD bits in the Channel x Control A register.

If the DMAC completes the read operations before the threshold is reached, the write to the destination is automatically enabled. If the FIFO is empty and the read from source is ongoing, the DMA will wait again until the FIFO threshold is reached before it requests a bus access to write the destination.

21.6.2.9 Error Handling

If a bus error is received from an AHB slave during a DMA data transfer, the corresponding active channel is disabled and the corresponding Channel Transfer Error Interrupt flag in the Channel Interrupt Status and Clear register (CHINTFLAG.TERR) is set. If enabled, the optional transfer error interrupt is generated. The transfer counter will not be decremented and its current value is written-back in the write-back memory section before the channel is disabled.

When the DMAC fetches an invalid descriptor (BTCTRL.VALID=0) or when the channel is resumed and the DMA fetches the next descriptor with null address (DESCADDR=0x00000000), the corresponding channel operation is suspended, the Channel Suspend Interrupt Flag in the Channel Interrupt Flag Status and Clear register (CHINTFLAG.SUSP) is set, and the Channel Fetch Error bit in the Channel Status register (CHSTATUS.FERR) is set. If enabled, the optional suspend interrupt is generated.

21.6.3 Additional Features

21.6.3.1 Linked Descriptors

A transaction can consist of either a single block transfer or of several block transfers. When a transaction consists of several block transfers it is done with the help of linked descriptors.

Memory Sections illustrates how linked descriptors work, see *Memory Sections* figure in the *Transfer Descriptors* from Related Links. When the first block transfer is completed on DMA channel 0, the DMAC fetches the next transfer descriptor, which is pointed to by the value stored in the Next Descriptor Address (DESCADDR) register of the first transfer descriptor. Fetching the next transfer descriptor (DESCADDR) is continued until the last transfer descriptor. When the block transfer for the last transfer descriptor is executed and DESCADDR = 0x00000000, the transaction is terminated. For further details on how the next descriptor is fetched from SRAM, see *Data Transmission* from Related Links.

Related Links

- [21.6.2.3. Transfer Descriptors](#)
- [21.6.2.5. Data Transmission](#)

21.6.3.1.1 Adding Descriptor to the End of a List

To add a new descriptor at the end of the descriptor list, create the descriptor in SRAM, with DESCADDR = 0x00000000 indicating that it is the new last descriptor in the list, and modify the DESCADDR value of the current last descriptor to the address of the newly created descriptor.

21.6.3.1.2 Modifying a Descriptor in a List

In order to add descriptors to a linked list, the following actions must be performed:

1. Enable the Suspend interrupt for the DMA channel.
2. Enable the DMA channel.
3. Reserve memory space in SRAM to configure a new descriptor.
4. Configure the new descriptor:
 - Set the next descriptor address (DESCADDR)
 - Set the destination address (DESCADDR)
 - Set the source address (SRCADDR)
 - Configure the block transfer control (BTCTRL) including
 - Optionally enable the suspend block action
 - Set the descriptor VALID bit
5. Clear the VALID bit for the existing list and for the descriptor which has to be updated.
6. Read DESCADDR from the write-back memory.
 - If the DMA has not already fetched the descriptor that requires changes (in other words, DESCADDR is wrong):
 - Update the DESCADDR location of the descriptor from the list
 - Optionally clear the suspend block action
 - Set the descriptor VALID bit to '1'
 - Optionally enable the Resume Software command
 - If the DMA is executing the same descriptor as the one that requires changes:
 - Set the Channel Suspend Software command and wait for the suspend interrupt
 - Update the next descriptor address (DESCADDR) in the write-back memory
 - Clear the interrupt sources and set the Resume Software command
 - Update the DESCADDR location of the descriptor from the list
 - Optionally clear the suspend block action
 - Set the descriptor VALID bit to '1'
7. Go to step 4 if needed.

21.6.3.1.3 Adding a Descriptor Between Existing Descriptors

To insert a new descriptor 'C' between two existing descriptors ('A' and 'B'), the descriptor currently executed by the DMA must be identified.

1. If DMA is executing descriptor B, descriptor C cannot be inserted.
2. If DMA has not started to execute descriptor A, follow the steps:
 - a. Set the descriptor A VALID bit to '0'.
 - b. Set the DESCADDR value of descriptor A to point to descriptor C instead of descriptor B, see *DESCADDR* in the *DMAC Register Summary* from Related Links.
 - c. Set the DESCADDR value of descriptor C to point to descriptor B, see *DESCADDR* in the *DMAC Register Summary* from Related Links.
 - d. Set the descriptor A VALID bit to '1'.
3. If DMA is executing descriptor A:
 - a. Apply the software suspend command to the channel and
 - b. Perform steps 2.1 through 2.4.
 - c. Apply the software resume command to the channel.

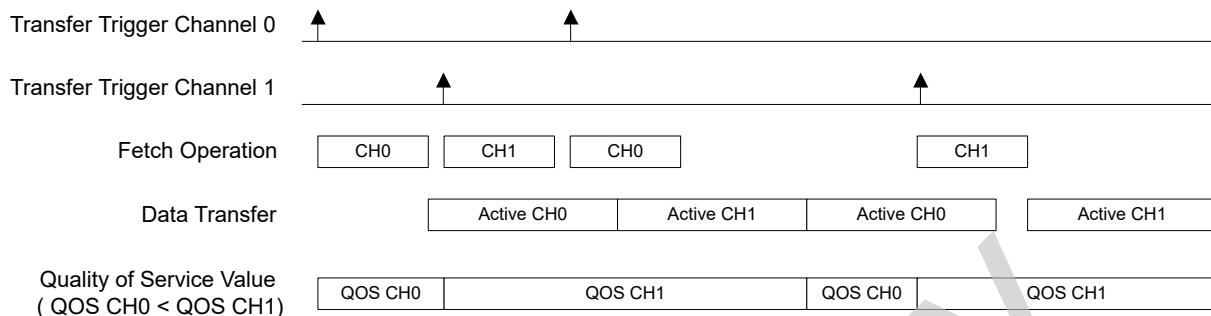
Related Links

- 21.9. DMAC Register Summary (SRAM)

21.6.3.2 Transfer Quality of Service

Each priority level group has dedicated quality of service settings. The setting can be written in the corresponding Quality of Service bit group in the Priority Control x register (PRICTRL0.QOSn).

Figure 21-10. Quality of Service



When a channel is stored in the Pre-Fetch or Active Channel, the corresponding PRICTRLx.QOS bits value is stored in the respective channel. As shown in Quality of Service, the DMAC will select the highest QOS value between Active and Pre-Fetch channels. This value will apply to all DMAC buses.

21.6.3.3 Channel Suspend

The channel operation can be suspended at any time by software by writing a '1' to the Suspend command in the Command bit field of Channel Control B register (CHCTRLB.CMD). After the ongoing burst transfer is completed, the channel operation is suspended and the suspend command is automatically cleared.

When suspended, the Channel Suspend Interrupt flag in the Channel Interrupt Status and Clear register is set (CHINTFLAG.SUSP=1) and the optional suspend interrupt is generated.

By configuring the block action to suspend by writing Block Action bit group in the Block Transfer Control register (BTCTRL.BLOCKACT is 0x2 or 0x3), the DMA channel will be suspended after it has completed a block transfer. The DMA channel will be kept enabled and will be able to receive transfer triggers, but it will be removed from the arbitration scheme.

If an invalid transfer descriptor (BTCTRL.VALID=0) is fetched from SRAM, the DMA channel will be suspended, and the Channel Fetch Error bit in the Channel Status register(CHASTATUS.FERR) will be set.

Note: Only enabled DMA channels can be suspended. If a channel is disabled when it is attempted to be suspended, the internal suspend command will be ignored.

For more details on transfer descriptors, see *Transfer Descriptors* from Related Links.

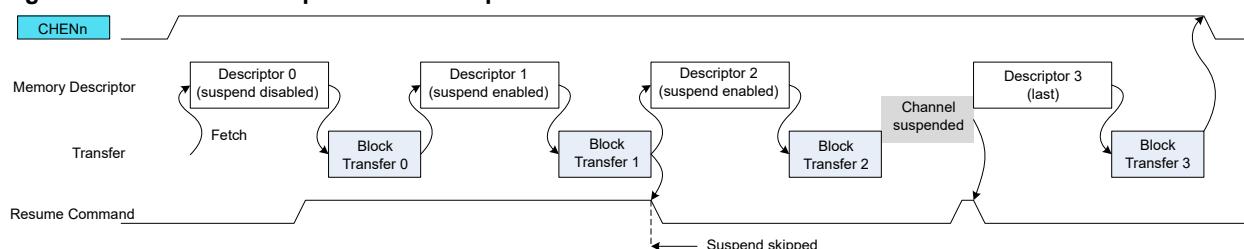
Related Links

21.6.2.3. Transfer Descriptors

21.6.3.4 Channel Resume and Next Suspend Skip

A channel operation can be resumed by software by setting the Resume command in the Command bit field of the Channel Control B register (CHCTRLB.CMD). If the channel is already suspended, the channel operation resumes from where it previously stopped when the Resume command is detected. When the Resume command is issued before the channel is suspended, the next suspend action is skipped and the channel continues the normal operation.

Figure 21-11. Channel Suspend/Resume Operation



21.6.3.5 Event Input Actions

The event input actions are available only on the least significant DMA channels. For more details on channels with event input support, see *Event System (EVSYS)* from Related Links.

Before using event input actions, the event controller must be configured first according to the following table, and the Channel Event Input Enable bit in the Channel Event Control register (CHEVCTRL.EVIE) must be written to '1'. See *Events* from Related Links.

Table 21-1. Event Input Action

Action	CHEVCTRL.EVACT	CHCTRLA.TRIGSRC
None	NOACT	-
Normal Transfer	TRIG	DISABLE
Conditional Transfer on Strobe	TRIG	Any peripheral
Conditional Transfer	CTRIG	
Conditional Block Transfer	CBLOCK	
Channel Suspend	SUSPEND	
Channel Resume	RESUME	
Skip Next Block Suspend	SSKIP	
Increase priority	INCPRI	

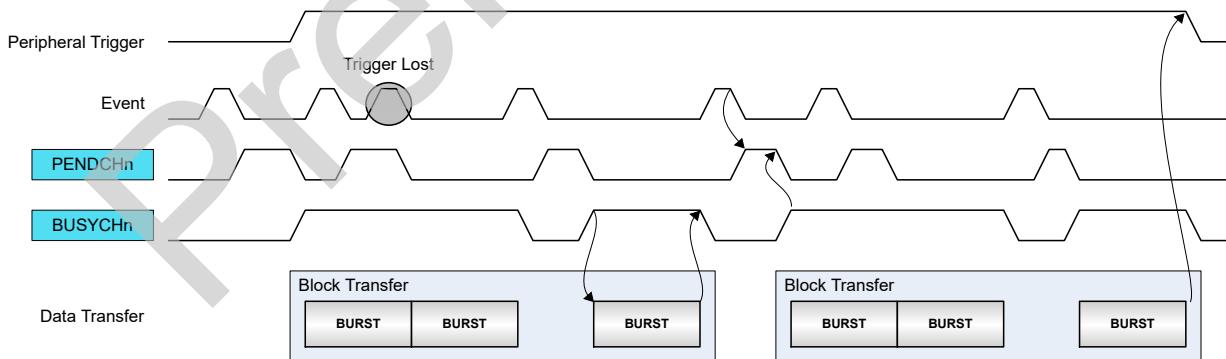
Normal Transfer

The event input is used to trigger a beat or burst transfer on peripherals.

The event is acknowledged as soon as the event is received. When received, both the Channel Pending status bit in the Channel Status register (CHSTATUS.PEND) and the corresponding Channel n bit in the Pending Channels register (PENDCH.PENDCHn) are set. If the event is received while the channel is pending, the event trigger is lost.

The following figure shows an example where beat transfers are enabled by internal events.

Figure 21-12. Burst Event Trigger Action



Conditional Transfer on Strobe

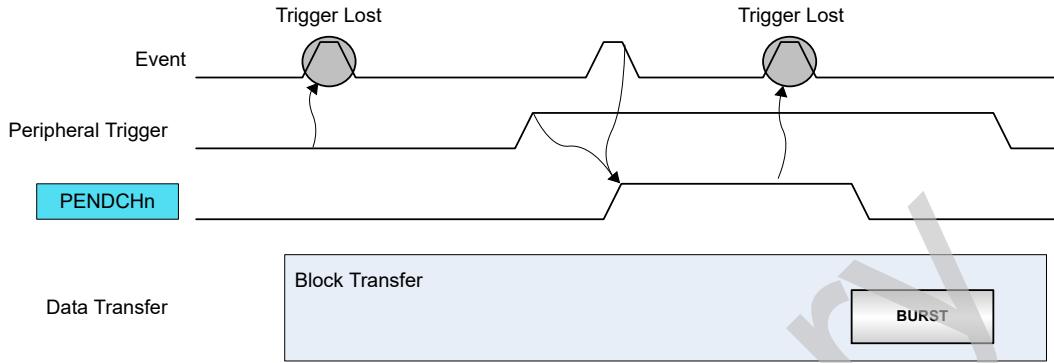
The event input is used to trigger a transfer on peripherals with pending transfer requests. This event action is intended to be used with peripheral triggers, for example, for timed communication protocols or periodic transfers between peripherals: only when the peripheral trigger coincides with the occurrence of a (possibly cyclic) event the transfer is issued.

The event is acknowledged as soon as the event is received. The peripheral trigger request is stored internally when the previous trigger action is completed (in other words, the channel is not pending) and when an active event is received. If the peripheral trigger is active, the DMA waits for an event before the peripheral trigger

is internally registered. When both event and peripheral transfer trigger are active, both CHSTATUS.PEND and PENDCH.PENDChn are set. A software trigger will now trigger a transfer.

The following figure shows an example where the peripheral beat transfer is started by a conditional strobe event action.

Figure 21-13. Periodic Event with Burst Peripheral Triggers



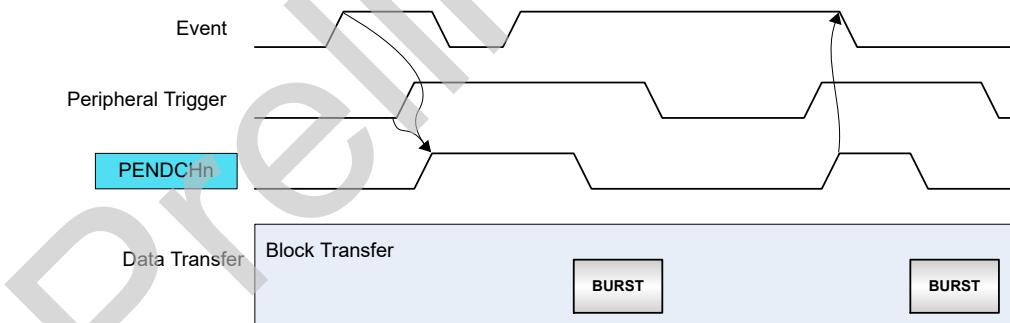
Conditional Transfer

The event input is used to trigger a conditional transfer on peripherals with pending transfer requests. As example, this type of event can be used for peripheral-to-peripheral transfers, where one peripheral is the source of event and the second peripheral is the source of the trigger.

Each peripheral trigger is stored internally when the event is received. When the peripheral trigger is stored internally, the Channel Pending status bit is set (CHSTATUS.PEND), the respective Pending Channel n Bit in the Pending Channels register is set (PENDCH.PENDChn), and the event is acknowledged. A software trigger will now trigger a transfer.

The following figure shows an example where conditional event is enabled with peripheral beat trigger requests.

Figure 21-14. Conditional Event with Burst Peripheral Triggers



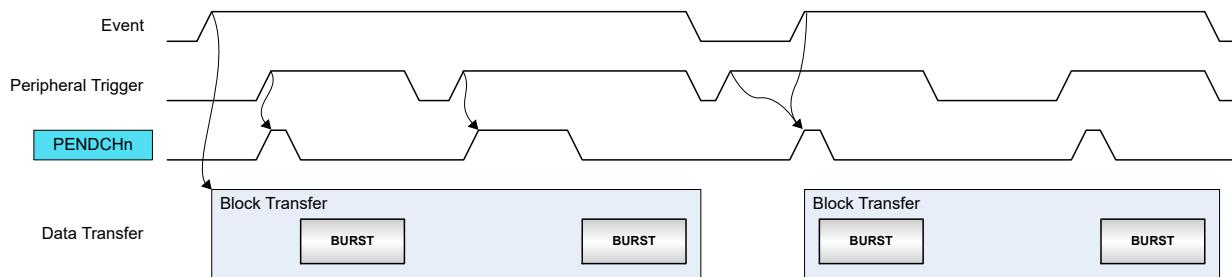
Conditional Block Transfer

The event input is used to trigger a conditional block transfer on peripherals.

Before starting transfers within a block, an event must be received. When received, the event is acknowledged when the block transfer is completed. A software trigger will trigger a transfer.

The following figure shows an example where conditional event block transfer is started with peripheral beat trigger requests.

Figure 21-15. Conditional Block Transfer with Burst Peripheral Triggers



Channel Suspend

The event input is used to suspend an ongoing channel operation. The event is acknowledged when the current AHB access is completed. For more details on Channel Suspend, see *Channel Suspend* from Related Links.

Channel Resume

The event input is used to resume a suspended channel operation. The event is acknowledged as soon as the event is received and the Channel Suspend Interrupt Flag (CHINTFLAG.SUSP) is cleared. See *Channel Suspend* from Related Links.

Skip Next Block Suspend

This event can be used to skip the next block suspend action. If the channel is suspended before the event rises, the channel operation is resumed and the event is acknowledged. If the event rises before a suspend block action is detected, the event is kept until the next block suspend detection. When the block transfer is completed, the channel continues the operation (not suspended) and the event is acknowledged.

Increase priority

This event can be used to increase a channel priority and to request higher quality of service (QOS), when critical transfers must be done. When the event is detected, the channel will have the highest priority and the output Quality of Service value is internally forced to the maximum value. The event is acknowledged when the trigger action execution is completed. When acknowledged, the channel will recover its initial priority level and quality of service settings.

Related Links

- [21.6.3.3. Channel Suspend](#)
- [21.6.6. Events](#)
- [27. Event System \(EVSYS\)](#)

21.6.3.6 Event Output Selection

The event output selections are available only for channels supporting event outputs.

The Channel Event Output Enable can be set in the corresponding Channel n Event Control register (CHEVCTRL.EVOE). The Event Output Mode bits in Channel n Event Control register (CHEVCTRL.EVOMODE) selects the event type the channel should generate.

The transfer events (CHEVCTRL.EVOMODE = DEFAULT) are strobe events and their duration is one CLK_DMAC_AHB clock period. The transfer event type selection is available in each Descriptor Block Control location (BTCTRL.EVOSEL). Block or burst event output generation is supported.

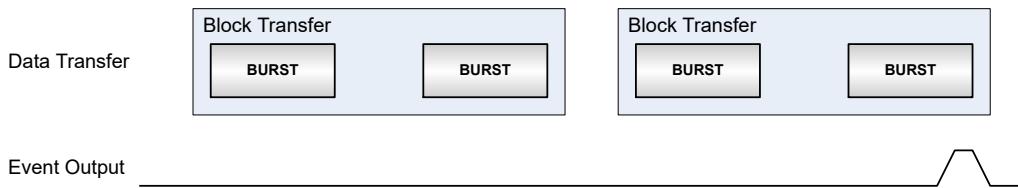
The trigger action event (CHEVCTRL.EVOMODE = TRIGACT) is a level, active while the trigger action execution is not completed.

Block event output

When the block event output is selected, an event strobe is generated when the block transfer is completed. The pulse width of a block event output from a channel is one AHB clock cycle. It is also possible to use this event type to generate an event when the transaction is complete. For this type of application, the block event selection must be set in the last transfer descriptor only, as shown below.

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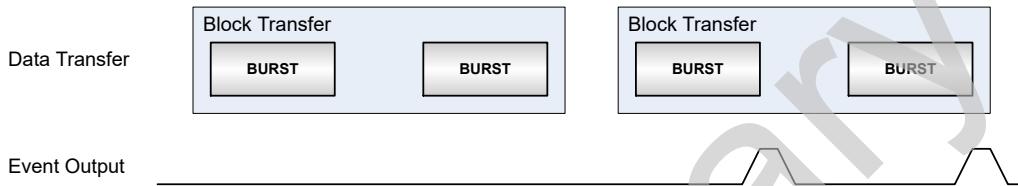
Figure 21-16. Block Event Output Generation



Burst event output

When the burst event output is selected, an event strobe is generated when each burst transfer within the corresponding block is completed. The pulse width of a burst event output from a channel is one AHB clock cycle. The figure below shows an example where the burst event output is set in the second descriptor of a linked list.

Figure 21-17. Burst Event Output Generation

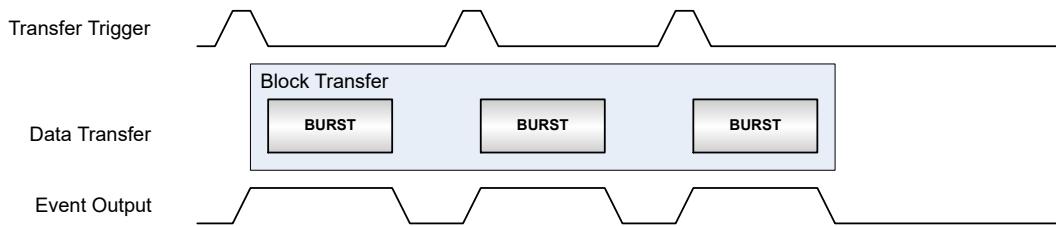


Trigger action event output

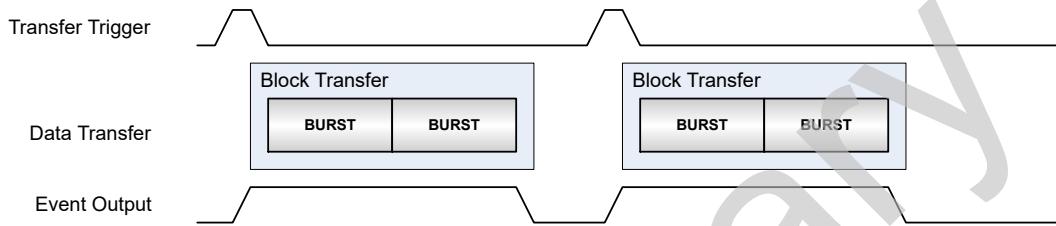
When the trigger action event output is selected, an event level is generated. Then event output is set when the transfer trigger occurred, and cleared when the corresponding trigger action is completed. The figure below shows an example for each trigger action type.

Figure 21-18. Trigger Action Event Output Generation

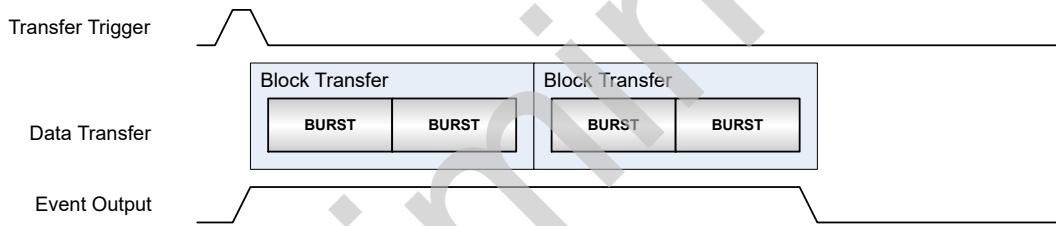
Burst Trigger Action Event Output



Block Trigger Action Event Output



Transaction Trigger Action Event Output



21.6.3.7 Aborting Transfers

Transfers on any channel can be aborted gracefully by software by disabling the corresponding DMA channel. It is also possible to abort all ongoing or pending transfers by disabling the DMAC.

When a DMA channel disable request or DMAC disable request is detected:

- Ongoing transfers of the active channel will be disabled when the ongoing beat transfer is completed and the write-back memory section is updated. This prevents transfer corruption before the channel is disabled.
- All other enabled channels will be disabled in the next clock cycle.

The corresponding Channel Enable bit in the Channel Control A register is cleared (CHCTRLA.ENABLE=0) when the channel is disabled.

The corresponding DMAC Enable bit in the Control register is cleared (CTRL.DMAENABLE=0) when the entire DMAC module is disabled.

21.6.3.8 CRC Operation

A Cyclic Redundancy Check (CRC) is an error detection technique used to find errors in data. It is commonly used to determine whether the data during a transmission, or data present in data and program memories has been corrupted or not. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum.

When the data is received, the device or application repeats the calculation: If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

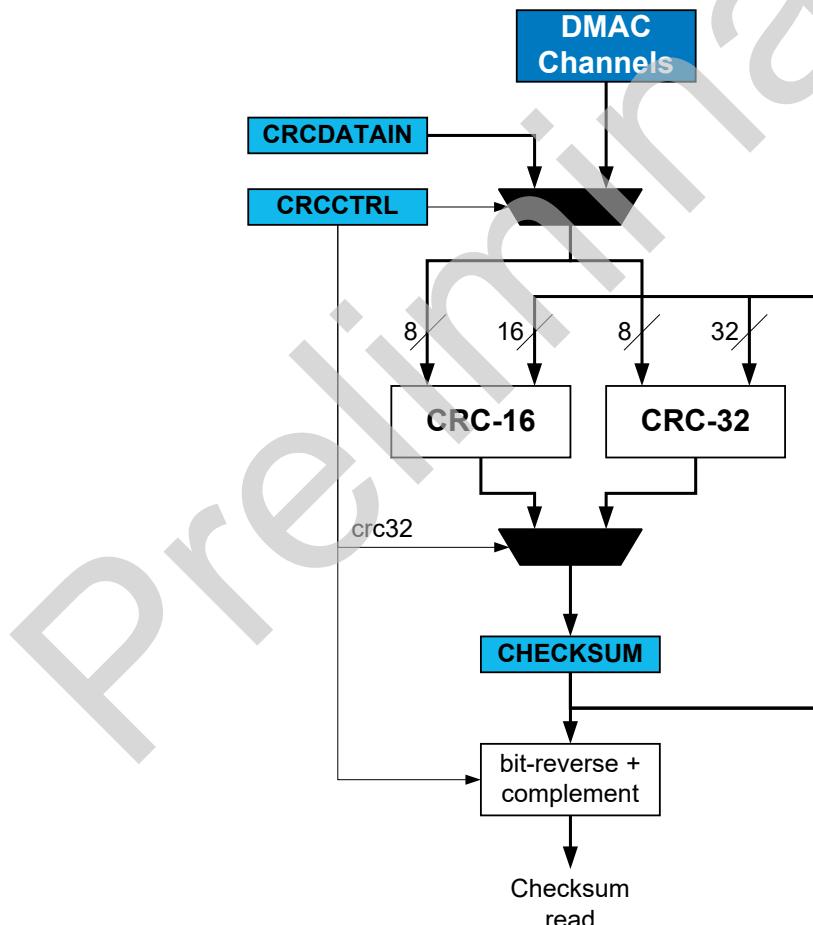
The CRC engine in DMAC supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). Typically, applying CRC-n (CRC-16 or CRC-32) to a data block of arbitrary length will detect any single alteration that is $\leq n$ bits in length, and will detect the fraction 1-2- n of all longer error bursts.

- CRC-16:
 - Polynomial: $x^{16} + x^{12} + x^5 + 1$
 - Hex value: 0x1021
- CRC-32:
 - Polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
 - Hex value: 0x04C11DB7

The data source for the CRC engine can either be one of the DMA channels or the APB bus interface, and must be selected by writing to the CRC Input Source bits in the CRC Control register (CRCCTRL.CRCSRC). The CRC engine then takes data input from the selected source and generates a checksum based on these data. The checksum is available in the CRC Checksum register (CRCCHKSUM). When CRC-32 polynomial is used, the final checksum read is bit reversed and complemented, as shown in the following figure.

The CRC polynomial is selected by writing to the CRC Polynomial Type bit in the CRC Control register (CRCCTRL.CRCPOLY), the default is CRC-16. The CRC engine operates on byte only. When the DMA is used as data source for the CRC engine, the DMA channel beat size setting will be used. When used with APB bus interface, the application must select the CRC Beat Size bit field of CRC Control register (CRCCTRL.CRCBEATSIZE). 8-, 16-, or 32-bit bus transfer access type is supported. The corresponding number of bytes will be written in the CRCDATAIN register and the CRC engine will operate on the input data in a byte by byte manner.

Figure 21-19. CRC Generator Block Diagram



CRC on DMA data CRC-16 or CRC-32 calculations can be performed on data passing through any DMA channel. Once a DMA channel is selected as the source, the CRC engine will continuously generate the CRC on the data passing through the DMA channel. The checksum is available for readout once the DMA transaction is completed or aborted. A CRC can also be generated on SRAM, Flash, or I/O memory by passing these

data through a DMA channel. If the latter is done, the destination register for the DMA data can be the data input (CRCDATAIN) register in the CRC engine.

CRC using the I/O interface Before using the CRC engine with the I/O interface, the application must set the CRC Beat Size bits in the CRC Control register (CRCCTRL.CRCBEATSIZE). 8/16/32-bit bus transfer type can be selected.

CRC can be performed on any data by loading them into the CRC engine using the CPU and writing the data to the CRCDATAIN register. Using this method, an arbitrary number of bytes can be written to the register by the CPU, and CRC is done continuously for each byte. This means if a 32-bit data is written to the CRCDATAIN register the CRC engine takes four cycles to calculate the CRC. The CRC complete is signaled by a set CRCBUSY bit in the CRCSTATUS register. New data can be written only when CRCBUSY flag is not set.

21.6.3.9 Memory CRC Generation

When enabled, it is possible to automatically calculate a memory block checksum. When the channel is enabled and the descriptor is fetched, the CRC Checksum register (CRCCHKSUM) is reloaded with the initial checksum value (CHKINIT) stored in the Block Transfer Destination Address register (DSTADDR). The DMA read and calculate the checksum over the data from the source address. When the checksum calculation is completed, the CRC value is stored in the CRC Checksum register (CRCCHKSUM), the Transfer Complete interrupt flag is set (CHINTFLAGn.TCMPL) and optional interrupt is generated.

If linked descriptor is in the list (DESCADDR !=0), the DMA will fetch the next descriptor and CRC calculation continues as described above. When the last list descriptor is executed, the channel is automatically disabled.

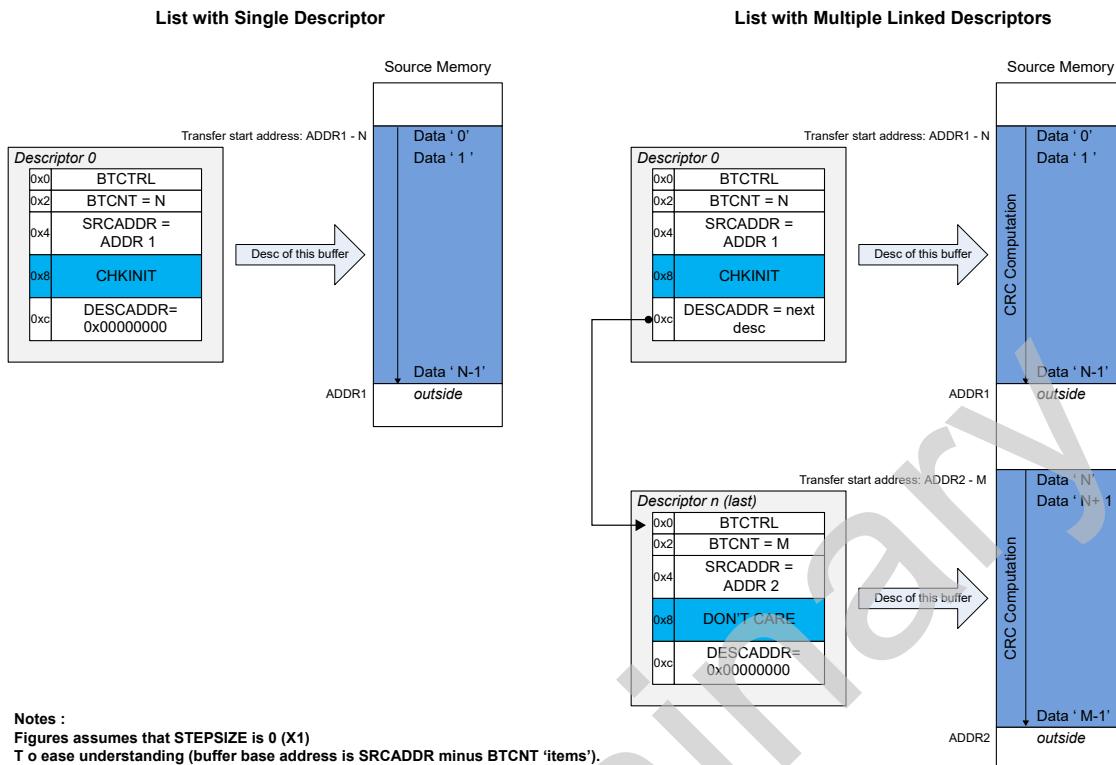
In order to enable the memory CRC generation, the following actions must be performed:

1. The CRC module must be set to be used with a DMA channel (CRCCTRL.CRCSRC)
2. Reserve memory space addresses to configure a descriptor or a list of descriptors
3. Configure each descriptor:
 - Set the next descriptor address (DESCADDR)
 - Set the destination address with the initial checksum value (DSTADDR = CHKINIT) in the first descriptor in a list
 - Set the transfer source address (SRCADDR)
 - Set the block transfer count (BTCNT)
 - Set the memory CRC generation operation mode (CRCCTRL.CRCMODE = CRCGEN)
 - Enable optional interrupts
4. Enable the corresponding DMA channel (CHCTRLAn.ENABLE)

The figure below shows the CRC computation slots and descriptor configuration when single or linked-descriptors transfers are enabled.

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Figure 21-20. CRC Computation with Single Linked Transfers



21.6.3.10 Memory CRC Monitor

When enabled, it is possible to continuously check a memory block data integrity by calculating and checking the CRC checksum. The expected CRC checksum value must be located in the last memory block location, as shown in the table below:

CRCCTRL.CRPCPOLY	CRCCTRL.CRCBEATSIZE	Last Memory Block Byte Locations Value (MSB Byte First)	CHECKSUM Result
CRC-16	Byte	Expected CRC[7:0]	0x00000000
	Half-word	Expected CRC[15:8]	
	Word	0x00 0x00 Expected CRC[7:0] Expected CRC[15:8]	
CRC-32	Byte	Expected CRC[31:24]	CRC Magic Number (0x2144DF1C)
	Half-word	Expected CRC[23:16]	
	Word	Expected CRC[15:8] Expected CRC[7:0]	

When the channel is enabled and the descriptor is fetched, the CRC Checksum register (CRCCHKSUM) is reloaded with the initial checksum value (CHKINIT), stored in the DSTADDR location of the first descriptor. The DMA read and calculate the checksum over the entire data from the source address. When the checksum calculation is completed the DMA read the last beat from the memory, the calculated CRC value from the CRC Checksum register is compared to zero or CRC magic number, depending on CRC polynomial selection.

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If the CHECKSUM does not match the comparison value the DMA channel is disabled, and both the CRC Error bit in the Channel n Status register (CHSTATUSn.CRCERR) and Transfer Error interrupt flag (CHINTFLAGn.TERR) are set. If enabled, the Transfer Error interrupt is generated.

If the calculated checksum value matches the compare value, the Transfer Complete interrupt flag (CHINTFLAGn.TCMPL) is set, optional interrupt is generated and the DMA will perform the following actions, depending on the descriptor list settings:

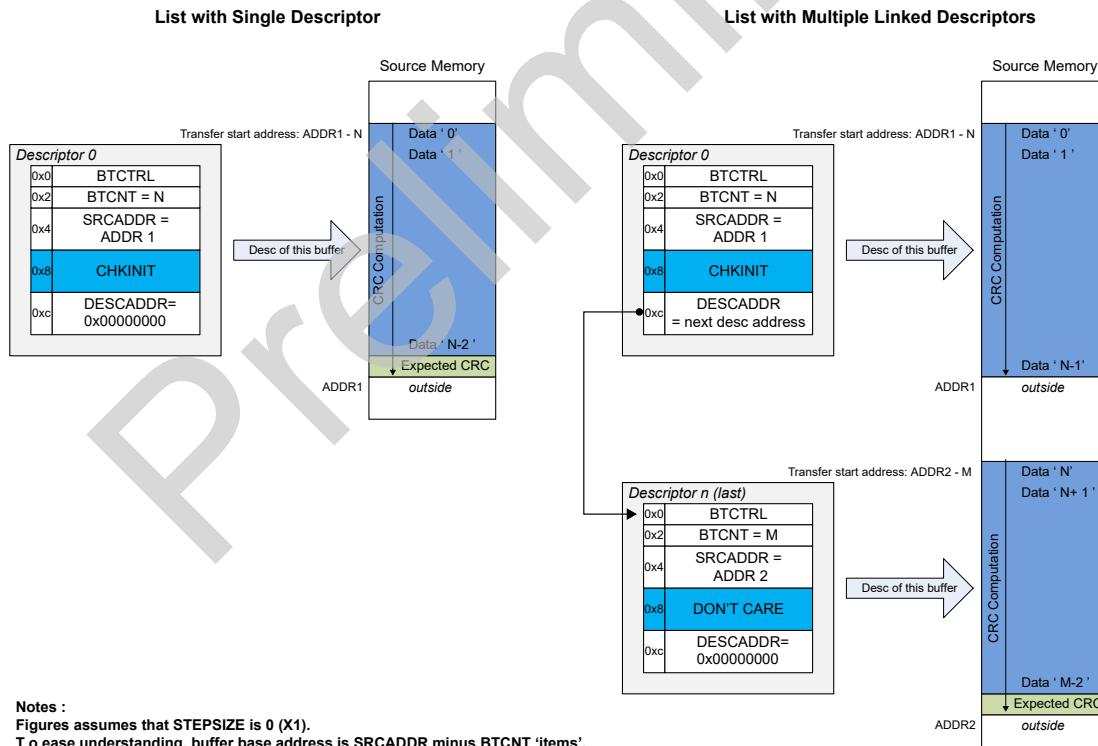
- If the list has only one descriptor, the DMA will re-fetch the descriptor
- If the current descriptor is the last descriptor from the list, the DMA will fetch the first descriptor from the list

When the fetch is completed, the DMA restarts the operations described above when new triggers are detected.

In order to enable the memory CRC monitor, the following actions must be performed:

1. The CRC module must be set to be used with a DMA channel (CRCCTRL.CRCSRC)
2. Reserve memory space addresses to configure a descriptor or a list of descriptors
3. Configure each descriptor
 - Set the next descriptor address (DESCADDR)
 - In the first list descriptor, set the destination address with the initial checksum value (DSTADDR = CHKINIT)
 - Set the transfer source address (SRCADDR)
 - Set the block transfer count (BTCNT)
 - Set the memory CRC monitor operation mode (CRCCTRL.CRCMODE = CRCMON)
 - Enable optional interrupts
4. Enable the corresponding DMA channel (CHCTRLn.ENABLE)

Figure 21-21. CRC Computation and Check with Single or Linked Transfers



21.6.4 DMA Operation

Not applicable.

21.6.5 Interrupts

The DMAC channels have the following interrupt sources:

- Transfer Complete (TCMPL): Indicates that a block transfer is completed on the corresponding channel. See *Data Transmission* from Related Links.
- Transfer Error (TERR): Indicates that a bus error has occurred during a burst transfer, or that an invalid descriptor has been fetched. See *Error Handling* from Related Links.
- Channel Suspend (SUSP): Indicates that the corresponding channel has been suspended. See *Channel Suspend* and *Data Transmission* from Related Links.

Each interrupt source has an Interrupt flag associated with it. The Interrupt flag in the Channel Interrupt Flag Status and Clear (CHINTFLAG) register is set when the Interrupt condition occurs. Each interrupt can be individually enabled by setting the corresponding bit in the Channel Interrupt Enable Set register (CHINTENSET=1), and disabled by setting the corresponding bit in the Channel Interrupt Enable Clear register (CHINTENCLR=1). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the Interrupt flag is cleared, the interrupt is disabled, the DMAC is reset or the corresponding DMA channel is reset. See CHINTFLAG for details on how to clear Interrupt flags. All interrupt requests are ORed together on system level to generate one combined interrupt request to the NVIC. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

The user must read the Channel Interrupt Status (INTSTATUS) register to identify the channels with pending interrupts and must read the Channel Interrupt Flag Status and Clear (CHINTFLAG) register to determine which Interrupt condition is present for the corresponding channel. It is also possible to read the Interrupt Pending register (INTPEND), which provides the lowest channel number with pending interrupt and the respective Interrupt flags.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

Related Links

- 21.6.2.5. Data Transmission
- 21.6.2.9. Error Handling
- 21.6.3.3. Channel Suspend
- 9.2. Nested Vector Interrupt Controller (NVIC)

21.6.6 Events

The DMAC can generate the following output events:

- Channel (CH): Generated when a block transfer for a given channel has been completed, or when a beat transfer within a block transfer for a given channel has been completed. See *Event Output Selection* from Related Links.

Setting the Channel Event Output Enable bit (CHEVCTRLx.EVOE = 1) enables the corresponding output event configured in the Event Output Selection bit group in the Block Transfer Control register (BTCTRL.EVOSEL). Clearing CHEVCTRLx.EVOE = 0 disables the corresponding output event.

The DMAC can take the following actions on an input event:

- Transfer and Periodic Transfer Trigger (TRIG): normal transfer or periodic transfers on peripherals are enabled
- Conditional Transfer Trigger (CTRIG): conditional transfers on peripherals are enabled
- Conditional Block Transfer Trigger (CBLOCK): conditional block transfers on peripherals are enabled
- Channel Suspend Operation (SUSPEND): suspend a channel operation
- Channel Resume Operation (RESUME): resume a suspended channel operation
- Skip Next Block Suspend Action (SSKIP): skip the next block suspend transfer condition
- Increase Priority (INCPRI): increase channel priority

Setting the Channel Event Input Enable bit (CHEVCTRLx.EVIE = 1) enables the corresponding action on input event. Clearing this bit disables the corresponding action on input event. Note that several actions can be enabled for incoming events. If several events are connected to the peripheral, any enabled action will be taken for any of the incoming events. See *Event Input Actions* from Related Links for more details on event input actions.

Note: Event input and outputs are not available for every channel. See *Features* from Related Links.

Related Links

- [21.6.3.6. Event Output Selection](#)
- [21.6.3.5. Event Input Actions](#)
- [21.2. Features](#)

21.6.7 Sleep Mode Operation

21.6.8 Synchronization

Not applicable.

Preliminary

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21.7 DMAC Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRL	7:0							DMAENABLE	SWRST
		15:8					LVLENx3	LVLENx2	LVLENx1	LVLENx0
0x02	CRCCTRL	7:0					CRCPOLY[1:0]		CRCBEATSIZE[1:0]	
		15:8	CRCMODE[1:0]				CRCSRC[5:0]			
0x04	CRCDATAIN	7:0					CRCDATAIN[7:0]			
		15:8					CRCDATAIN[15:8]			
		23:16					CRCDATAIN[23:16]			
		31:24					CRCDATAIN[31:24]			
0x08	CRCCHKSUM	7:0					CRCCHKSUM[7:0]			
		15:8					CRCCHKSUM[15:8]			
		23:16					CRCCHKSUM[23:16]			
		31:24					CRCCHKSUM[31:24]			
0x0C	CRCSTATUS	7:0						CRCERR	CRCZERO	CRCBUSY
0x0D	DBGCTRL	7:0								DBGRUN
0x0E	Reserved									
0x0F										
0x10	SWTRIGCTRL	7:0					SWTRIGN[7:0]			
		15:8					SWTRIGN[15:8]			
		23:16								
		31:24								
0x14	PRICTRL0	7:0	RRLVLEN0		QOS00[1:0]			LVLPRI0[4:0]		
		15:8	RRLVLEN1		QOS01[1:0]			LVLPRI1[4:0]		
		23:16	RRLVLEN2		QOS02[1:0]			LVLPRI2[4:0]		
		31:24	RRLVLEN3		QOS03[1:0]			LVLPRI3[4:0]		
0x18	Reserved									
0x1F										
0x20	INTPEND	7:0					ID[4:0]			
		15:8	PEND	BUSY	FERR	CRCERR		SUSP	TCMPL	TERR
0x22	Reserved									
0x23										
0x24	INTSTATUS	7:0					CHINTn[7:0]			
		15:8					CHINTn[15:8]			
		23:16								
		31:24								
0x28	BUSYCH	7:0					BUSYCHn[7:0]			
		15:8					BUSYCHn[15:8]			
		23:16								
		31:24								
0x2C	PENDCH	7:0	PENDCH7	PENDCH6	PENDCH5	PENDCH4	PENDCH3	PENDCH2	PENDCH1	PENDCH0
		15:8	PENDCH15	PENDCH14	PENDCH13	PENDCH12	PENDCH11	PENDCH10	PENDCH9	PENDCH8
		23:16								
		31:24								
0x30	ACTIVE	7:0					LVLEXx3	LVLEXx2	LVLEXx1	LVLEXx0
		15:8	ABUSY				ID[4:0]			
		23:16					BTCTNT[7:0]			
		31:24					BTCTNT[15:8]			
0x34	BASEADDR	7:0					BASEADDR[7:0]			
		15:8					BASEADDR[15:8]			
		23:16					BASEADDR[23:16]			
		31:24					BASEADDR[31:24]			

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x38	WRBADDR	7:0				WRBADDR[7:0]				
		15:8				WRBADDR[15:8]				
		23:16				WRBADDR[23:16]				
		31:24				WRBADDR[31:24]				
0x3C ... 0x3F	Reserved									
0x40	CHCTRLA0	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x44	CHCTRLB0	7:0							CMD[1:0]	
0x45	CHPRILVL0	7:0							PRILVL[1:0]	
0x46	CHEVCTRL0	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x47 ... 0x4B	Reserved									
0x4C	CHINTENCLR0	7:0						SUSP	TCMPL	TERR
0x4D	CHINTENSET0	7:0						SUSP	TCMPL	TERR
0x4E	CHINTFLAG0	7:0						SUSP	TCMPL	TERR
0x4F	CHSTATUS0	7:0					CRCERR	FERR	BUSY	PEND
0x50	CHCTRLA1	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x54	CHCTRLB1	7:0							CMD[1:0]	
0x55	CHPRILVL1	7:0							PRILVL[1:0]	
0x56	CHEVCTRL1	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x57 ... 0x5B	Reserved									
0x5C	CHINTENCLR1	7:0						SUSP	TCMPL	TERR
0x5D	CHINTENSET1	7:0						SUSP	TCMPL	TERR
0x5E	CHINTFLAG1	7:0						SUSP	TCMPL	TERR
0x5F	CHSTATUS1	7:0				CRCERR	FERR	BUSY	PEND	
0x60	CHCTRLA2	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x64	CHCTRLB2	7:0							CMD[1:0]	
0x65	CHPRILVL2	7:0							PRILVL[1:0]	
0x66	CHEVCTRL2	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x67 ... 0x6B	Reserved									
0x6C	CHINTENCLR2	7:0						SUSP	TCMPL	TERR
0x6D	CHINTENSET2	7:0						SUSP	TCMPL	TERR
0x6E	CHINTFLAG2	7:0						SUSP	TCMPL	TERR
0x6F	CHSTATUS2	7:0				CRCERR	FERR	BUSY	PEND	
0x70	CHCTRLA3	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x74	CHCTRLB3	7:0							CMD[1:0]	
0x75	CHPRILVL3	7:0							PRILVL[1:0]	
0x76	CHEVCTRL3	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x77 ... 0x7B	Reserved									

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Direct Memory Access Controller (DMAC)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x7C	CHINTENCLR3	7:0						SUSP	TCMPL	TERR
0x7D	CHINTENSET3	7:0						SUSP	TCMPL	TERR
0x7E	CHINTFLAG3	7:0						SUSP	TCMPL	TERR
0x7F	CHSTATUS3	7:0					CRCERR	FERR	BUSY	PEND
		7:0	RUNSTDBY						ENABLE	SWRST
0x80	CHCTRLA4	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
									CMD[1:0]	
0x84	CHCTRLB4	7:0								PRILVL[1:0]
0x85	CHPRILVL4	7:0								
0x86	CHEVCTRL4	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x87	...									
0x8B	Reserved									
0x8C	CHINTENCLR4	7:0						SUSP	TCMPL	TERR
0x8D	CHINTENSET4	7:0						SUSP	TCMPL	TERR
0x8E	CHINTFLAG4	7:0						SUSP	TCMPL	TERR
0x8F	CHSTATUS4	7:0					CRCERR	FERR	BUSY	PEND
		7:0	RUNSTDBY						ENABLE	SWRST
0x90	CHCTRLA5	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
									CMD[1:0]	
0x94	CHCTRLB5	7:0								PRILVL[1:0]
0x95	CHPRILVL5	7:0								
0x96	CHEVCTRL5	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x97	...									
0x9B	Reserved									
0x9C	CHINTENCLR5	7:0						SUSP	TCMPL	TERR
0x9D	CHINTENSET5	7:0						SUSP	TCMPL	TERR
0x9E	CHINTFLAG5	7:0						SUSP	TCMPL	TERR
0x9F	CHSTATUS5	7:0					CRCERR	FERR	BUSY	PEND
		7:0	RUNSTDBY						ENABLE	SWRST
0xA0	CHCTRLA6	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
									CMD[1:0]	
0xA4	CHCTRLB6	7:0								PRILVL[1:0]
0xA5	CHPRILVL6	7:0								
0xA6	CHEVCTRL6	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0xA7	...									
0xAB	Reserved									
0xAC	CHINTENCLR6	7:0						SUSP	TCMPL	TERR
0xAD	CHINTENSET6	7:0						SUSP	TCMPL	TERR
0xAE	CHINTFLAG6	7:0						SUSP	TCMPL	TERR
0xAF	CHSTATUS6	7:0					CRCERR	FERR	BUSY	PEND
		7:0	RUNSTDBY						ENABLE	SWRST
0xB0	CHCTRLA7	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
									CMD[1:0]	
0xB4	CHCTRLB7	7:0								PRILVL[1:0]
0xB5	CHPRILVL7	7:0								
0xB6	CHEVCTRL7	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0xB7	...									
0xBB	Reserved									
0xBC	CHINTENCLR7	7:0						SUSP	TCMPL	TERR
0xBD	CHINTENSET7	7:0						SUSP	TCMPL	TERR
0xBE	CHINTFLAG7	7:0						SUSP	TCMPL	TERR

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xBF	CHSTATUS7	7:0					CRCERR	FERR	BUSY	PEND
		7:0		RUNSTDBY					ENABLE	SWRST
0xC0	CHCTRLA8	15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0xC4	CHCTRLB8	7:0							CMD[1:0]	
0xC5	CHPRILVL8	7:0							PRILVL[1:0]	
0xC6	CHEVCTRL8	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0xC7	Reserved									
0xCB										
0xCC	CHINTENCLR8	7:0					SUSP	TCMPL	TERR	
0xCD	CHINTENSET8	7:0					SUSP	TCMPL	TERR	
0xCE	CHINTFLAG8	7:0					SUSP	TCMPL	TERR	
0xCF	CHSTATUS8	7:0				CRCERR	FERR	BUSY	PEND	
		7:0		RUNSTDBY					ENABLE	SWRST
0xD0	CHCTRLA9	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]		BURSTLEN[3:0]			
0xD4	CHCTRLB9	7:0						CMD[1:0]		
0xD5	CHPRILVL9	7:0						PRILVL[1:0]		
0xD6	CHEVCTRL9	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0xD7	Reserved									
0xDB										
0xDC	CHINTENCLR9	7:0					SUSP	TCMPL	TERR	
0xDD	CHINTENSET9	7:0					SUSP	TCMPL	TERR	
0xDE	CHINTFLAG9	7:0					SUSP	TCMPL	TERR	
0xDF	CHSTATUS9	7:0				CRCERR	FERR	BUSY	PEND	
		7:0		RUNSTDBY					ENABLE	SWRST
0xE0	CHCTRLA10	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]		BURSTLEN[3:0]			
0xE4	CHCTRLB10	7:0						CMD[1:0]		
0xE5	CHPRILVL10	7:0						PRILVL[1:0]		
0xE6	CHEVCTRL10	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0xE7	Reserved									
0xEB										
0xEC	CHINTENCLR10	7:0					SUSP	TCMPL	TERR	
0xED	CHINTENSET10	7:0					SUSP	TCMPL	TERR	
0xEE	CHINTFLAG10	7:0					SUSP	TCMPL	TERR	
0xEF	CHSTATUS10	7:0				CRCERR	FERR	BUSY	PEND	
		7:0		RUNSTDBY					ENABLE	SWRST
0xF0	CHCTRLA11	15:8			TRIGSRC[7:0]					
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]		BURSTLEN[3:0]			
0xF4	CHCTRLB11	7:0						CMD[1:0]		
0xF5	CHPRILVL11	7:0						PRILVL[1:0]		
0xF6	CHEVCTRL11	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0xF7	Reserved									
0xFB										
0xFC	CHINTENCLR11	7:0					SUSP	TCMPL	TERR	
0xFD	CHINTENSET11	7:0					SUSP	TCMPL	TERR	
0xFE	CHINTFLAG11	7:0					SUSP	TCMPL	TERR	
0xFF	CHSTATUS11	7:0				CRCERR	FERR	BUSY	PEND	

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0100	CHCTRLA12	7:0		RUNSTDBY					ENABLE	SWRST
		15:8								
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]				BURSTLEN[3:0]	
0x0104	CHCTRLB12	7:0							CMD[1:0]	
0x0105	CHPRILVL12	7:0							PRILVL[1:0]	
0x0106	CHEVCTRL12	7:0	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
0x0107	...									
0x010B	Reserved									
0x010C	CHINTENCLR12	7:0						SUSP	TCMPL	TERR
0x010D	CHINTENSET12	7:0						SUSP	TCMPL	TERR
0x010E	CHINTFLAG12	7:0						SUSP	TCMPL	TERR
0x010F	CHSTATUS12	7:0				CRCERR	FERR	BUSY	PEND	
0x0110	CHCTRLA13	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x0114	CHCTRLB13	7:0							CMD[1:0]	
0x0115	CHPRILVL13	7:0							PRILVL[1:0]	
0x0116	CHEVCTRL13	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0x0117	...									
0x011B	Reserved									
0x011C	CHINTENCLR13	7:0						SUSP	TCMPL	TERR
0x011D	CHINTENSET13	7:0						SUSP	TCMPL	TERR
0x011E	CHINTFLAG13	7:0						SUSP	TCMPL	TERR
0x011F	CHSTATUS13	7:0				CRCERR	FERR	BUSY	PEND	
0x0120	CHCTRLA14	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x0124	CHCTRLB14	7:0							CMD[1:0]	
0x0125	CHPRILVL14	7:0							PRILVL[1:0]	
0x0126	CHEVCTRL14	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0x0127	...									
0x012B	Reserved									
0x012C	CHINTENCLR14	7:0						SUSP	TCMPL	TERR
0x012D	CHINTENSET14	7:0						SUSP	TCMPL	TERR
0x012E	CHINTFLAG14	7:0						SUSP	TCMPL	TERR
0x012F	CHSTATUS14	7:0				CRCERR	FERR	BUSY	PEND	
0x0130	CHCTRLA15	7:0		RUNSTDBY					ENABLE	SWRST
		15:8				TRIGSRC[7:0]				
		23:16			TRIGACT[1:0]					
		31:24			THRESHOLD[1:0]			BURSTLEN[3:0]		
0x0134	CHCTRLB15	7:0							CMD[1:0]	
0x0135	CHPRILVL15	7:0							PRILVL[1:0]	
0x0136	CHEVCTRL15	7:0	EVOE	EVIE	EVOMODE[1:0]			EVACT[2:0]		
0x0137	...									
0x013B	Reserved									
0x013C	CHINTENCLR15	7:0						SUSP	TCMPL	TERR
0x013D	CHINTENSET15	7:0						SUSP	TCMPL	TERR
0x013E	CHINTFLAG15	7:0						SUSP	TCMPL	TERR
0x013F	CHSTATUS15	7:0				CRCERR	FERR	BUSY	PEND	

21.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

[21.5.7. Register Access Protection](#)

Preliminary

21.8.1 Control

Name: CTRL
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
Access					LVLENx3	LVLENx2	LVLENx1	LVLENx0
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access							DMAENABLE	SWRST
Reset							0	0

Bits 8, 9, 10, 11 – LVLENxx Priority Level x Enable

When this bit is set, all requests with the corresponding level will be fed into the arbiter block. When cleared, all requests with the corresponding level will be ignored.

For details on arbitration schemes, see *Arbitration* from Related Links.

These bits are not enable-protected.

Value	Description
0	Transfer requests for Priority level x will not be handled.
1	Transfer requests for Priority level x will be handled.

Bit 1 – DMAENABLE DMA Enable

Setting this bit will enable the DMA module.

Writing a '0' to this bit will disable the DMA module. When writing a '0' during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit when the DMAC module is disabled (DMAENABLE bit set to "0"), resets all registers in the DMAC (except DBGCTRL) to their initial state. If either the DMAC or CRC module is enabled, the Reset request will be ignored and the DMAC will return an access error.

Value	Description
0	There is no Reset operation ongoing.
1	A Reset operation is ongoing.

Related Links

[21.6.2.4. Arbitration](#)

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21.8.2 CRC Control

Name: CRCCTRL
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	CRCMODE[1:0]		CRCSRC[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CRCPOLY[1:0]					CRCBEATSIZE[1:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 15:14 – CRCMODE[1:0] CRC Operating Mode

These bits define the block transfer mode.

Value	Name	Description
0x0	DEFAULT	Default operating mode
0x1		Reserved
0x2	CRCMON	Memory CRC monitor operating mode
0x3	CRCGEN	Memory CRC generation operating mode

Bits 13:8 – CRCSRC[5:0] CRC Input Source

These bits select the input source for generating the CRC. The selected source is locked until either the CRC generation is completed or the CRC module is disabled. This means the CRCSRC cannot be modified when the CRC operation is ongoing. The lock is signaled by the CRCBUSY status bit. CRC generation complete is generated and signaled from the selected source when used with the DMA channel.

Value	Name	Description
0x00	NOACT	No action
0x01	IO	I/O interface
0x02 - 0x1F		Reserved
0x20	CH0	DMA channel 0
0x21	CH1	DMA channel 1
0x22	CH2	DMA channel 2
0x23	CH3	DMA channel 3
0x24	CH4	DMA channel 4
0x25	CH5	DMA channel 5
0x26	CH6	DMA channel 6
0x27	CH7	DMA channel 7
0x28	CH8	DMA channel 8
0x29	CH9	DMA channel 9
0x2A	CH10	DMA channel 10
0x2B	CH11	DMA channel 11
0x2C	CH12	DMA channel 12
0x2D	CH13	DMA channel 13
0x2E	CH14	DMA channel 14
0x2F	CH15	DMA channel 15
0x30	CH16	DMA channel 16
0x31	CH17	DMA channel 17
0x32	CH18	DMA channel 18
0x33	CH19	DMA channel 19

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Value	Name	Description
0x34	CH20	DMA channel 20
0x35	CH21	DMA channel 21
0x36	CH22	DMA channel 22
0x37	CH23	DMA channel 23
0x38	CH24	DMA channel 24
0x39	CH25	DMA channel 25
0x3A	CH26	DMA channel 26
0x3B	CH27	DMA channel 27
0x3C	CH28	DMA channel 28
0x3D	CH29	DMA channel 29
0x3E	CH30	DMA channel 30
0x3F	CH31	DMA channel 31

Bits 3:2 – CRCPOLY[1:0] CRC Polynomial Type

These bits select the CRC polynomial type.

Value	Name	Description
0x0	CRC16	CRC-16 (CRC-CCITT)
0x1	CRC32	CRC32 (IEEE 802.3)
0x2–0x3		Reserved

Bits 1:0 – CRCBEATSIZE[1:0] CRC Beat Size

These bits define the size of the data transfer for each bus access when the CRC is used with I/O interface.

Value	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	HWORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
0x3		Reserved

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21.8.3 CRC Data Input

Name: CRCDATAIN
Offset: 0x04
Reset: 0x00000000
Property: PAC Write Protection

Bit	31	30	29	28	27	26	25	24
CRCDATAIN[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CRCDATAIN[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CRCDATAIN[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CRCDATAIN[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CRCDATAIN[31:0] CRC Data Input

These bits store the data for which the CRC checksum is computed. A new CRC checksum is ready (CRCBEAT+ 1) clock cycles after the CRCDATAIN register is written.

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21.8.4 CRC Checksum

Name: CRCCHKSUM
Offset: 0x08
Reset: 0x00000000
Property: PAC Write Protection, Enable-Protected

The CRCCHKSUM represents the 16- or 32-bit checksum value and the generated CRC. The register is reset to zero by default, but it is possible to reset all bits to one by writing the CRCCHKSUM register directly. It is possible to write this register only when the CRC module is disabled. If CRC-32 is selected and the CRC Status Busy flag is cleared (i.e., CRC generation is completed or aborted), the bit reversed (bit 31 is swapped with bit 0, bit 30 with bit 1, etc.) and complemented result will be read from CRCCHKSUM. If CRC-16 is selected or the CRC Status Busy flag is set (i.e., CRC generation is ongoing), CRCCHKSUM will contain the actual content.

Bit	31	30	29	28	27	26	25	24
CRCCHKSUM[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
CRCCHKSUM[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
CRCCHKSUM[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
CRCCHKSUM[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CRCCHKSUM[31:0] CRC Checksum

These bits store the generated CRC result. The 16 MSB bits are always read zero when CRC-16 is enabled.

21.8.5 CRC Status

Name: CRCSTATUS
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access						CRCERR	CRCZERO	CRCBUSY
Reset						R	R	R/W

Bit 2 – CRCERR CRC Error

This bit is read '1' when the memory CRC monitor detects data corruption.

Bit 1 – CRCZERO CRC Zero

This bit is cleared when a new CRC source is selected.

This bit is set when the CRC generation is complete and the CRC Checksum is zero.

Bit 0 – CRCBUSY CRC Module Busy

When used with an I/O interface ([CRCCTRL.CRCSRC=0x1](#)):

- This bit is cleared by writing a '1' to it
- This bit is set when the CRC Data Input (CRCDATAIN) register is written
- Writing a '1' to this bit will clear the CRC Module Busy bit
- Writing a '0' to this bit has no effect

When used with a DMA channel ([CRCCTRL.CRCSRC=0x20..0x3F](#)):

- This bit is cleared when the corresponding DMA channel is disabled
- This bit is set when the corresponding DMA channel is enabled
- Writing a '1' to this bit has no effect
- Writing a '0' to this bit has no effect

Related Links

[21.7. DMAC Register Summary](#)

21.8.6 Debug Control

Name: DBGCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGRUN 0

Bit 0 – DBGRUN Debug Run

This bit is not reset by a Software Reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The DMAC is halted when the CPU is halted by an external debugger.
1	The DMAC continues normal operation when the CPU is halted by an external debugger.

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21.8.7 Software Trigger Control

Name: SWTRIGCTRL
Offset: 0x10
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SWTRIGN[15:0] Channel n Software Trigger [n = 15..0]

This bit is cleared when the Channel Pending bit in the Channel Status register (CHSTATUS.PEND) for the corresponding channel is either set, or by writing a '1' to it. See CHSTATUS in the DMAC Register Summary from Related Links.

This bit is set if CHSTATUS.PEND is already '1' when writing a '1' to that bit. See CHSTATUS in the DMAC Register Summary from Related Links.

Writing a '0' to this bit will clear the bit.

Writing a '1' to this bit will generate a DMA software trigger on channel x, if CHSTATUS.PEND=0 for channel x.

CHSTATUS.PEND will be set and SWTRIGN will remain cleared. See CHSTATUS in the DMAC Register Summary from Related Links.

Related Links

[21.7. DMAC Register Summary](#)

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21.8.8 Priority Control 0

Name: PRICTRL0
Offset: 0x14
Reset: 0x40404040
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	RRLVLEN3	QOS03[1:0]		LVLPRI3[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	RRLVLEN2	QOS02[1:0]		LVLPRI2[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	RRLVLEN1	QOS01[1:0]		LVLPRI1[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RRLVLEN0	QOS00[1:0]		LVLPRI0[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

Bits 7, 15, 23, 31 – RRLVLEN Level Round-Robin Scheduling Enable

For details on arbitration schemes, see *Arbitration* from Related Links.

Value	Description
0	Static arbitration scheme for channels with level 0 priority.
1	Round-robin arbitration scheme for channels with level 0 priority.

Bits 5:6, 13:14, 21:22, 29:30 – QOS Level Quality of Service

0x0	DISABLE Background (no sensitive operation)
0x1	LOW Sensitive to bandwidth
0x2	MEDIUM Sensitive to latency
0x3	Critical Latency

Bits 0:4, 8:12, 16:20, 24:28 – LVLPRI Level Channel Priority Number

When round-robin arbitration is enabled (PRICTRL0.RRLVLEN0=1) for priority level 0, this register holds the channel number of the last DMA channel being granted access as the active channel with priority level 0.

When static arbitration is enabled (PRICTRL0.RRLVLEN0=0) for priority level 0, and the value of this bit group is non-zero, it will not affect the static priority scheme.

This bit group is not reset when round-robin arbitration gets disabled (PRICTRL0.RRLVLEN0 written to '0').

Related Links

[21.6.2.4. Arbitration](#)

21.8.9 Interrupt Pending

Name: INTPEND
Offset: 0x20
Reset: 0x0000
Property: -

This register allows the user to identify the lowest DMA channel with pending interrupt.

An interrupt that handles several channels should consult the INTPEND register to find out which channel number has priority (ignoring/filtering each channel that has its own interrupt line). An interrupt dedicated to only one channel must not use the INTPEND register.

Bit	15	14	13	12	11	10	9	8
	PEND	BUSY	FERR	CRCERR		SUSP	TCMPL	TERR
Access	R	R	R	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
					ID[4:0]			
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – PEND Pending

This bit will read '1' when the channel selected by Channel ID field (ID) is pending.

Bit 14 – BUSY Busy

This bit will read '1' when the channel selected by Channel ID field (ID) is busy.

Bit 13 – FERR Fetch Error

This bit will read '1' when the channel selected by Channel ID field (ID) fetched an invalid descriptor.

Bit 12 – CRCERR CRC Error

This bit will read '1' when the channel selected by Channel ID field (ID) has a CRC Error Status Flag bit set, and is set when the CRC monitor detects data corruption.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn), where n is determined by the Channel ID bit field (ID).

Bit 10 – SUSP Channel Suspend

This bit will read '1' when the channel selected by Channel ID field (ID) has pending Suspend interrupt.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn), where n is determined by the Channel ID bit field (ID).

Bit 9 – TCMPL Transfer Complete

This bit will read '1' when the channel selected by Channel ID field (ID) has pending Transfer Complete interrupt.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn), where n is determined by the Channel ID bit field (ID).

Bit 8 – TERR Transfer Error

This bit will read '1' when the channel selected by Channel ID field (ID) has pending Transfer Error interrupt.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn), where n is determined by the Channel ID bit field (ID).

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Bits 4:0 – ID[4:0] Channel ID

These bits store the lowest channel number with pending interrupts. The number is valid if Suspend (SUSP), Transfer Complete (TCMPL) or Transfer Error (TERR) bits are set. The Channel ID field is refreshed when a new channel (with channel number less than the current one) with pending interrupts is detected, or when the application clears the corresponding channel interrupt sources. When no pending channels interrupts are available, these bits will always return zero value when read.

When the bits are written, indirect access to the corresponding Channel Interrupt Flag register is enabled.

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21.8.10 Interrupt Status

Name: INTSTATUS
Offset: 0x24
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CHINTn[15:0] Channel n Pending Interrupt [n=15..0]

This bit is set when Channel n has a pending interrupt/the interrupt request is received.

This bit is cleared when the corresponding Channel n interrupts are disabled or the interrupts sources are cleared.

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21.8.11 Busy Channels

Name: BUSYCH
Offset: 0x28
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUSYCHn[15:0] Busy Channel n [x=15..0]

This bit is cleared when the channel trigger action for DMA channel n is complete, when a bus error for DMA channel n is detected, or when DMA channel n is disabled.

This bit is set when DMA channel n starts a DMA transfer.

21.8.12 Pending Channels

Name: PENDCH
Offset: 0x2C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
PENDCH15	PENDCH14	PENDCH13	PENDCH12	PENDCH11	PENDCH10	PENDCH9	PENDCH8	
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
PENDCH7	PENDCH6	PENDCH5	PENDCH4	PENDCH3	PENDCH2	PENDCH1	PENDCH0	
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 – PENDCH_n Pending Channel n [n=0..15]

This bit is cleared when trigger execution defined by channel trigger action settings for DMA channel n is started, when a bus error for DMA channel n is detected or when DMA channel n is disabled. For details on trigger action settings, refer to CHCTRLB.TRIGACT.

This bit is set when a transfer is pending on DMA channel n.

21.8.13 Active Channel and Levels

Name: ACTIVE
Offset: 0x30
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
BTCNT[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
BTCNT[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
ABUSY ID[4:0]								
Access	R			R	R	R	R	R
Reset	0			0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
LVLEXx3 LVLEXx2 LVLEXx1 LVLEXx0								
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bits 31:16 – BTCNT[15:0] Active Channel Block Transfer Count

These bits hold the 16-bit block transfer count of the ongoing transfer. This value is stored in the active channel and written back in the corresponding Write-Back channel memory location when the arbiter grants a new channel access. The value is valid only when the active channel Active Busy flag (ABUSY) is set.

Bit 15 – ABUSY Active Channel Busy

This bit is cleared when the active transfer count is written back in the write-back memory section.

This bit is set when the next descriptor transfer count is read from the write-back memory section.

Bits 12:8 – ID[4:0] Active Channel ID

These bits hold the channel index currently stored in the active channel registers. The value is updated each time the arbiter grants a new channel transfer access request.

Bits 0, 1, 2, 3 – LVLEXxx Level x Channel Trigger Request Executing [x=3..0]

This bit is set when a level-x channel trigger request is executing or pending.

This bit is cleared when no request is pending or being executed.

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21.8.14 Descriptor Memory Section Base Address

Name: BASEADDR
Offset: 0x34
Reset: 0x00000000
Property: PAC Write Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
BASEADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
BASEADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
BASEADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
BASEADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BASEADDR[31:0] Descriptor Memory Base Address

These bits store the Descriptor memory section base address. The value must be 64-bit aligned.

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21.8.15 Write-Back Memory Section Base Address

Name: WRBADDR
Offset: 0x38
Reset: 0x00000000
Property: PAC Write Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
WRBADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
WRBADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
WRBADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
WRBADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – WRBADDR[31:0] Write-Back Memory Base Address

These bits store the Write-Back memory base address. The value must be 64-bit aligned.

21.8.16 Channel Control A

Name: CHCTRLA
Offset: 0x40 + n*0x10 [n=0..15]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
			THRESHOLD[1:0]		BURSTLEN[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
			TRIGACT[1:0]					
Access			R/W	R/W				
Reset			0	0				
Bit	15	14	13	12	11	10	9	8
			TRIGSRC[7:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	R/W
Reset		0					0	0

Bits 29:28 – THRESHOLD[1:0] FIFO Threshold

These bits define the threshold from which the DMA starts to write to the destination. These bits have no effect in the case of single beat transfers.

These bits are not enable-protected.

Value	Name	Description
0x0	1BEAT	Destination write starts after each beat source address read
0x1	2BEATS	Destination write starts after 2-beats source address read
0x2	4BEATS	Destination write starts after 4-beats source address read
0x3	8BEATS	Destination write starts after 8-beats source address read

Bits 27:24 – BURSTLEN[3:0] Burst Length

These bits define the burst mode.

These bits are not enable-protected.

Value	Name	Description
0x0	SINGLE	Single-beat burst
0x1	2BEAT	2-beats burst length
0x2	3BEAT	3-beats burst length
0x3	4BEAT	4-beats burst length
0x4	5BEAT	5-beats burst length
0x5	6BEAT	6-beats burst length
0x6	7BEAT	7-beats burst length
0x7	8BEAT	8-beats burst length
0x8	9BEAT	9-beats burst length
0x9	10BEAT	10-beats burst length
0xA	11BEAT	11-beats burst length
0xB	12BEAT	12-beats burst length
0xC	13BEAT	13-beats burst length
0xD	14BEAT	14-beats burst length

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Value	Name	Description
0xE	15BEAT	15-beats burst length
0xF	16BEAT	16-beats burst length

Bits 21:20 – TRIGACT[1:0] Trigger Action

These bits define the trigger action used for a transfer.

These bits are not enable-protected.

Value	Name	Description
0x0	BLOCK	One trigger required for each block transfer
0x1		Reserved
0x2	BURST	One trigger required for each burst transfer
0x3	TRANSACTION	One trigger required for each transaction

Bits 15:8 – TRIGSRC[7:0] Trigger Source

These bits define the peripheral that will be the source of a trigger.

Table 21-2. Triggers Map

Number	Name
0	Unused (Tied to 1'b0)
1	RTC_DMAC_ID_TIMESTAMP
2	DSU_DMAC_ID_DCC0
3	DSU_DMAC_ID_DCC1
4	SERCOM0_DMAC_ID_RX
5	SERCOM0_DMAC_ID_TX
6	SERCOM1_DMAC_ID_RX
7	SERCOM1_DMAC_ID_TX
8	SERCOM2_DMAC_ID_RX
9	SERCOM2_DMAC_ID_TX
10	SERCOM3_DMAC_ID_RX
11	SERCOM3_DMAC_ID_TX
12	TCC0_DMAC_ID_OVF
13	TCC0_DMAC_ID_MC_0
14	TCC0_DMAC_ID_MC_1
15	TCC0_DMAC_ID_MC_2
16	TCC0_DMAC_ID_MC_3
17	TCC0_DMAC_ID_MC_4
18	TCC0_DMAC_ID_MC_5
19	TCC1_DMAC_ID_OVF
20	TCC1_DMAC_ID_MC_0
21	TCC1_DMAC_ID_MC_1
22	TCC1_DMAC_ID_MC_2
23	TCC1_DMAC_ID_MC_3
24	TCC1_DMAC_ID_MC_4
25	TCC1_DMAC_ID_MC_5
26	TCC2_DMAC_ID_OVF
27	TCC2_DMAC_ID_MC_0
28	TCC2_DMAC_ID_MC_1
29	TC0_DMAC_ID_OVF
30	TC0_DMAC_ID_MC_0
31	TC0_DMAC_ID_MC_1
32	TC1_DMAC_ID_OVF
33	TC1_DMAC_ID_MC_0
34	TC1_DMAC_ID_MC_1
35	TC2_DMAC_ID_OVF
36	TC2_DMAC_ID_MC_0
37	TC2_DMAC_ID_MC_1

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.....continued

Number	Name
38	TC3_DMAC_ID_OVF
39	TC3_DMAC_ID_MC_0
40	TC3_DMAC_ID_MC_1
41	AES_DMAC_ID_WR
42	AES_DMAC_ID_RD
43	QSPI_DMAC_ID_RX
44	QSPI_DMAC_ID_TX

Bit 6 – RUNSTDBY Channel run in standby

This bit is used to keep the DMAC channel running in standby mode.

This bit is not enable-protected.

Value	Description
0	The DMAC channel is halted in standby.
1	The DMAC channel continues to run in standby.

Bit 1 – ENABLE Channel Enable

Writing a '0' to this bit during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

Writing a '1' to this bit will enable the DMA channel.

This bit is not enable-protected.

Value	Description
0	DMA channel is disabled.
1	DMA channel is enabled.

Bit 0 – SWRST Channel Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the channel registers to their initial state. The bit can be set when the channel is disabled (ENABLE=0). Writing a '1' to this bit will be ignored as long as ENABLE=1. This bit is automatically cleared when the reset is completed.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

21.8.17 Channel Control B

Name: CHCTRLB
Offset: 0x44 + n*0x10 [n=0..15]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	CMD[1:0]
Access									R/W
Reset									0 R/W 0

Bits 1:0 – CMD[1:0] Software Command

These bits define the software commands. See *Channel Suspend* and *Channel Resume and Next Suspend Skip* from Related Links.

These bits are not enable-protected.

CMD[1:0]	Name	Description
0x0	NOACT	No action
0x1	SUSPEND	Channel suspend operation
0x2	RESUME	Channel resume operation
0x3	-	Reserved

Related Links

[21.6.3.3. Channel Suspend](#)

[21.6.3.4. Channel Resume and Next Suspend Skip](#)

21.8.18 Channel Priority Level

Name: CHPRILVL
Offset: 0x45 + n*0x10 [n=0..15]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	PRILVL[1:0]
Access									R/W
Reset									0 R/W 0

Bits 1:0 – PRILVL[1:0] Channel Priority Level

These bits define the priority level used for the DMA channel. The available levels are shown below, where a high level has priority over a low level. These bits are not enable-protected.

Value	Name	Description
0x0	LVL0	Channel Priority Level 0 (Lowest Level)
0x1	LVL1	Channel Priority Level 1
0x2	LVL2	Channel Priority Level 2
0x3	LVL3	Channel Priority Level 3 (Highest Level)

21.8.19 Channel Event Control

Name: CHEVCTRL
Offset: 0x46 + n*0x10 [n=0..15]
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	EVOE	EVIE	EVOMODE[1:0]				EVACT[2:0]	
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 7 – EVOE Channel Event Output Enable

This bit indicates if the Channel event generation is enabled. The event will be generated for every condition defined in the Channel Event Output Selection bits (CHEVCTRL.EVOMODE).

Value	Description
0	Channel event generation is disabled.
1	Channel event generation is enabled.

Bit 6 – EVIE Channel Event Input Enable

Value	Description
0	Channel event action will not be executed on any incoming event.
1	Channel event action will be executed on any incoming event.

Bits 5:4 – EVOMODE[1:0] Channel Event Output Mode

These bits define the channel event output selection. For more details on event output generation, see *Event Output Selection* from Related Links.

Value	Name	Description
0x0	DEFAULT	Block event output selection. See BTCTRL.EVOSEL for available selections.
0x1	TRIGACT	Ongoing trigger action
0x2–0x3		Reserved

Bits 2:0 – EVACT[2:0] Channel Event Input Action

These bits define the event input action. The action is executed only if the corresponding EVIE bit in the CHEVCTRL register of the channel is set. For more details on event actions, see *Event Input Actions* from Related Links.. These bits are available only for channels with event input support.

Value	Name	Description
0x0	NOACT	No action
0x1	TRIG	Transfer and periodic transfer trigger
0x2	CTRIG	Conditional transfer trigger
0x3	CBLOCK	Conditional block transfer
0x4	SUSPEND	Channel suspend operation
0x5	RESUME	Channel resume operation
0x6	SSKIP	Skip next block suspend action
0x7	INCPRI	Increase priority

Related Links

[21.6.3.5. Event Input Actions](#)

[21.6.3.6. Event Output Selection](#)

21.8.20 Channel Interrupt Enable Clear

Name: CHINTENCLR
Offset: 0x4C + n*0x10 [n=0..15]
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Channel Interrupt Enable Set (CHINTENSET) register.

Bit	7	6	5	4	3	2	1	0
Access						SUSP	TCMPL	TERR
Reset						0	0	0

Bit 2 – SUSP Channel Suspend Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Suspend Interrupt Enable bit, which disables the Channel Suspend interrupt.

Value	Description
0	The Channel Suspend interrupt is disabled.
1	The Channel Suspend interrupt is enabled.

Bit 1 – TCMPL Channel Transfer Complete Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Transfer Complete Interrupt Enable bit, which disables the Channel Transfer Complete interrupt.

Value	Description
0	The Channel Transfer Complete interrupt is disabled. When block action is set to none, the TCMPL flag will not be set when a block transfer is completed.
1	The Channel Transfer Complete interrupt is enabled.

Bit 0 – TERR Channel Transfer Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Transfer Error Interrupt Enable bit, which disables the Channel Transfer Error interrupt.

Value	Description
0	The Channel Transfer Error interrupt is disabled.
1	The Channel Transfer Error interrupt is enabled.

21.8.21 Channel Interrupt Enable Set

Name: CHINTENSET
Offset: 0x4D + n*0x10 [n=0..15]
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Channel Interrupt Enable Clear (CHINTENCLR) register.

Bit	7	6	5	4	3	2	1	0
Access						SUSP	TCMPL	TERR
Reset						0	0	0

Bit 2 – SUSP Channel Suspend Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Suspend Interrupt Enable bit, which enables the Channel Suspend interrupt.

Value	Description
0	The Channel Suspend interrupt is disabled.
1	The Channel Suspend interrupt is enabled.

Bit 1 – TCMPL Channel Transfer Complete Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Transfer Complete Interrupt Enable bit, which enables the Channel Transfer Complete interrupt.

Value	Description
0	The Channel Transfer Complete interrupt is disabled.
1	The Channel Transfer Complete interrupt is enabled.

Bit 0 – TERR Channel Transfer Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Transfer Error Interrupt Enable bit, which enables the Channel Transfer Error interrupt.

Value	Description
0	The Channel Transfer Error interrupt is disabled.
1	The Channel Transfer Error interrupt is enabled.

21.8.22 Channel Interrupt Flag Status and Clear

Name: CHINTFLAG
Offset: 0x4E + n*0x10 [n=0..15]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
Access						SUSP	TCMPL	TERR
Reset						R/W	R/W	R/W

Bit 2 – SUSP Channel Suspend

This flag is cleared by writing a '1' to it.

This flag is set when a block transfer with suspend block action is completed, when a software suspend command is executed, when a suspend event is received or when an invalid descriptor is fetched by the DMA.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Suspend interrupt flag for the corresponding channel.

For details on available software commands, see *CHCTRLB* in the *DMAC Register Summary* from Related Links.

For details on available event input actions, see *CHCTRLB* in the *DMAC Register Summary* from Related Links.

For details on available block actions, see *BTCTRL* in the *DMAC Register Summary (SRAM)* from Related Links.

Bit 1 – TCMPL Channel Transfer Complete

This flag is cleared by writing a '1' to it.

This flag is set when a block transfer is completed and the corresponding interrupt block action is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transfer Complete interrupt flag for the corresponding channel.

Bit 0 – TERR Channel Transfer Error

This flag is cleared by writing a '1' to it.

This flag is set when a bus error is detected during a beat transfer or when the DMAC fetches an invalid descriptor.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transfer Error interrupt flag for the corresponding channel.

Related Links

[21.9. DMAC Register Summary \(SRAM\)](#)

[21.7. DMAC Register Summary](#)

21.8.23 Channel Status

Name: CHSTATUS
Offset: 0x4F + n*0x10 [n=0..15]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
Access					CRCERR	FERR	BUSY	PEND
Reset					R/W	R	R	R

Bit 3 – CRCERR Channel CRC Error

This bit is set when the CRC monitor detects data corruption. This bit is cleared by writing '1' to it, or by clearing the CRC Error bit in the INTPEND register (INTPEND.CRCERR). See *INTPEND* in the *DMAC Register Summary* from Related Links.

Bit 2 – FERR Channel Fetch Error

This bit is cleared when a software resume command is executed.

This bit is set when an invalid descriptor is fetched.

Bit 1 – BUSY Channel Busy

This bit is cleared when the channel trigger action is completed, when a bus error is detected or when the channel is disabled.

This bit is set when the DMA channel starts a DMA transfer.

Bit 0 – PEND Channel Pending

This bit is cleared when the channel trigger action is started, when a bus error is detected or when the channel is disabled. For details on trigger action settings, see *CHCTRLB* in the *DMAC Register Summary* from Related Links.

This bit is set when a transfer is pending on the DMA channel, as soon as the transfer request is received.

Related Links

[21.7. DMAC Register Summary](#)

21.9 DMAC Register Summary (SRAM)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	BTCTRL	7:0				BLOCKACT[1:0]		EVOSEL[1:0]		VALID
		15:8		STEPSIZE[2:0]		STEPSEL	DSTINC	SRCINC		BEATSIZE[1:0]
0x02	BTCNT	7:0				BTCNT[7:0]				
		15:8				BTCNT[15:8]				
0x04	SRCADDR	7:0				SRCADDR[7:0]				
		15:8				SRCADDR[15:8]				
		23:16				SRCADDR[23:16]				
		31:24				SRCADDR[31:24]				
0x08	DSTADDR	7:0				DSTADDR[7:0]				
		15:8				DSTADDR[15:8]				
		23:16				DSTADDR[23:16]				
		31:24				DSTADDR[31:24]				
0x0C	DESCADDR	7:0				DESCADDR[7:0]				
		15:8				DESCADDR[15:8]				
		23:16				DESCADDR[23:16]				
		31:24				DESCADDR[31:24]				

21.10 Register Description - SRAM

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

[21.5.7. Register Access Protection](#)

21.10.1 Block Transfer Control

Name: BTCTRL
Offset: 0x00
Reset: 0x0000
Property: -

The BTCTRL register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	15	14	13	12	11	10	9	8
	STEP SIZE[2:0]			STEPSEL	DSTINC	SRCINC	BEAT SIZE[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				BLOCKACT[1:0]	EVOSEL[1:0]		VALID	
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 15:13 – STEP SIZE[2:0] Address Increment Step Size

These bits select the address increment step size. The setting apply to source or destination address, depending on STEPSEL setting.

Value	Name	Description
0x0	X1	Next ADDR = ADDR + (Beat size in byte) * 1
0x1	X2	Next ADDR = ADDR + (Beat size in byte) * 2
0x2	X4	Next ADDR = ADDR + (Beat size in byte) * 4
0x3	X8	Next ADDR = ADDR + (Beat size in byte) * 8
0x4	X16	Next ADDR = ADDR + (Beat size in byte) * 16
0x5	X32	Next ADDR = ADDR + (Beat size in byte) * 32
0x6	X64	Next ADDR = ADDR + (Beat size in byte) * 64
0x7	X128	Next ADDR = ADDR + (Beat size in byte) * 128

Bit 12 – STEPSEL Step Selection

This bit selects if source or destination addresses are using the step size settings.

Value	Name	Description
0x0	DST	Step size settings apply to the destination address
0x1	SRC	Step size settings apply to the source address

Bit 11 – DSTINC Destination Address Increment Enable

Writing a '0' to this bit will disable the destination address incrementation. The address will be kept fixed during the data transfer.

Writing a '1' to this bit will enable the destination address incrementation. By default, the destination address is incremented by 1. If the STEPSEL bit is cleared, flexible step-size settings are available in the STEPSIZE register.

Value	Description
0	The Destination Address Increment is disabled
1	The Destination Address Increment is enabled

Bit 10 – SRCINC Source Address Increment Enable

Writing a '0' to this bit will disable the source address incrementation. The address will be kept fixed during the data transfer.

Writing a '1' to this bit will enable the source address incrementation. By default, the source address is incremented by 1. If the STEPSEL bit is set, flexible step-size settings are available in the STEPSIZE register.

Value	Description
0	The Source Address Increment is disabled
1	The Source Address Increment is enabled

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Bits 9:8 – BEATSIZE[1:0] Beat Size

These bits define the size of one beat. A beat is the size of one data transfer bus access, and the setting apply to both read and write accesses.

Value	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	HWORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
other		Reserved

Bits 4:3 – BLOCKACT[1:0] Block Action

These bits define what actions the DMAC should take after a block transfer has completed.

BLOCKACT[1:0]	Name	Description
0x0	NOACT	Channel will be disabled if it is the last block transfer in the transaction
0x1	INT	Channel will be disabled if it is the last block transfer in the transaction and block interrupt
0x2	SUSPEND	Channel suspend operation is completed
0x3	BOTH	Both channel suspend operation and block interrupt

Bits 2:1 – EVOSEL[1:0] Event Output Selection

These bits define the event output selection.

EVOSEL[1:0]	Name	Description
0x0	DISABLE	Event generation disabled
0x1	BLOCK	Event strobe when block transfer complete
0x2		Reserved
0x3	BEAT	Event strobe when beat transfer complete

Bit 0 – VALID Descriptor Valid

Writing a '0' to this bit in the Descriptor or Write-Back memory will suspend the DMA channel operation when fetching the corresponding descriptor.

The bit is automatically cleared in the Write-Back memory section when channel is aborted, when an error is detected during the block transfer, or when the block transfer is completed.

Value	Description
0	The descriptor is not valid
1	The descriptor is valid

Related Links

[21.9. DMAC Register Summary \(SRAM\)](#)

21.10.2 Block Transfer Count

Name: BTCNT
Offset: 0x02
Property: -

The BTCNT register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	15	14	13	12	11	10	9	8
BTCNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BTCNT[7:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BTCNT[15:0] Block Transfer Count

This bit group holds the 16-bit block transfer count.

During a transfer, the internal counter value is decremented by one after each beat transfer. The internal counter is written to the corresponding write-back memory section for the DMA channel when the DMA channel loses priority, is suspended or gets disabled. The DMA channel can be disabled by a complete transfer, a transfer error or by software.

21.10.3 Block Transfer Source Address

Name: SRCADDR
Offset: 0x04
Property: -

The SRCADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	31	30	29	28	27	26	25	24
	SRCADDR[31:24]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	23	22	21	20	19	18	17	16
	SRCADDR[23:16]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	15	14	13	12	11	10	9	8
	SRCADDR[15:8]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	7	6	5	4	3	2	1	0
	SRCADDR[7:0]							
Access	-	-	-	-	-	-	-	-
Reset								

Bits 31:0 – SRCADDR[31:0] Transfer Source Address

This bit field holds the block transfer source address.

When source address incrementation is disabled (BTCTRL.SRCINC = 0), SRCADDR corresponds to the last beat transfer address in the block transfer.

When source address incrementation is enabled (BTCTRL.SRCINC = 1), SRCADDR is calculated as follows:
If BTCTRL.STEPSEL = 1:

$$\text{SRCADDR} = \text{SRCADDR}_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1) \cdot 2^{\text{STEPSIZE}}$$

If BTCTRL.STEPSEL = 0:

$$\text{SRCADDR} = \text{SRCADDR}_{\text{START}} + \text{BTCNT} \cdot (\text{BEATSIZE} + 1)$$

- SRCADDR_{START} is the source address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

21.10.4 Block Transfer Destination Address

Name: DSTADDR
Offset: 0x08
Property: -

The DSTADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	31	30	29	28	27	26	25	24
Access	DSTADDR[31:24]							
Reset	-	-	-	-	-	-	-	-
Bit	23	22	21	20	19	18	17	16
Access	DSTADDR[23:16]							
Reset	-	-	-	-	-	-	-	-
Bit	15	14	13	12	11	10	9	8
Access	DSTADDR[15:8]							
Reset	-	-	-	-	-	-	-	-
Bit	7	6	5	4	3	2	1	0
Access	DSTADDR[7:0]							
Reset	-	-	-	-	-	-	-	-

Bits 31:0 – DSTADDR[31:0] Transfer Destination Address

This bit field holds the block transfer destination address.

When destination address incrementation is disabled (BTCTRL.DSTINC = 0), DSTADDR corresponds to the last beat transfer address in the block transfer.

When destination address incrementation is enabled (BTCTRL.DSTINC = 1), DSTADDR is calculated as follows:

If BTCTRL.STEPSEL = 1:

$$DSTADDR = DSTADDR_{START} + BTCNT \cdot (BEATSIZE + 1)$$

If BTCTRL.STEPSEL = 0:

$$DSTADDR = DSTADDR_{START} + BTCNT \cdot (BEATSIZE + 1) \cdot 2^{STEP SIZE}$$

- DSTADDR_{START} is the destination address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

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21.10.5 Next Descriptor Address

Name: DESCADDR
Offset: 0x0C
Property: -

The DESCADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	31	30	29	28	27	26	25	24
	DESCADDR[31:24]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	23	22	21	20	19	18	17	16
	DESCADDR[23:16]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	15	14	13	12	11	10	9	8
	DESCADDR[15:8]							
Access	-	-	-	-	-	-	-	-
Reset								
Bit	7	6	5	4	3	2	1	0
	DESCADDR[7:0]							
Access	-	-	-	-	-	-	-	-
Reset								

Bits 31:0 – DESCADDR[31:0] Next Descriptor Address

This bit group holds the SRAM address of the next descriptor. The value must be 128-bit aligned. If the value of this SRAM register is 0x00000000, the transaction will be terminated when the DMAC tries to load the next transfer descriptor.

22. EIC – External Interrupt Controller

22.1 Overview

The External Interrupt Controller (EIC) allows external pins to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt on rising, falling, both edges, or on high or low levels. Each external pin has a configurable filter to remove spikes. Also, each external pin can be configured to be asynchronous in order to wake-up the device from Sleep modes where all clocks have been disabled. External pins can generate an event.

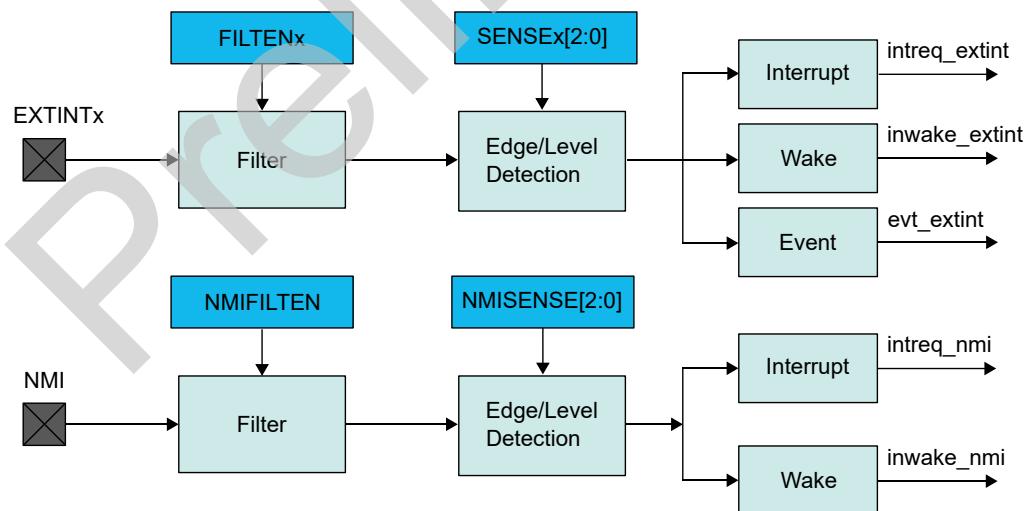
A separate Non-Maskable Interrupt (NMI) is supported. It has properties similar to the other external interrupts, but is connected to the NMI request of the CPU, enabling it to interrupt any other Interrupt mode.

22.2 Features

- Up to four external pins (EXTINT_x), plus one non-maskable pin (NMI)
- Dedicated, Individually Maskable Interrupt for Each Pin
- Interrupt on Rising, Falling, or Both Edges
- Synchronous or Asynchronous Edge Detection mode
- Interrupt pin Debouncing
- Interrupt on High or Low Levels
- Asynchronous Interrupts for Sleep Modes Without Clock
- Filtering of External Pins
- Event Generation from EXTINT_x

22.3 Block Diagram

Figure 22-1. EIC Block Diagram



22.4 Signal Description

Signal Name	Type	Description
EXTINT[3..0]	Digital Input	External interrupt pin

.....continued

Signal Name	Type	Description
NMI	Digital Input	Non-maskable interrupt pin

One signal may be available on several pins.

22.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

22.5.1 I/O Lines

Using the EIC's I/O lines requires the I/O pins to be configured.

22.5.2 Power Management

All interrupts are available down to STANDBY Sleep mode, but the EIC can be configured to automatically mask some interrupts in order to prevent device wake-up.

The EIC will continue to operate in any Sleep mode where the selected source clock is running. The EIC's interrupts can be used to wake up the device from Sleep modes. Events connected to the Event System can trigger other operations in the system without exiting Sleep modes.

22.5.3 Clocks

The EIC bus clock (PB1_CLK) can be enabled and disabled by the CRU, the default state of PB1_CLK can be found in the CRU and PMD registers.

Some optional functions need a peripheral clock, which can either be a generic clock (GCLK_EIC, for wider frequency selection) or a Ultra Low-Power 32 KHz clock (CLK_ULP32K, for highest power efficiency). One of the clock sources must be configured and enabled before using the peripheral:

GCLK_EIC is configured and enabled in the CRU registers, see *Clock and Reset (CRU)* from Related Links.

CLK_ULP32K is provided by the internal Ultra Low-Power (OSCULP32K) Oscillator in the CRU module.

Both GCLK_EIC and CLK_ULP32K are asynchronous to the user interface clock (PB1_CLK). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains.

Related Links

[12. Clock and Reset Unit \(CRU\)](#)

22.5.4 DMA

Not applicable.

22.5.5 Interrupts

There are several interrupt request lines, some (the number depends on the product variant) for the external interrupts (EXTINT) and one for Non-Maskable Interrupt (NMI).

Each EXTINT interrupt request line is connected to the interrupt controller. Using the EIC interrupt requires the interrupt controller to be configured first.

The NMI interrupt request line is connected to the interrupt controller, but does not require the interrupt to be configured.

22.5.6 Events

The events are connected to the Event System. Using the events requires the Event System to be configured first.

Related Links

[27. Event System \(EVSYS\)](#)

22.5.7 Debug Operation

When the CPU is halted in Debug mode, the EIC continues normal operation. If the EIC is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

22.5.8 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Flag Status and Clear register (INTFLAG)
- Non-Maskable Interrupt Flag Status and Clear register (NMIFLAG)

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

PAC write protection does not apply to accesses through an external debugger.

22.5.9 Analog Connections

Not applicable.

22.6 Functional Description

22.6.1 Principle of Operation

The EIC detects edge or level condition to generate interrupts to the CPU interrupt controller or events to the Event System. Each external interrupt pin (EXTINT) can be filtered using majority vote filtering, clocked by GCLK_EIC or by CLK_ULP32K.

22.6.2 Basic Operation

22.6.2.1 Initialization

The EIC must be initialized in the following order:

1. If required, configure the NMI by writing the Non-Maskable Interrupt Control register (NMICTRL)
2. Enable GCLK_EIC or CLK_ULP32K when one of the following configuration is selected:
 - The NMI uses edge detection or filtering.
 - One EXTINT uses filtering.
 - One EXTINT uses synchronous edge detection.
 - One EXTINT uses debouncing.

GCLK_EIC is used when a frequency higher than 32 KHz is required for filtering.

CLK_ULP32K is recommended when power consumption is the priority. For CLK_ULP32K write a '1' to the Clock Selection bit in the Control A register (CTRLA.CKSEL).

3. Configure the EIC input sense and filtering by writing the Configuration register (CONFIG).
4. Optionally, enable the asynchronous mode.
5. Optionally, enable the debouncer mode.
6. Enable the EIC by writing a '1' to CTRLA.ENABLE.

The following bits are enable-protected, meaning that it can only be written when the EIC is disabled (CTRLA.ENABLE=0):

- Clock Selection bit in Control A register (CTRLA.CKSEL)

The following registers are enable-protected:

- Event Control register (EVCTRL)
- Configuration register (CONFIG)
- External Interrupt Asynchronous Mode register (ASYNCH)

- Debouncer Enable register (DEBOUNCEN)
- Debounce Prescaler register (DPRESCALER)

Enable-protected bits in the CTRLA register can be written at the same time when setting CTRLA.ENABLE to '1', but not at the same time as CTRLA.ENABLE is being cleared.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

See *NMICTRL*, *CTRLA*, *CONFIG*, *ASYNCH*, *DEBOUNCEN*, *DPRESCALER*, *EVCTRL* registers in the *EIC Register Summary* from Related Links.

Related Links

[22.7. EIC Register Summary](#)

22.6.2.2 Enabling, Disabling, and Resetting

The EIC is enabled by writing a '1' to the Enable bit in Control A register (CTRLA.ENABLE). The EIC is disabled by writing CTRLA.ENABLE to '0'.

The EIC is reset by setting the Software Reset bit in the Control register (CTRLA.SWRST). All registers in the EIC will be reset to their initial state, and the EIC will be disabled.

22.6.3 External Pin Processing

Each external pin can be configured to generate an interrupt/event on edge detection (rising, falling or both edges) or level detection (high or low). The sense of external interrupt pins is configured by writing the Input Sense x bits in the Config n register (CONFIG.SENSEx). The corresponding interrupt flag (INTFLAG.EXTINT[x]) in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition is met.

When the interrupt flag has been cleared in edge-sensitive mode, INTFLAG.EXTINT[x] will only be set if a new interrupt condition is met.

In level-sensitive mode, when interrupt has been cleared, INTFLAG.EXTINT[x] will be set immediately if the EXTINTx pin still matches the interrupt condition.

Each external pin can be filtered by a majority vote filtering, clocked by GCLK_EIC or CLK_ULP32K. Filtering is enabled if bit Filter Enable x in the Configuration n register (CONFIG.FILTENx) is written to '1'. The majority vote filter samples the external pin three times with GCLK_EIC or CLK_ULP32K and outputs the value when two or more samples are equal.

Table 22-1. Majority Vote Filter

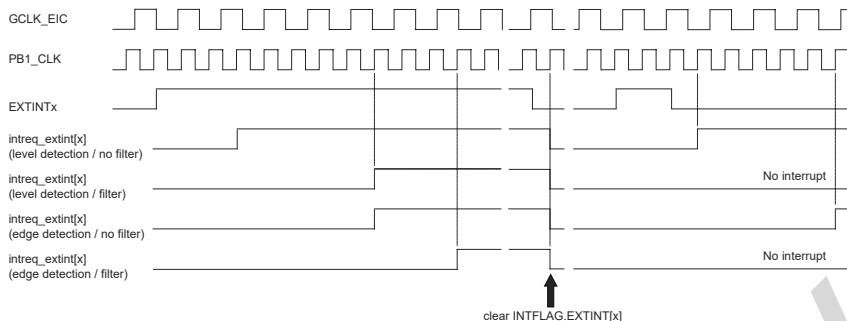
Samples [0, 1, 2]	Filter Output
[0,0,0]	0
[0,0,1]	0
[0,1,0]	0
[0,1,1]	1
[1,0,0]	0
[1,0,1]	1
[1,1,0]	1
[1,1,1]	1

When an external interrupt is configured for level detection and when filtering is disabled, detection is done asynchronously. Level detection and asynchronous edge detection does not require GCLK_EIC or CLK_ULP32K, but interrupt and events can still be generated.

If filtering or synchronous edge detection or debouncing is enabled, the EIC automatically requests GCLK_EIC or CLK_ULP32K to operate. The selection between these two clocks is done by writing the Clock Selection bits in the Control A register (CTRLA.CKSEL). GCLK_EIC must be enabled in the CRU. In these modes the external pin

is sampled at the EIC clock rate, thus pulses with duration lower than two EIC clock periods may not be properly detected.

Figure 22-2. Interrupt Detection Latency by modes (Rising Edge)



The detection latency depends on the detection mode.

Table 22-2. Detection Latency

Detection mode	Latency (worst case)
Level without filter	Five PB1_CLK periods
Level with filter	Four GCLK_EIC/CLK_ULP32K periods + five PB1_CLK periods
Edge without filter	Four GCLK_EIC/CLK_ULP32K periods + five PB1_CLK periods
Edge with filter	Six GCLK_EIC/CLK_ULP32K periods + five PB1_CLK periods

22.6.4 Additional Features

22.6.4.1 Non-Maskable Interrupt (NMI)

The non-maskable interrupt pin can also generate an interrupt on edge or level detection, but it is configured with the dedicated NMI Control register (NMICTRL). To select the sense for NMI, write to the NMISENSE bit group in the NMI Control register (NMICTRL.NMISENSE). NMI filtering is enabled by writing a '1' to the NMI Filter Enable bit (NMICTRL.NMIFILTEN).

If edge detection or filtering is required, enable GCLK_EIC or CLK_ULP32K.

NMI detection is enabled only by the NMICTRL.NMISENSE value, and the EIC module is not required to be enabled.

When an NMI is detected, the Non-maskable Interrupt flag in the NMI Flag Status and Clear register is set (NMIFLAG.NMI). NMI interrupt generation is always enabled, and NMIFLAG.NMI generates an interrupt request when set.

22.6.4.2 Asynchronous Edge Detection Mode (No Debouncing)

The EXTINT edge detection operates synchronously or asynchronously, as selected by the Asynchronous Control Mode bit for external pin x in the External Interrupt Asynchronous Mode register (ASYNCH.ASYNCH[x]). The EIC edge detection is operated synchronously when the Asynchronous Control Mode bit (ASYNCH.ASYNCH[x]) is '0' (default value). It is operated asynchronously when ASYNCH.ASYNCH[x] is written to '1'.

In Synchronous Edge Detection Mode, the external interrupt (EXTINT) or the non-maskable interrupt (NMI) pins are sampled using the EIC clock as defined by the Clock Selection bit in the Control A register (CTRLA.CKSEL). The External Interrupt flag (INTFLAG.EXTINT[x]) or Non-Maskable Interrupt flag (NMIFLAG.NMI) is set when the last sampled state of the pin differs from the previously sampled state. The EIC clock is needed in this mode.

The Synchronous Edge Detection Mode can be used in Idle and Standby sleep modes.

In Asynchronous Edge Detection Mode, the external interrupt (EXTINT) pins or the non-maskable interrupt (NMI) pins set the External Interrupt flag or Non-Maskable Interrupt flag (INTFLAG.EXTINT[x] or NMIFLAG) directly. The EIC clock is not needed in this mode.

Note: The asynchronous edge detection mode can be used in Idle and Standby sleep modes.

22.6.4.3 Interrupt Pin Debouncing

The external interrupt pin (EXTINT) edge detection can use a debouncer to improve input noise immunity. When selected, the debouncer can work in the synchronous mode or the asynchronous mode, depending on the configuration of the ASYNCH.ASYNCH[x] bit for the pin. The debouncer uses the EIC clock as defined by the bit CTRLA.CKSEL to clock the debouncing circuitry. The debouncing time frame is set with the debouncer prescaler DPRESCALER.PRESCALERn, which provides the *low frequency clock* tick that is used to reject higher frequency signals.

The debouncing mode for pin EXTINT x can be selected only if the Sense bits in the Configuration y register (CONFIG.SENSEx) are set to RISE, FALL or BOTH. If the debouncing mode for pin EXTINT x is selected, the filter mode for that pin (CONFIG.FILTENx) can not be selected.

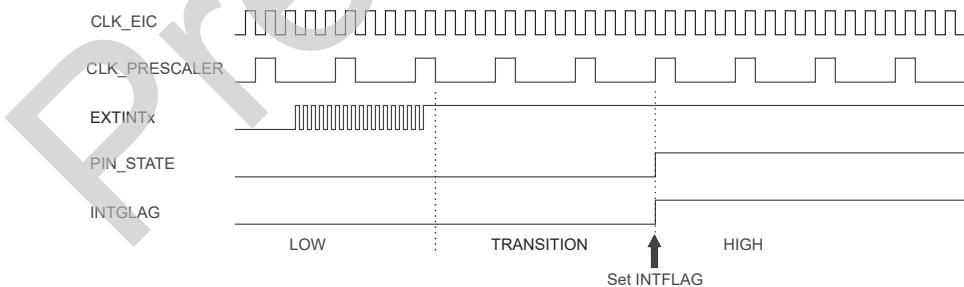
The debouncer manages an internal “valid pin state” that depends on the external interrupt (EXTINT) pin transitions, the debouncing mode and the debouncer prescaler frequency. The valid pin state reflects the pin value after debouncing. The external interrupt pin (EXTINT) is sampled continuously on EIC clock. The sampled value is evaluated on each *low frequency clock* tick to detect a transitional edge when the sampled value is different of the current valid pin state. The sampled value is evaluated on each EIC clock when DPRESCALER.TICKON=0 or on each *low frequency clock* tick when DPRESCALER.TICKON=1, to detect a bounce when the sampled value is equal to the current valid pin state. Transitional edge detection increments the transition counter of the EXTINT pin, while bounce detection resets the transition counter. The transition counter must exceed the transition count threshold as defined by the DPRESCALER.STATESn bitfield. In the synchronous mode the threshold is 4 when DPRESCALER.STATESn=0 or 8 when DPRESCALER.STATESn=1. In the asynchronous mode the threshold is 4.

The valid pin state for the pins can be accessed by reading the register PINSTATE for both synchronous or asynchronous debouncing mode.

Synchronous edge detection In this mode the external interrupt (EXTINT) pin is sampled continuously on EIC clock.

1. A pin edge transition will be validated when the sampled value is consistently different of the current valid pin state for 4 (or 8 depending on bit DPRESCALER.STATESn) consecutive ticks of the low frequency clock.
2. Any pin sample, at the *low frequency clock* tick rate, with a value opposite to the current valid pin state will increment the transition counter.
3. Any pin sample, at EIC clock rate (when DPRESCALER.TICKON=0) or the *low frequency clock* tick (when DPRESCALER.TICKON=1), with a value identical to the current valid pin state will return the transition counter to zero.
4. When the transition counter meets the count threshold, the pin edge transition is validated and the pin state PINSTATE.PINSTATE[x] is changed to the detected level.
5. The external interrupt flag (INTFLAG.EXTINT[x]) is set when the pin state PINSTATE.PINSTATE[x] is changed.

Figure 22-3. EXTINT Pin Synchronous Debouncing (Rising Edge)



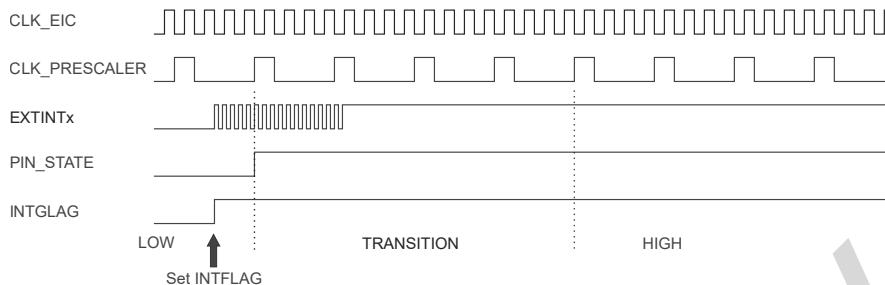
In the synchronous edge detection mode, the EIC clock is required. The synchronous edge detection mode can be used in Idle and Standby sleep modes.

Asynchronous edge detection In this mode, the external interrupt (EXTINT) pin directly drives an asynchronous edges detector which triggers any rising or falling edge on the pin:

1. Any edge detected that indicates a transition from the current valid pin state will immediately set the valid pin state PINSTATE.PINSTATE[x] to the detected level.
2. The external interrupt flag (INTFLAG.EXTINT[x]) is immediately changed.
3. The edge detector will then be idle until no other rising or falling edge transition is detected during 4 consecutive ticks of the low frequency clock.

4. Any rising or falling edge transition detected during the idle state will return the transition counter to 0.
5. After 4 consecutive ticks of the low frequency clock without bounce detected, the edge detector is ready for a new detection.

Figure 22-4. EXTINT Pin Asynchronous Debouncing (Rising Edge)



In this mode, the EIC clock is requested. The asynchronous edge detection mode can be used in Idle and Standby sleep modes.

22.6.5 DMA Operation

Not applicable.

22.6.6 Interrupts

The EIC has the following interrupt sources:

- External interrupt (EXTINT_x) pins. See *Basic Operation* from Related Links.
- Non-maskable interrupt (NMI) pin. See *Non-Maskable Interrupt (NMI)* from Related Links

Each interrupt source has an associated Interrupt flag. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when an Interrupt condition occurs (NMIFLAG for NMI). Each interrupt, except NMI, can be individually enabled by setting the corresponding bit in the Interrupt Enable Set register (INTENSET = 1), and disabled by setting the corresponding bit in the Interrupt Enable Clear register (INTENCLR = 1). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the EIC is reset. See the INTFLAG register for details on how to clear Interrupt flags. The EIC has one interrupt request line for each external interrupt (EXTINT_x) and one line for NMI. The user must read the INTFLAG (or NMIFLAG) register to determine which Interrupt condition is present.

Notes:

1. Interrupts must be globally enabled for interrupt requests to be generated.
2. If an external interrupt (EXTINT) is common on two or more I/O pins, only one will be active (the first one programmed).

Related Links

[22.6.2. Basic Operation](#)

[22.6.4.1. Non-Maskable Interrupt \(NMI\)](#)

22.6.7 Events

The EIC can generate the following output events:

- External event from pin (EXTINT0-3).

Setting an Event Output Control register (EVCTRL.EXTINTEO) enables the corresponding output event. Clearing this bit disables the corresponding output event. For more details on configuring the event system, see *Event System (EVSYS)* from Related Links.

When the condition on pin EXTINT_x matches the configuration in the CONFIG register, the corresponding event is generated, if enabled.

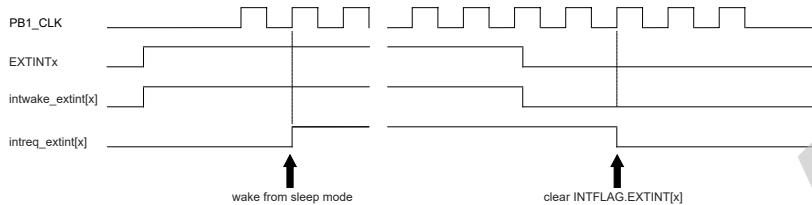
Related Links

[27. Event System \(EVSYS\)](#)

22.6.8 Sleep Mode Operation

In sleep modes, an EXTINT x pin can wake up the device if the corresponding condition matches the configuration in the CONFIG register, and the corresponding bit in the Interrupt Enable Set register (INTENSET) is written to '1'.

Figure 22-5. Wake-up Operation Example (High-Level Detection, No Filter, Interrupt Enable Set)



22.6.9 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in control register (CTRLA.SWRST)
- Enable bit in control register (CTRLA.ENABLE)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

See *CTRLA* from Related Links.

Related Links

[22.8.1. CTRLA](#)

22.7 EIC Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0				CKSEL			ENABLE	SWRST
0x01	NMICTRL	7:0				NMIASYNCH	NMIFILTEN		NMISENSE[2:0]	
0x02	NMIFLAG	7:0								NMI
0x03	Reserved									
0x04	SYNCBUSY	7:0							ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x08	EVCTRL	7:0					EXTINTEO[3:0]			
		15:8								
		23:16								
		31:24								
0x0C	INTENCLR	7:0					EXTINT[3:0]			
		15:8								
		23:16								
		31:24								
0x10	INTENSET	7:0					EXTINT[3:0]			
		15:8								
		23:16								
		31:24								
0x14	INTFLAG	7:0					EXTINT[3:0]			
		15:8								
		23:16								
		31:24								
0x18	ASYNCH	7:0					ASYNCH[3:0]			
		15:8								
		23:16								
		31:24								
0x1C	CONFIG	7:0	FILTEN1		SENSE1[2:0]	FILTEN0		SENSE0[2:0]		
		15:8	FILTEN3		SENSE3[2:0]	FILTEN2		SENSE2[2:0]		
		23:16								
		31:24								
0x20 ... 0x2F	Reserved									
0x30	DEBOUNCEN	7:0					DEBOUNCEN[3:0]			
		15:8								
		23:16								
		31:24								
0x34	DPRESCALER	7:0	STATES1		PRESCALER1[2:0]	STATES0		PRESCALERO[2:0]		
		15:8								
		23:16							TICKON	
		31:24								
0x38	PINSTATE	7:0					PINSTATE[3:0]			
		15:8								
		23:16								
		31:24								

22.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

PIC32CX-BZ2 and WBZ45 Family

EIC – External Interrupt Controller

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

Preliminary

22.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
				CKSEL			ENABLE	SWRST
Access				RW			RW	W
Reset				0			0	0

Bit 4 – CKSEL Clock Selection

The EIC can be clocked either by GCLK_EIC (when a frequency higher than 32.768 KHz is required for filtering) or by CLK_ULP32K (when power consumption is the priority).

This bit is not Write-Synchronized.

Value	Description
0	The EIC is clocked by GCLK_EIC.
1	The EIC is clocked by CLK_ULP32K.

Bit 1 – ENABLE Enable

Due to synchronization there is a delay between writing to CTRLA.ENABLE until the peripheral is enabled/disabled.

The value written to CTRLA.ENABLE will read back immediately and the Enable bit in the Synchronization Busy register will be set (SYNCBUSY.ENABLE=1). SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

Value	Description
0	The EIC is disabled.
1	The EIC is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the EIC to their initial state, and the EIC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

This bit is not Enable-Protected.

This bit is Write-Synchronized.

Value	Description
0	There is no ongoing reset operation.
1	The reset operation is ongoing.

22.8.2 Non-Maskable Interrupt Control

Name: NMICTRL
Offset: 0x01
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				NMISYNCH	NMIFILTEN		NMISENSE[2:0]	
Access				R/W	R/W	R/W	R/W	R/W

Value	Description
0	The NMI edge detection is synchronously operated.
1	The NMI edge detection is asynchronously operated.

Bit 4 – NMISYNCH NMI Asynchronous Edge Detection Mode

The NMI edge detection can be operated synchronously or asynchronously to the EIC clock.

Value	Description
0	NMI filter is disabled.
1	NMI filter is enabled.

Bit 3 – NMIFILTEN Non-Maskable Interrupt Filter Enable

Value	Description
0	NMI filter is disabled.
1	NMI filter is enabled.

Bits 2:0 – NMISENSE[2:0] Non-Maskable Interrupt Sense Configuration

These bits define on which edge or level the NMI triggers.

Value	Name	Description
0x0	NONE	No detection
0x1	RISE	Rising-edge detection
0x2	FALL	Falling-edge detection
0x3	BOTH	Both-edge detection
0x4	HIGH	High-level detection
0x5	LOW	Low-level detection
0x6 – 0x7	-	Reserved

22.8.3 Non-Maskable Interrupt Flag Status and Clear

Name: NMIFLAG
Offset: 0x2
Reset: 0x00

Bit	7	6	5	4	3	2	1	0	NMI
Access									RW
Reset									0

Bit 0 – NMI Non-Maskable Interrupt

This flag is cleared by writing a '1' to it.

This flag is set when the NMI pin matches the NMI sense configuration, and will generate an interrupt request.

Writing a '0' to this bit has no effect.

22.8.4 Synchronization Busy

Name: SYNCBUSY
Offset: 0x04
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access							R	R
Reset							0	0

Bit 1 – ENABLE Enable Synchronization Busy Status

Value	Description
0	Write synchronization for CTRLA.ENABLE bit is complete.
1	Write synchronization for CTRLA.ENABLE bit is ongoing.

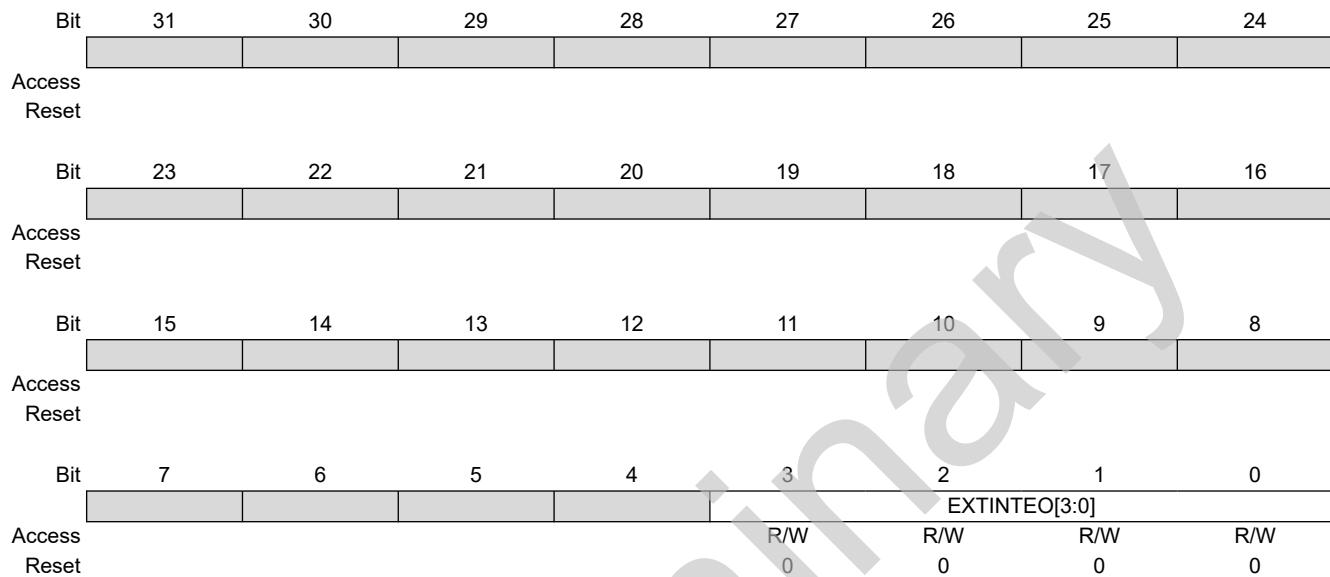
Bit 0 – SWRST Software Reset Synchronization Busy Status

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	Write synchronization for CTRLA.SWRST bit is complete.
1	Write synchronization for CTRLA.SWRST bit is ongoing.

22.8.5 Event Control

Name: EVCTRL
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected



Bits 3:0 – EXTINTEO[3:0] External Interrupt Event Output Enable

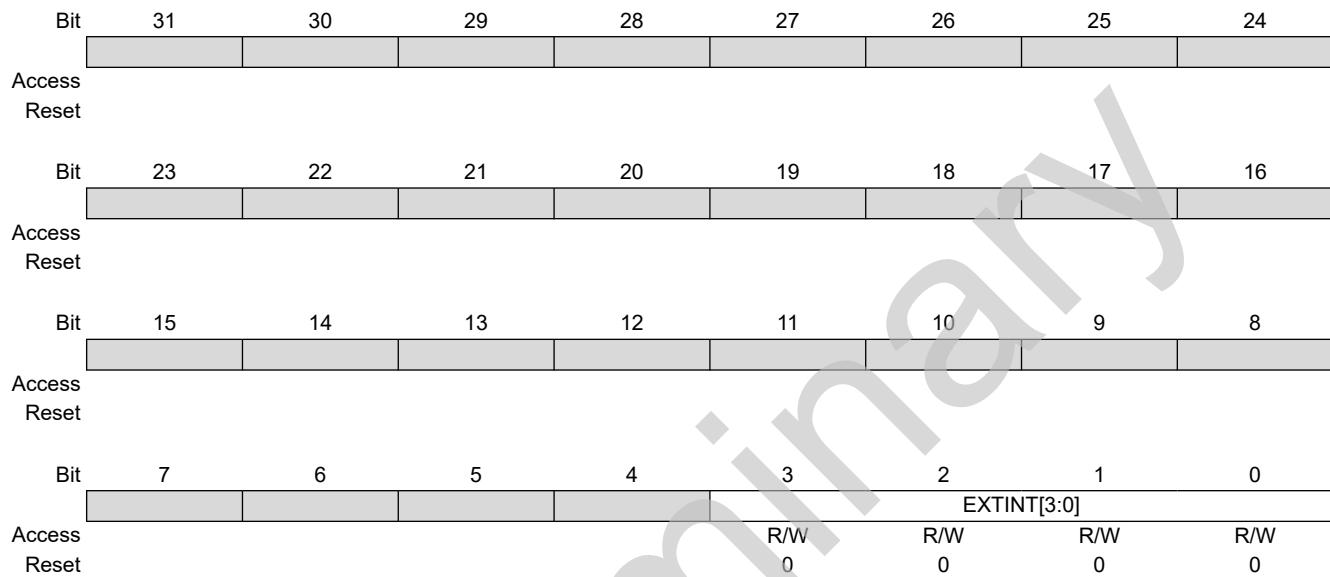
The bit x of EXTINTEO enables the event associated with the EXTINT_x pin.

Value	Description
0	Event from pin EXTINT _x is disabled.
1	Event from pin EXTINT _x is enabled and will be generated when EXTINT _x pin matches the external interrupt sensing configuration.

22.8.6 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x0C
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).



Bits 3:0 – EXTINT[3:0] External Interrupt Enable

The bit x of EXTINT disables the interrupt associated with the EXTINT_x pin.

Writing a '0' to bit x has no effect.

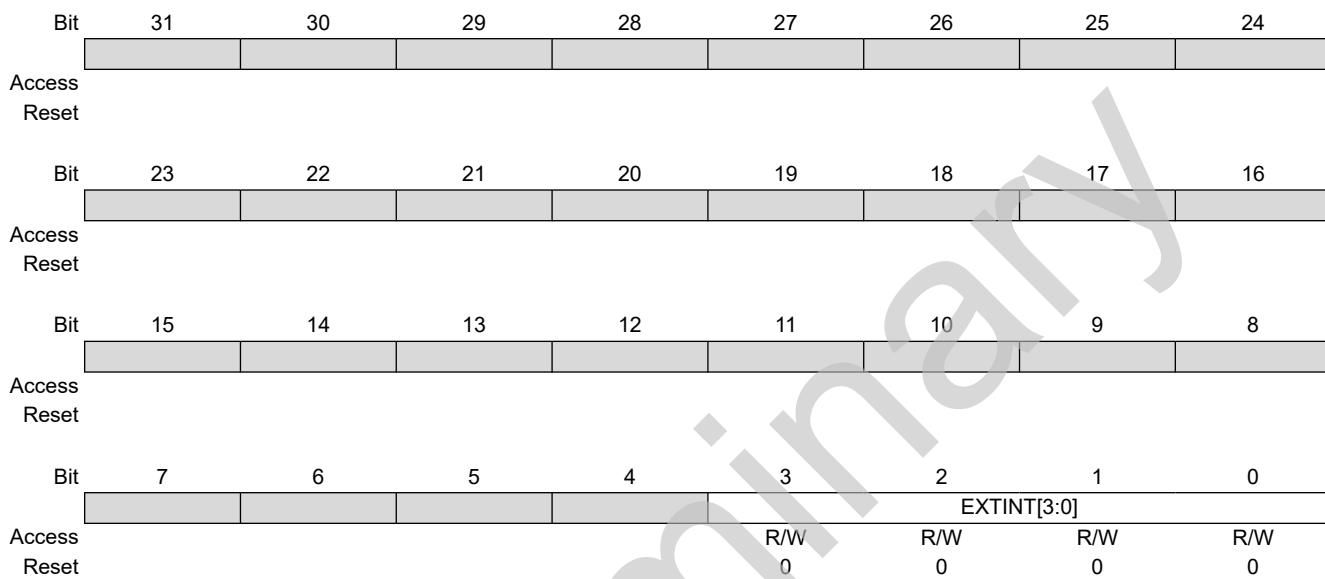
Writing a '1' to bit x will clear the External Interrupt Enable bit x, which disables the external interrupt EXTINT_x.

Value	Description
0	The external interrupt x is disabled.
1	The external interrupt x is enabled.

22.8.7 Interrupt Enable Set

Name: INTENSET
Offset: 0x10
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.



Bits 3:0 – EXTINT[3:0] External Interrupt Enable

The bit x of EXTINT enables the interrupt associated with the EXTINT_x pin.

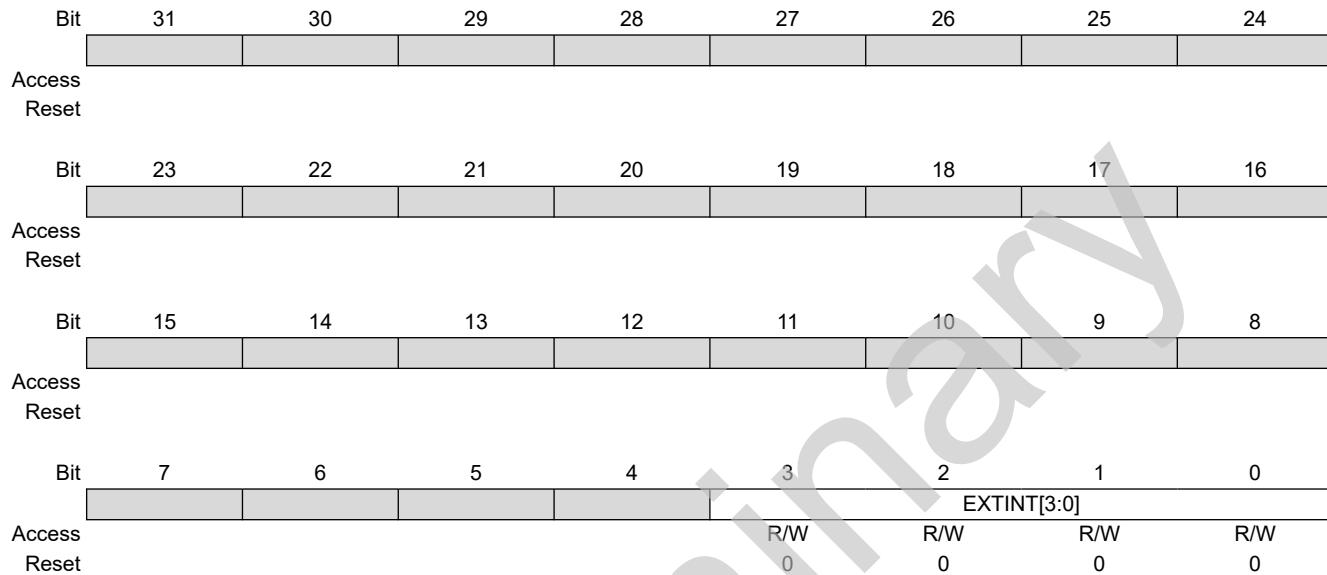
Writing a '0' to bit x has no effect.

Writing a '1' to bit x will set the External Interrupt Enable bit x, which enables the external interrupt EXTINT_x.

Value	Description
0	The external interrupt x is disabled.
1	The external interrupt x is enabled.

22.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x14
Reset: 0x00000000
Property: -



Bits 3:0 – EXTINT[3:0] External Interrupt

The flag bit x is cleared by writing a '1' to it.

This flag is set when EXTINT_x pin matches the external interrupt sense configuration and will generate an interrupt request if INTENCLR/SET.EXTINT[x] is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the External Interrupt x flag.

22.8.9 External Interrupt Asynchronous Mode

Name: ASYNCH
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
					ASYNCH[3:0]			
Access					RW	RW	RW	RW
Reset					0	0	0	0

Bits 3:0 – ASYNCH[3:0] Asynchronous Edge Detection Mode

The bit x of ASYNCH set the Asynchronous Edge Detection Mode for the interrupt associated with the EXTINT_x pin.

Value	Description
0	The EXTINT _x edge detection is synchronously operated.
1	The EXTINT _x edge detection is asynchronously operated.

22.8.10 External Interrupt Sense Configuration

Name: CONFIG
Offset: 0x1C
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	FILTEN3		SENSE3[2:0]		FILTEN2		SENSE2[2:0]	
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FILTEN1		SENSE1[2:0]		FILTEN0		SENSE0[2:0]	
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 3, 7, 11, 15 – FILTENx Filter Enable x [x=3..0]

Note: The filter must be disabled if the asynchronous detection is enabled.

Value	Description
0	Filter is disabled for EXTINT[x] input.
1	Filter is enabled for EXTINT[x] input.

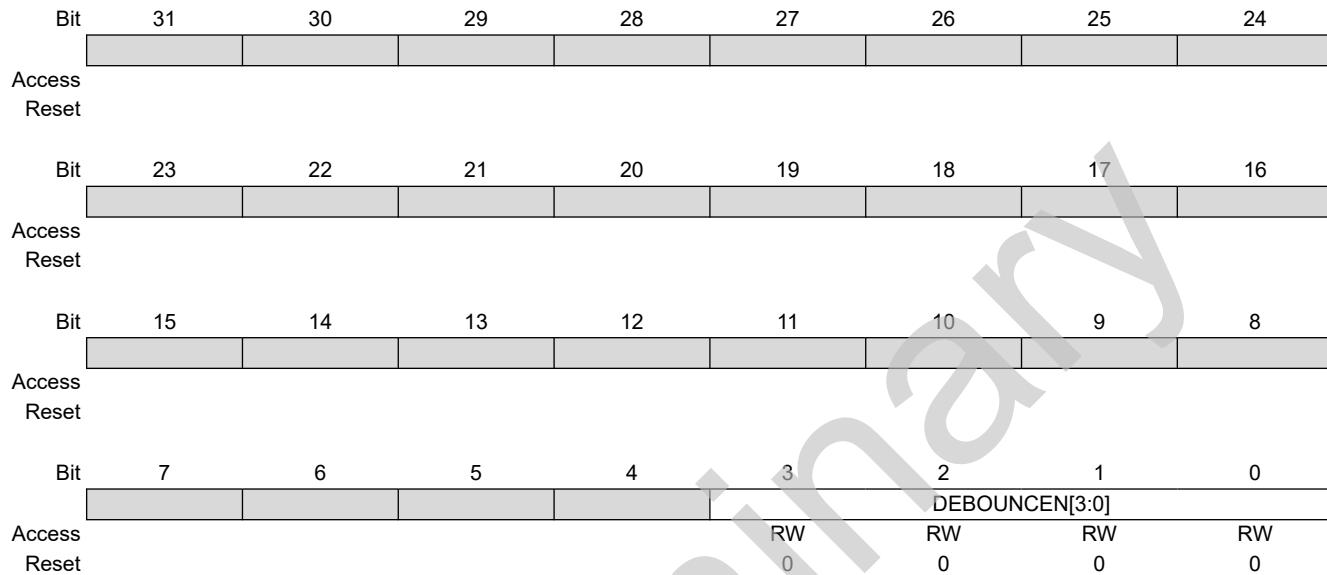
Bits 0:2, 4:6, 8:10, 12:14 – SENSEx Input Sense Configuration x [x=3..0]

These bits define on which edge or level the interrupt or event for EXTINT[x] will be generated.

Value	Name	Description
0x0	NONE	No detection
0x1	RISE	Rising-edge detection
0x2	FALL	Falling-edge detection
0x3	BOTH	Both-edge detection
0x4	HIGH	High-level detection
0x5	LOW	Low-level detection
0x6 – 0x7	-	Reserved

22.8.11 Debouncer Enable

Name: DEBOUNCEN
Offset: 0x30
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected



Bits 3:0 – DEBOUNCEN[3:0] Debouncer Enable

The bit x of DEBOUNCEN set the Debounce mode for the interrupt associated with the EXTINT_x pin.

Value	Description
0	The EXTINT x edge input is not debounced.
1	The EXTINT x edge input is debounced.

22.8.12 Debouncer Prescaler

Name: DPRESCALER
Offset: 0x34
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								RW
Reset								0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	RW							
Reset	0	0	0	0	0	0	0	0

Bit 16 – TICKON Pin Sampler frequency selection

This bit selects the clock used for the sampling of bounce during transition detection.

Value	Description
0	The bounce sampler is using GCLK_EIC.
1	The bounce sampler is using the low frequency clock.

Bits 3, 7 – STATESx Debouncer number of states x

This bit selects the number of samples by the debouncer low frequency clock needed to validate a transition from current pin state to next pin state in synchronous debouncing mode for pins EXTINT[7+(8x):8x].

Value	Description
0	The number of low frequency samples is 3.
1	The number of low frequency samples is 7.

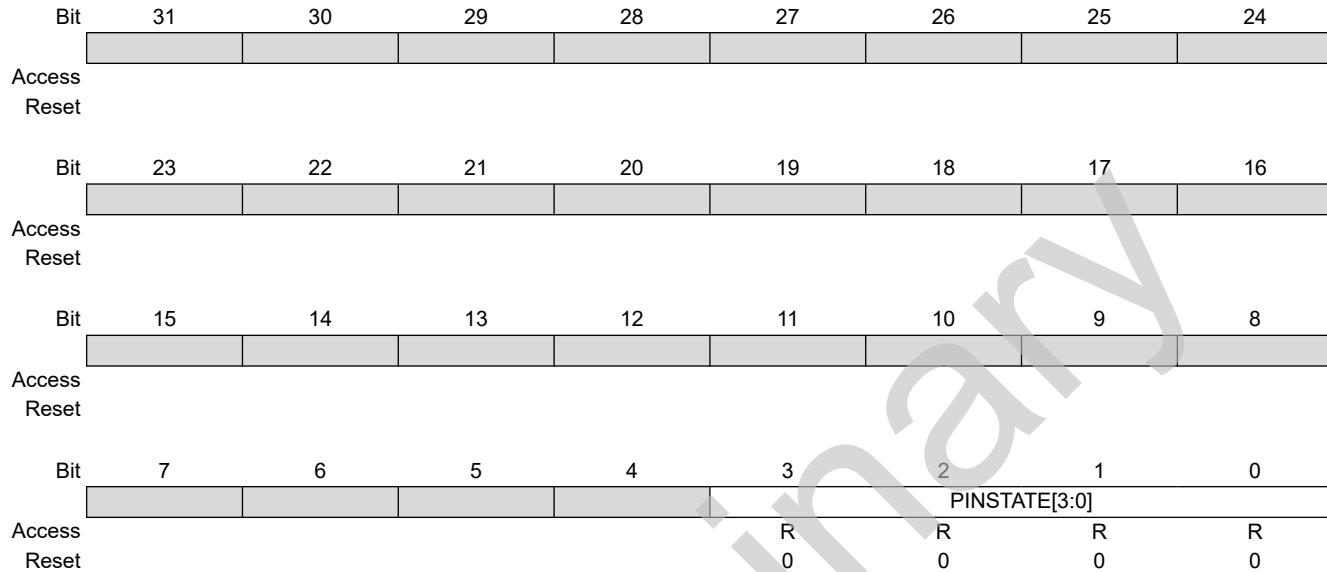
Bits 0:2, 4:6 – PRESCALERx Debouncer Prescaler x

These bits select the debouncer low frequency clock for pins EXTINT[7+(8x):8x].

Value	Name	Description
0x0	F/2	EIC clock divided by 2
0x1	F/4	EIC clock divided by 4
0x2	F/8	EIC clock divided by 8
0x3	F/16	EIC clock divided by 16
0x4	F/32	EIC clock divided by 32
0x5	F/64	EIC clock divided by 64
0x6	F/128	EIC clock divided by 128
0x7	F/256	EIC clock divided by 256

22.8.13 Pin State

Name: PINSTATE
Offset: 0x38
Reset: 0x00000000



Bits 3:0 – PINSTATE[3:0] Pin State

These bits return the valid pin state of the debounced external interrupt pin EXTINT_x.

23. Flash Memory

PIC32CX-BZ2 devices contain single bank of Flash memory with their Program Flash Memory (PFM) partition and Boot Flash Memory (BFM) partition for storing user code or non-volatile data. Flash controller is used to access the Flash memory. Peripheral bus interface is used for commands and configuration of Flash controller

23.1 Features

Flash Controller:

- PB-PIC Bridge interface that provides access to the Flash controller registers
- AHB Initiator for bus master reads the row programming data from SRAM
- Write Protect for Program flash (PFM)
 - Single page protection resolution
 - Protect “Less Than” Address
 - Protect “Greater Than or Equal to” Address
- Individual page write protection for boot Flash (BFM)
- Error-correction code (ECC) support
- Supports chip and page erase
- Supports Single Word, Quad Word and row program options
- Supports flash Erase/Retry to increase Retention and Endurance

Flash Memory:

- 128-bit Flash Memory
- 4 Kbytes page size (1K Instruction Word (IW))
- Row size is 1 KB (256 IW)
- Flash based OTP (one-time-programmable) page

Flash controller allows the Flash memory to be accessed through following methods:

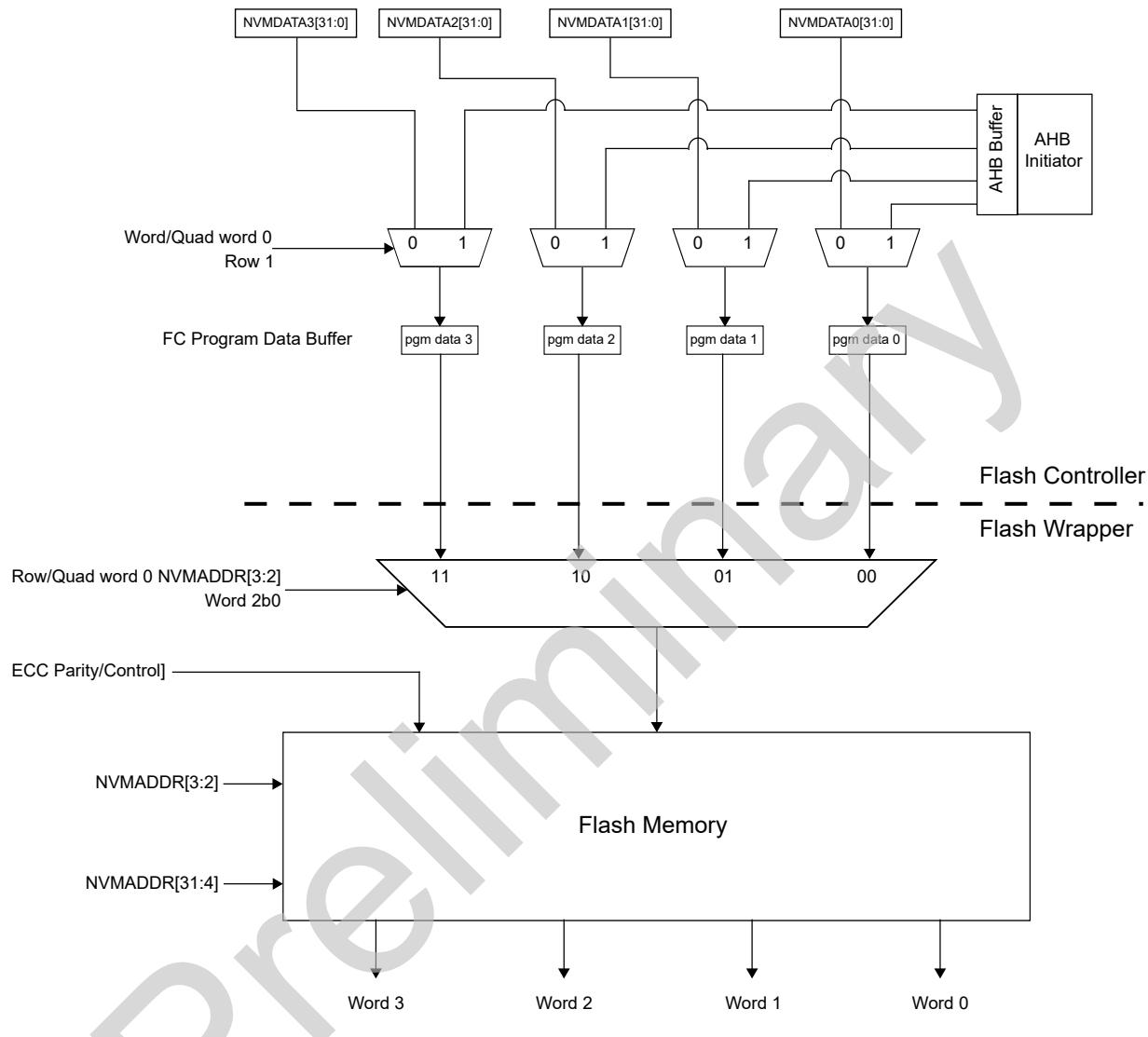
1. Run-Time Self-Programming (RTSP)
2. Serial Wire Debug (SWD) programming using DSU (See *Device Service Unit (DSU)* from Related Links and *PIC32CX-BZ2 Programming Specification*)

Related Links

11. [Device Service Unit \(DSU\)](#)

23.2 Functional Block Diagram

Figure 23-1. Flash Memory Block Diagram



23.3 Flash Memory Addressing

Flash memory addressing uses physical addresses only, for more information on addressing, see *Product Memory Mapping Overview* from Related Links.

Related Links

7. [Product Memory Mapping Overview](#)

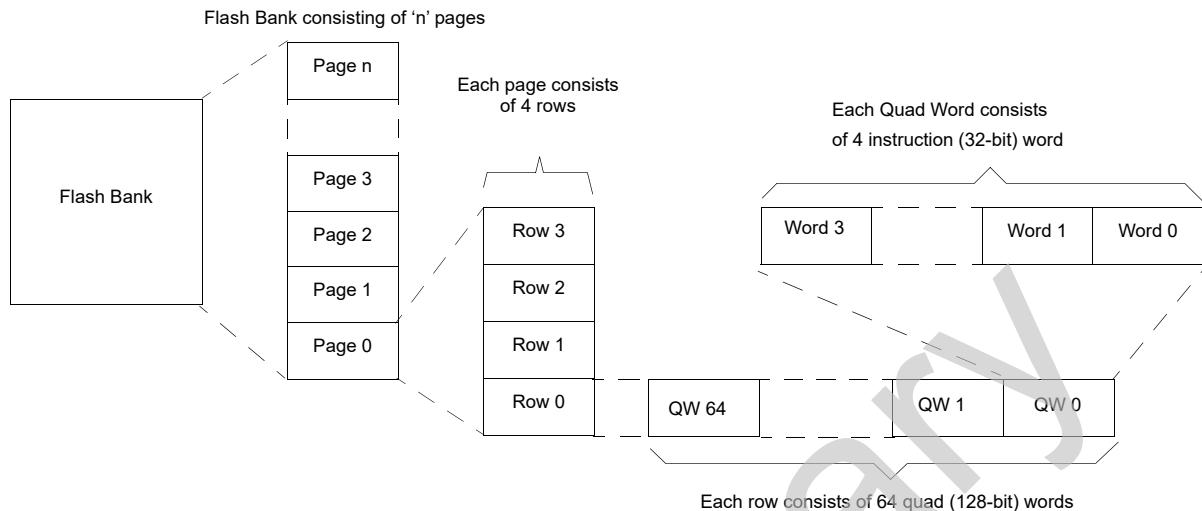
23.4 Memory Configuration

23.4.1 Flash Memory Construction

Flash memory is divided into pages. A page is the smallest unit of memory that can be erased at one time. Each page of memory is segmented into four rows. A row is the largest unit of memory that can be programmed at one

time. A row consists of 64 Quad (128-bit) Word. Each Quad Word consists of four instruction (32-bit) Word. Flash memory can be programmed in rows, Quad Word (128-bit) or Single Word (32-bit) units.

Figure 23-2. Flash Construction



23.4.2 Flash Memory Organization

The device flash memory is divided into two logical flash partitions:

1. Main Program Flash Memory (PFM)
2. Boot/Configuration Flash Memory (BFM)
 - a. Boot Flash
 - b. Device/Boot Config - Device and Boot configuration data
 - c. OTP (One Time Programmable) - User system calibration data

Each flash section has different protection status, refer to the following table.

Table 23-1. Protection Status

Flash Partition	Memory Region	Write Protection	Erase Protection	Chip Erase through DSU
BFM	Boot Flash	Yes. Pagewise Configurable	Yes. Pagewise Configurable	Erased
	Device/Boot Config	Yes. Configurable	Yes. Configurable	Erased
	OTP (One-Time-Programmable)	Yes. Configurable	Always Erase protected. Can not be erased	Not Erased
PFM	Program Flash	Yes. Configurable	Yes. Configurable	Erased

23.5 Boot Flash Memory (BFM) Partitions

23.5.1 BFM Write Protection

Pages in the BFM regions can be protected individually using bits in the NVMLBWP register. At reset, all pages are in a write-protected state and must be disabled prior to performing any programming operations on the BFM regions. There is also unlock bit, ULOCK(NVMLBWP[31]), which is set at reset and can be cleared by user software. When cleared, changes to write protection for that region can no longer be made. Once cleared, the ULOCK bit can only be set by a reset.

The NVMLBWP write-protect register can only be changed when the unlock sequence is followed. See *NVMKEY Register Unlocking Sequence* from Related Links.

Related Links

[23.10. NVMKEY Register Unlocking Sequence](#)

23.6 Program Flash Memory (PFM) Partitions

23.6.1 PFM Write Protection

Write protection for the PFM region is implemented by pages, defined by the NVMPWPLT and NVMPWPGTE registers. The NVMPWP* registers define an area within program space (PFM) that is write protected. This write protect address resolves to flash page boundaries, so the 12 LSBs for a 4KB page flash of any address written to the NVMPWP* registers are ignored. The width of each NVMPWP* address register is determined by the size of the flash. The NVMPWPLT register is used to set the program flash pages lower than provided address as a write protected. The NVMPWPGTE register is used to set the program flash pages greater than or equal to the provided address as a write protected. Therefore, a value of all 0's in the NVMPWPLT register and all 1's in the NVMPWPGTE register results in no region of flash being write protected (default state at reset).

There is also an unlock bit, ULOCK (NVMPWPLT [31] and NVMPWPGTE[31]), which is set at Reset and can be cleared by user software. When cleared, changes to write protection of the PFM can no longer be made, including the ULOCK bit. The NVMPWPLT and NVMPWPGTE write-protect register can only be changed when the unlock sequence is followed. See *NVMKEY Register Unlocking Sequence* from Related Links.

Related Links

[23.10. NVMKEY Register Unlocking Sequence](#)

23.7 Error Correcting Code (ECC) and Flash Programming

PIC32CX-BZ2 devices incorporate Error Correcting Code (ECC) features, which detect and correct errors resulting in extended Flash memory life. For more details on this feature, see *Prefetch Cache* from Related Links.

ECC is implemented in 128-bit Quad Flash Words or 32-bit Single Word. As a result, when programming Flash memory on a device where ECC is employed, the programming operation must be at minimum four instruction words or in groups of four instruction words. This is the reason that the Quad Word programming command exists and why row programming always programs multiples of four words.

For a given software application, ECC can be enabled at all times, disabled at all times, or dynamically enabled using the ECCCTL Configuration bits in the CFGCON0 register. When ECC is enabled at all times, the Single Word NVMOP programming command does not function, and the Quad Word is the smallest unit of memory that can be programmed. When ECC is disabled or enabled dynamically, both the Single Word and Quad Word programming NVMOP commands are functional and the programming method used determines how ECC is handled.

In the case of dynamic ECC, if the memory was programmed with the Single Word command, ECC is turned off for that Word, and when it is read, no error correction is performed. If the memory was programmed with the Quad Word or Row Programming commands, ECC data is written and tested for errors (and corrected if needed) when read. Following table describes the different ECC scenarios.

Table 23-2. ECC Programming Summary

ECCCTL Setting	Programming Operation			Data Read
	Single Word Write	Quad Word Write	Row Write	
Disabled	Allowed	Allowed	Allowed	ECC is never applied on a Flash read
Enabled	Not allowed	Allowed	Allowed	ECC is applied on every Flash Word read

.....continued				
ECCCTL Setting	Programming Operation			Data Read
	Single Word Write	Quad Word Write	Row Write	
Dynamic	Allowed, but when used, the programmed word is flagged to NOT USE ECC	Writes ECC data and flags programmed words to USE ECC	Writes ECC data and flags programmed words to USE ECC	ECC is only applied on words that are flagged to USE ECC

Note: When using dynamic ECC, all non-ECC locations must be programmed with the 32-bit Word programming command, while all ECC enabled locations must be programmed with a 128-bit Quad Word or Row programming command. Divisions between ECC and non-ECC memory must be on even Quad Word boundaries (address bits 0 through 3 are equal to '0').

Related Links

- 8. Prefetch Cache

23.8 Interrupts

An interrupt is generated when the WR bit is cleared by the Flash Controller upon completion of a Flash program or erase operation. The interrupt event will cause a CPU interrupt if it has been configured and enabled in the Nested Interrupt Vector Controller. See *Nested Vector Interrupt Controller* from Related Links for vector mapping table. The interrupt occurs regardless of the outcome of the program or erase operation; successful or unsuccessful. The only exception is the No Operation (NOP) programming operation (NVMOP = 0), which is used to manually clear the error flags and does not create an interrupt event on completion, but does clear the WR bit.

Flash Controller interrupts are not persistent, and therefore, no additional steps are required to clear the cause or source of the interrupt.

Once the Interrupt Controller is configured, the Flash event causes the CPU to jump to the vector assigned to the Flash event. The CPU starts executing the code at the vector address. The user software at this vector address should perform the required operations, and then exit.

Related Links

- 9.2. Nested Vector Interrupt Controller (NVIC)

23.8.1 Interrupts and CPU Stalling

Code cannot be fetched by the CPU from the same Flash bank, either BFM or PFM, which is the target of the programming operation. When this operation is attempted, the CPU will cease to execute code (stall) while the programming operation is in progress. CPU code execution does not resume until the programming operation is complete, and when this occurs, any pending interrupts, including those from the Flash Controller, will be processed in order of priority.

Note that code that is already loaded into the processor cache will continue to execute up to the point where an attempt is made to fetch code or data from the same Flash bank as the active programming operation. At this point the CPU will stall.

Stalling of CPU can also be avoided by placing any needed executable code in SRAM during Flash programming.

23.9 Error Detection

The NVMCON register includes two bits for detecting error conditions during a program or erase operation. They are Low-Voltage detect error, LVDERR bit (NVMCON[12]) and Write Error, WRERR bit (NVMCON[13]).

The WRERR is set each time the WR bit (NVMCON[15]) is set, initiating a programming operation. When the Flash operation is complete, indicated by hardware clearing the value of the WR bit (i.e. WR bit is set to a '0'), hardware will update the value in WRERR bit to indicate if an error occurred. Firmware should check the value of the WR bit to see if the flash operation has completed before checking the value of the WRERR bit. When the WRERR is set, any

future attempt to initiate programming or erase operation is ignored. WRERR must be cleared before commencing Flash program or erase operations.

The LVDERR bit is set when a Brown-out Reset (BOR) occurs during a programming operation. The only reset which clears the LVDERR bit is a Power-on Reset (POR). Other reset types do not affect the LVDERR bit. When the LVDERR bit is set, any attempt to initiate programming or erase operation is ignored. The LVDERR bit must be cleared before commencing Flash program or erase operations.

Both the WRERR and LVDERR bits must be cleared manually in software by initiating a Flash operation (setting WR) referred to as NOP (0x00) (see the NVMOP bit fields). Note that executing the NVMOP NOP command clears WRERR, LVDERR and WR bits, but does not generate an interrupt event on completion.

Table 23-3. Programming Error Cause and Effects

Cause of Error	Effect on Programming/Erase Operation	Indication
A low-voltage event occurred during a programming sequence.	The last programming or erase operation may not have completed.	LVDERR = 1, WRERR = 1
A non-POR reset occurred during programming.	Programming or erase operation is aborted.	WRERR = 1
Attempt to program or erase a page out of the Flash memory range.	Erase or programming operation is not initiated.	WRERR = 1
Attempt to erase or program a write protected PFM page.	Erase or programming operation is not initiated.	WRERR = 1
Attempt to erase or program a write protected BFM page.	Operation occurs, but the page is not programmed or erased.	WRERR = 0
Bus master error or row programming data underrun error during programming.	Programming or erase operation is aborted.	WRERR = 1

23.10 NVMKEY Register Unlocking Sequence

Important register settings that could compromise the Flash memory if inadvertently changed are protected by a register unlocking sequence. This feature is implemented using the NVMKEY register. The NVMKEY register is a write-only register that is used to implement an unlock sequence to help prevent accidental writes or erasures of Flash memory.

In some instances, the operation is also dependent on the setting of the WREN bit (NVMCON[14]), as shown in the following table.

Table 23-4. NVMKEY Register Unlocking and WREN

Operation	WREN Setting	Unlock Sequence Required
Changing value of NVMOP[3:0] (NVMCON[3:0])	0	No
Setting WR (NVMCON[15]) to start a write or erase operation	1	Yes
Changing any fields in the NVMPWP* register	Don't care	Yes
Changing any fields in the NVMLBWP register	Don't care	Yes

The following steps must be followed in the exact order as shown to enable writes to registers that require this unlock sequence:

1. Write 0x00000000 to NVMKEY.
2. Write 0xAA996655 to NVMKEY.
3. Write 0x556699AA to NVMKEY.
4. Write the value to the register NVMCON, NVMCON2, NVMPWP* or NVMLBWP requiring the unlock sequence.

When using the unlock sequence to set or clear bits in the NVMCON register, as shown in Step 4, Steps 2 through 4 must be executed without any other activity on the peripheral bus that is in use by the Flash Controller. Interrupts and DMA transfers that access the same peripheral bus as the Flash Controller must be disabled. In addition, the operation in Step 4 must be atomic. The Set, Clear, and Invert registers may be used, where applicable, for the target register in Step 4.

Following code shows code written in the C language to initiate a NVM Operation (NVMOP) command. In this particular example, the WR bit is being set in the NVMCON register, and therefore, must include the unlock sequence.

Initiate NVM Operation (System Unlock Sequence Example)

```
void NVMInitiateOperation(void)
{
    // Disable Interrupts
    asm volatile("di%0" : "=r"(int_status));
    uint32_t globalInterruptState= __get_PRIMASK();
    // Disable Interrupts
    disable_irq();
    NVMKEY = 0x0;
    NVMKEY = 0xAA996655;
    NVMKEY = 0x556699AA;
    NVMCONSET = 1 << 15;// must be an atomic instruction

    // Restore Interrupts
    __set_PRIMASK(globalInterruptState);
}
```

Note: Once the unlock codes have been written to the NVMKEY register, the next activity on the same peripheral bus as the Flash Controller will reset the lock. As a result, only atomic operations can be used. Note to use of the NVMCONSET register, which sets the WR bit in a single instruction without changing other bits in the register. Using NVMCONbits.WR = 1 will fail, as this line of code compiles to a read-modify-write sequence.

23.11 Word Programming

The smallest block of data that can be programmed in a single operation is one Flash write word (64-bit). The data to be programmed must be written to the NVMDATA0 register, and the address of the word must be loaded into the NVMADDR register before the programming sequence is initiated. The instruction word at the physical location pointed to by the NVMADDR register is then programmed. Programming occurs on 32-bit word boundaries; therefore, bits 0 and 1 of the NVMADDR register are ignored.

Once a word is programmed, it must be erased before it can be programmed again, even if changing a bit from an erased '1' state to a '0' state.

Word programming will only succeed if the target address is in a page that is not write-protected. Programming to a write-protected PFM page will fail and result in the WRERR bit being set in the NVMCON register. Programming a write-protected BFM page will fail, but does not set the WRERR bit.

A programming sequence consists of the following steps:

1. Write 32-bit data to be programmed to the NVMDATA0 register.
2. Load the NVMADDR register with the address to be programmed.
3. Set the WREN bit = 1 and NVMOP bits = 1 in the NVMCON register. This defines and enables the programming operation.
4. Initiation of the programming operation (See *NVMKEY Register Unlocking Sequence* from Related Links.).
5. Monitor the WR bit of the NVMCON register to flag completion of the operation.
6. Clear the WREN bit in the NVMCON register.

7. Check for errors and process accordingly.

Following code shows code for Word programming, where a value of 0x12345678 is programmed into location 0x1008000.

Word Programming:

```
...
// Set up Address and Data Registers
NVMADDR= 0x1008000;           // physical address
NVMDATA0 = 0x12345678;        // value

// set the operation, assumes WREN = 0
NVMCONbits.NVMOP = 0x1;       // NVMOP for Word programming

// Enable Flash for write operation and set the NVMOP
NVMCONbits.WREN = 1;

// Start programming
NVMInitiateOperation();          // see Initiate NVM Operation (Unlock Sequence Example)

// Wait for WR bit to clear
while (NVMCONbits.WR);

// Disable future Flash Write/Erase operations
NVMCONbits.WREN = 0;

// Check Error Status
if(NVMCON & 0x3000)           // mask for WRERR and LVDERR
{
    // process errors
}
...
...
```

Related Links

[23.10. NVMKEY Register Unlocking Sequence](#)

23.12 Quad Word Programming

The process for Quad Word programming is identical to Word programming except that all four of the NVMDATAx registers are used. The value of the NVMDATA0 register is programmed at address NVMADDR, NVMDATA1 at NVMADDR + 0x4, NVMDATA2 at NVMADDR + 0x8, and NVMDATA3 at address NVMDATA + 0xC.

Quad Word programming is always performed on a Quad Word boundary; therefore, bits 3 through 0 are ignored.

Quad Word programming will only succeed if the target address is in a page that is not write-protected. Once a Quad Word is programmed, it must be erased before any Word in it can be programmed again, even if changing a bit from an erased '1' state to a '0' state.

Where a value of 0x11111111 is programmed into location 0x1008000, 0x22222222 into 0x1008004, 0x33333333 into 0x1008008, and 0x44444444 into location 0x100800C. Refer to the following code example for details.

Quad Word Programming Code Example

```
...
// Set up Address and Data Registers
NVMADDR = 0x1008000;           // physical address
NVMDATA0 = 0x11111111;         // value written to 0x1008000
NVMDATA1 = 0x22222222;         // value written to 0x1008004
NVMDATA2 = 0x33333333;         // value written to 0x1008008
NVMDATA3 = 0x44444444;         // value written to 0x100800C

// set the operation, assumes WREN = 0
NVMCONbits.NVMOP = 0x2;        // NVMOP for Quad Word programming

// Enable Flash for write operation and set the NVMOP
NVMCONbits.WREN = 1;

// Start programming
```

```

NVMInitiateOperation();      // see Initiate NVM Operation (Unlock Sequence Example)

// Wait for WR bit to clear
while(NVMCON & NVMCON_WR);

// Disable future Flash Write/Erase operations
NVMCONbits.WREN = 0;

// Check Error Status
if(NVMCON & 0x3000)        // mask for WRERR and LVDERR bits

```

23.13 Row Programming

The largest block of data that can be programmed is a row.

Unlike Word and Quad Word Programming, where the data source is stored in SFR memory, Row programming source data is stored in SRAM. The NVMSRCADDR register is a pointer to the physical location of the source data for Row programming.

Like other Non-volatile Memory (NVM) programming commands, the NVMADDR register points to the target address of the operation. Row programming always occurs on row boundaries with the row size of 1024, bits 0 through 9 of the NVMADDR register are ignored.

Row Word programming will only succeed if the target address is in a page that is not write-protected. Once a row is programmed, it must be erased before any Word in it can be programmed again, even if changing a bit from an erased '1' state to a '0' state.

Array `rowbuff` is populated with data and programmed into a row located at physical address `0x1008000`.

Note: When assigning the value to the NVMSRCADDR register, it must be converted to a physical address.

Row Programming Example Code

```

...
unsigned long rowbuff[256]; // example is for a 256 Word row size.
int x;                    // loop counter

// put some data in the source buffer
for (x = 0; x < (sizeof(rowbuff) * sizeof (int)); x++)
    ((char *)rowbuff)[x] = x;

// set destination row address
NVMADDR = 0x1008000;           // row physical address

// set source address. Must be converted to a physical address.
NVMSRCADDR = (unsigned int)((int)rowbuff & 0x1FFFFFF);

// define Flash operation
NVMCONbits.NVMOP = 0x3;          // NVMOP for Row programming

// Enable Flash Write
NVMCONbits.WREN = 1;

// commence programming
NVMInitiateOperation();          // see Initiate NVM Operation (Unlock Sequence Example)

// Wait for WR bit to clear
while(NVMCONbits.WR);

// Disable future Flash Write/Erase operations
NVMCONbits.WREN = 0;

// Check Error Status
if(NVMCON & 0x3000)            // mask for WRERR and LVDERR bits
{
    // process errors
}
...

```

23.14 Page Erase

A page erase performs an erase of a single page of either PFM or BFM.

The page to be erased is selected using the NVMADDR register. Pages are always erased on page boundaries; therefore, for a device with an instruction word page size of 4096, bits 0 through 11 of the NVMADDR register are ignored.

A page erase will only succeed if the target address is a page that is not write-protected. Erasing a write-protected page will fail and result in the WRERR bit being set in the NVMCON register.

Following code shows code for a single page erase operation at address 0x1008000.

Page Erase

```
...
// set destination page address
NVMADDR = 0x1008000;           // page physical address

// define Flash operation
NVMCONbits.NVMOP = 0x4;        // NVMOP for Page Erase

// Enable Flash Write
NVMCONbits.WREN = 1;

// commence programming
NVMInitiateOperation();        // see Initiate NVM Operation (Unlock Sequence Example)

// Wait for WR bit to clear
while(NVMCONbits.WR);

// Disable future Flash Write/Erase operations
NVMCONbits.WREN = 0;

// Check Error Status
if(NVMCON & 0x3000)           // mask for WRERR and LVDERR bits
{
    // process errors
}

...
...
```

23.14.1 Page Erase Retry

Erase Retry is a method to improve the life of a Flash by attempting the erase again if it didn't work. Erase Retry can only be used for a Page Erase.

Erase Retry works by increasing the voltage used on the Flash when erasing. Initially, the minimum voltage necessary is applied by setting the RETRY[1:0] bits (NVMCON2[9:8]) = 00. If the page erase does not work, the voltage may be increased by incrementing the setting of the RETRY[1:0] bits. Note that each Flash page, as it ages and wears, may have different voltage requirements, so a higher setting on one Flash page does not indicate that the same setting should be used on all pages. The maximum voltage for page erase is used when the RETRY[1:0] bits = 11. If page erase does not work when the RETRY[1:0] bits = 11, this means that the Flash for that page, or the words that did not erase, should be considered "non-functional".

Together with the normal Page Erase controls, Erase Retry also uses the WS[4:0], CREAD1, VREAD1, and RETRY[1:0] bits in the NVMCON2 register. The ERS[3:0] bits (NVMCON2[31:28]) are for the benefit of software performing the programming sequence in the event that a drop in power causes a BOR event, but not a POR event.

Perform the following steps to set up a Page Erase Retry:

1. Set the NVMADDR register with the address of the page to be erased.
2. Execute the write unlock sequence.
3. Save the value of the NVMCON2 register.
4. Do the following in the NVMCON2 register:
 - a. Set the ERS[3:0] bits as desired.
 - b. Set the WS[4:0] bits per the description.

- c. Set the VREAD1 bit to '1'.
- d. Set the CREAD1 bit to '1'.
- e. Set the RETRY[1:0] bits to '00'.
5. Run the unlock sequence using the Page Erase command to start the sequence.
6. Wait for the WR bit (NVMCON[15]) to be cleared by hardware.
7. Clear the WREN bit (NVMCON[14]).
8. Verify the erase using the CPU: To shorten the verify time, use CREAD1 = 1 to perform a hardware compare to logic 1 of each bit in the Flash Word including ECC. A successful compare yields a read of 0x00000001 in the lowest addressed word in a Flash Word (128 bits). This is the Compare Word. All other words are 0x00010000. If any bit is logic 0, all Words in the Flash Word read 0x00000000. Remember to increment the address by the number of bytes in a Flash Word between reads.
9. If all Compare Words verify correctly, the Erase Retry process is complete. Go to step 11.
10. If a Compare Word yields a read of 0x00000000, perform steps 4 through 9 up to three more times with the following change to step 4:
 - a. Increment the RETRY[1:0] bits by one.
 - b. Maintain all other fields.
11. Restore the value of the NVMCON2 register, which was saved in step 3.

Note:

1. When the VREAD1 = 1, the Flash uses the WS[3:0] bits for Flash access wait state generation to the panel selected by NVMADDR. Software is responsible for writing the VREAD1 bit back to '0' when both erase and verify is complete.
2. Device configuration boot page (the page containing the DEVCFGx values) does not support Erase Retry.

Following code provides code for a single page erase operation at address 0x1008000 where Erase Retry is used.

Page Erase Retry

```

uint32_t saveNVMCON2;
uint32_t *cmpPtr;
uint8_t erased;
uint8_t tryCount;

// set destination page address
NVMADDR = 0x1008000;      // Page physical address

// define flash operation
NVMCONbits.NVMOP = 0x4;    // NVMOP for Page Erase

// Unlock sequence
NVMKEY = 0x0;
NVMKEY = 0xAA996655;
NVMKEY = 0x556699AA;

// save NVMCON2
saveNVMCON2 = NVMCON2;

// set up Erase Retry
NVMCON2bits.ERS = 0;      // Stage 0 - SW use only
NVMCON2bits.VREAD1 = 1;
NVMCON2bits.CREAD1 = 1;
NVMCON2bits.RETRY = 0b00;

tryCount = 0;              // Up to 4 attempts

do {
    tryCount++;

    // commence programming
    NVMIinitiateOperation();

    // Wait for WR bit to clear
    while(NVMCONbits.WR);

    // Turn off WREN
    NVMCONbits.WREN = 0;
}

```

```

// Check that the page was erased
erased = 1;
cmpPtr = (uint32_t *)NVMADDR;
erased &= (*cmpPtr == 0x00000001);
cmpPtr++;
erased &= (*cmpPtr == 0x00010000);
cmpPtr++;
erased &= (*cmpPtr == 0x00010000);
cmpPtr++;
erased &= (*cmpPtr == 0x00010000);

if (!erased) {
    // Erase failed. Try with different settings.
    NVMCON2bits.RETRY++;

    NVMCONbits.NVMOP = 0x4;
    NVMCONbits.WREN = 1;
}
} while (!erased && (tryCount < 4));

// Restore settings
NVMCON2 = saveNVMCON2;

```

23.15 Program Flash Memory (PFM) Erase

Program Flash memory can be erased entirely. All the three discreet NVMOP values 0111, 0110, 0101 does the same operation of erase of entire flash.

When erasing the entire PFM area in case of RTSP (Run Time self programming), code must be executing from BFM.

When erasing the entire PFM area, PFM write protection must be completely disabled.

Following code shows code for erasing the entire Flash bank.

Program Flash Erase

```

...
// define Flash operation
NVMCONbits.NVMOP = 0x7;           // NVMOP for entire PFM erase

// Enable Flash Write
NVMCONbits.WREN = 1;

// commence programming
NVMIInitiateOperation();          // see Initiate NVM Operation (Unlock Sequence Example)

// Wait for WR bit to clear
while(NVMCONbits.WR);

// Disable future Flash Write/Erase operations
NVMCONbits.WREN = 0;

// Check Error Status
if(NVMCON & 0x3000)             // mask for WRERR and LVDERR bits
{
    // process errors
}

...

```

23.16 Pre-Program

PIC32CX-BZ2 Flash supports an option to programming that increase endurance and retention. This feature is called Pre-Program and requires the user to perform the programming operation twice, first with NVMCON2.NVMPREPG=1 and secondly with NVMCON2.NVMPREPG=0. Any of the programming operations (Single, Quad, Row) can be performed with this method. In all other respects the SFR setup is identical. To use this feature set or clear the

NVMCON2.NVMPREPG SFR bit prior to setting the NVMWR bit. Pre-Program typically double the native Endurance and Retention of the Flash.

23.17 Device Code Protection bit (CP)

PIC32CX-BZ2 family of devices feature code protection, which when enabled, prevents reading of the Flash memory by an external programming device (SWD through DSU).

Once code protection is enabled, it can only be disabled by erasing the device with the Chip Erase command through external programmer. See *Device Service Unit (DSU)* from Related Links.

When programming a device that has opted to utilize code protection, the external programming device must perform verification prior to enabling code protection. Enabling code protection should be the last step of the programming process. For location of the code protection enable bits refer to *PIC32CX-BZ2 Programming Specification* and *System Configuration Registers (CFG)* from Related Links.

23.18 Operation in Power-Saving Modes

The Flash Controller does not operate in power-saving modes. If a WAIT instruction is encountered when programming, the CPU will stop execution (stall), wait for the programming operation to complete, and then enter the Power-Saving mode.

23.19 Operation in Debug Mode

Programming operations will continue to completion if processor execution is halted in Debug mode.

23.20 Effects of Various Resets

Devices Resets other than a Power-on Reset (POR), reset the entire contents of the NVMPWP, and NVMLBWP registers. All other register content persists through a non-POR reset.

All Flash Controller registers are forced to their reset states upon a POR.

23.21 Control Registers

Note: Following conventions are used in the following registers:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
- -n = Value at POR
- HS = Hardware Set
- HC = Hardware Cleared

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Related Links

[5.1.9. CLR, SET, and INV Registers](#)

PIC32CX-BZ2 and WBZ45 Family Flash Memory

23.21.1 Register Summary

Following registers provides a brief summary of the Flash-programming-related registers.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	NVMCON	7:0					NVMOP[3:0]			
		15:8	WR	WREN	WRERR	LVDERR				HTDPGM
		23:16								
		31:24								
0x04 ...	Reserved									
0x10	NVMCON2	7:0								NVMPREPG
		15:8		TEMP	CREAD1	VREAD1				RETRY[1:0]
		23:16					WS[4:0]			
		31:24	ERS[3:0]							SLEEP
0x14 ...	Reserved									
0x20	NVMKEY	7:0	NVMKEY[7:0]							
		15:8	NVMKEY[15:8]							
		23:16	NVMKEY[23:16]							
		31:24	NVMKEY[31:24]							
0x24 ...	Reserved									
0x30	NVMAADDR	7:0	NVMAADDR[7:0]							
		15:8	NVMAADDR[15:8]							
		23:16	NVMAADDR[23:16]							
		31:24	NVMAADDR[31:24]							
0x34 ...	Reserved									
0x40	NVMDATA0	7:0	NVMDATA[7:0]							
		15:8	NVMDATA[15:8]							
		23:16	NVMDATA[23:16]							
		31:24	NVMDATA[31:24]							
0x44 ...	Reserved									
0x50	NVMDATA1	7:0	NVMDATA[7:0]							
		15:8	NVMDATA[15:8]							
		23:16	NVMDATA[23:16]							
		31:24	NVMDATA[31:24]							
0x54 ...	Reserved									
0x60	NVMDATA2	7:0	NVMDATA[7:0]							
		15:8	NVMDATA[15:8]							
		23:16	NVMDATA[23:16]							
		31:24	NVMDATA[31:24]							
0x64 ...	Reserved									
0x70	NVMDATA3	7:0	NVMDATA[7:0]							
		15:8	NVMDATA[15:8]							
		23:16	NVMDATA[23:16]							
		31:24	NVMDATA[31:24]							
0x74 ...	Reserved									

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xC0	NVMSRCADDR	7:0								NVMSRCADDR[7:0]
		15:8								NVMSRCADDR[15:8]
		23:16								NVMSRCADDR[23:16]
		31:24								NVMSRCADDR[31:24]
0xC4 ...	Reserved									
0xD0	NVMPWPLT	7:0								PWPLT[7:0]
		15:8								PWPLT[15:8]
		23:16								PWPLT[23:16]
		31:24	ULOCK							
0xD4 ...	Reserved									
0xE0	NVMPWPGE	7:0								PWPGTE[7:0]
		15:8								PWPGTE[15:8]
		23:16								PWPGTE[23:16]
		31:24	ULOCK							
0xE4 ...	Reserved									
0xF0	NVMLBWP	7:0								LBWP[7:0]
		15:8								LBWP[15:8]
		23:16								LBWP[23:16]
		31:24	ULOCK							

23.21.2 Register Description

Flash program, erase, and write protection operations are controlled using the following Non-Volatile Memory (NVM) control registers:

- NVMCON: Programming Control Register
 - This register is the control register for Flash program/erase operations. This register is used to select the operation to be performed, initiate the operation, and provide status of the result when the operation is complete.
- NVMCON2: Programming Control2 Register
 - This register is the control and status register for Flash program/erase operations.
- NVMKEY: Programming Unlock Register
 - This is a write-only register that is used to implement an unlock sequence to help prevent accidental writes/erasures of Flash memory and write permission settings.
- NVMAADDR: Flash Address Register
 - This register is used to store the physical target address for row, Quad Double Word and Single Double Word programming as well as page erasing.
- NVMDATAx: Flash Program Data Register ($x = 0-3$)
 - These registers hold the data to be programmed during Flash Word program operations.
- NVMSRCADDR: Source Data Address Register
 - This register is used to point to the physical address of the data to be programmed when executing a row program operation.
- NVMPWPLT: Flash Program Write Protect Lower Register
 - This register is used to set the program flash pages lower than provided address as a write protected.
- NVMPWPGE: Flash Program Write Protect Greater Register
 - This register is used to set the program flash pages greater than provided address as a write protected.
- NVMLBWP: Flash Boot Write Protect Register
 - This register is used to set the boot flash partition pages as a write protected.

23.21.2.1 NVMCON - Programming Control Register

Name: NVMCON
Offset: 0x00
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/HS/HC	R/W	R/HS/HC	R/HS/HC				HTDPGM
Reset	0	0	0	0				0
Bit	7	6	5	4	3	2	1	0
Access								
Reset								
						NVMOP[3:0]		
					R/W	R/W	R/W	R/W
					0	0	0	0

Bit 15 – WR Write Control Bit⁽¹⁾

Note: This field can only be modified when WREN = 1, TEMP = 1, and the NVMKEY unlock sequence is satisfied.

Value	Description
1	Initiate a Flash operation. Hardware clears this bit when the operation completes
0	Flash operation complete or inactive

Bit 14 – WREN Write Enable Bit⁽¹⁾

Value	Description
1	Enables writes to WR
0	Disables writes to WR

Bit 13 – WRERR Write Error Bit⁽¹⁾

Note: Cleared by setting NVMOP == 0000b and initiating a Flash operation (WR).

Value	Description
1	Program or erase sequence did not complete successfully
0	Program or erase sequence completed normally

Bit 12 – LVDERR Low Voltage Detect Error Bit⁽¹⁾

The error is only captured for programming/erase operations (when WR = 1).

Note: Cleared by setting NVMOP == 0000b and initiating a Flash operation (WR).

Value	Description
1	Low voltage is detected (possible data corruption if WRERR is set)
0	Normal voltage is detected

Bit 8 – HTDPGM High Temperature Detected during Program/Erase Operation bit

This status is only captured for programming/erase operations (when WR = 1).

Note: Cleared by setting NVMOP == 0000b and initiating a Flash operation (WR).

PIC32CX-BZ2 and WBZ45 Family

Flash Memory

Value	Description
1	High temperature is detected (possible data corruption, verify operation)
0	High temperature is not detected

Bits 3:0 – NVMOP[3:0] NVM Operation bits

These bits are only writable when WREN = 0.

Value	Description
1111	Reserved
1110	Chip Erase Operation: Erases PFM, BFM (except configuration page) when accessed through SWD interface only.
...	
...	
...	
1000	Reserved
0111	Program erase operation: erase all of program Flash memory (PFM) (all pages must be unprotected)
0110	Upper program Flash memory erase operation: erases only the upper mapped region of program Flash (all pages in that region must be unprotected). Its a single bank flash in PIC32CXBZ2, so this NVMOP performs same as NVMOP = 0111.
0101	Lower program Flash memory erase operation: erases only the lower mapped region of program Flash (all pages in that region must be unprotected). Its a single bank flash in PIC32CXBZ2, so this NVMOP performs same as NVMOP = 0111.
0100	Page erase operation: erases page selected by NVMAADDR, if it is not write-protected
0011	Row program operation: programs row selected by NVMAADDR, if it is not write-protected
0010	Quad Word (128-bit) program operation: programs the 128-bit Flash Word selected by NVMAADDR, if it is not write-protected
0001	Word program operation: programs word selected by NVMAADDR, if it is not write-protected ⁽²⁾
0000	No operation

Notes:

1. These bits are only reset by a POR and are not affected by other Reset sources.
2. This operation results in a No Operation (NOP) when the Dynamic Flash ECC Configuration bits = 00 (ECCCTL[1:0](CFGCON0[29:28])), which enables ECC at all times. For all other ECCCTL[1:0]bit settings, this command will execute, but will not write the ECC bits for the Word. It can cause DED (Double-bit Error Detected) errors if dynamic Flash ECC is enabled (ECCCTL[1:0] = 01).

23.21.2.2 NVMCON2 - Programming Control 2 Register

Name: NVMCON2
Offset: 0x10
Reset: 0x011F4000
Property: -

Bit	31	30	29	28	27	26	25	24
ERS[3:0]								
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				1
WS[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1
RETRY[1:0]								
Access		TEMP	CREAD1	VREAD1				R/W
Reset	1	0	0	0			0	0
NVMPREPG								
Access								R/W
Reset								0

Bits 31:28 – ERS[3:0] Erase Retry State

These bits are used by software to track the software state of the erase retry procedure in the event of a system Reset (NMCLR) or Brown Out Reset (BOR) event.

Bit 24 – SLEEP Power Down in Sleep mode

Note: This field can only be modified when the NVMKEY unlock sequence is satisfied.

Value	Description
1	Configures Flash for power down when the system is in Sleep mode
0	Configures Flash for standby when the system is in Sleep mode

Bits 20:16 – WS[4:0] Flash Access Wait State Control for VREAD1 = 1

Notes:

- When VREAD1 = '1', WS[4:0] only affects the memory containing NVMADDR[31:0].
- This field can only be modified when the NVMKEY unlock sequence is satisfied.

Value	Description
11111	31 wait states (32 total system clocks)
11110	30 wait states (31 total system clocks)
...	
00010	2 wait states (3 total system clocks)
00001	1 wait state (2 total system clocks)
00000	0 wait state (1 total system clock)

Bit 14 – TEMP Operating Temperature Control bit

Bit 13 – CREAD1 Compare Read of Logic 1 bit

Compare read 1 causes all bits in a Flash Word (including ECC if it exists) to be evaluated during the read. If all bits are '1', the lowest Word in the Flash Word evaluates to 0x0000_0001, all other Words are 0x0001_0000. If any bit is '0', the read evaluates to 0x0000_0000 for all Words in the Flash Word.

PIC32CX-BZ2 and WBZ45 Family Flash Memory

Notes:

1. When using erase retry in an ECC Flash system, CREAD1 = '1' must be used.
2. This field can only be modified when the NVMKEY unlock sequence is satisfied.

Value	Description
1	Compare read enabled, only if VREAD1 = 1
0	Compare read disabled

Bit 12 – VREAD1 Verify Read of logic 1 Control bit

Notes:

1. When VREAD1 = '1', Flash wait state control is from WS[4:0] for the memory containing NVMADDR[31:0].
2. Using erase retry and verify read procedure increase life of Flash memory.
3. This field can only be modified when NVMCON.WR == '0' and the NVMKEY unlock sequence is satisfied.

Value	Description
1	Selects erase retry procedure with verify read
0	Selects single erase without verify read

Bits 9:8 – RETRY[1:0] Erase Retry Control bit, only used when VREAD1 = 1

Note: This field can only be modified when NVMCON.WR == '0'.

Value	Description
11	Erase strength for last retry cycle
10	Erase strength for third retry cycle
01	Erase strength for second retry cycle
00	Erase strength for first retry cycle

Bit 0 – NVMPREPG NVM Pre-Program Control Bit

Note: This field can only be modified when NVMCON.NVMWR == '0'.

Value	Description
1	Program Operations include Pre-Program step
0	Program Operations exclude Pre-Program step

23.21.2.3 NVMKEY - Programming Unlock Register

Name: NVMKEY
Offset: 0x20
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMKEY[31:24]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
NVMKEY[23:16]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
NVMKEY[15:8]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
NVMKEY[7:0]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMKEY[31:0] Unlock Register bits

These bits are write only and read ‘0’ on any read.

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the program Flash.

23.21.2.4 NVMADDR - Flash Address Register

Name: NVMADDR
Offset: 0x30
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMADDR[31:0] Flash (Word) Address bits

Table 23-5. Flash (Word) Address bits

NVMOP	Flash Address Bits
Page erase	<ul style="list-style-type: none"> Address identifies the page to erase Any address within a 4 Kbytes page boundary will cause the page to be erased
Row program	<ul style="list-style-type: none"> Address identifies the row to program The value of the address must be aligned to a row boundary
Word program	<ul style="list-style-type: none"> Address identifies the 32-bit word to program NVMADDR[1:0] bits are ignored Must be aligned to a word boundary
Quad Word program	<ul style="list-style-type: none"> Address identifies the 128-bit Quad Word to program NVMADDR[3:0] bits are ignored Must be aligned to a Quad word boundary

Notes:

- Hardware prevents writes to this register when NVMCON.WR = 1.
- For all other NVMOP[3:0] bit settings, the Flash address is ignored. For additional information on these bits, see *NVMCON* register from Related Links.
- The bits in this register are only reset by a POR and are not affected by other Reset sources.

Related Links

[23.21.2.1. NVMCON](#)

23.21.2.5 NVMDATA0 - Flash program Data Register 0

Name: NVMDATA0
Offset: 0x40
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMDATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMDATA[31:0] Flash Programming Data bits

The value in this register is written to Flash when a program operation is commanded.

- Single Word program (32-bit)
 - Writes NVMDATA0 to the target Flash address defined in NVMADDR[31:2]
- Quad Word program (128-bit)
 - Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR[31:4]. NVMDATA0 contains the Least Significant Instruction Word

Notes:

1. Hardware prevents writes to this register when NVMCON.WR = 1.
2. The bits in this register are only reset on a Power-on reset (POR) and are unaffected by other reset sources.

23.21.2.6 NVMDATA1 - Flash program Data Register 1

Name: NVMDATA1
Offset: 0x50
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMDATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMDATA[31:0] Flash Programming Data bits

The value in this register is written to Flash when a program operation is commanded.

- Single Word program (32-bit)
 - Writes NVMDATA0 to the target Flash address defined in NVMADDR[31:2]
- Quad Word program (128-bit)
 - Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR[31:4]. NVMDATA0 contains the Least Significant Instruction Word

Notes:

1. Hardware prevents writes to this register when NVMCON.WR = 1.
2. The bits in this register are only reset on a Power-on reset (POR) and are unaffected by other reset sources.

23.21.2.7 NVMDATA2 - Flash program Data Register 2

Name: NVMDATA2
Offset: 0x60
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMDATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMDATA[31:0] Flash Programming Data bits

The value in this register is written to Flash when a program operation is commanded.

- Single Word program (32-bit)
 - Writes NVMDATA0 to the target Flash address defined in NVMADDR[31:2]
- Quad Word program (128-bit)
 - Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR[31:4]. NVMDATA0 contains the Least Significant Instruction Word

Notes:

1. Hardware prevents writes to this register when NVMCON.WR = 1.
2. The bits in this register are only reset on a Power-on reset (POR) and are unaffected by other reset sources.

23.21.2.8 NVMDATA3 - Flash program Data Register 3

Name: NVMDATA3
Offset: 0x70
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMDATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMDATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMDATA[31:0] Flash Programming Data bits

The value in this register is written to Flash when a program operation is commanded.

- Single Word program (32-bit)
 - Writes NVMDATA0 to the target Flash address defined in NVMADDR[31:2]
- Quad Word program (128-bit)
 - Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR[31:4]. NVMDATA0 contains the Least Significant Instruction Word

Notes:

1. Hardware prevents writes to this register when NVMCON.WR = 1.
2. The bits in this register are only reset on a Power-on reset (POR) and are unaffected by other reset sources.

23.21.2.9 NVMSRCADDR - Source Data Address Register

Name: NVMSRCADDR
Offset: 0xC0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
NVMSRCADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMSRCADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMSRCADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
NVMSRCADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NVMSRCADDR[31:0] Source Data (Word) Address bits

This is the system physical Word address of the data (in DRM) to be programmed into the Flash when NVMCON.NVMOP is set to row programming.

Notes:

1. Hardware prevents writes to this register when NVMCON.WR = 1.
2. The bits in this register are only reset on a Power-on reset (POR) and are unaffected by other reset sources.

23.21.2.10 NVMPWPLT - Flash Program Write Protect Lower Register

Name: NVMPWPLT
Offset: 0xD0
Reset: 0x80000000
Property: -

Bit	31	30	29	28	27	26	25	24
	ULOCK							
Access	R/C							
Reset	1							
Bit	23	22	21	20	19	18	17	16
	PWPLT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PWPLT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PWPLT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ULOCK NVMPWPLT Register Unlock bit

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied.
2. This field can be cleared at the same time as writing to PWPLT[23:0].

Value	Description
1	NVMPWPLT register is not locked and can be modified
0	NVMPWPLT register is locked and cannot be modified

Bits 23:0 – PWPLT[23:0] Flash Program Write Protect Less Than Address

Pages at Flash addresses less than this value are write protected.

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied, and ULOCK = 1.
2. This is a byte address force to align to page boundaries.

23.21.2.11 NVMPWPGTE - Flash Program Write Protect Greater Register

Name: NVMPWPGTE
Offset: 0xE0
Reset: 0x80FFFFFF
Property: -

Bit	31	30	29	28	27	26	25	24
	ULOCK							
Access	R/C							
Reset	1							
PWPGE[23:16]								
Bit	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
PWPGE[15:8]								
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
PWPGE[7:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 31 – ULOCK NVMPWPGTE Register Unlock bit

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied.
2. This field can be cleared at the same time as writing to PWPGE[23:0].

Value	Description
1	NVMPWPGTE register is not locked and can be modified
0	NVMPWPGTE register is locked and cannot be modified

Bits 23:0 – PWPGE[23:0] Flash Program Write Protect Address

Pages at Flash addresses greater than or equal to this value are write protected.

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied, and ULOCK = 1.
2. This is a byte address force to align to page boundaries.

23.21.2.12 NVMLBWP - Flash Boot Write Protect Register

Name: NVMLBWP
Offset: 0xF0
Reset: 0x80FFFFFF
Property: -

Bit	31	30	29	28	27	26	25	24	
	ULOCK								
Access	R/C								
Reset	1								
Bit	23	22	21	20	19	18	17	16	
	LBWP[23:16]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	1	1	1	1	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	
	LBWP[15:8]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	1	1	1	1	1	1	1	1	
Bit	7	6	5	4	3	2	1	0	
	LBWP[7:0]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	1	1	1	1	1	1	1	1	

Bit 31 – ULOCK Lower Boot Write Protect (LBWPn) Unlock bit

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied.
2. This field can be cleared at the same time as writing to LBWP[msb:lsb].

Value	Description
1	LBWPn bits are not locked and can be modified
0	LBWPn bits are locked and cannot be modified

Bits 23:0 – LBWP[23:0] Boot Pages Write Protect bits

Notes:

1. This field can only be modified when the NVMKEY unlock sequence is satisfied, and ULOCK = 1.
2. The OTP page is always erase protected and its associated LBWP bit is only for write protection.

Value	Description
1	Erase and write protection for upper boot page n is enabled
0	Erase and write protection for upper boot page n is disabled

24. ICM - Integrity Check Monitor

24.1 Overview

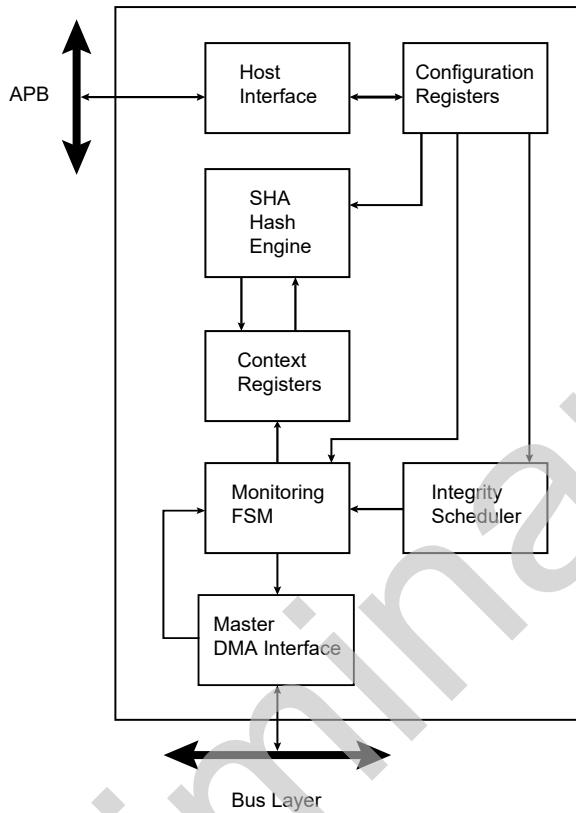
The Integrity Check Monitor (ICM) is a DMA controller that performs hash calculation over multiple memory regions using transfer descriptors located in memory (ICM Descriptor Area). The Hash function is based on the Secure Hash Algorithm (SHA). The ICM controller integrates two modes of operation. The first mode is used to hash a list of memory regions and save the digests to memory (ICM Hash Area). The second mode is an active monitoring of the memory. In this mode, the hash function is evaluated and compared to the digest located at a predefined memory address (ICM Hash Area). If a mismatch occurs, an interrupt is raised.

24.2 Features

- DMA AHB master interface
- Supports monitoring of up to four non-contiguous memory regions
- Supports block gathering using a linked list
- Supports Secure Hash Algorithm (SHA1, SHA256)
- Compliant with FIPS Publication 180-2
- Configurable processing period:
 - When SHA1 algorithm is processed, the run-time period is either 85 or 209 clock cycles
 - When SHA256 algorithm is processed, the run-time period is either 72 or 194 clock cycles
- Programmable bus burden

24.3 Block Diagram

Figure 24-1. Integrity Check Monitor Block Diagram



24.4 Signal Description

Not applicable.

24.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

24.5.1 Power Management

The ICM will run only when the source clocks are running, i.e. when the CPU is in Active mode.

24.5.2 Clocks

The ICM bus clocks (PB2_CLK) can be enabled and disabled in the CRU module or the PMD2.ICMMD bit. For more details, see *Peripheral Module Disable Register (PMD)* from Related Links.

Related Links

[19. Peripheral Module Disable Register \(PMD\)](#)

24.5.3 DMA

Not applicable.

24.5.4 Events

Not applicable.

24.5.5 Debug Operation

Not applicable.

24.6 Functional Description

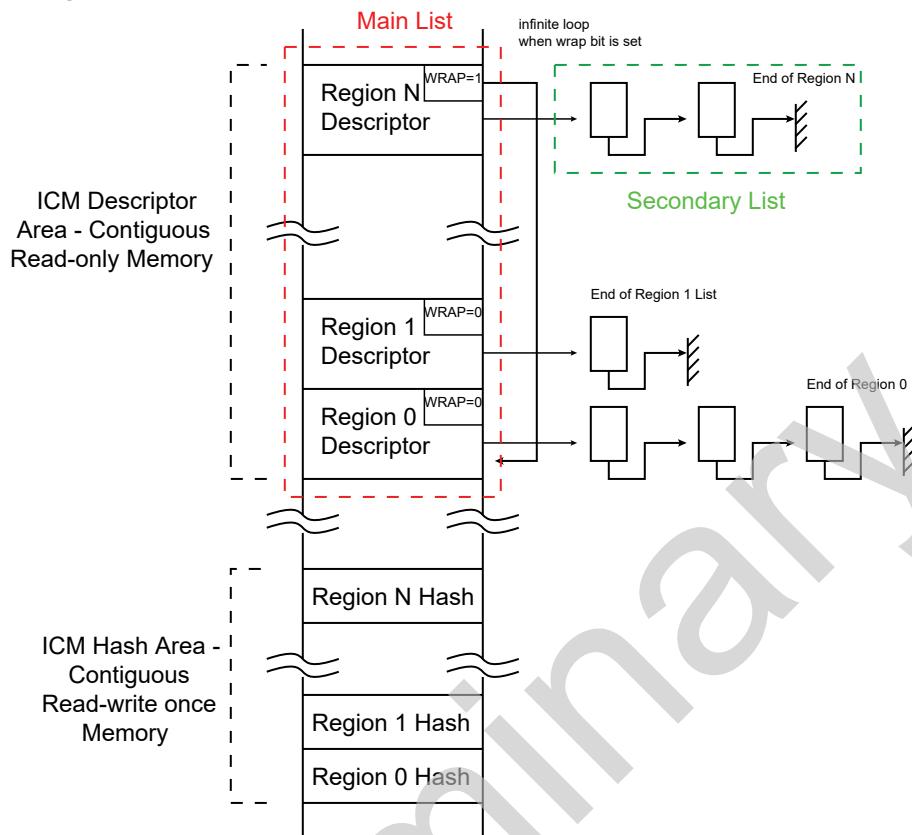
24.6.1 Overview

The Integrity Check Monitor (ICM) is a DMA controller that performs SHA-based memory hashing over memory regions. As shown in the Block Diagram (see *Block Diagram* from Related Links), it integrates a DMA interface, a Monitoring Finite State Machine (FSM), an integrity scheduler, a set of context registers, a SHA engine, an interface for configuration and status registers.

The SHA engine requires a message padded according to FIPS180-4 specification when used as a SHA calculation unit only. Otherwise, if the ICM is used as integrated check for memory content, the padding is not mandatory. The SHA module produces an N-bit message digest each time a block is read and a processing period ends. N is 160 for SHA1, 256 for SHA256.

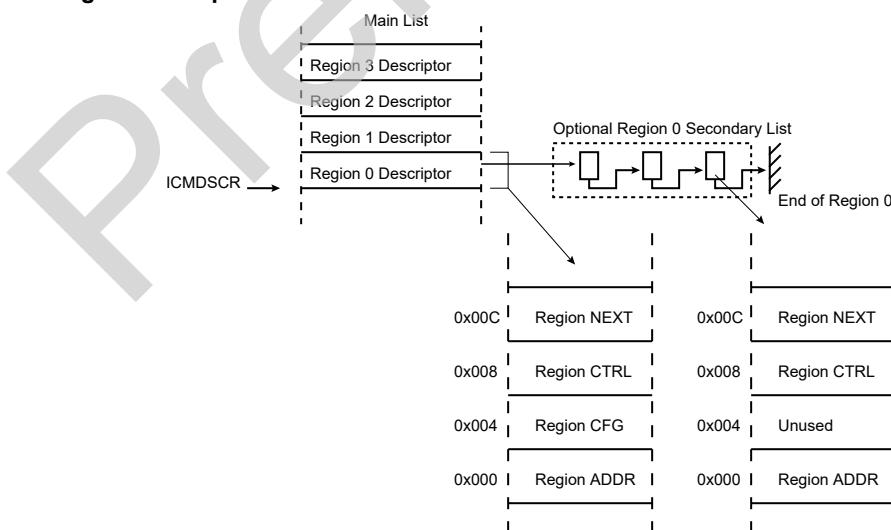
When the ICM module is enabled, it sequentially retrieves a circular list of region descriptors from the memory (Main List described in the following figure). Up to four regions may be monitored. Each region descriptor is composed of four words indicating the layout of the memory region (see *Region Descriptor Structure* from Related Links). It also contains the hashing engine configuration on a per region basis. As soon as the descriptor is loaded from the memory and context registers are updated with the data structure, the hashing operation starts. A programmable number of blocks (see TRSIZE field of the RCTRL structure member) is transferred from the memory to the SHA engine. When the desired number of blocks have been transferred, the digest is either moved to memory (Write Back function) or compared with a digest reference located in the system memory (Compare function). If a digest mismatch occurs, an interrupt is triggered if enabled. The ICM module parses through the region descriptor list until the end of the list marked by an end of list bit is set to one. To continuously monitor the list of regions, the WRAP bit must be set to one in the last data structure and EOM must be cleared.

Figure 24-2. ICM Region Descriptor and Hash Areas



Each region descriptor supports gathering of data through the use of the Secondary List. Unlike the Main List, the Secondary List cannot modify the configuration attributes of the region. When the end of the Secondary List has been encountered, the ICM returns to the Main List. Memory integrity monitoring can be considered as a background service and the mandatory bandwidth shall be very limited. In order to limit the ICM memory bandwidth, use the BBC field of the CFG register to control ICM memory load.

Figure 24-3. Region Descriptor



Related Links

[24.3. Block Diagram](#)

[24.6.3. Region Descriptor Structure](#)

PIC32CX-BZ2 and WBZ45 Family

ICM - Integrity Check Monitor

24.6.2 ICM Hash Area

The ICM Hash Area is a contiguous area of system memory that the controller and the processor can access. The physical location is configured in the ICM hash area start address register. This address is a multiple of bytes. If the CDWBN bit of the context register is cleared (i.e., Write Back activated), the ICM controller performs a digest write operation at the following starting location: *(HASH) + (RID<<), where RID is the current region context identifier. If the CDWBN bit of the context register is set (i.e., Digest Comparison activated), the ICM controller performs a digest read operation at the same address.

24.6.2.1 Message Digest Example

Considering the following 512 bits message (example given in FIPS 180-4):

The message is written to memory in a Little Endian (LE) system architecture.

Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000	80	63	62	61
0x004–0x038	00	00	00	00
0x03C	18	00	00	00

The digest is stored at the memory location pointed at by the ICM_HASH pointer with a Region Offset.

Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000	36	3e	99	a9
0x004	6a	81	06	47
0x008	71	25	3e	ba
0x00C	6c	c2	50	78
0x010	9d	d8	d0	9c

Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000	22	7d	09	23
0x004	22	d8	05	34
0x008	77	a4	42	86
0x00C	b3	55	a2	bd
0x010	e4	bc	ad	2a
0x014	f7	b3	a0	bd
0x018	a7	9d	6c	e3

Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000	bf	16	78	ba
0x004	ea	cf	01	8f

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.....continued				
Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x008	de	40	41	41
0x00C	23	22	ae	5d
0x010	a3	61	03	b0
0x014	9c	7a	17	96
0x018	61	ff	10	b4
0x01C	ad	15	00	f2

Considering the following 1024 bits message (example given in FIPS 180-4):

The message is written to memory in a Little Endian (LE) system architecture.

Memory Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000	80	63	62	61
0x004–0x078	00	00	00	00
0x07C	18	00	00	00

24.6.3 Region Descriptor Structure

The ICM Region Descriptor Area is a contiguous area of system memory that the controller and the processor can access. When the ICM controller is activated, the controller performs a descriptor fetch operation at the DSCR address. If the Main List contains more than one descriptor (i.e., more than one region is to be moderated), the fetch address is DSCR + RID<<4 where RID is the region identifier.

Table 24-1. Region Descriptor Structure (Main List)

Offset	Structure Member	Name
DSCR+0x00+RID*(0x10)	ICM Region Start Address	RADDR
DSCR+0x04+RID*(0x10)	ICM Region Configuration	RCFG
DSCR+0x08+RID*(0x10)	ICM Region Control	RCTRL
DSCR+0xC+RID*(0x10)	ICM Region Next Address	RNEXT

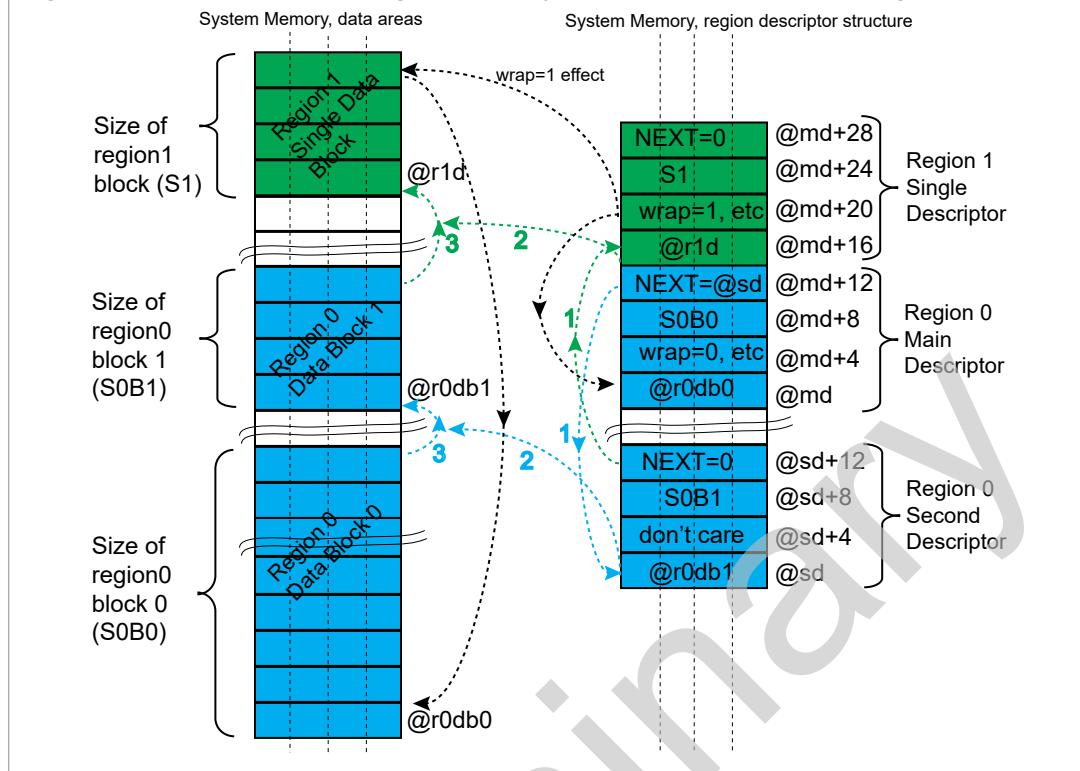
Example 24-1. ICM Monitoring of 3 Memory Data Blocks (Defined as 2 Regions)

The following figure shows the mandatory ICM settings to monitor three memory data blocks of the system memory (defined as two regions) with one region being not contiguous (two separate areas) and one contiguous memory area. For each said region, the SHA algorithm may be independently selected (different for each region). The wrap allows continuous monitoring.

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Figure 24-4. Example - Monitoring of 3 Memory Data Blocks (Defined as 2 Regions)



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24.6.3.1 Region Descriptor Structure Overview

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	RADDR	7:0				RADDR[7:0]				
		15:8				RADDR[15:8]				
		23:16				RADDR[23:16]				
		31:24				RADDR[31:24]				
0x04	RCFG	7:0	WCIEN	BEIEN	DMIEN	RHIEN		EOM	WRAP	CDWBN
		15:8			ALGO[2:0]			PROCDLY	SUIEN	ECIEN
		23:16								
		31:24								
0x08	RCTRL	7:0				TRSIZE[7:0]				
		15:8				TRSIZE[15:8]				
		23:16								
		31:24								
0x0C	RNEXT	7:0								
		15:8								
		23:16								
		31:24								

24.6.3.1.1 Region Start Address Structure Member

Name: RADDR
Offset: 0x00
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
RADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RADDR[31:0] Region Start Address

This field indicates the first byte address of the region

24.6.3.1.2 Region Configuration Structure Member

Name: RCFG
Offset: 0x04
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	1	1	1
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	1	1	1	1		0	0	0

Bits 14:12 – ALGO[2:0] User SHA Algorithm

Value	Name	Description
0	SHA1	SHA1 algorithm processed
1	SHA256	SHA256 algorithm processed
Other	-	Reserved

Bit 10 – PROCDLY Processing Delay

For a given SHA algorithm, the runtime period has two possible lengths:

Table 24-2. SHA Processing Runtime Periods

Algorithm	SHORTEST [number of cycles]	LONGEST [number of cycles]
SHA1	85	209
SHA256	72	194

Value	Name	Description
0	SHORTEST	SHA processing runtime is the shortest one
1	LONGEST	SHA processing runtime is the longest one

Bit 9 – SUIEN Monitoring Status Updated Condition Interrupt Enable

0: The RSU flag is set when the corresponding descriptor is loaded from memory to ICM.

1: The RSU flag remains cleared even if the condition is met.

Bit 8 – ECIEN End Bit Condition Interrupt Enable

0: The REC flag is set when the descriptor having the EOM bit set is processed.

1: The REC flag remains cleared even if the setting condition is met.

Bit 7 – WCINEN Wrap Condition Interrupt Disable

0: The RWC flag is set when the WRAP

1: The RWC flag remains cleared even if the setting condition is met.

Bit 6 – BEIEN Bus Error Interrupt Disable

0: The flag is set when an error is reported on the system bus by the bus MATRIX.

1: The flag remains cleared even if the setting condition is met.

Bit 5 – DMIEN Digest Mismatch Interrupt Disable

0: The RBE flag is set when the hash value just calculated from the processed region differs from expected hash value.

1: The RBE flag remains cleared even if the setting condition is met.

Bit 4 – RHien Region Hash Completed Interrupt Disable

0: The RHC flag is set when the field NEXT = 0 in a descriptor of the main or second list.

1: The RHC flag remains cleared even if the setting condition is met.

Bit 2 – EOM End of Monitoring

0: The current descriptor does not terminate the monitoring.

1: The current descriptor terminates the Main List. WRAP bit value has no effect.

Bit 1 – WRAP Wrap Command

0: The next region descriptor address loaded is the current region identifier descriptor address incremented by 0x10.

1: The next region descriptor address loaded is DSCR.

Bit 0 – CDWBN Compare Digest or Write Back Digest

0: The digest is written to the Hash area.

1: The digest value is compared to the digest stored in the Hash area.

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24.6.3.1.3 Region Control Structure Member

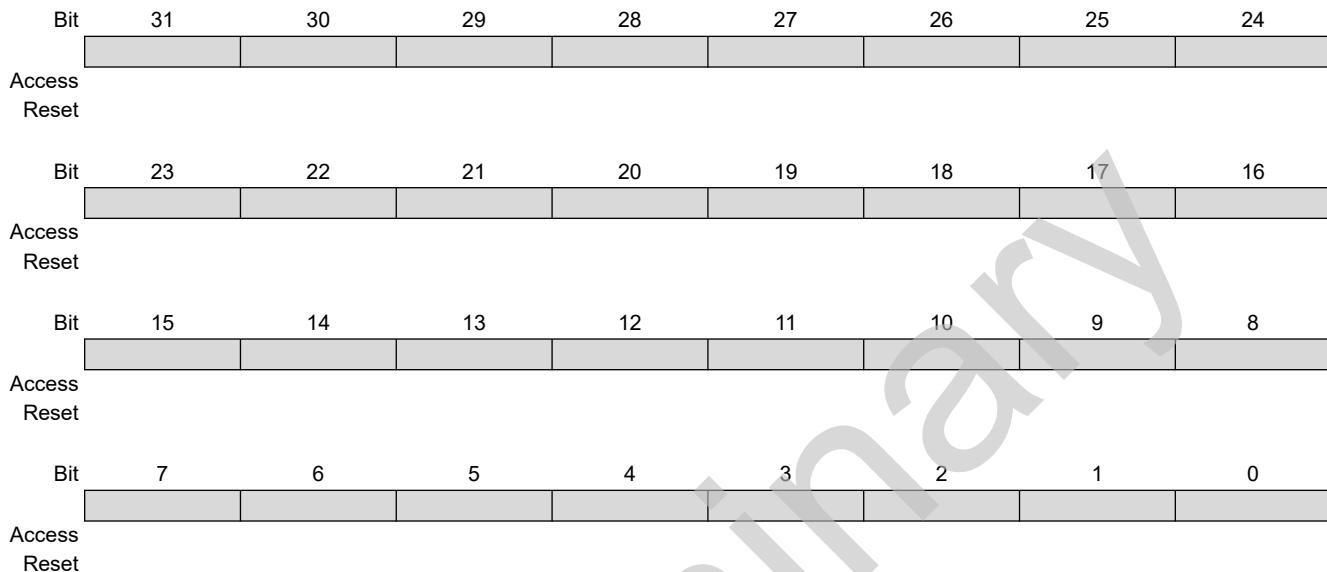
Name: RCTRL
Offset: 0x08
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
				TRSIZE[15:8]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				TRSIZE[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TRSIZE[15:0] Transfer Size for the Current Chunk of Data

24.6.3.1.4 Region Next Address Structure Member

Name: RNEXT
Offset: 0x0C
Reset: 0x00000000
Property: Read/Write



24.6.4 Using ICM as an SHA Engine

The ICM can be configured to only calculate a SHA1, SHA256 digest value.

24.6.4.1 Settings for Simple SHA Calculation

The start address of the system memory containing the data to hash must be configured in the transfer descriptor of the DMA embedded in the ICM.

The transfer descriptor is a system memory area integer multiple of 4 x 32-bit word and the start address of the descriptor must be configured in DSCR (the start address must be aligned on 64-bytes; six LSB must be cleared). If the data to hash is already padded according to SHA standards, only a single descriptor is required, and the EOM bit of RCFGn must be written to 1. If the data to hash does not contain a padding area, it is possible to define the padding area in another system memory location, the ICM can be configured to automatically jump from a memory area to another one by writing the descriptor register RNEXT with a value that differs from 0. Writing the RNEXT register with the start address of the padding area forces the ICM to concatenate both areas, thus providing the SHA result from the start address of the hash area configured in HASH.

Whether the system memory is configured as a single or multiple data block area, the bits CDWBN and WRAP must be cleared in the region descriptor structure member RCFGn. The bits WBDIS, EOMDIS, SLBDIS must be cleared in CFG.

Write the bits RHIEN and ECIEN in the Region Configuration Structure Member (RCFGn) to '0':

- The flag RHC[i], i being the region index, is set (if RHIEN is '0') when the hash result is available at address defined in HASH.
- The flag REC[i], i being the region index, is set (if ECIEN is '0') when the hash result is available at the address defined in HASH.

An interrupt is generated if the bit RHC[i] is written to '1' in the IER (if RHC[i] is set in RCTRL of region i) or if the bit REC[i] is written to 1 in the IER (if REC[i] is set in RCTRL of region i).

24.6.4.2 Processing Period

The SHA engine processing period can be configured by writing to the Region Configuration Structure Member register (RCFGn).

The short processing period allows to allocate bandwidth to the SHA module whereas the long processing period allocates more bandwidth on the system bus to other applications.

In SHA mode, the shortest processing period is 85 clock cycles + 2 clock cycles for start command synchronization. The longest period is 209 clock cycles + 2 clock cycles.

In SHA256 mode, the shortest processing period is 72 clock cycles + 2 clock cycles for start command synchronization. The longest period is 194 clock cycles + 2 clock cycles.

24.6.5 ICM Automatic Monitoring Mode

The ASCD bit of the CFG register is used to activate the ICM Automatic Mode. When CFG.ASCD is set, the ICM performs the following actions:

- The ICM controller passes through the Main List once with CDWBN bit in RCFGn at 0 (in other words, Write Back activated) and EOM bit in the RCFGn context register at 0.
- When RCFGn.WRAP=1, the ICM controller enters active monitoring, with CDWBN bit in context register now set, and EOM bit in context register cleared. Writing to the CDWBN and EOM bits in RCFGn has no effect.

24.6.6 ICM Configuration Parameters

Transfer Type	Main List	RCFG			RNEXT	Comments
		CDWBN	WRAP	EOM	NEXT	
Single Region	Contiguous list of blocks Digest written to memory Monitoring disabled	1 item	0	0	1	0
	Non-contiguous list of blocks Digest written to memory Monitoring disabled	1 item	0	0	1	Secondary List address of the current region identifier The Main List contains only one descriptor. The Secondary List describes the layout of the non-contiguous region.
	Contiguous list of blocks Digest comparison enabled Monitoring enabled	1 item	1	1	0	When the hash computation is terminated, the digest is compared with the one saved in memory.

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Transfer Type		Main List	RCFG			RNEXT	Comments
			CDWBN	WRAP	EOM	NEXT	
Multiple Regions	Contiguous list of blocks	More than one item	0	0	1 for the last, 0 otherwise	0	ICM passes through the list once.
	Digest written to memory						
	Monitoring disabled						
	Contiguous list of blocks	More than one item	1	1 for the last, 0 otherwise	0	0	ICM performs active monitoring of the regions. If a mismatch occurs, an interrupt is raised.
	Digest comparison is enabled						
	Monitoring is enabled						
	Non-contiguous list of blocks	More than one item	0	0	1	Secondary List address	ICM performs hashing and saves digests to the Hash area.
	Digest is written to memory						
	Monitoring is disabled						
	Non-contiguous list of blocks	More than one item	1	1	0	Secondary List address	ICM performs data gathering on a per region basis.
	Digest comparison is enabled						
	Monitoring is enabled						

24.6.7 Security Features

When an undefined register access occurs, the URAD bit in the Interrupt Status Register (ISR) is set if unmasked. Its source is then reported in the Undefined Access Status Register (UASR). Only the first undefined register access is available through the UASR.URAT field.

Several kinds of unspecified register accesses can occur:

- Unspecified structure member set to one detected when the descriptor is loaded
- Configuration register (CFG) modified during active monitoring
- Descriptor register (DSCR) modified during active monitoring
- Hash register (HASH) modified during active monitoring
- Write-only register read access

The URAD bit and the URAT field can only be reset by writing a 1 to the CTRL.SWRST bit.

24.7 Register Summary - ICM

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CFG	7:0	BBC[3:0]					SLBDIS	EOMDIS	WBDIS
		15:8	UALGO[2:0]			UIHASH			DUALBUFF	ASCD
		23:16								
		31:24								
0x04	CTRL	7:0	REHASH[3:0]					SWRST	DISABLE	ENABLE
		15:8	RMEN[3:0]					RMDIS[3:0]		
		23:16								
		31:24								
0x08	SR	7:0								ENABLE
		15:8	RMDIS[3:0]					RAWRMDIS[3:0]		
		23:16								
		31:24								
0x0C ...	Reserved									
0x10	IER	7:0	RDM[3:0]					RHC[3:0]		
		15:8	RWC[3:0]					RBE[3:0]		
		23:16	RSU[3:0]					REC[3:0]		
		31:24								URAD
0x14	IDR	7:0	RDM[3:0]					RHC[3:0]		
		15:8	RWC[3:0]					RBE[3:0]		
		23:16	RSU[3:0]					REC[3:0]		
		31:24								URAD
0x18	IMR	7:0	RDM[3:0]					RHC[3:0]		
		15:8	RWC[3:0]					RBE[3:0]		
		23:16	RSU[3:0]					REC[3:0]		
		31:24								URAD
0x1C	ISR	7:0	RDM[3:0]					RHC[3:0]		
		15:8	RWC[3:0]					RBE[3:0]		
		23:16	RSU[3:0]					REC[3:0]		
		31:24								URAD
0x20	UASR	7:0						URAT[2:0]		
		15:8								
		23:16								
		31:24								
0x24 ...	Reserved									
0x30	DSCR	7:0	DASA[1:0]							
		15:8						DASA[9:2]		
		23:16						DASA[17:10]		
		31:24						DASA[25:18]		
0x34	HASH	7:0								
		15:8								
		23:16								
		31:24								
0x38	UIHVALx0	7:0						VAL[7:0]		
		15:8						VAL[15:8]		
		23:16						VAL[23:16]		
		31:24						VAL[31:24]		
0x3C	UIHVALx1	7:0						VAL[7:0]		
		15:8						VAL[15:8]		
		23:16						VAL[23:16]		
		31:24						VAL[31:24]		

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x40	UIHVALx2	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			
0x44	UIHVALx3	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			
0x48	UIHVALx4	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			
0x4C	UIHVALx5	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			
0x50	UIHVALx6	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			
0x54	UIHVALx7	7:0					VAL[7:0]			
		15:8					VAL[15:8]			
		23:16					VAL[23:16]			
		31:24					VAL[31:24]			

24.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to [21.5.7. Register Access Protection](#).

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

24.8.1 Configuration Register

Name: CFG
Offset: 0x00
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access		UALGO[2:0]		UIHASH			DUALBUFF	ASCD
Reset	-	-	-	-			-	R/W
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bits 15:13 – UALGO[2:0] User SHA Algorithm

Value	Name	Description
0	SHA1	SHA1 algorithm processed
1	SHA256	SHA256 algorithm processed
Other	-	Reserved

Bit 12 – UIHASH User Initial Hash Value

Value	Description
0	The secure hash standard provides the initial hash value.
1	The initial hash value is programmable. Field UALGO provides the SHA algorithm. The ALGO field of the RCFGn structure member has no effect.

Bit 9 – DUALBUFF Dual Input Buffer

Value	Description
0	Dual Input buffer mode is disabled.
1	Dual Input buffer mode is enabled (Better performances, higher bandwidth required on system bus).

Bit 8 – ASCD Automatic Switch To Compare Digest

Value	Description
0	Automatic mode is disabled.
1	When this mode is enabled, the ICM controller automatically switches to active monitoring after the first Main List pass. Both CDWBN and WBDIS bits have no effect. A '1' must be written to the End of Monitoring bit in the Region Configuration register (RCFG.EOM) to terminate the monitoring.

Bits 7:4 – BBC[3:0] Bus Burden Control

This field is used to control the burden of the ICM system bus. The number of system clock cycles between the end of the current processing and the next block transfer is set to 2^{BBC} . Up to 32768 cycles can be inserted.

Bit 2 – SLBDIS Secondary List Branching Disable

Value	Description
0	Branching to the Secondary List is permitted.
1	Branching to the Secondary List is forbidden. The NEXT field of the RNEXT structure member has no effect and is always considered as zero.

Bit 1 – EOMDIS End of Monitoring Disable

Value	Description
0	End of Monitoring is permitted.
1	End of Monitoring is forbidden. The EOM bit of the RCFG structure member has no effect.

Bit 0 – WBDIS Write Back Disable

1:

When the Automatic Switch to Compare Digest bit of this register (CFG.ASCD) is written to '1', this bit value has no effect.

Value	Description
0	Write Back Operations are permitted.
1	Write Back Operations are forbidden: Context register CDWBN bit is internally set to '1' and cannot be modified by a linked list element. The CDWBN bit of the RCFG structure member has no effect.

24.8.2 Control Register

Name: CTRL
Offset: 0x04
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	W	W	W	W	W	W	W	W
Reset								
Bit	7	6	5	4	3	2	1	0
Access	W	W	W	W		W	W	W
Reset						0	0	

Bits 15:12 – RMEN[3:0] Region Monitoring Enable

Value	Description
0	No effect.
1	When bit RMEN[i] is written to '1', the monitoring of region with identifier i is activated.

Bits 11:8 – RMDIS[3:0] Region Monitoring Disable

Value	Description
0	No effect.
1	When REHASH[i] is written to '1', Region i digest is re-computed. This bit is only available when region monitoring is disabled.

Bits 7:4 – REHASH[3:0] Recompute Internal Hash

Value	Description
0	No effect.
1	When REHASH[i] is written to '1', Region i digest is re-computed. This bit is only available when region monitoring is disabled.

Bit 2 – SWRST Software Reset

Value	Description
0	No effect.
1	Resets the ICM controller.

Bit 1 – DISABLE ECM Disable

Value	Description
0	No effect.
1	The ICM controller is disabled. If a region is activated, the region is terminated.

Bit 0 – ENABLE ICM Enable

Value	Description
0	No effect.

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Value	Description
1	The ICM controller is activated.

Preliminary

24.8.3 Status Register

Name: SR
Offset: 0x08
Property: Read-Only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	RMDIS[3:0]				RAWRMDIS[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access								
Reset								
	ENABLE							
								R
								0

Bits 15:12 – RMDIS[3:0] Region Monitoring Disabled Status

Value	Description
0	Region i is being monitored (occurs after integrity check value has been calculated and written to Hash area).
1	Region i is not being monitored.

Bits 11:8 – RAWRMDIS[3:0] Region Monitoring Disabled Raw Status

Value	Description
0	Region i monitoring has been activated by writing a 1 in RMEN[i] of CTRL
1	Region i monitoring has been deactivated by writing a 1 in RMDIS[i] of CTRL

Bit 0 – ENABLE ICM Controller Enable Register

Value	Description
0	ICM controller is disabled.
1	ICM controller is activated.

24.8.4 Interrupt Enable Register

Name: IER
Offset: 0x10
Reset: 0x00000000
Property: Write-Only

Bit	31	30	29	28	27	26	25	24
Access								URAD
Reset								0
Bit	23	22	21	20	19	18	17	16
			RSU[3:0]				REC[3:0]	
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
			RWC[3:0]				RBE[3:0]	
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
			RDM[3:0]				RHC[3:0]	
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 24 – URAD Undefined Register Access Detection Interrupt Enable

0: No effect

1: The Undefined Register Access interrupt is enabled.

Bits 23:20 – RSU[3:0] Region Status Updated Interrupt Enable

0: No effect

1: When RSU[i] is written to '1', the region i Status Updated interrupt is enabled.

Bits 19:16 – REC[3:0] Region End bit Condition Detected Interrupt Enable

0: No effect

1: When REC[i] is written to '1', the region i End bit Condition interrupt is enabled.

Bits 15:12 – RWC[3:0] Region Wrap Condition detected Interrupt Enable

0: No effect

1: When RWC[i] is written to '1', the Region i Wrap Condition interrupt is enabled.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Enable

Value	Description
0	No effect.
1	When RBE[i] is written to '1', the Region i Bus Error interrupt is enabled.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Enable

Value	Description
0	No effect.
1	When RDM[i] is written to '1', the Region i Digest Mismatch interrupt is enabled.

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Enable

Value	Description
0	No effect.

PIC32CX-BZ2 and WBZ45 Family

ICM - Integrity Check Monitor

Value	Description
1	When RHC[i] is written to '1', the Region i Hash Completed interrupt is enabled.

Preliminary

24.8.5 Interrupt Disable Register

Name: IDR
Offset: 0x14
Property: Write-Only

Bit	31	30	29	28	27	26	25	24	
Access								URAD	
Reset									W
Bit	23	22	21	20	19	18	17	16	
Access			RSU[3:0]			REC[3:0]			
Reset	W	W	W	W	W	W	W	W	
Bit	15	14	13	12	11	10	9	8	
Access			RWC[3:0]			RBE[3:0]			
Reset	W	W	W	W	W	W	W	W	
Bit	7	6	5	4	3	2	1	0	
Access			RDM[3:0]			RHC[3:0]			
Reset	W	W	W	W	W	W	W	W	

Bit 24 – URAD Undefined Register Access Detection Interrupt Disable

Value	Description
0	No effect.
1	Undefined Register Access Detection interrupt is disabled.

Bits 23:20 – RSU[3:0] Region Status Updated Interrupt Disable

Value	Description
0	No effect.
1	When RSU[i] is written to '1', the region i Status Updated interrupt is disabled.

Bits 19:16 – REC[3:0] Region End bit Condition detected Interrupt Disable

Value	Description
0	No effect.
1	When REC[i] is written to '1', the region i End bit Condition interrupt is disabled.

Bits 15:12 – RWC[3:0] Region Wrap Condition Detected Interrupt Disable

Value	Description
0	No effect.
1	When RWC[i] is written to '1', the Region i Wrap Condition interrupt is disabled.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Disable

Value	Description
0	No effect.
1	When RBE[i] is written to '1', the Region i Bus Error interrupt is disabled.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Disable

Value	Description
0	No effect.
1	When RDM[i] is written to '1', the Region i Digest Mismatch interrupt is disabled.

PIC32CX-BZ2 and WBZ45 Family

ICM - Integrity Check Monitor

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Disable

Value	Description
0	No effect.
1	When RHC[i] is written to '1', the Region i Hash Completed interrupt is disabled.

Preliminary

24.8.6 Interrupt Mask Register

Name: IMR
Offset: 0x18
Reset: 0x00000000
Property: Read-Only

Bit	31	30	29	28	27	26	25	24
Access								URAD
Reset								0
Bit	23	22	21	20	19	18	17	16
			RSU[3:0]			REC[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
			RWC[3:0]			RBE[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
			RDM[3:0]			RHC[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 24 – URAD Undefined Register Access Detection Interrupt Mask

Value	Description
0	The interrupt is disabled.
1	The interrupt is enabled.

Bits 23:20 – RSU[3:0] Region Status Updated Interrupt Mask

Value	Description
0	When RSU[i] is reading '0', the interrupt is disabled for region i.
1	When RSU[i] is reading '1', the interrupt is enabled for region i.

Bits 19:16 – REC[3:0] Region End bit Condition Detected Interrupt Mask

Value	Description
0	When REC[i] is reading '0', the interrupt is disabled for region i.
1	When REC[i] is reading '1', the interrupt is enabled for region i.

Bits 15:12 – RWC[3:0] Region Wrap Condition Detected Interrupt Mask

Value	Description
0	When RWC[i] is reading '0', the interrupt is disabled for region i.
1	When RWC[i] is reading '1', the interrupt is enabled for region i.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Mask

Value	Description
0	When RBE[i] is reading '0', the interrupt is disabled for region i.
1	When RBE[i] is reading '1', the interrupt is enabled for region i.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Mask

Value	Description
0	When RDM[i] is reading '0', the interrupt is disabled for region i.

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Value	Description
1	When RDM[i] is reading '1', the interrupt is enabled for region i.

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Mask

Value	Description
0	When RHC[i] is reading '0', the interrupt is disabled for region i.
1	When RHC[i] is reading '1', the interrupt is enabled for region i.

24.8.7 Interrupt Status Register

Name: ISR
Offset: 0x1C
Reset: 0x0
Property: Read-Only

Bit	31	30	29	28	27	26	25	24
Access								URAD
Reset								0
Bit	23	22	21	20	19	18	17	16
			RSU[3:0]			REC[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
			RWC[3:0]			RBE[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
			RDM[3:0]			RHC[3:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 24 – URAD Undefined Register Access Detection Status

The URAD bit is only reset by the SWRST bit in the CTRL register.

The Undefined Register Access Trace bit field in the Undefined Access Status Register (UASR.URAT) indicates the unspecified access type.

Value	Description
0	No undefined register access has been detected since the last SWRST.
1	At least one undefined register access has been detected since the last SWRST.

Bits 23:20 – RSU[3:0] Region Status Updated Detected
RSU[i] is set when a region status updated condition is detected.

Bits 19:16 – REC[3:0] Region End bit Condition Detected
REC[i] is set when an end bit condition is detected.

Bits 15:12 – RWC[3:0] Region Wrap Condition Detected
RWC[i] is set when a wrap condition is detected.

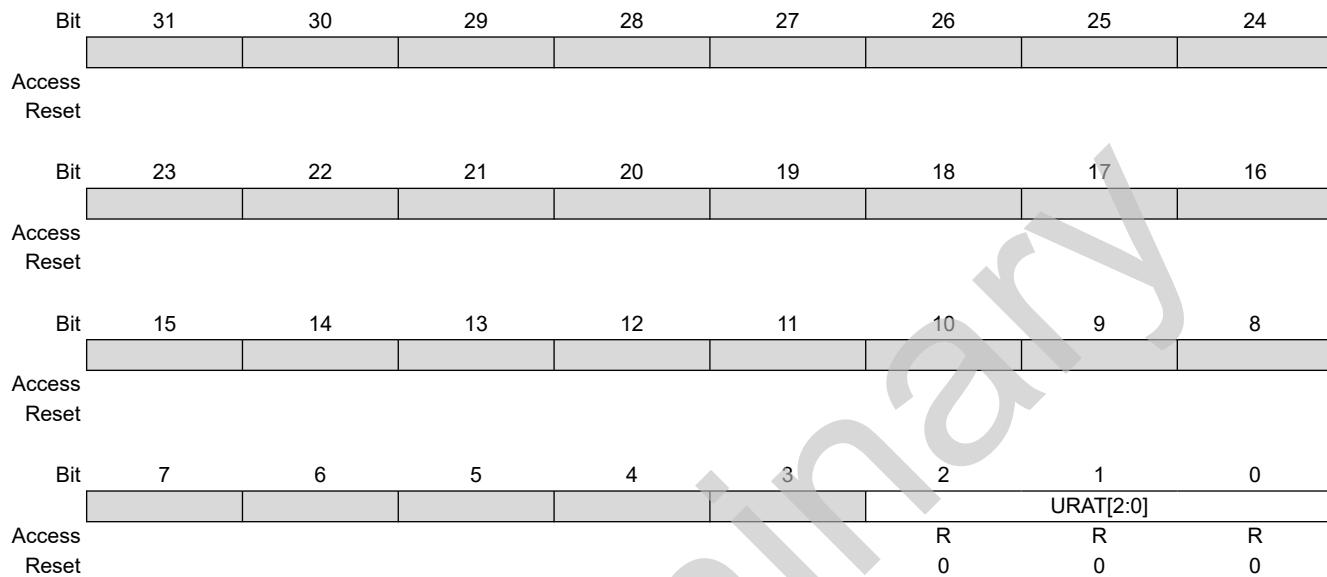
Bits 11:8 – RBE[3:0] Region Bus Error
RBE[i] is set when a bus error is detected while hashing memory region i.

Bits 7:4 – RDM[3:0] Region Digest Mismatch
RDM[i] is set when there is a digest comparison mismatch between the hash value of region i and the reference value located in the Hash Area.

Bits 3:0 – RHC[3:0] Region Hash Completed
RHC[i] is set when the ICM has completed the region with identifier i.

24.8.8 Undefined Access Status Register

Name: UASR
Offset: 0x20
Reset: 0x0
Property: Read-Only



Bits 2:0 – URAT[2:0] Undefined Register Access Trace

Only the first Undefined Register Access Trace is available through the URAT field.

The URAT field is only reset by the Software Reset bit in the Control register (CTRL.SWRST).

Value	Name	Description
0	UNSPEC_STRUCT_MEMBER	Unspecified structure member set to '1' detected when the descriptor is loaded.
1	ICM_CFG_MODIFIED	CFG modified during active monitoring.
2	ICM_DSCR_MODIFIED	DSCR modified during active monitoring.
3	ICM_HASH_MODIFIED	HASH modified during active monitoring
4	READ_ACCESS	Write-only register read access Only the first Undefined Register Access Trace is available through the URAT field. The URAT field is only reset by the SWRST bit in the CTRL register.

24.8.9 Descriptor Area Start Address Register

Name: DSCR
Offset: 0x30
Reset: 0x0
Property: -

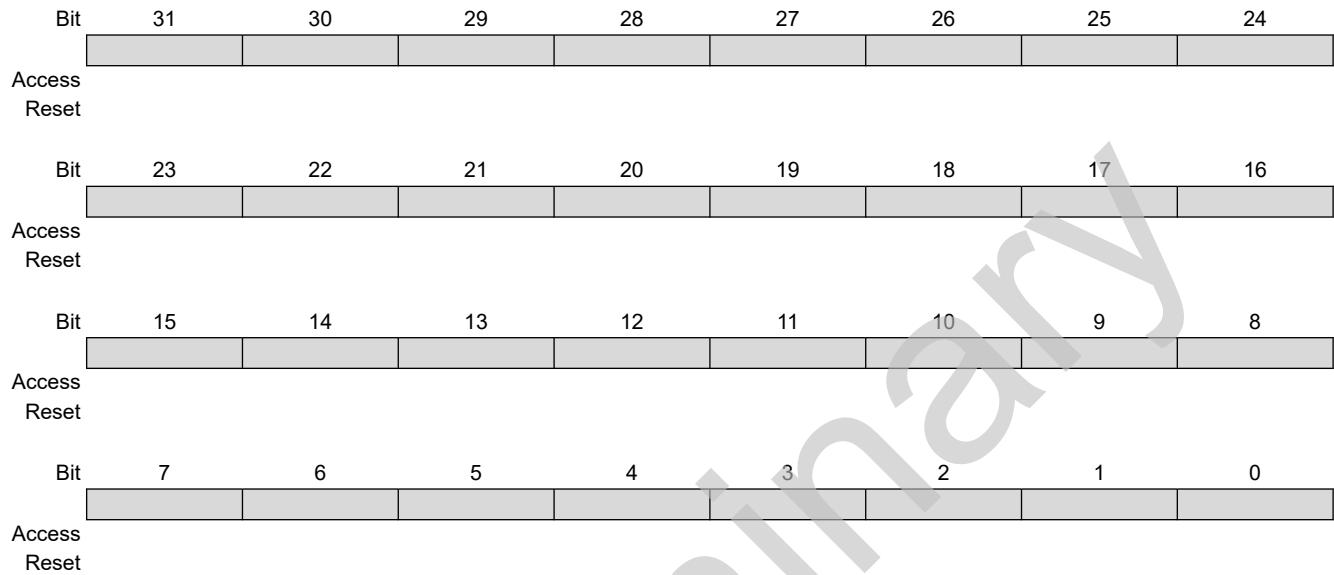
Bit	31	30	29	28	27	26	25	24
DASA[25:18]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DASA[17:10]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DASA[9:2]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DASA[1:0]								
Access	R/W	R/W						
Reset	0	0						

Bits 31:6 – DASA[25:0] Descriptor Area Start Address

The start address is a multiple of the total size of the data structure (64 bytes).

24.8.10 Hash Area Start Address Register

Name: HASH
Offset: 0x34
Reset: 0x00000000
Property: -



24.8.11 User Initial Hash Value Register

Name: UIHVALx
Offset: 0x38 + x*0x04 [x=0..7]
Reset: 0
Property: -

Bit	31	30	29	28	27	26	25	24
VAL[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
VAL[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
VAL[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
VAL[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – VAL[31:0] Initial Hash Value

When UIHASH bit of CFG register is set, the Initial Hash Value is user-programmable.

To meet the desired standard, use the following example values.

For UIHVAL0 field:

Example	Comment
0x67452301	SHA1 algorithm
0x6A09E667	SHA256 algorithm

For UIHVAL1 field:

Example	Comment
0xEFCDAB89	SHA1 algorithm
0xBB67AE85	SHA256 algorithm

For UIHVAL2 field:

Example	Comment
0x98BADCCE	SHA1 algorithm
0x3C6EF372	SHA256 algorithm

For UIHVAL3 field:

Example	Comment
0x10325476	SHA1 algorithm
0xA54FF53A	SHA256 algorithm

For UIHVAL4 field:

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Example	Comment
0xC3D2E1F0	SHA1 algorithm
0x510E527F	SHA256 algorithm

For UIHVAL5 field:

Example	Comment
0x9B05688C	SHA256 algorithm

For UIHVAL6 field:

Example	Comment
0x1F83D9AB	SHA256 algorithm

For UIHVAL7 field:

Example	Comment
0x5BE0CD19	SHA256 algorithm

Example of Initial Value for SHA-1 Algorithm

Register Address	Address Offset / Byte Lane			
	0x3 / 31:24	0x2 / 23:16	0x1 / 15:8	0x0 / 7:0
0x000 UIHVAL0	01	23	45	67
0x004 UIHVAL1	89	ab	cd	ef
0x008 UIHVAL2	fe	dc	ba	98
0x00C UIHVAL3	76	54	32	10
0x010 UIHVAL4	f0	e1	d2	c3

25. Peripheral Access Controller (PAC)

25.1 Overview

The Peripheral Access Controller provides an interface for the locking and unlocking of peripheral registers within the device. It reports all violations that could happen when accessing a peripheral: write protected access, illegal access, enable protected access, access when clock synchronization or software reset is on-going. These errors are reported in a unique interrupt flag for a peripheral. The PAC module also reports errors occurring at the slave bus level, when an access to a non-existing address is detected.

Note: The modules attached to PB-PIC bridge and wireless subsystem as well as RTCC, DSCON, PUKCC, and ICM excluded from PAC. The protection mechanism described in System Configuration Registers (CFG) to protects critical system registers, see *System Configuration Registers (CFG)* from Related Links.

Related Links

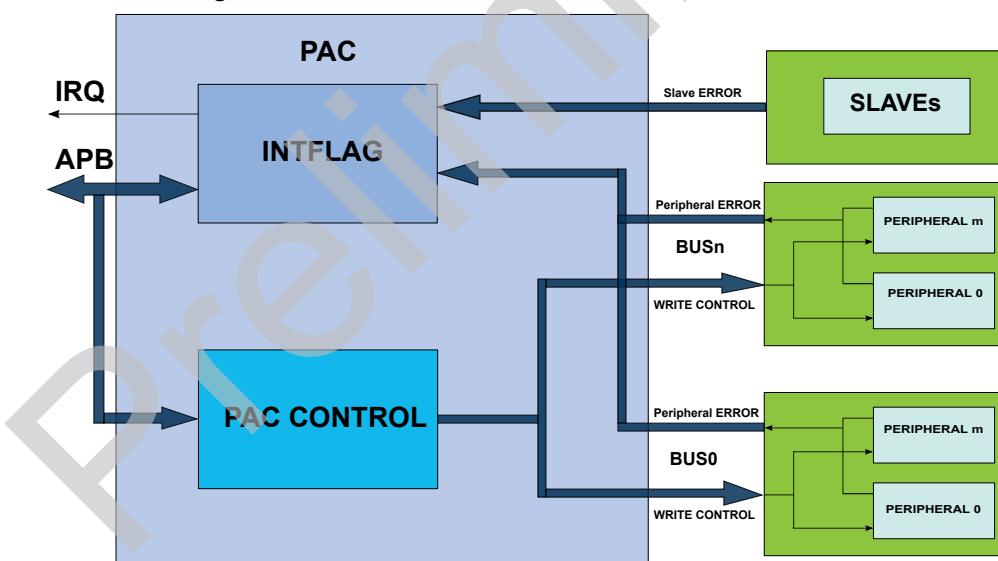
[17. System Configuration and Locking \(CFG\)](#)

25.2 Features

- Manages write protection access and reports access errors for the peripheral modules or bridges.

25.3 Block Diagram

Figure 25-1. PAC Block Diagram



25.4 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

25.4.1 IO Lines

Not applicable.

25.4.2 Power Management

The PAC can continue to operate in any Sleep mode where the selected source clock is running. The PAC interrupts can be used to wake up the device from Sleep modes. The events can trigger other operations in the system without exiting sleep modes.

25.4.3 DMA

Not applicable.

25.4.4 Interrupts

The interrupt request line is connected to the Interrupt Controller (NVIC). Using the PAC interrupt requires the Interrupt Controller to be configured first.

Table 25-1. Interrupt Lines

Instances	NVIC Line
PAC	PACERR

25.4.5 Events

The events are connected to the Event System, which may need configuration. See *Event System (EVSYS)* from Related Links.

Related Links

[27. Event System \(EVSYS\)](#)

25.4.6 Debug Operation

When the CPU is halted in Debug mode, write protection of all peripherals is disabled and the PAC continues normal operation.

25.4.7 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following PAC registers:

- Write Control (WRCTRL) register
- AHB Slave Bus Interrupt Flag Status and Clear (INTFLAGAHB) register
- Peripheral Interrupt Flag Status and Clear (INTFLAG A/B/C...) registers

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

Note: PAC write protection does not apply to accesses through an external debugger.

25.5 Functional Description

25.5.1 Principle of Operation

The Peripheral Access Control module allows the user to set a write protection on peripheral modules and generate an interrupt in case of a peripheral access violation. The peripheral's protection can be set, cleared or locked at the user discretion. A set of Interrupt Flag and Status registers informs the user on the status of the violation in the peripherals. In addition, slave bus errors can be also reported in the cases where reserved area is accessed by the application.

25.5.2 Basic Operation

25.5.2.1 Initialization, Enabling and Resetting

The PAC is always enabled after reset.

Only a hardware reset will reset the PAC module.

25.5.2.2 Operations

The PAC module allows the user to set, clear or lock the write protection status of all peripherals on all Peripheral Bridges, except the peripherals on PB-PIC bus.

If a peripheral register violation occurs, the Peripheral Interrupt Flag n registers (INTFLAGn) are updated to inform the user on the status of the violation in the peripherals connected to the Peripheral Bridge n (n = A,B,C ...). The corresponding Peripheral Write Control Status n register (STATUSn) gives the state of the write protection for all peripherals connected to the corresponding Peripheral Bridge n. See *Peripheral Access Errors* from Related Links.

The PAC module also report the errors occurring at slave bus level when an access to reserved area is detected. AHB Slave Bus Interrupt Flag register (INTFLAGAHB) informs the user on the status of the violation in the corresponding slave. See *AHB Slave Bus Errors* from Related Links.

Related Links

[25.5.2.3. Peripheral Access Errors](#)

[25.5.2.6. AHB Slave Bus Errors](#)

25.5.2.3 Peripheral Access Errors

The following events will generate a Peripheral Access Error:

- Protected write: To avoid unexpected writes to a peripheral's registers, each peripheral can be write protected. Only the registers denoted as "PAC Write-Protection" in the module's datasheet can be protected. If a peripheral is not write protected, write data accesses are performed normally. If a peripheral is write protected and if a write access is attempted, data will not be written and peripheral returns an access error. The corresponding interrupt flag bit in the INTFLAGn register will be set.
- Illegal access: Access to an unimplemented register within the module.
- Synchronized write error: For write-synchronized registers an error will be reported if the register is written while a synchronization is ongoing.

When any of the INTFLAGn registers bit are set, an interrupt will be requested if the PAC interrupt enable bit is set.

25.5.2.4 Write Access Protection Management

Peripheral access control can be enabled or disabled by writing to the WRCTRL register.

The data written to the WRCTRL register is composed of two fields; WRCTRL.PERID and WRCTRL.KEY. The WRCTRL.PERID is an unique identifier corresponding to a peripheral. The WRCTRL.KEY is a key value that defines the operation to be done on the control access bit. These operations can be "clear protection", "set protection" and "set and lock protection bit".

The "clear protection" operation will remove the write access protection for the peripheral selected by WRCTRL.PERID. Write accesses are allowed for the registers in this peripheral.

The "set protection" operation will set the write access protection for the peripheral selected by WRCTRL.PERID. Write accesses are not allowed for the registers with write protection property in this peripheral.

The "set and lock protection" operation will set the write access protection for the peripheral selected by WRCTRL.PERID and locks the access rights of the selected peripheral registers. The write access protection will only be cleared by a hardware reset.

The peripheral access control status can be read from the corresponding STATUSn register.

25.5.2.5 Write Access Protection Management Errors

Only word-wise writes to the WRCTRL register will effectively change the access protection. Other type of accesses will have no effect and will cause a PAC write access error. This error is reported in the INTFLAGA.PAC bit.

PAC also offers an additional safety feature for correct program execution with an interrupt generated on double write clear protection or double write set protection. If a peripheral is write protected and a subsequent set protection operation is detected then the PAC returns an error, and similarly for a double clear protection operation.

In addition, an error is generated when writing a "set and lock" protection to a write-protected peripheral or when a write access is done to a locked set protection. This can be used to ensure that the application follows the intended program flow by always following a write protect with an unprotect and conversely. However in applications where a write protected peripheral is used in several contexts, e.g. interrupt, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulates the write protection status or when

the interrupt handler needs to unprotect the peripheral based on the current protection status by reading the STATUS register.

The errors generated while accessing the PAC module registers (eg. key error, double protect error...) will set the INTFLAGA.PAC flag.

25.5.2.6 AHB Slave Bus Errors

The PAC module reports errors occurring at the AHB Slave bus level. These errors are generated when an access is performed at an address where no slave (bridge or peripheral) is mapped . These errors are reported in the corresponding bits of the INTFLAGAHB register.

25.5.2.7 Generating Events

The PAC module can also generate an event when any of the Interrupt Flag registers bit are set. To enable the PAC event generation, the control bit EVCTRL.ERREO must be set a '1'.

25.5.3 DMA Operation

Not applicable.

25.5.4 Interrupts

The PAC has the following interrupt source:

- Error (ERR): Indicates that a peripheral access violation occurred in one of the peripherals controlled by the PAC module, or a bridge error occurred in one of the bridges reported by the PAC
 - This interrupt is a synchronous wake-up source.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAGAHB and INTFLAGn) registers is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the PAC is reset. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAGAHB and INTFLAGn registers to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated.

25.5.5 Events

The PAC can generate the following output event:

- Error (ERR): Generated when one of the interrupt flag registers bits is set

Writing a '1' to an Event Output bit in the Event Control Register (EVCTRL.ERREO) enables the corresponding output event. Writing a '0' to this bit disables the corresponding output event.

25.5.6 Sleep Mode Operation

In Sleep mode, the PAC is kept enabled if an available bus master (CPU, DMA) is running. The PAC will continue to catch access errors from the module and generate interrupts or events.

25.5.7 Synchronization

Not applicable.

25.6 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	WRCTRL	7:0					PERID[7:0]			
		15:8					PERID[15:8]			
		23:16					KEY[7:0]			
		31:24								
0x04	EVCTRL	7:0								ERREO
0x05 ...	Reserved									
0x07										
0x08	INTENCLR	7:0								ERR
0x09	INTENSET	7:0								ERR
0x0A ...	Reserved									
0x0F										
0x10	INTFLAGAHB	7:0	PBBB	PBAB	PFLASH	CFLASH	SRAM3	SRAM2	SRAM1	SRAM0
		15:8					PUKCC	QSPI	PBPICB	PBCB
		23:16								
		31:24								
0x14	INTFLAGA	7:0	TC2	TC1	TC0	SERCOM1	SERCOM0	EIC	FREQM	PAC
		15:8					TCC2	TCC1	TCC0	TC3
		23:16								
		31:24								
0x18	INTFLAGB	7:0				RAMECC	EVSYS	DMAC		DSU
		15:8								
		23:16								
		31:24								
0x1C	INTFLAGC	7:0	AC	CCL		SERCOM3	SERCOM2		AES	QSPI
		15:8						TRNG		
		23:16								
		31:24								
0x20 ...	Reserved									
0x33										
0x34	STATUSA	7:0	TC2	TC1	TC0	SERCOM1	SERCOM0	EIC	FREQM	PAC
		15:8					TCC2	TCC1	TCC0	TC3
		23:16								
		31:24								
0x38	STATUSB	7:0				RAMECC	EVSYS	DMAC		DSU
		15:8								
		23:16								
		31:24								
0x3C	STATUSC	7:0	AC	CCL		SERCOM3	SERCOM2		AES	QSPI
		15:8						TRNG		
		23:16								
		31:24								

25.7 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to the related links.

25.7.1 Write Control

Name: WRCTRL
Offset: 0x00
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
KEY[7:0]								
Access	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
PERID[15:8]								
Access	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
PERID[7:0]								
Access	RW							
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – KEY[7:0] Peripheral Access Control Key

These bits define the peripheral access control key:

Value	Name	Description
0x0	OFF	No action
0x1	CLEAR	Clear the peripheral write control
0x2	SET	Set the peripheral write control
0x3	LOCK	Set and lock the peripheral write control until the next hardware reset

Bits 15:0 – PERID[15:0] Peripheral Identifier

The PERID represents the peripheral whose control is changed using the WRCTRL.KEY. The Peripheral Identifier is calculated following formula:

$$PERID = 32 * \text{BridgeNumber} + N$$

Where BridgeNumber represents the Peripheral Bridge Number (0 for Peripheral Bridge A, 1 for Peripheral Bridge B, etc.). N represents the peripheral index from the respective Bridge Number, which can be found in the tables of Section 12 Peripheral Configuration Summary in the "PAC, Index" column.

Table 25-2. PERID Values

Periph. Bridge Name	BridgeNumber	PERID Values
A	0	0+N
B	1	32+N
C	2	64+N
D	3	96+N

25.7.2 Event Control

Name: EVCTRL
Offset: 0x04
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0	ERREO
Access									RW
Reset									0

Bit 0 – ERREO Peripheral Access Error Event Output

This bit indicates if the Peripheral Access Error Event Output is enabled or disabled. When enabled, an event will be generated when one of the interrupt flag registers bits (INTFLAGAHB, INTFLAGn) is set:

Value	Description
0	Peripheral Access Error Event Output is disabled.
1	Peripheral Access Error Event Output is enabled.

25.7.3 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0	ERR
Access									RW
Reset								0	

Bit 0 – ERR Peripheral Access Error Interrupt Disable

This bit indicates that the Peripheral Access Error Interrupt is enabled and an interrupt request will be generated when one of the interrupt flag registers bits (INTFLAGAHB, INTFLAGn) is set:

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Peripheral Access Error interrupt Enable bit and disables the corresponding interrupt request.

Value	Description
0	Peripheral Access Error interrupt is disabled.
1	Peripheral Access Error interrupt is enabled.

25.7.4 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENCLR).

Bit	7	6	5	4	3	2	1	0	ERR
Access									RW
Reset								0	

Bit 0 – ERR Peripheral Access Error Interrupt Enable

This bit indicates that the Peripheral Access Error Interrupt is enabled and an interrupt request will be generated when one of the interrupt flag registers bits (INTFLAGAHB, INTFLAGn) is set:

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Peripheral Access Error interrupt Enable bit and enables the corresponding interrupt request.

Value	Description
0	Peripheral Access Error interrupt is disabled.
1	Peripheral Access Error interrupt is enabled.

25.7.5 Bridge Interrupt Flag Status

Name: INTFLAGAHB
Offset: 0x10
Reset: 0x00000000
Property: -

These flags are cleared by writing a '1' to the corresponding bit.

These flags are set when an access error is detected by the corresponding AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					PUKCC	QSPI	PBPICB	PBCB
Reset					RW	RW	RW	RW
Bit	7	6	5	4	3	2	1	0
Access	PBBB	PBAB	PFLASH	CFLASH	SRAM3	SRAM2	SRAM1	SRAM0
Reset	RW	RW	RW	RW	RW	U	U	RW
	0	0	0	0	0	0	0	0

Bit 11 – PUKCC Interrupt Flag for PUKCC

This flag is set when an access error is detected by the PUKCC AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PUKCC interrupt flag.

Bit 10 – QSPI Interrupt Flag for QSPI

This flag is set when an access error is detected by the QSPI AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the QSPI interrupt flag.

Bit 9 – PBPICB Interrupt Flag for PBPICB (PB-PIC-Bridge)

This flag is set when an access error is detected by the PBPICB AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PBPICB interrupt flag.

Bit 8 – PBCB Interrupt Flag for PBCB (PB-Bridge-C)

This flag is set when an access error is detected by the PBCB AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PBCB interrupt flag.

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Bit 7 – PBBB Interrupt Flag for PBBB (PB-Bridge-B)

This flag is set when an access error is detected by the PBBB AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PBBB interrupt flag.

Bit 6 – PBAB Interrupt Flag for HPB1 (PB-Bridge-A)

This flag is set when an access error is detected by the PBAB AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PBAB interrupt flag.

Bit 5 – PFLASH Interrupt Flag for PFLASH (Peripheral Flash)

This flag is set when an access error is detected by the PFLASH AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the PFLASH interrupt flag.

Bit 4 – CFLASH Interrupt Flag for CFLASH (CPU Flash)

This flag is set when an access error is detected by the CFLASH AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the CFLASH interrupt flag.

Bit 3 – SRAM3 Interrupt Flag for SRAM3

This flag is set when an access error is detected by the SRAM3 AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the SRAM3 interrupt flag.

Bit 2 – SRAM2 Interrupt Flag for SRAM2

This flag is set when an access error is detected by the SRAM2 AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the SRAM2 interrupt flag.

Bit 1 – SRAM1 Interrupt Flag for SRAM1

This flag is set when an access error is detected by the SRAM1 AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the SRAM1 interrupt flag.

Bit 0 – SRAM0 Interrupt Flag for SRAM0

This flag is set when an access error is detected by the SRAM0 AHB Slave, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' has no effect.

Writing a '1' to this bit will clear the SRAM0 interrupt flag.

25.7.6 Peripheral Interrupt Flag Status - Bridge A

Name: INTFLAGA
Offset: 0x14
Reset: 0x00000000
Property: -

These flags are set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGx bit, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to these bits has no effect.

Writing a '1' to these bits will clear the corresponding INTFLAGx interrupt flag.

Access	Bit 31	30	29	28	27	26	25	24
Reset								
Access	Bit 23	22	21	20	19	18	17	16
Reset								
Access	Bit 15	14	13	12	TCC2	TCC1	TCC0	TC3
Reset					RW 0	RW 0	RW 0	RW 0
Access	Bit 7	6	5	4	SERCOM1	SERCOM0	EIC	FREQM
Reset	TC2	TC1	TC0	RW 0	RW 0	RW 0	RW 0	RW 0
Access	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
Reset								

Bit 11 – TCC2 Interrupt Flag for TCC2

This bit is set when a Peripheral Access Error occurs while accessing the TCC2, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 10 – TCC1 Interrupt Flag for TCC1

This bit is set when a Peripheral Access Error occurs while accessing the TCC1, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 9 – TCC0 Interrupt Flag for TCC0

This bit is set when a Peripheral Access Error occurs while accessing the TCC0, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 8 – TC3 Interrupt Flag for TC3

This bit is set when a Peripheral Access Error occurs while accessing the TC3, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 7 – TC2 Interrupt Flag for TC2

This bit is set when a Peripheral Access Error occurs while accessing the TC2, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 6 – TC1 Interrupt Flag for TC1

This bit is set when a Peripheral Access Error occurs while accessing the TC1, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 5 – TC0 Interrupt Flag for TC0

This bit is set when a Peripheral Write Access Error occurs while accessing the TC0, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 4 – SERCOM1 Interrupt Flag for SERCOM1

This bit is set when a Peripheral Access Error occurs while accessing the SERCOM1, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 3 – SERCOM0 Interrupt Flag for SERCOM0

This bit is set when a Peripheral Access Error occurs while accessing the SERCOM0, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 2 – EIC Interrupt Flag for EIC

This bit is set when a Peripheral Access Error occurs while accessing the EIC, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 1 – FREQM Interrupt Flag for FREQM

This bit is set when a Peripheral Access Error occurs while accessing the FREQM, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 0 – PAC Interrupt Flag for PAC

This bit is set when a Peripheral Write Access Error occurs while accessing the PAC, and will generate an interrupt request if SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

25.7.7 Peripheral Interrupt Flag Status - Bridge B

Name: INTFLAGB
Offset: 0x18
Reset: 0x00000000
Property: –

These flags are set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGx bit, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to these bits has no effect.

Writing a '1' to these bits will clear the corresponding INTFLAGx interrupt flag.

Bit	31	30	29	28	27	26	25	24	
Access	[]	[]	[]	[]	[]	[]	[]	[]	
Reset	[]	[]	[]	[]	[]	[]	[]	[]	
Bit	23	22	21	20	19	18	17	16	
Access	[]	[]	[]	[]	[]	[]	[]	[]	
Reset	[]	[]	[]	[]	[]	[]	[]	[]	
Bit	15	14	13	12	11	10	9	8	
Access	[]	[]	[]	[]	[]	[]	[]	[]	
Reset	[]	[]	[]	[]	[]	[]	[]	[]	
Bit	7	6	5	4	RAMECC	EVSYS	DMAC	1	0
Access	[]	[]	[]	RW	RW	RW	[]	[]	RW
Reset	[]	[]	[]	0	0	0	[]	[]	0

Bit 4 – RAMECC Interrupt Flag for RAMECC

This flag is set when a Peripheral Access Error occurs while accessing the RAMECC, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the RAMECC interrupt flag.

Bit 3 – EVSYS Interrupt Flag for EVSYS

This flag is set when a Peripheral Access Error occurs while accessing the EVSYS, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the EVSYS interrupt flag.

Bit 2 – DMAC Interrupt Flag for DMAC

This flag is set when a Peripheral Access Error occurs while accessing the DMAC, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the DMAC interrupt flag.

Bit 0 – DSU Interrupt Flag for DSU

This flag is set when a Peripheral Access Error occurs while accessing the DSU, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the DSU interrupt flag.

25.7.8 Peripheral Interrupt Flag Status - Bridge C

Name: INTFLAGC
Offset: 0x1C
Reset: 0x00000000
Property: -

These flags are set when a Peripheral Access Error occurs while accessing the peripheral associated with the respective INTFLAGx bit, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to these bits has no effect.

Writing a '1' to these bits will clear the corresponding INTFLAGx interrupt flag.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access						TRNG		
Reset						RW		
Bit	7	6	5	4	3	2	1	0
Access	AC	CCL		SERCOM3	SERCOM2		AES	QSPI
Reset	RW	RW		RW	RW		RW	RW

Bit 10 – TRNG Interrupt Flag for TRNG

This flags is set when a Peripheral Access Error occurs while accessing the peripheral associated with the TRNG, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the TRNG interrupt flag.

Bit 7 – AC Interrupt Flag for AC

This flags is set when a Peripheral Access Error occurs while accessing the peripheral associated with the AC, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the AC interrupt flag.

Bit 6 – CCL Interrupt Flag for CCL

This flags is set when a Peripheral Access Error occurs while accessing the peripheral associated with the CCL, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the CCL interrupt flag.

Bit 4 – SERCOM3 Interrupt Flag for SERCOM3

This flags is set when a Peripheral Access Error occurs while accessing the peripheral associated with the SERCOM3, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the SERCOM3 interrupt flag.

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Bit 3 – SERCOM2 Interrupt Flag for SERCOM2

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the SERCOM2, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the SERCOM2 interrupt flag.

Bit 1 – AES Interrupt Flag for AES

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the AES, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the AES interrupt flag.

Bit 0 – QSPI Interrupt Flag for QSPI

This flag is set when a Peripheral Access Error occurs while accessing the peripheral associated with the QSPI, and will generate an interrupt request if INTENCLR/SET.ERR is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the QSPI interrupt flag.

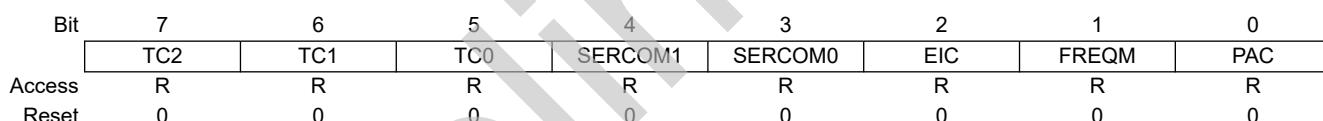
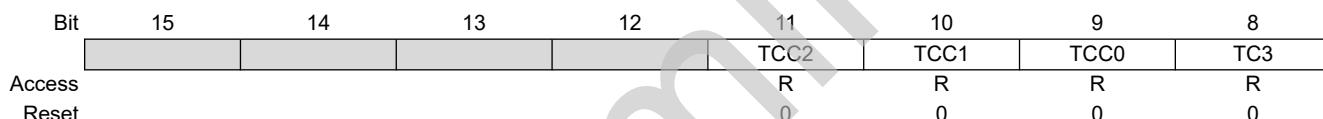
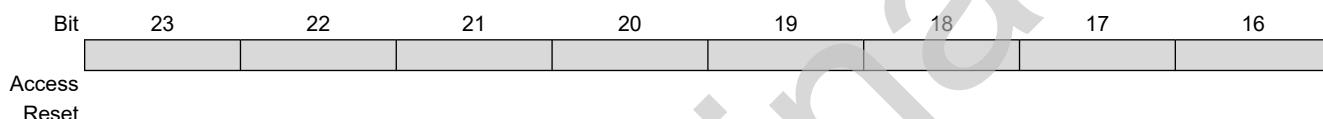
25.7.9 Peripheral Write Protection Status A

Name: STATUSA
Offset: 0x34
Reset: 0x00010000
Property: PAC Write-Protection

Writing to this register has no effect.

Reading STATUS register returns peripheral write protection status:

Value	Description							
0	Peripheral is not write protected.							
1	Peripheral is write protected.							



Bit 11 – TCC2 TCC2 APB Protect Enable

Value	Description
0	TCC2 is not write protected
1	TCC2 is write protected

Bit 10 – TCC1 TCC1 APB Protect Enable

Value	Description
0	TCC1 is not write protected
1	TCC1 is write protected

Bit 9 – TCC0 TCC0 APB Protect Enable

Value	Description
0	TCC0 is not write protected
1	TCC0 is write protected

Bit 8 – TC3 TC3 APB Protect Enable

Value	Description
0	TC3 is not write protected
1	TC3 is write protected

Bit 7 – TC2 TC2 APB Protect Enable

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Value	Description
0	TC2 is not write protected
1	TC2 is write protected

Bit 6 – TC1 TC1 APB Protect Enable

Value	Description
0	TC1 is not write protected
1	TC1 is write protected

Bit 5 – TC0 TC0 APB Protect Enable

Value	Description
0	TC0 is not write protected
1	TC0 is write protected

Bit 4 – SERCOM1 SERCOM1 APB Protect Enable

Value	Description
0	SERCOM1 is not write protected
1	SERCOM1 is write protected

Bit 3 – SERCOM0 SERCOM0 APB Protect Enable

Value	Description
0	SERCOM0 is not write protected
1	SERCOM0 is write protected

Bit 2 – EIC EIC APB Protect Enable

Value	Description
0	EIC is not write protected
1	EIC is write protected

Bit 1 – FREQM FREQM APB Protect Enable

Value	Description
0	FREQM is not write protected
1	FREQM is write protected

Bit 0 – PAC PAC APB Protect Enable

Value	Description
0	PAC is not write protected
1	PAC is write protected

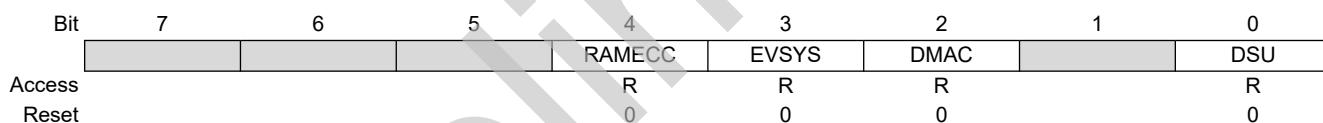
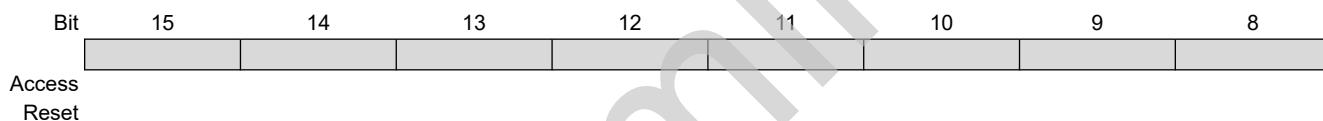
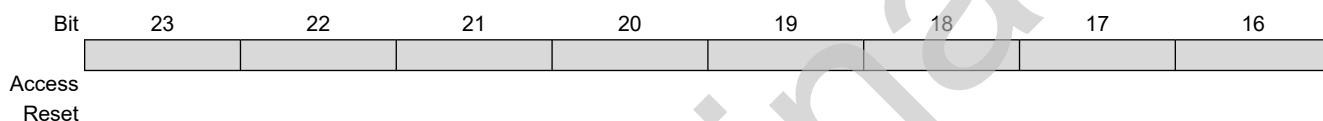
25.7.10 Peripheral Write Protection Status - Bridge B

Name: STATUSB
Offset: 0x38
Reset: 0x00000002
Property: PAC Write-Protection

Writing to this register has no effect.

Reading STATUS register returns peripheral write protection status:

Value	Description							
0	Peripheral is not write protected.							
1	Peripheral is write protected.							



Bit 4 – RAMECC RAMECC APB Protect Enable

Value	Description
0	RAMECC peripheral is not write protected
1	RAMECC peripheral is write protected

Bit 3 – EVSYS EVSYS APB Protect Enable

Value	Description
0	EVSYS peripheral is not write protected
1	EVSYS peripheral is write protected

Bit 2 – DMAC DMAC APB Protect Enable

Value	Description
0	DMAC peripheral is not write protected
1	DMAC peripheral is write protected

Bit 0 – DSU DSU APB Protect Enable

Value	Description
0	DSU peripheral is not write protected
1	DSU peripheral is write protected

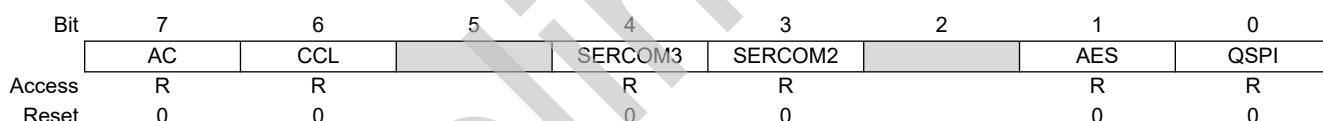
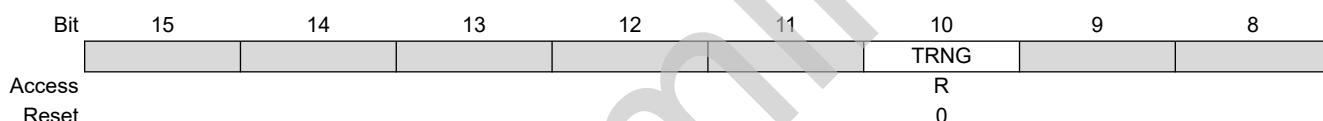
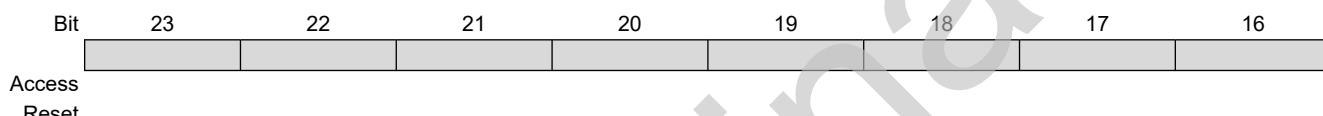
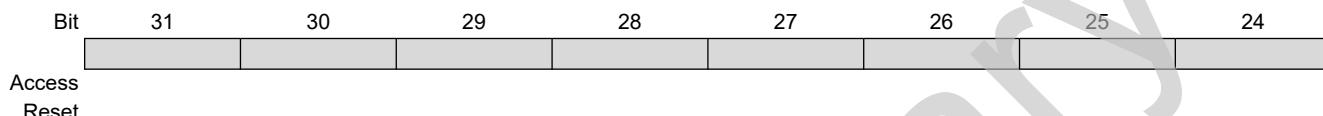
25.7.11 Peripheral Write Protection Status - Bridge C

Name: STATUSC
Offset: 0x3C
Reset: 0x00000000
Property: PAC Write-Protection

Writing to this register has no effect.

Reading STATUS register returns peripheral write protection status:

Value	Description							
0	Peripheral is not write protected.							
1	Peripheral is write protected.							



Bit 10 – TRNG TRNG APB Protection Enable

Value	Description	
0	Peripheral is not write protected	
1	Peripheral is write protected	

Bit 7 – AC AC APB Protection Enable

Value	Description	
0	Peripheral is not write protected	
1	Peripheral is write protected	

Bit 6 – CCL CCL APB Protection Enable

Value	Description	
0	Peripheral is not write protected	
1	Peripheral is write protected	

Bit 4 – SERCOM3 SERCOM3 APB Protection Enable

Value	Description	
0	Peripheral is not write protected	
1	Peripheral is write protected	

Bit 3 – SERCOM2 SERCOM2 APB Protection Enable

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Value	Description
0	Peripheral is not write protected
1	Peripheral is write protected

Bit 1 – AES AES APB Protection Enable

Value	Description
0	Peripheral is not write protected
1	Peripheral is write protected

Bit 0 – QSPI QSPI APB Protection Enable

Value	Description
0	Peripheral is not write protected
1	Peripheral is write protected

26. FREQM – Frequency Meter

26.1 Overview

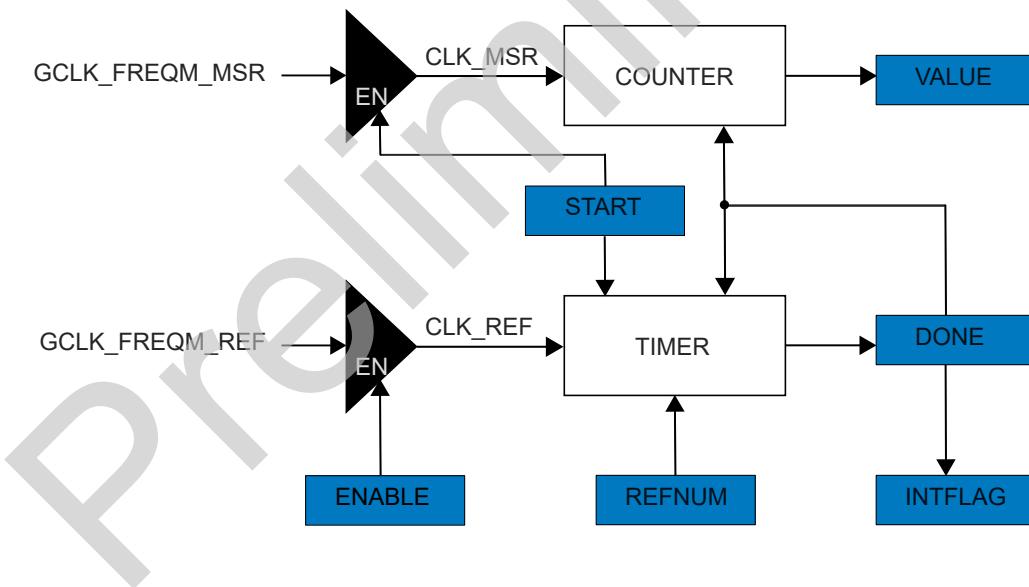
The Frequency Meter (FREQM) can be used to accurately measure the frequency of a clock by comparing it to a known reference clock.

26.2 Features

- Ratio can be measured with 24-bit accuracy
- Accurately measures the frequency of an input clock with respect to a reference clock
- Reference clock can be selected from the available GCLK_FREQM_REF sources
- Measured clock can be selected from the available GCLK_FREQM_MSR sources

26.3 Block Diagram

Figure 26-1. FREQM Block Diagram



26.4 Signal Description

Not applicable.

26.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

26.5.1 I/O Lines

The REFO lines (REFO[4:1]) can be used as measurement or reference clock sources. This requires the I/O pins to be configured.

26.5.2 Power Management

The FREQM will continue to operate in idle sleep mode where the selected source clock is running. The FREQM's interrupts can be used to wake up the device from idle sleep mode. See *Power Management Unit (PMU)* from Related Links for details on the different sleep modes.

Related Links

[14. Power Management Unit \(PMU\)](#)

26.5.3 Clocks

Two generic clocks are used by the FREQM: Reference Clock (GCLK_FREQM_REF) and Measurement Clock (GCLK_FREQM_MSR).

GCLK_FREQM_REF is required to clock the internal reference timer, which acts as the frequency reference.

GCLK_FREQM_MSR is required to clock a ripple counter for frequency measurement. These clocks must be configured and enabled in the generic clock controller before using the FREQM.

26.5.4 DMA

Not applicable.

26.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using FREQM interrupt requires the interrupt controller to be configured first.

26.5.6 Events

Not applicable.

26.5.7 Debug Operation

When the CPU is halted in debug mode the FREQM continues its normal operation. The FREQM cannot be halted when the CPU is halted in debug mode. If the FREQM is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

26.5.8 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

- Control B register (CTRLB)
- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

26.6 Functional Description

26.6.1 Principle of Operation

FREQM counts the number of periods of the measured clock (GCLK_FREQM_MSR) with respect to the reference clock (GCLK_FREQM_REF). The measurement is done for a period of $\text{REFNUM}/f_{\text{CLK_REF}}$ and stored in the Value register (VALUE.VALUE). REFNUM is the number of Reference clock cycles selected in the Configuration A register (CFG_A.REFNUM).

The frequency of the measured clock, $f_{\text{CLK_MSR}}$, is calculated by

$$f_{\text{CLK_MSR}} = \left(\frac{\text{VALUE}}{\text{REFNUM}} \right) f_{\text{CLK_REF}}. \text{ The error can be maximum two measured clock cycles.}$$

26.6.2 Basic Operation

26.6.2.1 Initialization

Before enabling FREQM, the device and peripheral must be configured:

- Each of the generic clocks (GCLK_FREQM_REF and GCLK_FREQM_MSR) must be configured and enabled.
- Write the number of Reference clock cycles for which the measurement is to be done in the Configuration A register ([CFG.A.REFNUM](#)). This must be a non-zero number.

The following register is enable-protected, meaning that it can only be written when the FREQM is disabled (CTRLA.ENABLE=0):

- Configuration A register (CFG.A)

Enable-protection is denoted by the "Enable-Protected" property in the register description.

26.6.2.2 Enabling, Disabling and Resetting

The FREQM is enabled by writing a '1' to the Enable bit in the Control A register ([CTRLA.ENABLE](#)). The peripheral is disabled by writing CTRLA.ENABLE=0.

The FREQM is reset by writing a '1' to the Software Reset bit in the Control A register ([CTRLA.SWRST](#)). On software reset, all registers in the FREQM will be reset to their initial state, and the FREQM will be disabled.

Then ENABLE and SWRST bits are write-synchronized.

Related Links

26.6.7. Synchronization

26.6.2.3 Measurement

In the Configuration A register, the Number of Reference Clock Cycles field (CFG.A.REFNUM) selects the duration of the measurement. The measurement is given in number of GCLK_FREQM_REF periods.

Note: The REFNUM field must be written before the FREQM is enabled.

After the FREQM is enabled, writing a '1' to the START bit in the Control B register (CTRLB.START) starts the measurement. The BUSY bit in Status register (STATUS.BUSY) is set when the measurement starts, and cleared when the measurement is complete.

There is also an interrupt request for Measurement Done: When the Measurement Done bit in Interrupt Enable Set register (INTENSET.DONE) is '1' and a measurement is finished, the Measurement Done bit in the Interrupt Flag Status and Clear register (INTFLAG.DONE) will be set and an interrupt request is generated.

The result of the measurement can be read from the Value register (VALUE.VALUE). The frequency of the measured clock GCLK_FREQM_MSR is then:

$$f_{\text{CLK_MSR}} = \left(\frac{\text{VALUE}}{\text{REFNUM}} \right) f_{\text{CLK_REF}}$$

Notes:

1. In order to make sure the measurement result (VALUE.VALUE[23:0]) is valid, the overflow status (STATUS.OVF) should be checked.
2. Due to asynchronous operations, the VALUE Error measurement can be up to two samples.

In case an overflow condition occurred, indicated by the overflow bit in the STATUS register (STATUS.OVF), either the number of reference clock cycles must be reduced (CFG.A.REFNUM), or a faster reference clock must be configured. Once the configuration is adjusted, clear the overflow status by writing a '1' to STATUS.OVF. Then another measurement can be started by writing a '1' to CTRLB.START.

Note: See CFG.A, CTRLB, STATUS, INTENSET, INTFLAG, VALUE registers in the *FREQM Register Summary* from Related Links.

Related Links

[26.7. FREQM Register Summary](#)

26.6.3 DMA Operation

Not applicable.

26.6.4 Interrupts

The FREQM has one interrupt source:

- DONE: A frequency measurement is done.

The interrupt flag in the Interrupt Flag Status and Clear ([26.8.6. INTFLAG](#)) register is set when the interrupt condition occurs. The interrupt can be enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set ([26.8.5. INTENSET](#)) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear ([26.8.4. INTENCLR](#)) register. The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the FREQM is reset. See [26.8.6. INTFLAG](#) for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the [26.8.6. INTFLAG](#) register to determine which interrupt condition is present.

This interrupt is a synchronous wake-up source.

Note that interrupts must be globally enabled for interrupt requests to be generated.

26.6.5 Events

Not applicable.

26.6.6 Sleep Mode Operation

The FREQM will continue to operate in Idle Sleep mode where the selected source clock is running. The FREQM's interrupts can be used to wake up the device from Idle Sleep mode.

For lowest chip power consumption in sleep modes, FREQM should be disabled before entering a Sleep mode.

26.6.7 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits and registers are write-synchronized:

- Software Reset bit in Control A register (CTRLA.SWRST)
- Enable bit in Control A register (CTRLA.ENABLE)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

26.7 FREQM Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0							ENABLE	SWRST
0x01	CTRLB	7:0								START
0x02	CFG A	7:0					REFNUM[7:0]			
		15:8								
0x04 ...	Reserved									
0x07										
0x08	INTENCLR	7:0								DONE
0x09	INTENSET	7:0								DONE
0x0A	INTFLAG	7:0								DONE
0x0B	STATUS	7:0							OVF	BUSY
0x0C	SYNCBUSY	7:0							ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x10	VALUE	7:0				VALUE[7:0]				
		15:8				VALUE[15:8]				
		23:16				VALUE[23:16]				
		31:24								

26.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

26.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access							ENABLE	SWRST
Reset							R/W	R/W
							0	0

Bit 1 – ENABLE Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled or disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the FREQM to their initial state, and the FREQM will be disabled.

Writing a '1' to this bit will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will be cleared when the Reset is complete.

Value	Description
0	There is no ongoing Reset operation.
1	The Reset operation is ongoing.

26.8.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0	START
Access									W
Reset									0

Bit 0 – START Start Measurement

Value	Description
0	Writing a '0' has no effect.
1	Writing a '1' starts a measurement.

26.8.3 Configuration A

Name: CFGA
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-protected

Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	REFNUM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – REFNUM[7:0] Number of Reference Clock Cycles

Selects the duration of a measurement in number of CLK_FREQM_REF cycles. This must be a non-zero value, i.e. 0x01 (one cycle) to 0xFF (255 cycles).

26.8.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	DONE
Access									R/W
Reset									0

Bit 0 – DONE Measurement Done Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Measurement Done Interrupt Enable bit, which disables the Measurement Done interrupt.

Value	Description
0	The Measurement Done interrupt is disabled.
1	The Measurement Done interrupt is enabled.

26.8.5 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	DONE
Access									R/W
Reset									0

Bit 0 – DONE Measurement Done Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Measurement Done Interrupt Enable bit, which enables the Measurement Done interrupt.

Value	Description
0	The Measurement Done interrupt is disabled.
1	The Measurement Done interrupt is enabled.

26.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0	DONE
Access									R/W
Reset									0

Bit 0 – DONE Mesurement Done

This flag is cleared by writing a '1' to it.

This flag is set when the STATUS.BUSY bit has a one-to-zero transition.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the DONE interrupt flag.

26.8.7 Status

Name: STATUS
Offset: 0x0B
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
Access							OVF	BUSY
Reset							R/W	R

Bit 1 – OVF Sticky Count Value Overflow

This bit is cleared by writing a '1' to it.

This bit is set when an overflow condition occurs to the value counter.

Writing a '0' to this bit has no effect.

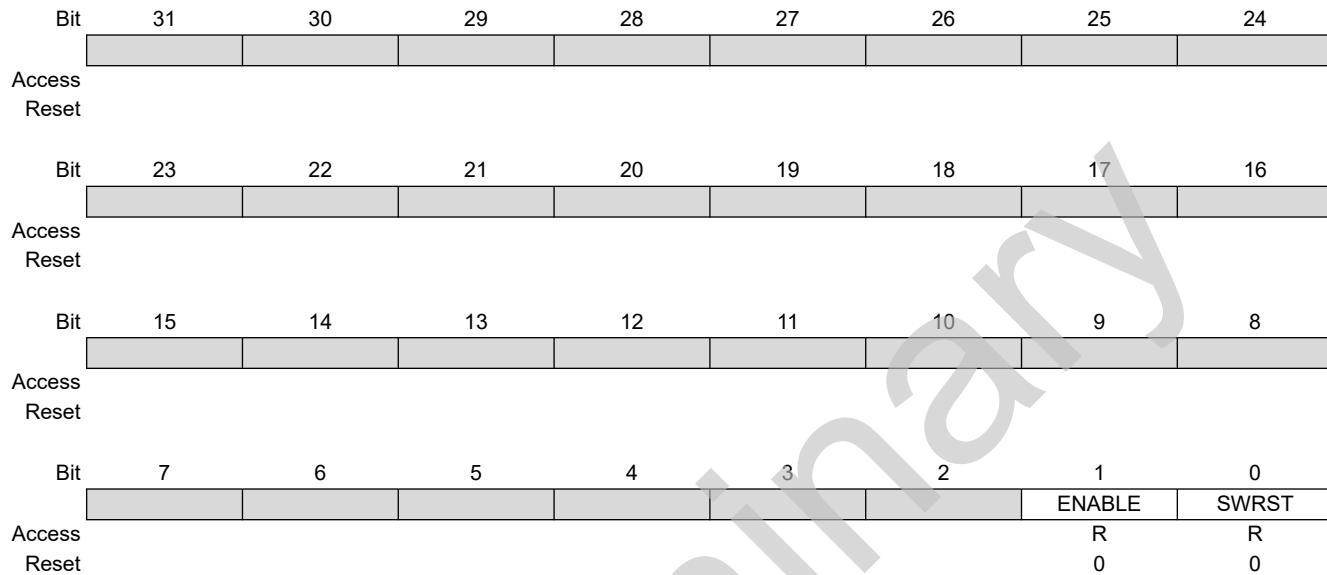
Writing a '1' to this bit will clear the OVF status.

Bit 0 – BUSY FREQM Status

Value	Description
0	No ongoing frequency measurement.
1	Frequency measurement is ongoing.

26.8.8 Synchronization Busy

Name: SYNCBUSY
Offset: 0x0C
Reset: 0x00000000
Property: –



Bit 1 – ENABLE Enable

This bit is cleared when the synchronization of CTRLA.ENABLE is complete.
This bit is set when the synchronization of CTRLA.ENABLE is started.

Bit 0 – SWRST Synchronization Busy

This bit is cleared when the synchronization of CTRLA.SWRST is complete.
This bit is set when the synchronization of CTRLA.SWRST is started.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

26.8.9 Value

Name: VALUE
Offset: 0x10
Reset: 0x00000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	VALUE[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	VALUE[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	VALUE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – VALUE[23:0] Measurement Value
Result from measurement.

27. Event System (EVSYS)

27.1 Overview

The Event System (EVSYS) allows autonomous, low-latency and configurable communication between peripherals.

Several peripherals can be configured to generate and/or respond to signals known as events. The exact condition to generate an event, or the action taken upon receiving an event, is specific to each peripheral. Peripherals that respond to events are called event users. Peripherals that generate events are called event generators. A peripheral can have one or more event generators and can have one or more event users.

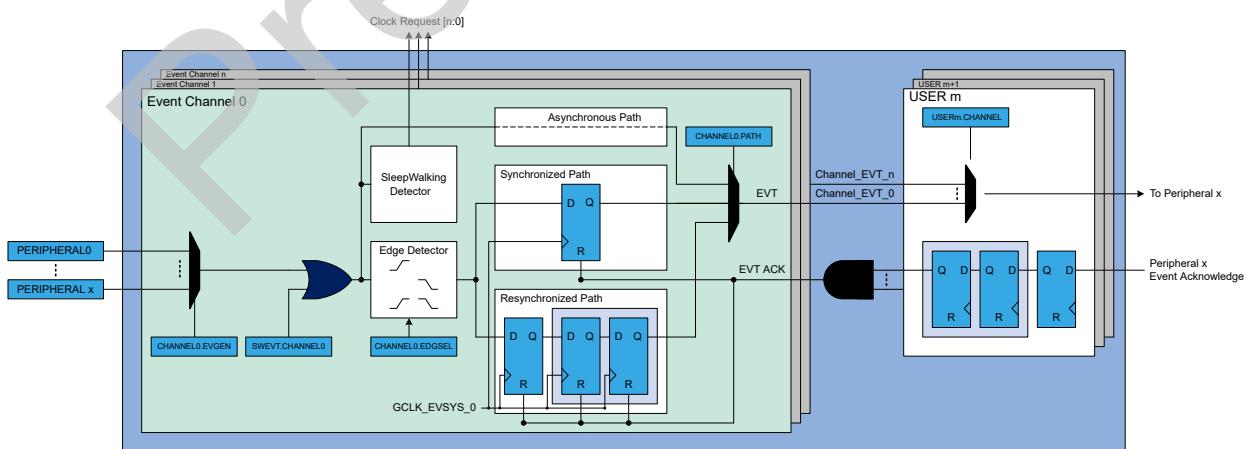
Communication is made without CPU intervention and without consuming system resources such as bus or RAM bandwidth. This reduces the load on the CPU and other system resources, compared to a traditional interrupt-based system.

27.2 Features

- 32 configurable event channels:
 - All channels can be connected to any event generator
 - All channels provide a pure asynchronous path
 - Twelve channels provide a resynchronized or synchronous path
- 69 event generators.
- 52 event users.
- Configurable edge detector.
- Peripherals can be event generators, event users, or both.
- SleepWalking and interrupt for operation in sleep modes.
- Software event generation.
- Each event user can choose which channel to respond to.
- Optional Static or Round-Robin interrupt priority arbitration.

27.3 Block Diagram

Figure 27-1. Event System Block Diagram



27.4 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

27.4.1 I/O Lines

Not applicable.

27.4.2 Power Management

The EVSYS can be used to wake up the CPU from all sleep modes (BACKUP and OFF Mode), even if the clock used by the EVSYS channel and the EVSYS bus clock are disabled. See *Power Management Unit (PMU)* from Related Links for details on the different sleep modes.

Although the clock for the EVSYS is stopped, the device still can wake up the EVSYS clock. Some event generators can generate an event when their clocks are stopped. The generic clock for the channel (GCLK_EVSYs_CHANNEL_n) will be restarted if that channel uses a synchronized path or a resynchronized path. It does not need to wake the system from sleep.

Related Links

[14. Power Management Unit \(PMU\)](#)

27.4.3 Clocks

Each EVSYS channel which can be configured as synchronous or resynchronized has a dedicated generic clock (GCLK_EVSYs_CHANNEL_n). These are used for event detection and propagation for each channel. These clocks must be configured and enabled in the generic clock controller before using the EVSYS, see *Clock and Reset (CRU)* from Related Links.



Important: Only EVSYS channel 0 to 11 can be configured as synchronous or resynchronized.

Related Links

[12. Clock and Reset Unit \(CRU\)](#)

27.4.4 DMA

Not applicable.

27.4.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the EVSYS interrupts requires the interrupt controller to be configured first, see *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

27.4.6 Events

Not applicable.

27.4.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging.

27.4.8 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Channel Pending Interrupt (INTPEND)
- Channel n Interrupt Flag Status and Clear (CHINTFLAGn)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

27.4.9 Analog Connections

Not applicable.

27.5 Functional Description

27.5.1 Principle of Operation

The Event System consists of channels which route the internal events from peripherals (generators) to other internal peripherals. Each event generator can be selected as source for multiple channels, but a channel cannot be set to use multiple event generators at the same time.

A channel path can be configured in asynchronous, synchronous or resynchronized mode of operation. The mode of operation must be selected based on the requirements of the application.

When using synchronous or resynchronized path, the Event System includes options to transfer events to users when rising, falling or both edges are detected on event generators.

See *Channel Path* from Related Links.

Related Links

[27.5.2.6. Channel Path](#)

27.5.2 Basic Operation

27.5.2.1 Initialization

Before enabling event routing within the system, the Event Users Multiplexer and Event Channels must be selected in the Event System (EVSYS), and the two peripherals that generate and use the event must be configured. Follow these steps to configure the event:

1. In the peripheral generating the event, enable output of event by writing a '1' to the respective Event Output Enable bit ("EO") in the peripheral's Event Control register, for example, AC.EVCTRL.WINEO0 or RTC.EVCTRL.OVFEO.
2. Configure the EVSYS:
 - a. Configure the Event User multiplexer by writing the respective EVSYS.USERm register, refer to [27.5.2.3. User Multiplexer Setup](#).
 - b. Configure the Event Channel by writing the respective EVSYS.CHANNELn register, refer to [27.5.2.4. Event System Channel](#).
3. Configure the action to be executed by the event user peripheral by writing to the Event Action bits (EVACTION) in the respective Event control register, for example, TC.EVCTRL.EVACT, PDEC.EVCTRL.EVACT.
Note: This step is not applicable for all the peripherals.
4. In the event user peripheral, enable event input by writing a '1' to the respective Event Input Enable bit ("EI") in the peripheral's Event Control register, for example, AC.EVCTRL.IVEI0, ADC.EVCTRL.STARTEI.

27.5.2.2 Enabling, Disabling, and Resetting

The EVSYS is always enabled.

The EVSYS is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the EVSYS will be reset to their initial state and all ongoing events will be canceled.

Refer to [CTRLA.SWRST](#) register for details.

27.5.2.3 User Multiplexer Setup

The user multiplexer defines the channel to be connected to which event user. Each user multiplexer is dedicated to one event user. A user multiplexer receives all event channels output and must be configured to select one of these channels, as shown in Block Diagram section. The channel is selected with the Channel bit group in the User register (USERm.CHANNEL).

The user multiplexer must always be configured before the channel. A list of all user multiplexers is found in the User (USERm) register description.

Related Links

[27.3. Block Diagram](#)

27.5.2.4 Event System Channel

An event channel can select one event from a list of event generators. Depending on configuration, the selected event could be synchronized, resynchronized or asynchronously sent to the users. When synchronization or resynchronization is required, the channel includes an internal edge detector, allowing the Event System to generate internal events when rising, falling or both edges are detected on the selected event generator.

An event channel is able to generate internal events for the specific software commands. A channel block diagram is shown in *Block Diagram* section.

Related Links

[27.3. Block Diagram](#)

27.5.2.5 Event Generators

Each event channel can receive the events from all event generators. All event generators are listed in the Event Generator bit field in the Channel n register (CHANNELn.EVGEN). For details on event generation, refer to the corresponding module chapter. The channel event generator is selected by the Event Generator bit group in the Channel register (CHANNELn.EVGEN). By default, the channels are not connected to any event generators (ie, CHANNELn.EVGEN = 0)

27.5.2.6 Channel Path

There are different ways to propagate the event from an event generator:

- Asynchronous path
- Synchronous path
- Resynchronized path

The path is decided by writing to the Path Selection bit group of the Channel register (CHANNELn.PATH).

Asynchronous Path

When using the asynchronous path, the events are propagated from the event generator to the event user without intervention from the Event System. The GCLK for this channel (GCLK_EVSYS_CHANNEL_n) is not mandatory, meaning that an event will be propagated to the user without any clock latency.

When the asynchronous path is selected, the channel cannot generate any interrupts, and the Channel x Status register (CHSTATUSx) is always zero. The edge detection is not required and must be disabled by software. Each peripheral event user has to select which event edge must trigger internal actions. For further details, refer to each peripheral chapter description.

Synchronous Path

The synchronous path should be used when the event generator and the event channel share the same generator for the generic clock. If they do not share the same clock, a logic change from the event generator to the event channel might not be detected in the channel, which means that the event will not be propagated to the event user.

When using the synchronous path, the channel is able to generate interrupts. The channel status bits in the Channel Status register (CHSTATUS) are also updated and available for use.

Resynchronized Path

The resynchronized path are used when the event generator and the event channel do not share the same generator for the generic clock. When the resynchronized path is used, resynchronization of the event from the event generator is done in the channel.

When the resynchronized path is used, the channel is able to generate interrupts. The channel status bits in the Channel Status register (CHSTATUS) are also updated and available for use.

27.5.2.7 Edge Detection

When synchronous or resynchronized paths are used, edge detection must be enabled. The event system can execute edge detection in three different ways:

- Generate an event only on the rising edge
- Generate an event only on the falling edge

- Generate an event on rising and falling edges.

Edge detection is selected by writing to the Edge Selection bit group of the Channel register (CHANNELn.EDGSEL).

27.5.2.8 Event Latency

The latency from event generator to event user depends on the channel's configuration:

- Asynchronous Path: The maximum routing latency of an external event is related to the internal signal routing and it is device dependent.
- Synchronous Path: The maximum routing latency of an external event is one GCLK_EVSYS_CHANNEL_n clock cycle.
- Resynchronized Path: The maximum routing latency of an external event is three GCLK_EVSYS_CHANNEL_n clock cycles.

The maximum propagation latency of a user event to the peripheral clock core domain is three peripheral clock cycles.

The event generators, event channel and event user clocks ratio must be selected in relation with the internal event latency constraints. Events propagation or event actions in peripherals may be lost if the clock setup violates the internal latencies.

27.5.2.9 The Overrun Channel n Interrupt

The Overrun Channel n Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAGn.OVR) will be set, and the optional interrupt will be generated in the following cases:

- One or more event users on channel n is not ready when there is a new event
- An event occurs when the previous event on channel m has not been handled by all event users connected to that channel

The flag will only be set when using synchronous or resynchronized paths. In the case of asynchronous path, the INTFLAGn.OVR is always read as zero.

27.5.2.10 The Event Detected Channel n Interrupt

The Event Detected Channel n Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAGn.EVD) is set when an event coming from the event generator configured on channel n is detected.

The flag will only be set when using a synchronous or resynchronized path. In the case of an asynchronous path, the INTFLAGn.EVD is always zero.

27.5.2.11 Channel Status

The Channel Status register (CHSTATUS) shows the status of the channels when using a synchronous or resynchronized path. There are two different status bits in CHSTATUS for each of the available channels:

- The CHSTATUSn.BUSYCH bit will be set when an event on the corresponding channel n has not been handled by all event users connected to that channel.
- The CHSTATUSn.RDYUSR bit will be set when all event users connected to the corresponding channel are ready to handle incoming events on that channel.

27.5.2.12 Software Event

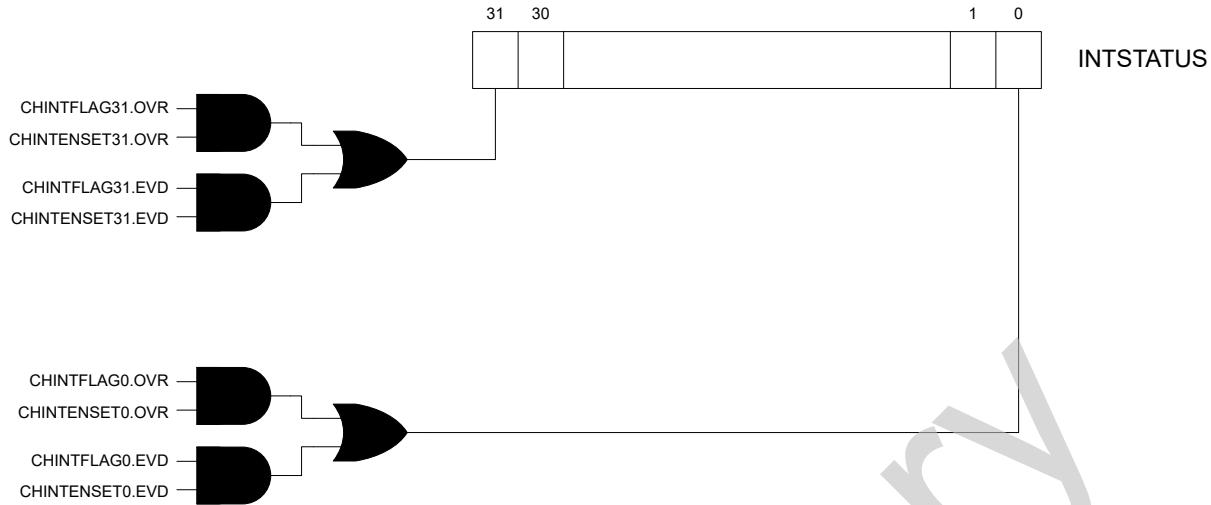
A software event can be initiated on a channel by writing a '1' to the Software Event bit in the Channel register (CHANNELm.SWEVT). Then the software event can be serviced as any event generator; i.e., when the bit is set to '1', an event will be generated on the respective channel.

27.5.2.13 Interrupt Status and Interrupts Arbitration

The Interrupt Status register stores all channels with pending interrupts, as shown below.

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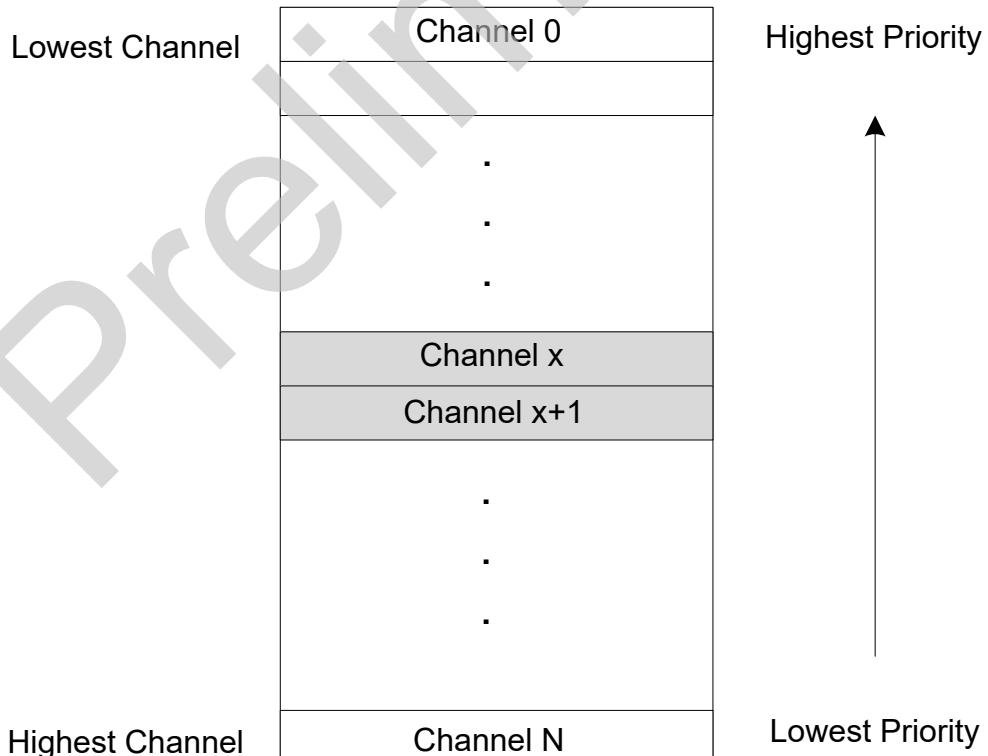
Figure 27-2. Interrupt Status Register



The Event System can arbitrate between all channels with pending interrupts. The arbiter can be configured to prioritize statically or dynamically the incoming events. The priority is evaluated each time a new channel has an interrupt pending, or an interrupt has been cleared. The Channel Pending Interrupt register (INTPEND) will provide the channel number with the highest interrupt priority, and the corresponding channel interrupt flags and status bits.

By default, static arbitration is enabled (PRICTRL.RREN_x is '0'), the arbiter will prioritize a low channel number over a high channel number as shown below. When using the status scheme, there is a risk of high channel numbers never being granted access by the arbiter. This can be avoided using a dynamic arbitration scheme.

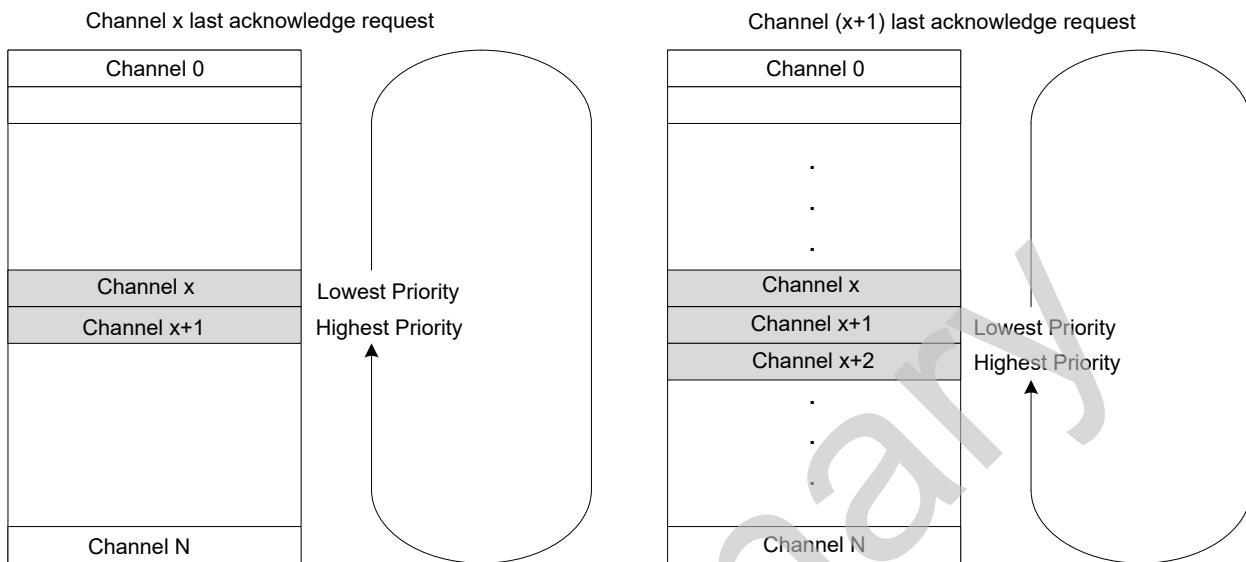
Figure 27-3. Static Priority



The dynamic arbitration scheme available in the Event System is round-robin. Round-robin arbitration is enabled by writing PRICTRL.RREN to one. With the round-robin scheme, the channel number of the last channel being granted

access will have the lowest priority the next time the arbiter has to grant access to a channel, as shown below. The channel number of the last channel being granted access, will be stored in the Channel Priority Number bit group in the Priority Control register (PRICTRL.PRI).

Figure 27-4. Round-Robin Scheduling



The Channel Pending Interrupt register (INTPEND) also offers the possibility to indirectly clear the interrupt flags of a specific channel. Writing a flag to one in this register, will clear the corresponding interrupt flag of the channel specified by the INTPEND.ID bits.

27.5.3 Interrupts

The EVSYS has the following interrupt sources for each channel:

- Overrun Channel n interrupt (OVR)
- Event Detected Channel n interrupt (EVD)

These interrupt events are asynchronous wake-up sources.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the corresponding Channel n Interrupt Flag Status and Clear (CHINTFLAG) register is set when the interrupt condition occurs.

Note: Interrupts must be globally enabled to allow the generation of interrupt requests.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Channel n Interrupt Enable Set (CHINTENSET) register, and disabled by writing a '1' to the corresponding bit in the Channel n Interrupt Enable Clear (CHINTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled or the Event System is reset. All interrupt requests are ORed together on system level to generate one combined interrupt request to the NVIC.

The user must read the Channel Interrupt Status (INTSTATUS) register to identify the channels with pending interrupts, and must read the Channel n Interrupt Flag Status and Clear (CHINTFLAG) register to determine which interrupt condition is present for the corresponding channel. It is also possible to read the Interrupt Pending register (INTPEND), which provides the highest priority channel with pending interrupt and the respective interrupt flags.

27.5.4 Sleep Mode Operation

The Event System can generate interrupts to wake up the device from IDLE or STANDBY sleep mode.

To be able to run in standby, the Run in Standby bit in the Channel register (CHANNELn.RUNSTDBY) must be set to '1'. When the Generic Clock On Demand bit in Channel register (CHANNELn.ONDEMAND) is set to '1' and the event generator is detected, the event channel will request its clock (GCLK_EVSYS_CHANNEL_n). The event latency for a resynchronized channel path will increase by two GCLK_EVSYS_CHANNEL_n clock (i.e., up to five GCLK_EVSYS_CHANNEL_n clock cycles).

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A channel will behave differently in different sleep modes regarding to CHANNELn.RUNSTDBY and CHANNELn.ONDEMAND:

Table 27-1. Event Channel Sleep Behavior

CHANNELn.PATH	CHANNELn. ONDEMAND	CHANNELn. RUNSTDBY	Sleep Behavior
ASYNC	0	0	Only run in IDLE sleep modes if an event must be propagated. Disabled in STANDBY sleep mode.
SYNC/RESYNC	0	1	Run in both IDLE and STANDBY sleep modes.
SYNC/RESYNC	1	0	Only run in IDLE sleep modes if an event must be propagated. Disabled in STANDBY sleep mode. Two GCLK_EVSYS_n latency added in RESYNC path before the event is propagated internally.
SYNC/RESYNC	1	1	Run in both IDLE and STANDBY sleep modes. Two GCLK_EVSYS_n latency added in RESYNC path before the event is propagated internally.

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

27.6 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0								SWRST
0x01 ...	Reserved									
0x03										
0x04	SWEVT	7:0 15:8 23:16 31:24	CHANNEL7 CHANNEL15 CHANNEL23 CHANNEL31	CHANNEL6 CHANNEL14 CHANNEL22 CHANNEL30	CHANNEL5 CHANNEL13 CHANNEL21 CHANNEL29	CHANNEL4 CHANNEL12 CHANNEL20 CHANNEL28	CHANNEL3 CHANNEL11 CHANNEL19 CHANNEL27	CHANNEL2 CHANNEL10 CHANNEL18 CHANNEL26	CHANNEL1 CHANNEL9 CHANNEL17 CHANNEL25	CHANNEL0 CHANNEL8 CHANNEL16 CHANNEL24
0x08	PRICTRL	7:0	RREN							PRI[4:0]
0x09 ...	Reserved									
0x0F										
0x10	INTPEND	7:0 15:8	BUSY	READY					ID[4:0]	
0x12 ...	Reserved								EVD	OVR
0x13										
0x14	INTSTATUS	7:0 15:8 23:16 31:24	CHINT7	CHINT6	CHINT5	CHINT4	CHINT3	CHINT2	CHINT1	CHINT0
0x18	BUSYCH	7:0 15:8 23:16 31:24	BUSYCH7	BUSYCH6	BUSYCH5	BUSYCH4	BUSYCH3	BUSYCH2	BUSYCH1	BUSYCH0
0x1C	READYUSR	7:0 15:8 23:16 31:24	READYUSR7	READYUSR6	READYUSR5	READYUSR4	READYUSR3	READYUSR2	READYUSR1	READYUSR0
0x20	CHANNEL0	7:0 15:8 23:16 31:24	ONDEMAND	RUNSTDBY				EDGSEL[1:0]	PATH[1:0]	
0x24	CHINTENCLR0	7:0							EVD	OVR
0x25	CHINTENSET0	7:0							EVD	OVR
0x26	CHINTFLAG0	7:0							EVD	OVR
0x27	CHSTATUSn0	7:0							BUSYCH	RDYUSR
0x28	CHANNEL1	7:0 15:8 23:16 31:24	ONDEMAND	RUNSTDBY				EDGSEL[1:0]	PATH[1:0]	
0x2C	CHINTENCLR1	7:0							EVD	OVR
0x2D	CHINTENSET1	7:0							EVD	OVR
0x2E	CHINTFLAG1	7:0							EVD	OVR
0x2F	CHSTATUSn1	7:0							BUSYCH	RDYUSR
0x30	CHANNEL2	7:0 15:8 23:16 31:24	ONDEMAND	RUNSTDBY				EDGSEL[1:0]	PATH[1:0]	
0x34	CHINTENCLR2	7:0							EVD	OVR
0x35	CHINTENSET2	7:0							EVD	OVR
0x36	CHINTFLAG2	7:0							EVD	OVR
0x37	CHSTATUSn2	7:0							BUSYCH	RDYUSR

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x38	CHANNEL3	7:0								
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x3C	CHINTENCLR3	7:0							EVD	OVR
0x3D	CHINTENSET3	7:0							EVD	OVR
0x3E	CHINTFLAG3	7:0							EVD	OVR
0x3F	CHSTATUSn3	7:0							BUSYCH	RDYUSR
0x40	CHANNEL4	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x44	CHINTENCLR4	7:0							EVD	OVR
0x45	CHINTENSET4	7:0							EVD	OVR
0x46	CHINTFLAG4	7:0							EVD	OVR
0x47	CHSTATUSn4	7:0							BUSYCH	RDYUSR
0x48	CHANNEL5	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x4C	CHINTENCLR5	7:0							EVD	OVR
0x4D	CHINTENSET5	7:0							EVD	OVR
0x4E	CHINTFLAG5	7:0							EVD	OVR
0x4F	CHSTATUSn5	7:0							BUSYCH	RDYUSR
0x50	CHANNEL6	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x54	CHINTENCLR6	7:0							EVD	OVR
0x55	CHINTENSET6	7:0							EVD	OVR
0x56	CHINTFLAG6	7:0							EVD	OVR
0x57	CHSTATUSn6	7:0							BUSYCH	RDYUSR
0x58	CHANNEL7	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x5C	CHINTENCLR7	7:0							EVD	OVR
0x5D	CHINTENSET7	7:0							EVD	OVR
0x5E	CHINTFLAG7	7:0							EVD	OVR
0x5F	CHSTATUSn7	7:0							BUSYCH	RDYUSR
0x60	CHANNEL8	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x64	CHINTENCLR8	7:0							EVD	OVR
0x65	CHINTENSET8	7:0							EVD	OVR
0x66	CHINTFLAG8	7:0							EVD	OVR
0x67	CHSTATUSn8	7:0							BUSYCH	RDYUSR
0x68	CHANNEL9	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x6C	CHINTENCLR9	7:0							EVD	OVR
0x6D	CHINTENSET9	7:0							EVD	OVR
0x6E	CHINTFLAG9	7:0							EVD	OVR
0x6F	CHSTATUSn9	7:0							BUSYCH	RDYUSR

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x70	CHANNEL10	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x74	CHINTENCLR10	7:0							EVD	OVR
0x75	CHINTENSET10	7:0							EVD	OVR
0x76	CHINTFLAG10	7:0							EVD	OVR
0x77	CHSTATUSn10	7:0							BUSYCH	RDYUSR
0x78	CHANNEL11	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x7C	CHINTENCLR11	7:0							EVD	OVR
0x7D	CHINTENSET11	7:0							EVD	OVR
0x7E	CHINTFLAG11	7:0							EVD	OVR
0x7F	CHSTATUSn11	7:0							BUSYCH	RDYUSR
0x80	CHANNEL12	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x84	Reserved									
0x87										
0x88	CHANNEL13	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x8C	Reserved									
0x8F										
0x90	CHANNEL14	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x94	Reserved									
0x97										
0x98	CHANNEL15	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x9C	Reserved									
0x9F										
0xA0	CHANNEL16	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xA4	Reserved									
0xA7										
0xA8	CHANNEL17	7:0						EVGEN[7:0]		
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xAC	Reserved									
0xAF										

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xB0	CHANNEL18	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xB4 ...	Reserved									
0xB8	CHANNEL19	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xBC ...	Reserved									
0xC0	CHANNEL20	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xC4 ...	Reserved									
0xC8	CHANNEL21	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xCC ...	Reserved									
0xD0	CHANNEL22	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xD4 ...	Reserved									
0xD8	CHANNEL23	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xDC ...	Reserved									
0xE0	CHANNEL24	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xE4 ...	Reserved									
0xE8	CHANNEL25	7:0					EVGEN[7:0]			
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xEC ...	Reserved									

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xF0	CHANNEL26	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xF4 ...	Reserved									
0xF8	CHANNEL27	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0xFC ...	Reserved									
0x0100	CHANNEL28	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x0104 ...	Reserved									
0x0108	CHANNEL29	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x010C ...	Reserved									
0x0110	CHANNEL30	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x0114 ...	Reserved									
0x0118	CHANNEL31	7:0								EVGEN[7:0]
		15:8	ONDEMAND	RUNSTDBY				EDGSEL[1:0]		PATH[1:0]
		23:16								
		31:24								
0x011C ...	Reserved									
0x0120	USER0	7:0								CHANNEL[7:0]
...										
0x0153	USER51	7:0								CHANNEL[7:0]

27.7 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

For more details, see *Register Access Protection* and *Peripheral Access Controller (PAC)* from Related Links.

PIC32CX-BZ2 and WBZ45 Family Event System (EVSYS)

Related Links

- [27.4.8. Register Access Protection](#)
- [25. Peripheral Access Controller \(PAC\)](#)

Preliminary

27.7.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	SWRST
Access									W
Reset									0

Bit 0 – SWRST Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the EVSYS to their initial state.

Note: Before applying a Software Reset it is recommended to disable the event generators.

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27.7.2 Software Event

Name: SWEVT
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	CHANNEL31	CHANNEL30	CHANNEL29	CHANNEL28	CHANNEL27	CHANNEL26	CHANNEL25	CHANNEL24
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CHANNEL23	CHANNEL22	CHANNEL21	CHANNEL20	CHANNEL19	CHANNEL18	CHANNEL17	CHANNEL16
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CHANNEL15	CHANNEL14	CHANNEL13	CHANNEL12	CHANNEL11	CHANNEL10	CHANNEL9	CHANNEL8
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CHANNEL7	CHANNEL6	CHANNEL5	CHANNEL4	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 –
CHANNELx Channel x Software Selection [x=0..7]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will trigger a software event for channel x.

These bits always return '0' when read.

27.7.3 Priority Control

Name: PRICTRL
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	RREN	PRI[4:0]						
Access	RW			RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0

Bit 7 – RREN Round-Robin Scheduling Enable

For details on scheduling schemes, refer to [Interrupt Status and Interrupts Arbitration](#)

Value	Description
0	Static scheduling scheme for channels with level priority
1	Round-robin scheduling scheme for channels with level priority

Bits 4:0 – PRI[4:0] Channel Priority Number

When round-robin arbitration is enabled (PRICTRL.RREN=1) for priority level, this register holds the channel number of the last EVSYS channel being granted access as the active channel with priority level. The value of this bit group is updated each time the INTPEND or any of CHINTFLAG registers are written.

When static arbitration is enabled (PRICTRL.RREN=0) for priority level, and the value of this bit group is nonzero, it will not affect the static priority scheme.

This bit group is not reset when round-robin scheduling gets disabled (PRICTRL.RREN written to zero).

27.7.4 Channel Pending Interrupt

Name: INTPEND
Offset: 0x10
Reset: 0x4000

An interrupt that handles several channels should consult the INTPEND register to find out which channel number has priority (ignoring/filtering each channel that has its own interrupt line). An interrupt dedicated to only one channel must not use the INTPEND register.

Bit	15	14	13	12	11	10	9	8
	BUSY	READY					EVD	OVR
Access	R	R					RW	RW
Reset	0	1					0	0
Bit	7	6	5	4	3	2	1	0
						ID[4:0]		
Access				RW	RW	RW	RW	RW
Reset				0	0	0	0	0

Bit 15 – BUSY Busy

This bit is read '1' when the event on a channel selected by Channel ID field (ID) has not been handled by all the event users connected to this channel.

Bit 14 – READY Ready

This bit is read '1' when all event users connected to the channel selected by Channel ID field (ID) are ready to handle incoming events on this channel.

Bit 9 – EVD Channel Event Detected

This flag is set on the next CLK_EVSYS_APB cycle when an event is being propagated through the channel, and an interrupt request will be generated if CHINTENCLR/SET.EVD is '1'.

When the event channel path is asynchronous, the EVD bit will not be set.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn) of this peripheral, where n is determined by the Channel ID bit field (ID) in this register.

Bit 8 – OVR Channel Overrun

This flag is set on the next CLK_EVSYS cycle after an overrun channel condition occurs, and an interrupt request will be generated if CHINTENCLR/SET.OVRx is '1'.

There are two possible overrun channel conditions:

- One or more of the event users on channel selected by Channel ID field (ID) are not ready when a new event occurs.
- An event happens when the previous event on channel selected by Channel ID field (ID) has not yet been handled by all event users

When the event channel path is asynchronous, the OVR interrupt flag will not be set.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn) of this peripheral, where n is determined by the Channel ID bit field (ID) in this register.

Bits 4:0 – ID[4:0] Channel ID

These bits store the channel number of the highest priority.

When the bits are written, indirect access to the corresponding Channel Interrupt Flag register is enabled.

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27.7.5 Interrupt Status

Name: INTSTATUS
Offset: 0x14
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					CHINT11	CHINT10	CHINT9	CHINT8
Reset					R 0	R 0	R 0	R 0
Bit	7	6	5	4	3	2	1	0
Access	CHINT7 R	CHINT6 R	CHINT5 R	CHINT4 R	CHINT3 R	CHINT2 R	CHINT1 R	CHINT0 R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – CHINT_x Channel x Pending Interrupt

This bit is set when Channel x has a pending interrupt.

This bit is cleared when the corresponding Channel x interrupts are disabled, or the source interrupt sources are cleared.

27.7.6 Busy Channels

Name: BUSYCH
Offset: 0x18
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access				BUSYCH11	BUSYCH10	BUSYCH9	BUSYCH8	
Reset				R 0	R 0	R 0	R 0	
Bit	7	6	5	4	3	2	1	0
Access	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – BUSYCH_x Busy Channel x

This bit is set if an event occurs on channel x has not been handled by all event users connected to channel x.

This bit is cleared when channel x is idle.

When the event channel x path is asynchronous, this bit is always read '0'.

27.7.7 Ready Users

Name: READYUSR
Offset: 0x1C
Reset: 111111111111

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					READYUSR11	READYUSR10	READYUSR9	READYUSR8
Reset					R 1	R 1	R 1	R 1
Bit	7	6	5	4	3	2	1	0
Access	R 1	R 1	R 1	R 1	R 1	R 1	R 1	R 1
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – READYUSRn Ready User for Channel n

This bit is set when all event users connected to channel n are ready to handle incoming events on channel n.

This bit is cleared when at least one of the event users connected to the channel is not ready.

When the event channel n path is asynchronous, this bit is always read zero.

27.7.8 Channel n Control

Name: CHANNEL
Offset: 0x20 + n*0x08 [n=0..31]
Reset: 0x00008000
Property: PAC Write-Protection

This register allows the user to configure channel n. To write to this register, do a single, 32-bit write of all the configuration data.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
ONDEMAND	RUNSTDBY			EDGSEL[1:0]		PATH[1:0]		
Access	RW	RW		RW	RW	RW	RW	RW
Reset	1	0		0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				EVGEN[7:0]				
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit 15 – ONDEMAND Generic Clock On Demand

Value	Description
0	Generic clock for a channel is always on, if the channel is configured and generic clock source is enabled.
1	Generic clock is requested on demand while an event is handled

Bit 14 – RUNSTDBY Run in Standby

This bit is used to define the behavior during standby sleep mode.

Value	Description
0	The channel is disabled in standby sleep mode.
1	The channel is not stopped in standby sleep mode and depends on the CHANNEL.ONDEMAND bit.

Bits 11:10 – EDGSEL[1:0] Edge Detection Selection

These bits set the type of edge detection to be used on the channel.

These bits must be written to zero when using the asynchronous path.

Value	Name	Description
0x0	NO_EVT_OUTPUT	No event output when using the resynchronized or synchronous path
0x1	RISING_EDGE	Event detection only on the rising edge of the signal from the event generator
0x2	FALLING_EDGE	Event detection only on the falling edge of the signal from the event generator
0x3	BOTH_EDGES	Event detection on rising and falling edges of the signal from the event generator

Bits 9:8 – PATH[1:0] Path Selection

These bits are used to choose which path will be used by the selected channel.

Note: The path choice can be limited by the channel source, see *USERm* from Related Links.



Important: Only EVSYS channel 0 to 3 can be configured as synchronous or resynchronized.

Value	Name	Description
0x0	SYNCHRONOUS	Synchronous path
0x1	RESYNCHRONIZED	Resynchronized path
0x2	ASYNCHRONOUS	Asynchronous path
Other	-	Reserved

Bits 7:0 – EVGEN[7:0] Event Generator Selection

These bits are used to choose the event generator to connect to the selected channel.

Table 27-2. Event Generator Selection

Value	Name	Description
0x00 - 0x07	RTC_PERx	RTC period x=0..7
0x08 - 0x0B	RTC_CMPx	RTC comparison x=0..3
0x0C	RTC_TAMPER	RTC tamper detection
0x0D	RTC_OVF	RTC Overflow
0x0E - 0x11	EIC_EXTINTx	EIC external interrupt x=0..3
0x12 - 0x15	DMAC_CHx	DMA channel x=0..3
0x16	PAC_ACCERR	PAC Acc. error
0x17	TCC0_OVF	TCC0 Overflow
0x18	TCC0_TRG	TCC0 Trigger Event
0x19	TCC0_CNT	TCC0 Counter
0x1A-0x1F	TCC0_MCx	TCC0 Match/Compare x=0..5
0x20	TCC1_OVF	TCC1 Overflow
0x21	TCC1_TRG	TCC1 Trigger Event
0x22	TCC1_CNT	TCC1 Counter
0x23 - 0x28	TCC1_MCx	TCC1 Match/Compare x=0..5
0x29	TCC2_OVF	TCC2 Overflow
0x2A	TCC2_TRG	TCC2 Trigger Event
0x2B	TCC2_CNT	TCC2 Counter
0x2C - 0x2D	TCC2_MCx	TCC2 Match/Compare x=0..1
0x2E	TC0_OVF	TC0 Overflow
0x2F-0x30	TC0_MCx	TC0 Match/Compare x=0..1
0x31	TC1_OVF	TC1 Overflow
0x32 - 0x33	TC1_MCx	TC1 Match/Compare x=0..1
0x34	TC2_OVF	TC2 Overflow
0x35 - 0x36	TC2_MCx	TC2 Match/Compare x=0..1
0x37	TC3_OVF	TC3 Overflow
0x38 - 0x39	TC3_MCx	TC3 Match/Compare x=0..1
0x3A	ADC_RESRDY	ADC End-Of-Scan Ready Interrupt
0x3B - 0x3C	Not used	
0x3D - 0x3E	AC_COMPx	AC Comparator, x=0..1
0x3F	AC_WIN_0	AC0 Window
0x40	TRNG_READY	TRNG ready
0x41 - 0x42	CCL_LUTOUTx	CCL LUTOUT x=0..1
0x43	ZB_TX_TS_ACTIVE	ZB Transmit Packet Active time
0x44	ZB_RX_TS_ACTIVE	ZB Receive Packet Active time

Related Links

[27.7.13. USERm](#)

27.7.9 Channel n Interrupt Enable Clear

Name: CHINTENCLR
Offset: 0x24 + n*0x08 [n=0..11]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access							EVD	OVR
Reset							RW	RW

Bit 1 – EVD Channel Event Detected Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Event Detected Channel Interrupt Enable bit, which disables the Event Detected Channel interrupt.

Value	Description
0	The Event Detected Channel interrupt is disabled.
1	The Event Detected Channel interrupt is enabled.

Bit 0 – OVR Channel Overrun Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overrun Channel Interrupt Enable bit, which disables the Overrun Channel interrupt.

Value	Description
0	The Overrun Channel interrupt is disabled.
1	The Overrun Channel interrupt is enabled.

27.7.10 Channel n Interrupt Enable Set

Name: CHINTENSET
Offset: 0x25 + n*0x08 [n=0..11]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access							EVD	OVR
Reset							RW	RW
							0	0

Bit 1 – EVD Channel Event Detected Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Event Detected Channel Interrupt Enable bit, which enables the Event Detected Channel interrupt.

Value	Description
0	The Event Detected Channel interrupt is disabled.
1	The Event Detected Channel interrupt is enabled.

Bit 0 – OVR Channel Overrun Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overrun Channel Interrupt Enable bit, which enables the Overrun Channel interrupt.

Value	Description
0	The Overrun Channel interrupt is disabled.
1	The Overrun Channel interrupt is enabled.

27.7.11 Channel n Interrupt Flag Status and Clear

Name: CHINTFLAG
Offset: 0x26 + n*0x08 [n=0..11]
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
Access							EVD	OVR
Reset							RW	RW

Bit 1 – EVD Channel Event Detected

This flag is set on the next CLK_EVSYS_APB cycle when an event is being propagated through the channel, and an interrupt request will be generated if CHINTENCLR/SET.EVD is '1'.

When the event channel path is asynchronous, the EVD interrupt flag will not be set.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Event Detected Channel interrupt flag.

Bit 0 – OVR Channel Overrun

This flag is set on the next CLK_EVSYS cycle after an overrun channel condition occurs, and an interrupt request will be generated if CHINTENCLR/SET.OVRx is '1'.

There are two possible overrun channel conditions:

- One or more of the event users on the channel are not ready when a new event occurs.
- An event happens when the previous event on channel has not yet been handled by all event users.

When the event channel path is asynchronous, the OVR interrupt flag will not be set.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overrun Channel interrupt flag.

27.7.12 Channel n Status

Name: CHSTATUSn
Offset: 0x27 + n*0x08 [n=0..11]
Reset: 0x01

Bit	7	6	5	4	3	2	1	0
Access							BUSYCH	RDYUSR
Reset							R	R

Bit 1 – BUSYCH Busy Channel

This bit is cleared when channel is idle.

This bit is set if an event on channel has not been handled by all event users connected to channel.

When the event channel path is asynchronous, this bit is always read '0'.

Bit 0 – RDYUSR Ready User

This bit is cleared when at least one of the event users connected to the channel is not ready.

This bit is set when all event users connected to channel are ready to handle incoming events on the channel.

When the event channel path is asynchronous, this bit is always read zero.

27.7.13 Event User m

Name: USERm
Offset: 0x0120 + m*0x01 [m=0..51]
Reset: 0x0
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
CHANNEL[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CHANNEL[7:0] Channel Event Selection

These bits select channel n to connect to the event user m.

Note: A value x of this bit field selects channel n = x-1.

Table 27-3. User Multiplexer Number m

USERm	User Multiplexer	Description	Path Type ⁽¹⁾
m = 0	RTC_TAMPER	RTC Tamper	A, S, R
m = 1..8	DMAC_CH0..7	Channel 0..7	S, R
m = 9	CM4_TRACE_START	CM4 trace start	A, S, R
m = 10	CM4_TRACE_STOP	CM4 trace stop	A, S, R
m = 11	CM4_TRACE_TRIG	CM4 trace trigger	A, S, R
m = 12..13	TCC0_EV0..1	TCC0 EVx	A, S, R
m = 14..19	TCC0_MC0..5	TCC0 MCx	A, S, R
m = 20..21	TCC1_EV0..1	TCC1 EVx	A, S, R
m = 22..27	TCC1_MC0..5	TCC1 MCx	A, S, R
m = 28..29	TCC2_EV0..1	TCC2 EVx	A, S, R
m = 30..31	TCC2_MC0..1	TCC2 MCx	A, S, R
m = 32	TC0_EVU	TC0 EVU	A, S, R
m = 33	TC1_EVU	TC1 EVU	A, S, R
m = 34	TC2_EVU	TC2 EVU	A, S, R
m = 35	TC3_EVU	TC3 EVU	A, S, R
m = 36..47	ADC_TRIGGER5..16	ADC_TRIGGERx	A, S, R
m = 48..49	AC_SOC0..1	AC_SOCx	A, S, R
m = 50..51	CCL_LUTIN0..1	CCL_LUTINx	A, S, R

1) A = Asynchronous path, S = Synchronous path, R = Resynchronized path

28. SERCOM – Serial Communication Interface

28.1 Overview

There are four instances of the Serial Communication interface (SERCOM) peripheral.

A SERCOM can be configured to support a number of modes: I²C, SPI, and USART. When an instance of SERCOM is configured and enabled, all of the resources of that SERCOM instance will be dedicated to the selected mode.

The SERCOM serial engine consists of a transmitter and receiver, baud-rate generator and address matching functionality. It can use the internal generic clock or an external clock. Using an external clock allows the SERCOM to be operated in all Sleep modes.

28.2 Features

- Interface for Configuring into one of the Following:
 - Inter-Integrated Circuit (I²C) two-wire serial interface
 - System Management Bus (SMBus™) compatible
 - Serial Peripheral Interface (SPI)
 - Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
- Single Transmit Buffer and Double Receive Buffer
- Baud-rate Generator
- Address Match/mask Logic
- Operational in all Sleep modes with an External Clock Source
- Can be used with DMA
- 32-bit Extension for Better System Bus Utilization

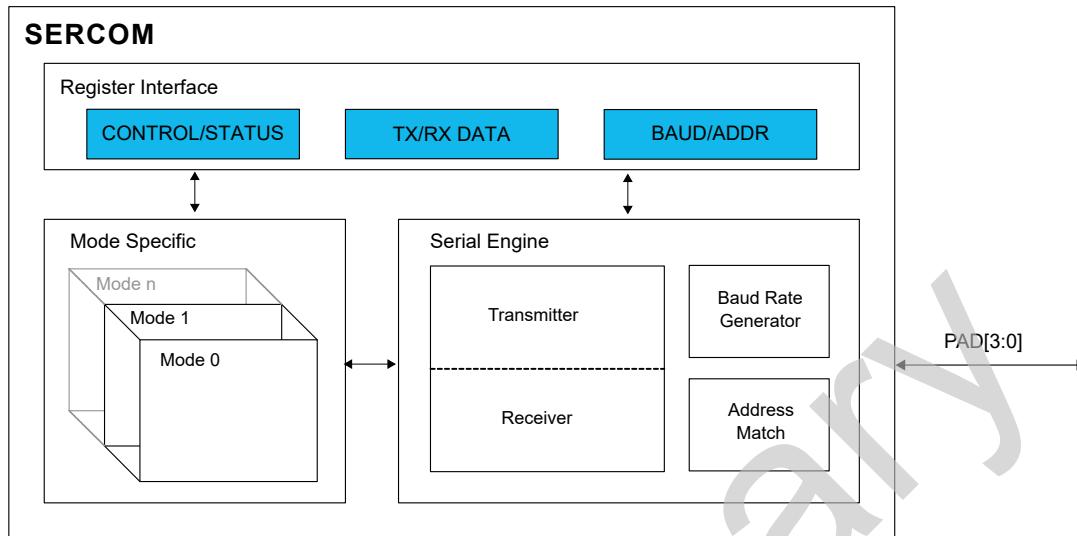
See the Related Links for full feature lists of the interface configurations.

Related Links

- [29. SERCOM USART - SERCOM Synchronous and Asynchronous Receiver and Transmitter](#)
- [30. SERCOM SPI – SERCOM Serial Peripheral Interface](#)
- [31. SERCOM I²C – Inter-Integrated Circuit](#)

28.3 Block Diagram

Figure 28-1. SERCOM Block Diagram



28.4 Signal Description

See the respective SERCOM mode chapters for details.

Related Links

- [29. SERCOM USART - SERCOM Synchronous and Asynchronous Receiver and Transmitter](#)
- [30. SERCOM SPI – SERCOM Serial Peripheral Interface](#)
- [31. SERCOM I2C – Inter-Integrated Circuit](#)

28.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

28.5.1 I/O Lines

Using the SERCOM I/O lines requires the I/O pins to be configured using the System Configuration registers or PPS registers.

The SERCOM has four internal pads, PAD[3:0], and the signals from I²C, SPI and USART are routed through these SERCOM pads through a multiplexer. The configuration of the multiplexer is available from the different SERCOM modes. Refer to the mode specific chapters for additional information.

28.5.2 Power Management

The SERCOM can operate in any Sleep mode provided the selected clock source is running. SERCOM interrupts can be configured to wake the device from sleep modes.

28.5.3 Clocks

The SERCOM uses two generic clocks: GCLK_SERCOMx_CORE and GCLK_SERCOMx_SLOW/GCLK_SERCOMx_SLOW. The core clock (GCLK_SERCOMx_CORE) is required to clock the SERCOM while working as a master. The slow clock (GCLK_SERCOMx_SLOW) is only required for certain functions. See specific mode chapters for details.

These clocks must be configured and enabled in the Clock and Reset Unit (CRU) registers before using the SERCOM.

The generic clocks are asynchronous to the bus clock (PBx_CLK). Therefore, writing to certain registers will require synchronization between the clock domains.

28.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). The DMAC must be configured before the SERCOM DMA requests are used.

28.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller (NVIC). The NVIC must be configured before the SERCOM interrupts are used.

28.5.6 Events

Not applicable.

28.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

28.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC).

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

PAC write protection does not apply to accesses through an external debugger.

28.5.9 Analog Connections

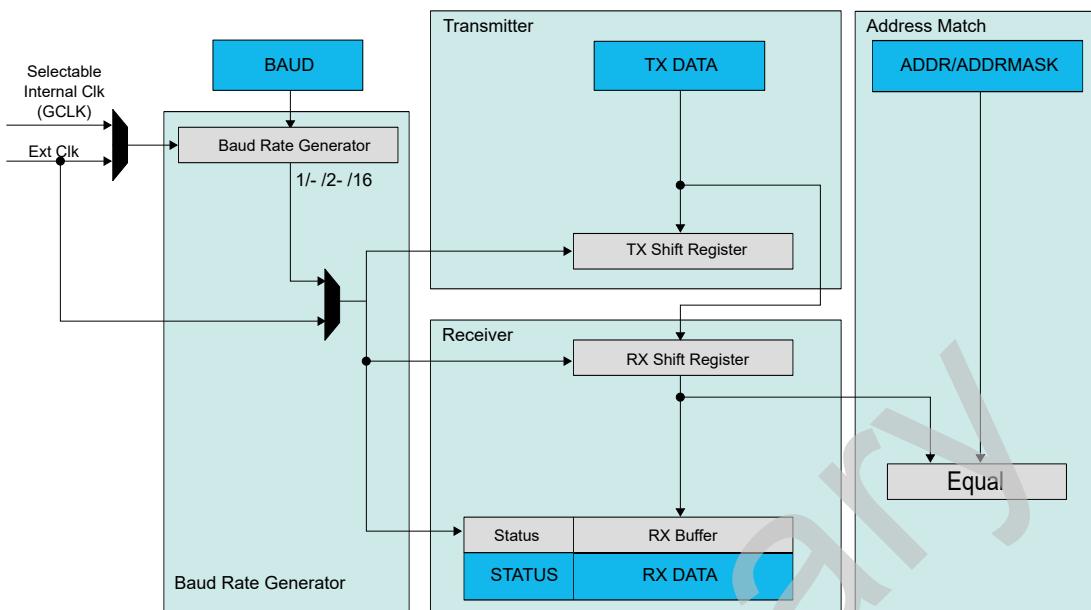
Not applicable.

28.6 Functional Description

28.6.1 Principle of Operation

The basic structure of the SERCOM serial engine is shown in [Figure 28-2](#). Labels in capital letters are synchronous to the system clock and accessible by the CPU; labels in lowercase letters can be configured to run on the GCLK_SERCOMx_CORE clock or an external clock.

Figure 28-2. SERCOM Serial Engine



The transmitter consists of a single write buffer and a Shift register.

The receiver consists of a one-level (I²C), two-level (USART, SPI) receive buffer and a Shift register.

The baud-rate generator is capable of running on the GCLK_SERCOMx_CORE clock or an external clock.

Address matching logic is included for SPI and I²C operation.

28.6.2 Basic Operation

28.6.2.1 Initialization

The SERCOM must be configured to the desired mode by writing the Operating Mode bits in the Control A register (CTRLA.MODE) as shown in the table below.

Table 28-1. SERCOM Modes

CTRLA.MODE	Description
0x0	USART with external clock
0x1	USART with internal clock
0x2	SPI in client operation
0x3	SPI in host operation
0x4	I ² C client operation
0x5	I ² C host operation
0x6-0x7	Reserved

For further initialization information, see the respective SERCOM mode chapters:

Related Links

- [29. SERCOM USART - SERCOM Synchronous and Asynchronous Receiver and Transmitter](#)
- [30. SERCOM SPI – SERCOM Serial Peripheral Interface](#)
- [31. SERCOM I2C – Inter-Integrated Circuit](#)

28.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

Refer to the CTRLA register description for details.

28.6.2.3 Clock Generation – Baud-Rate Generator

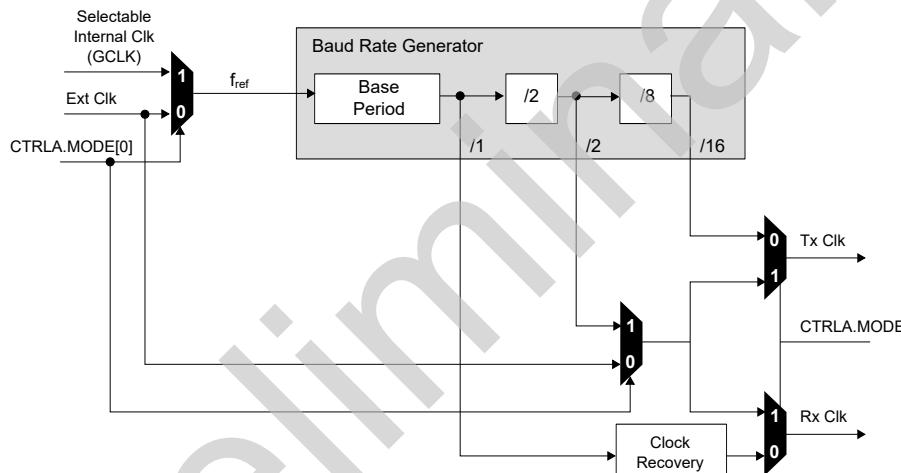
The baud-rate generator, as shown in the following figure, generates internal clocks for asynchronous and synchronous communication. The output frequency (f_{BAUD}) is determined by the Baud register (BAUD) setting and the baud reference frequency (f_{ref}). The baud reference clock is the serial engine clock, and it can be internal or external.

For asynchronous communication, the /16 (divide-by-16) output is used when transmitting, whereas the /1 (divide-by-1) output is used while receiving.

For synchronous communication, the /2 (divide-by-2) output is used.

This functionality is automatically configured, depending on the selected operating mode.

Figure 28-3. Baud Rate Generator



The following table contains equations for the baud rate (in bits per second) and the BAUD register value for each operating mode.

For asynchronous operation, there are two modes:

- *Arithmetic mode*: the BAUD register value is 16 bits (0 to 65,535)
- *Fractional mode*: the BAUD register value is 13 bits, while the fractional adjustment is 3 bits. In this mode the BAUD setting must be greater than or equal to 1.

Fractional mode, the BAUD register value is 13 bits, while the fractional adjustment is 3 bits. In this mode the BAUD setting must be greater than or equal to 1.

For synchronous operation, the BAUD register value is 8 bits (0 to 255).

Table 28-2. Baud Rate Equations

Operating Mode	Condition	Baud Rate (Bits Per Second)	BAUD Register Value Calculation
Asynchronous Arithmetic	$f_{BAUD} \leq \frac{f_{ref}}{16}$	$f_{BAUD} = \frac{f_{ref}}{16} \left(1 - \frac{BAUD}{65536}\right)$	$BAUD = 65536 \cdot \left(1 - S \cdot \frac{f_{BAUD}}{f_{ref}}\right)$
Asynchronous Fractional	$f_{BAUD} \leq \frac{f_{ref}}{S}$	$f_{BAUD} = \frac{f_{ref}}{S \cdot \left(BAUD + \frac{FP}{8}\right)}$	$BAUD = \frac{f_{ref}}{S \cdot f_{BAUD}} - \frac{FP}{8}$

.....continued

Operating Mode	Condition	Baud Rate (Bits Per Second)	BAUD Register Value Calculation
Synchronous	$f_{BAUD} \leq \frac{f_{ref}}{2}$	$f_{BAUD} = \frac{f_{ref}}{2 \cdot (BAUD + 1)}$	$BAUD = \frac{f_{ref}}{2 \cdot f_{BAUD}} - 1$

S - Number of samples per bit, which can be 16, 8, or 3.

The Asynchronous Fractional option is used for auto-baud detection.

The baud rate error is represented by the following formula:

$$\text{Error} = 1 - \left(\frac{\text{ExpectedBaudRate}}{\text{ActualBaudRate}} \right)$$

28.6.3 Additional Features

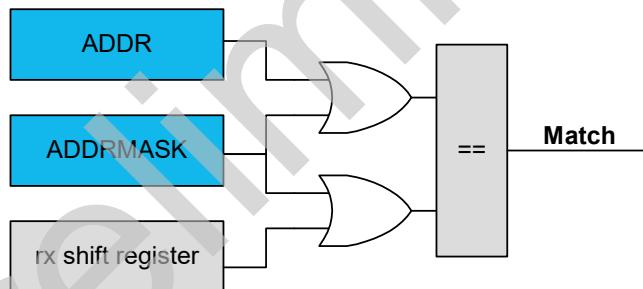
28.6.3.1 Address Match and Mask

The SERCOM address match and mask feature is capable of matching either one address, two unique addresses, or a range of addresses with a mask, based on the mode selected. The match uses seven or eight bits, depending on the mode.

Address With Mask

An address written to the Address bits in the Address register (ADDR.ADDR), and a mask written to the Address Mask bits in the Address register (ADDR.ADDRMASK) will yield an address match. All bits that are masked are not included in the match. Note that writing the ADDR.ADDRMASK to 'all zeros' will match a single unique address, while writing ADDR.ADDRMASK to 'all ones' will result in all addresses being accepted.

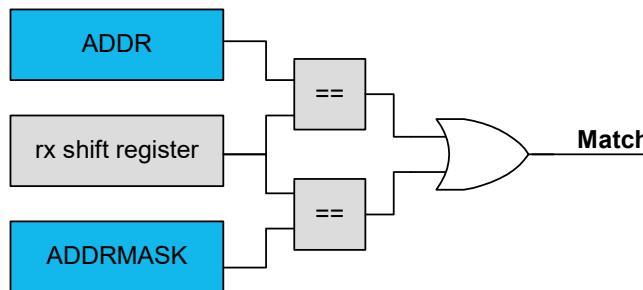
Figure 28-4. Address With Mask



Two Unique Addresses

The two addresses written to ADDR and ADDRMASK will cause a match.

Figure 28-5. Two Unique Addresses



Address Range

The range of addresses between and including ADDR.ADDR and ADDR.ADDRMASK will cause a match. ADDR.ADDR and ADDR.ADDRMASK can be set to any two addresses, with ADDR.ADDR acting as the upper limit and ADDR.ADDRMASK acting as the lower limit.

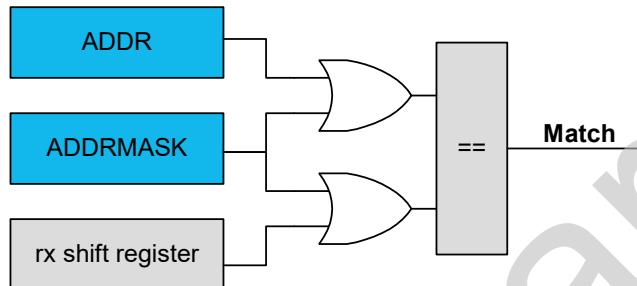
Figure 28-6. Address Range



28.6.3.1.1 Address With Mask

An address written to the Address bits in the Address register (ADDR.ADDR), and a mask written to the Address Mask bits in the Address register (ADDR.ADDRMASK) will yield an address match. All bits that are masked are not included in the match. Note that writing the ADDR.ADDRMASK to 'all zeros' will match a single unique address, while writing ADDR.ADDRMASK to 'all ones' will result in all addresses being accepted.

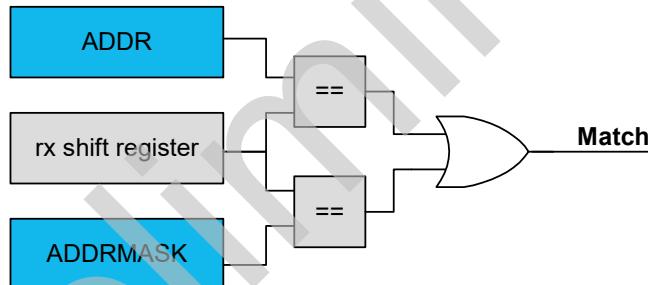
Figure 28-7. Address With Mask



28.6.3.1.2 Two Unique Addresses

The two addresses written to ADDR and ADDRMASK will cause a match.

Figure 28-8. Two Unique Addresses



28.6.3.1.3 Address Range

The range of addresses between and including ADDR.ADDR and ADDR.ADDRMASK will cause a match. ADDR.ADDR and ADDR.ADDRMASK can be set to any two addresses, with ADDR.ADDR acting as the upper limit and ADDR.ADDRMASK acting as the lower limit.

Figure 28-9. Address Range



28.6.4 DMA Operation

The available DMA interrupts and their depend on the operation mode of the SERCOM peripheral. Refer to the Functional Description sections of the respective SERCOM mode.

Related Links

- 29. SERCOM USART - SERCOM Synchronous and Asynchronous Receiver and Transmitter
- 30. SERCOM SPI – SERCOM Serial Peripheral Interface
- 31. SERCOM I2C – Inter-Integrated Circuit

28.6.5 Interrupts

Interrupt sources are mode specific. See the respective SERCOM mode chapters for details.

Each interrupt source has its own Interrupt flag.

The Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the Interrupt condition is met.

Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the Interrupt flag is cleared, the interrupt is disabled, or the SERCOM is reset. For details on clearing Interrupt flags, refer to the INTFLAG register description.

The value of INTFLAG indicates which Interrupt condition occurred. The user must read the INTFLAG register to determine which Interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests.

28.6.6 Events

Not applicable.

28.6.7 Sleep Mode Operation

The peripheral can operate in any Sleep mode where the selected serial clock is running. This clock can be external or generated by the internal baud-rate generator.

The SERCOM interrupts can be used to wake-up the device from Sleep modes. Refer to the different SERCOM mode chapters for details.

28.6.8 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

29. SERCOM USART - SERCOM Synchronous and Asynchronous Receiver and Transmitter

29.1 Overview

The Universal Synchronous and Asynchronous Receiver and Transmitter (USART) is one of the available modes in the Serial Communication Interface (SERCOM).

The USART uses the SERCOM transmitter and receiver, see *USART Block Diagram* in the *Block Diagram* section from Related Links. Labels in uppercase letters are synchronous to PB_x_CLK and accessible for CPU. Labels in lowercase letters can be programmed to run on the internal generic clock or an external clock.

The transmitter consists of a single write buffer, a Shift register, and control logic for different frame formats. The write buffer supports data transmission without any delay between frames. The receiver consists of a two-level receive buffer and a Shift register. Status information of the received data is available for error checking. Data and clock recovery units ensure robust synchronization and noise filtering during asynchronous data reception.

Related Links

[29.3. Block Diagram](#)

29.2 USART Features

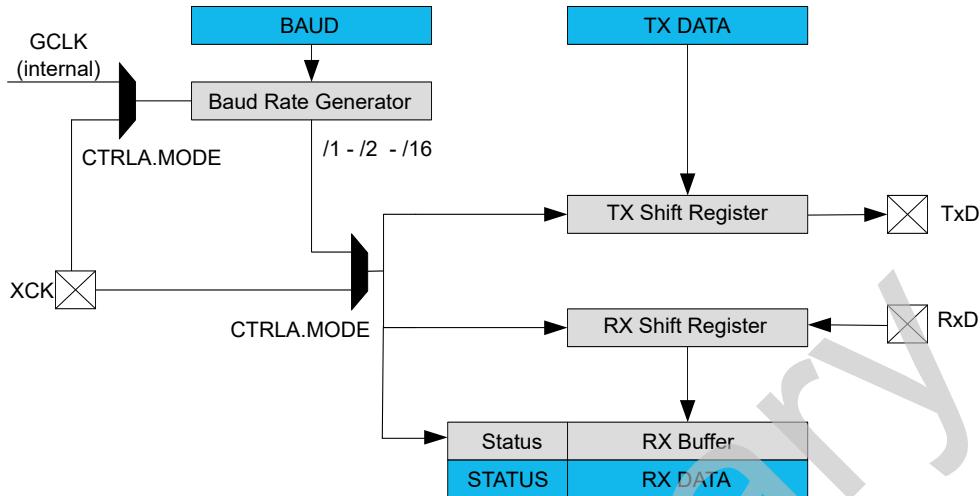
- Full-duplex Operation
- Asynchronous (with Clock Reconstruction) or Synchronous Operation
- Internal or External Clock source for Asynchronous and Synchronous Operation
- Baud-rate Generator
- Supports Serial Frames with 5, 6, 7, 8 or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check
- Selectable LSB- or MSB-first Data Transfer
- Buffer Overflow and Frame Error Detection
- Noise Filtering, Including False Start bit Detection and Digital Low-pass Filter
- Collision Detection
- Can Operate in all Sleep modes
- Operation at Speeds up to Half the System Clock for Internally Generated Clocks
- Operation at Speeds up to the System Clock for Externally Generated Clocks
- RTS and CTS Flow Control
- IrDA Modulation and Demodulation up to 115.2kbps
- LIN Master Support
- LIN Slave Support
 - Auto-baud and break character detection
- ISO 7816 T=0 or T=1 protocols for Smart Card Interfacing
- RS485 Support
- Start-of-frame detection
- Two-Level Receive Buffer
- Can work with DMA
- 32-bit Extension for Better System Bus Utilization

Related Links

[28.2. Features](#)

29.3 Block Diagram

Figure 29-1. USART Block Diagram



29.4 Signal Description

Table 29-1. SERCOM USART Signals

Signal Name	Type	Description
PAD[3:0]	Digital I/O	General SERCOM pins

One signal can be mapped to one of several pins.

29.5 Product Dependencies

To use this peripheral, other parts of the system must be configured correctly, as described below.

29.5.1 I/O Lines

Using the USART's I/O lines requires the I/O pins to be configured using the System Configuration registers or PPS registers.

When the SERCOM is used in USART mode, the SERCOM controls the direction and value of the I/O pins according to the table below. If the receiver or transmitter is disabled, these pins can be used for other purposes.

Table 29-2. USART Pin Configuration

Pin	Pin Configuration
TxD	Output
RxD	Input
XCK	Output or input

The combined configuration of PORT and the Transmit Data Pinout and Receive Data Pinout bit fields in the Control A register (CTRLA.TXPO and CTRLA.RXPO, respectively) will define the physical position of the USART signals in the above table.

29.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake-up the device from Sleep modes.

29.5.3 Clocks

A generic clock (GCLK_SERCOMx_CORE) is required to clock the SERCOMx_CORE. This clock must be configured and enabled in the CRU registers before using the SERCOMx_CORE. See *Clock and Reset (CRU)* and *Peripheral Module Disable Register (PMD)* from Related Links.

This generic clock is asynchronous to the bus clock (PBx_CLK). Therefore, writing to certain registers will require synchronization to the clock domains.

Related Links

- [19. Peripheral Module Disable Register \(PMD\)](#)
- [12. Clock and Reset Unit \(CRU\)](#)

29.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

- [21. Direct Memory Access Controller \(DMAC\)](#)

29.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

- [9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

29.5.6 Events

Not applicable.

29.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

Related Links

- [29.8.14. DBGCTRL](#)

29.5.8 Register Access Protection

Registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC).

PAC write protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)

Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

29.5.9 Analog Connections

Not applicable.

29.6 Functional Description

29.6.1 Principle of Operation

The USART uses the following lines for data transfer:

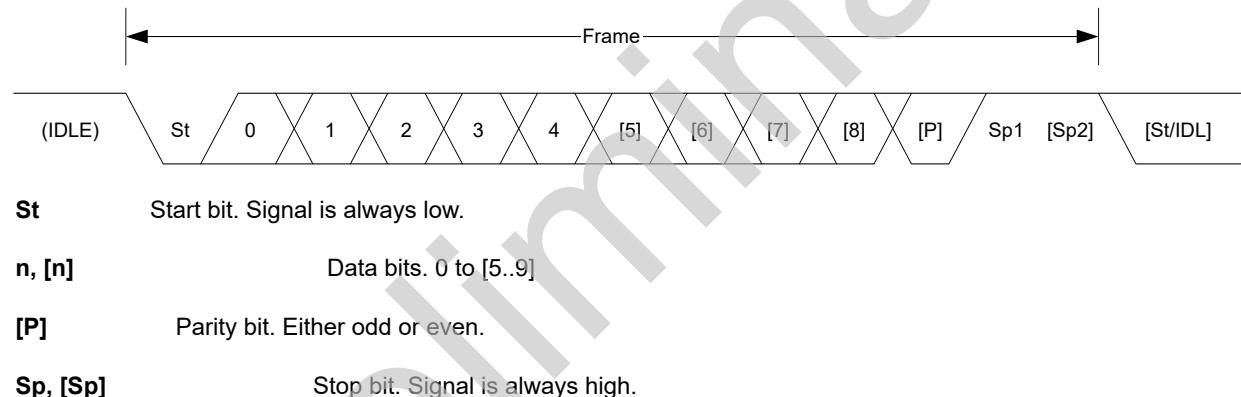
- RxD for receiving
- TxD for transmitting
- XCK for the transmission clock in synchronous operation

USART data transfer is frame based. A serial frame consists of:

- 1 start bit
- From 5 to 9 data bits (MSB or LSB first)
- No, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the Start bit followed by one character of Data bits. If enabled, the parity bit is inserted after the Data bits and before the first Stop bit. After the stop bit(s) of a frame, either the next frame can follow immediately, or the communication line can return to the Idle (high) state. The figure below illustrates the possible frame formats. Values inside brackets ([x]) denote optional bits.

Figure 29-2. Frame Formats



29.6.2 Basic Operation

29.6.2.1 Initialization

The following registers are enable-protected, meaning they can only be written when the USART is disabled (CTRLA.ENABLE=0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits.
- Control B register (CTRLB), except the Receiver Enable (RXEN) and Transmitter Enable (TXEN) bits.
- Baud register (BAUD)

When the USART is enabled or is being enabled (CTRLA.ENABLE=1), any writing attempt to these registers will be discarded. If the peripheral is being disabled, writing to these registers will be executed after disabling is completed. Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the USART is enabled, it must be configured by these steps:

1. Select either external (0x0) or internal clock (0x1) by writing the Operating Mode value in the CTRLA register (CTRLA.MODE).
2. Select either Asynchronous (0) or Synchronous (1) Communication mode by writing the Communication Mode bit in the CTRLA register (CTRLA.CMODE).

3. Select pin for receive data by writing the Receive Data Pinout value in the CTRLA register (CTRLA.RXPO).
4. Select pads for the transmitter and external clock by writing the Transmit Data Pinout bit in the CTRLA register (CTRLA.TXPO).
5. Configure the Character Size field in the CTRLB register (CTRLB.CHSIZE) for character size.
6. Set the Data Order bit in the CTRLA register (CTRLA.DORD) to determine MSB- or LSB-first data transmission.
7. To use parity mode:
 - a. Enable Parity mode by writing 0x1 to the Frame Format field in the CTRLA register (CTRLA.FORM).
 - b. Configure the Parity Mode bit in the CTRLB register (CTRLB.PMODE) for even or odd parity.
8. Configure the number of stop bits in the Stop Bit Mode bit in the CTRLB register (CTRLB.SBMODE).
9. When using an internal clock, write the Baud register (BAUD) to generate the desired baud rate.
10. Enable the transmitter and receiver by writing '1' to the Receiver Enable and Transmitter Enable bits in the CTRLB register (CTRLB.RXEN and CTRLB.TXEN).

29.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

Refer to the CTRLA register description for details.

29.6.2.3 Clock Generation and Selection

For both Synchronous and Asynchronous modes, the clock used for shifting and sampling data can be generated internally by the SERCOM baud-rate generator or supplied externally through the XCK line.

The Synchronous mode is selected by writing a '1' to the Communication Mode bit in the Control A register (CTRLA.CMODE), the Asynchronous mode is selected by writing '0' to CTRLA.CMODE.

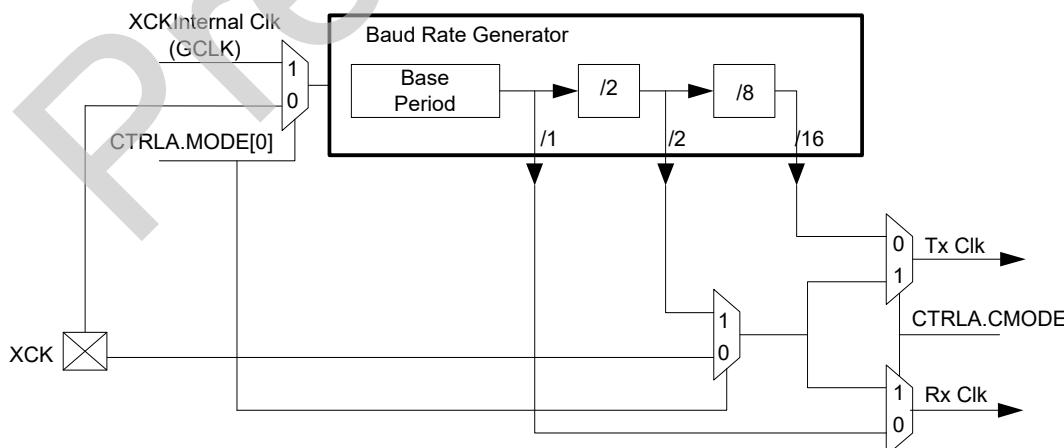
The internal clock source is selected by writing '1' to the Operation Mode bit field in the Control A register (CTRLA.MODE), the external clock source is selected by writing '0' to CTRLA.MODE.

The SERCOM baud-rate generator is configured as in the following figure.

In Asynchronous mode (CTRLA.CMODE=0), the 16-bit Baud register value is used.

In Synchronous mode (CTRLA.CMODE=1), the eight LSBs of the Baud register are used. For more details on configuring the baud rate, see *Clock Generation – Baud-Rate Generator* from Related Links.

Figure 29-3. Clock Generation



Related Links

[28.6.2.3. Clock Generation – Baud-Rate Generator](#)

29.6.2.3.1 Synchronous Clock Operation

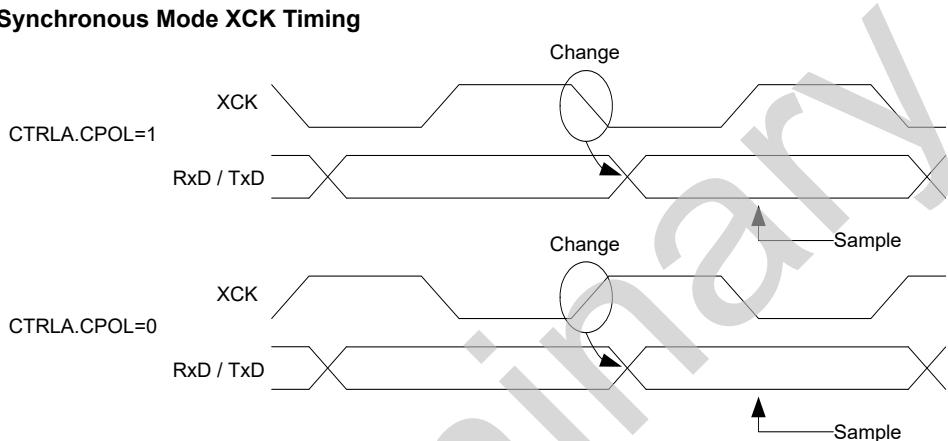
In Synchronous mode, the **CTRLA.MODE** bit field determines whether the transmission clock line (XCK) serves either as input or output. The dependency between clock edges, data sampling, and data change is the same for internal and external clocks. Data input on the RxD pin is sampled at the opposite XCK clock edge when data is driven on the TxD pin.

The Clock Polarity bit in the Control A register (CTRLA.CPOL) selects which XCK clock edge is used for RxD sampling, and which is used for TxD change:

When **CTRLA.CPOL** is '0', the data will be changed on the rising edge of XCK, and sampled on the falling edge of XCK.

When **CTRLA.CPOL** is '1', the data will be changed on the falling edge of XCK, and sampled on the rising edge of XCK.

Figure 29-4. Synchronous Mode XCK Timing



When the clock is provided through XCK (**CTRLA.MODE**=0x0), the Shift registers operate directly on the XCK clock. This means that XCK is not synchronized with the system clock and, therefore, can operate at frequencies up to the system frequency.

29.6.2.4 Data Register

The USART Transmit Data register (TxDATA) and USART Receive Data register (RxDATA) share the same I/O address, referred to as the Data register (DATA). Writing the DATA register will update the TxDATA register. Reading the DATA register will return the contents of the RxDATA register.

29.6.2.5 Data Transmission

Data transmission is initiated by writing the data to be sent into the DATA register. Then, the data in TxDATA will be moved to the Shift register when the Shift register is empty and ready to send a new frame. After the Shift register is loaded with data, the data frame will be transmitted.

When the entire data frame including Stop bit(s) has been transmitted and no new data was written to DATA, the Transmit Complete interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.TXC) will be set, and the optional interrupt will be generated.

The Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) indicates that the register is empty and ready for new data. The DATA register should only be written to when INTFLAG.DRE is set.

Disabling the Transmitter

The transmitter is disabled by writing '0' to the Transmitter Enable bit in the **CTRLB** register (CTRLB.TXEN).

Disabling the transmitter will complete only after any ongoing and pending transmissions are completed, i.e., there is no data in the transmit shift register and TxDATA to transmit.

29.6.2.5.1 Disabling the Transmitter

The transmitter is disabled by writing '0' to the Transmitter Enable bit in the **CTRLB** register (CTRLB.TXEN).

Disabling the transmitter will complete only after any ongoing and pending transmissions are completed, i.e., there is no data in the Transmit Shift register and TxDATA to transmit.

29.6.2.6 Data Reception

The receiver accepts data when a valid Start bit is detected. Each bit following the Start bit will be sampled according to the baud rate or XCK clock, and shifted into the receive Shift register until the first Stop bit of a frame is received. The second Stop bit will be ignored by the receiver.

When the first Stop bit is received and a complete serial frame is present in the Receive Shift register, the contents of the Shift register will be moved into the two-level receive buffer. Then, the Receive Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) will be set, and the optional interrupt will be generated.

The received data can be read from the DATA register when the Receive Complete Interrupt flag is set.

Disabling the Receiver

Writing '0' to the Receiver Enable bit in the CTRLB register (CTRLB.RXEN) will disable the receiver, flush the two-level receive buffer, and data from ongoing receptions will be lost.

Error Bits

The USART receiver has three error bits in the Status (STATUS) register: Frame Error (FERR), Buffer Overflow (BUFOVF), and Parity Error (PERR). Once an error happens, the corresponding error bit will be set until it is cleared by writing '1' to it. These bits are also cleared automatically when the receiver is disabled.

There are two methods for buffer overflow notification, selected by the Immediate Buffer Overflow Notification bit in the Control A register (CTRLA.IBON):

When CTRLA.IBON=1, STATUS.BUFOVF is raised immediately upon buffer overflow. Software can then empty the receive FIFO by reading RxDATA, until the receiver complete interrupt flag (INTFLAG.RXC) is cleared.

When CTRLA.IBON=0, the buffer overflow condition is attending data through the receive FIFO. After the received data is read, STATUS.BUFOVF will be set along with INTFLAG.RXC.

Asynchronous Data Reception

The USART includes a clock recovery and data recovery unit for handling asynchronous data reception.

The clock recovery logic can synchronize the incoming asynchronous serial frames at the RxD pin to the internally generated baud-rate clock.

The data recovery logic samples and applies a low-pass filter to each incoming bit, thereby improving the noise immunity of the receiver.

Asynchronous Operational Range

The operational range of the asynchronous reception depends on the accuracy of the internal baud-rate clock, the rate of the incoming frames, and the frame size (in number of bits). In addition, the operational range of the receiver is depending on the difference between the received bit rate and the internally generated baud rate. If the baud rate of an external transmitter is too high or too low compared to the internally generated baud rate, the receiver will not be able to synchronize the frames to the start bit.

There are two possible sources for a mismatch in baud rate: First, the reference clock will always have some minor instability. Second, the baud-rate generator cannot always do an exact division of the reference clock frequency to get the baud rate desired. In this case, the BAUD register value should be set to give the lowest possible error, see *Clock Generation – Baud-Rate Generator* from Related Links.

Recommended maximum receiver baud-rate errors for various character sizes are shown in the table below.

Table 29-3. Asynchronous Receiver Error for 16-fold Oversampling

D (Data bits+Parity)	R _{SLOW} [%]	R _{FAST} [%]	Max. total error [%]	Recommended max. Rx error [%]
5	94.12	107.69	+5.88/-7.69	±2.5
6	94.92	106.67	+5.08/-6.67	±2.0
7	95.52	105.88	+4.48/-5.88	±2.0

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.....continued

D (Data bits+Parity)	R _{SLOW} [%]	R _{FAST} [%]	Max. total error [%]	Recommended max. Rx error [%]
8	96.00	105.26	+4.00/-5.26	±2.0
9	96.39	104.76	+3.61/-4.76	±1.5
10	96.70	104.35	+3.30/-4.35	±1.5

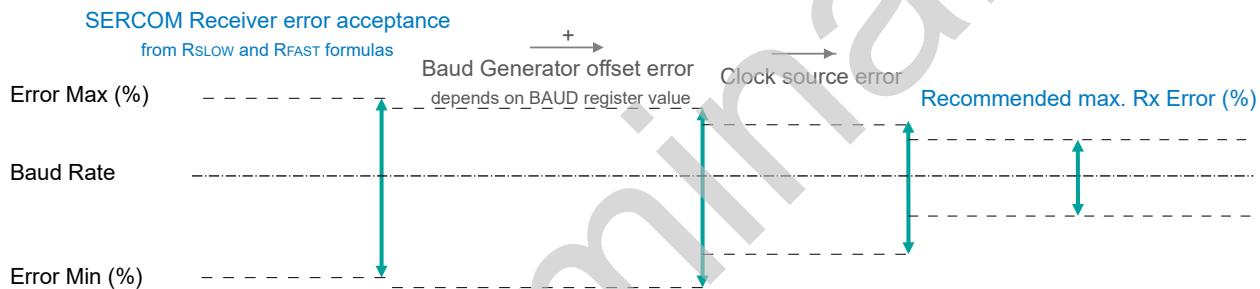
The following equations calculate the ratio of the incoming data rate and internal receiver baud rate:

$$R_{SLOW} = \frac{16(D + 1)}{16(D + 1) + 6} \quad , \quad R_{FAST} = \frac{16(D + 2)}{16(D + 1) + 8}$$

- R_{SLOW} is the ratio of the slowest incoming data rate that can be accepted in relation to the receiver baud rate
- R_{FAST} is the ratio of the fastest incoming data rate that can be accepted in relation to the receiver baud rate
- D is the sum of character size and parity size ($D = 5$ to 10 bits)

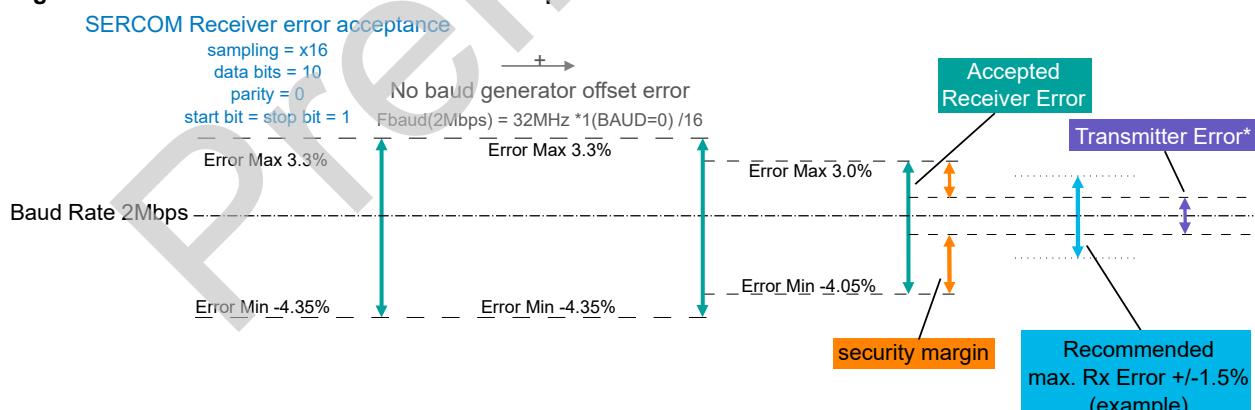
The recommended maximum Rx Error assumes that the receiver and transmitter equally divide the maximum total error. Its connection to the SERCOM Receiver error acceptance is depicted in this figure:

Figure 29-5. USART Rx Error Calculation



The recommendation values in the table above accommodate errors of the clock source and the baud generator. The following figure gives an example for a baud rate of 3Mbps:

Figure 29-6. USART Rx Error Calculation Example



*Transmitter Error depends on the external transmitter used in the application.

It is advised that it is within the Recommended max. Rx Error (+/-1.5% in this example).

Larger Transmitter Errors are acceptable but must lie within the Accepted Receiver Error.

Related Links

28.6.2.3. Clock Generation – Baud-Rate Generator

29.6.2.6.1 Disabling the Receiver

Writing '0' to the Receiver Enable bit in the CTRLB register (CTRLB.RXEN) will disable the receiver, flush the two-level receive buffer, and data from ongoing receptions will be lost.

29.6.2.6.2 Error Bits

The USART receiver has three error bits in the Status (STATUS) register: Frame Error (FERR), Buffer Overflow (BUFOVF), and Parity Error (PERR). Once an error happens, the corresponding error bit will be set until it is cleared by writing '1' to it. These bits are also cleared automatically when the receiver is disabled.

There are two methods for buffer overflow notification, selected by the Immediate Buffer Overflow Notification bit in the Control A register (CTRLA.IBON):

When CTRLA.IBON=1, STATUS.BUFOVF is raised immediately upon buffer overflow. Software can then empty the receive FIFO by reading RxDATA, until the Receiver Complete Interrupt flag (INTFLAG.RXC) is cleared.

When CTRLA.IBON=0, the Buffer Overflow condition travels with data through the receive FIFO. After the received data is read, STATUS.BUFOVF and INTFLAG.ERROR will be set along with INTFLAG.RXC.

29.6.2.6.3 Asynchronous Data Reception

The USART includes a clock recovery and data recovery unit for handling asynchronous data reception.

The clock recovery logic can synchronize the incoming asynchronous serial frames at the RxD pin to the internally generated baud-rate clock.

The data recovery logic samples and applies a low-pass filter to each incoming bit, thereby improving the noise immunity of the receiver.

29.6.2.6.4 Asynchronous Operational Range

The operational range of the asynchronous reception depends on the accuracy of the internal baud-rate clock, the rate of the incoming frames, and the frame size (in number of bits). In addition, the operational range of the receiver is depending on the difference between the received bit rate and the internally generated baud rate. If the baud rate of an external transmitter is too high or too low compared to the internally generated baud rate, the receiver will not be able to synchronize the frames to the start bit.

There are two possible sources for a mismatch in baud rate: First, the reference clock will always have some minor instability. Second, the baud-rate generator cannot always do an exact division of the reference clock frequency to get the baud rate desired. In this case, the BAUD register value should be set to give the lowest possible error, see *Clock Generation – Baud-Rate Generator* from Related Links.

Recommended maximum receiver baud-rate errors for various character sizes are shown in the table below.

Table 29-4. Asynchronous Receiver Error for 16-fold Oversampling

D (Data bits+Parity)	R _{SLOW} [%]	R _{FAST} [%]	Max. total error [%]	Recommended max. Rx error [%]
5	94.12	107.69	+5.88/-7.69	±2.5
6	94.92	106.67	+5.08/-6.67	±2.0
7	95.52	105.88	+4.48/-5.88	±2.0
8	96.00	105.26	+4.00/-5.26	±2.0
9	96.39	104.76	+3.61/-4.76	±1.5
10	96.70	104.35	+3.30/-4.35	±1.5

The following equations calculate the ratio of the incoming data rate and internal receiver baud rate:

$$R_{SLOW} = \frac{(D + 1)S}{S - 1 + D \cdot S + S_F} \quad , \quad R_{FAST} = \frac{(D + 2)S}{(D + 1)S + S_M}$$

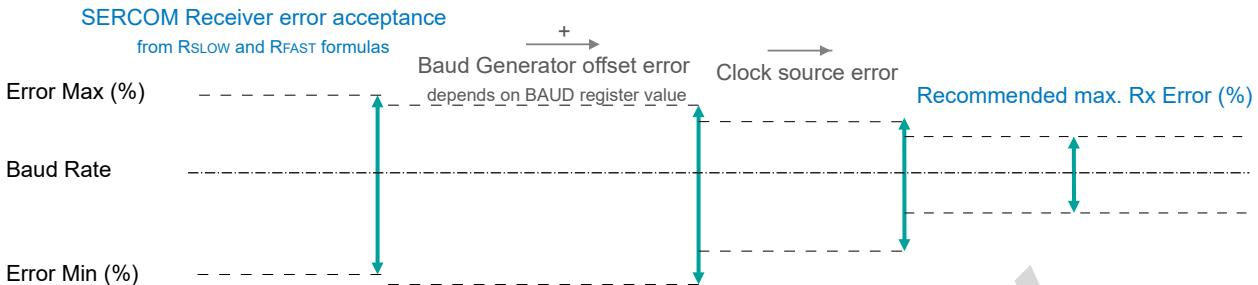
- R_{SLOW} is the ratio of the slowest incoming data rate that can be accepted in relation to the receiver baud rate
- R_{FAST} is the ratio of the fastest incoming data rate that can be accepted in relation to the receiver baud rate
- D is the sum of character size and parity size ($D = 5$ to 10 bits)
- S is the number of samples per bit ($S = 16$, 8 or 3)
- S_F is the first sample number used for majority voting ($S_F = 7$, 3 , or 2) when CTRLA.SAMPA=0.
- S_M is the middle sample number used for majority voting ($S_M = 8$, 4 , or 2) when CTRLA.SAMPA=0.

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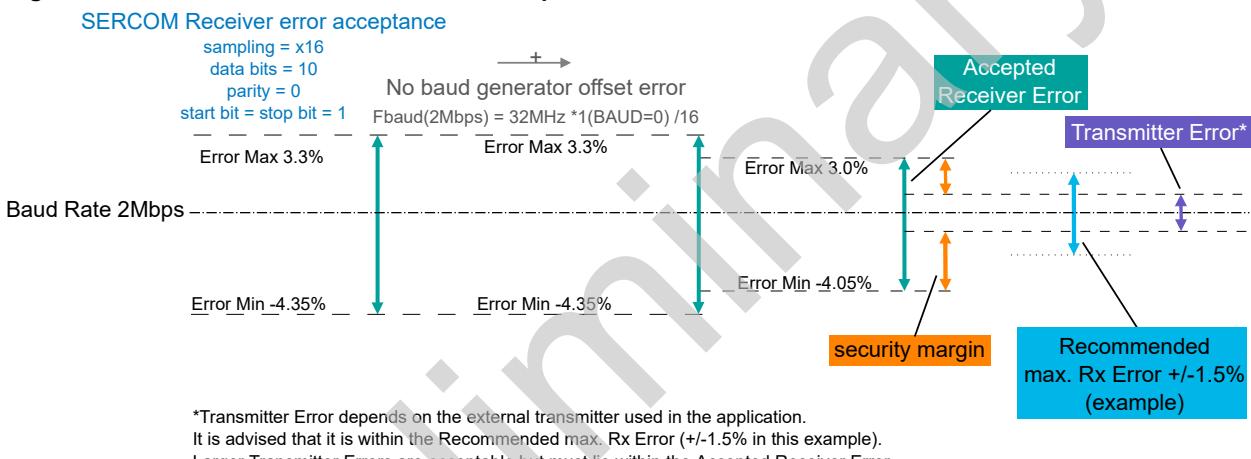
The recommended maximum Rx Error assumes that the receiver and transmitter equally divide the maximum total error. Its connection to the SERCOM Receiver error acceptance is depicted in this figure:

Figure 29-7. USART Rx Error Calculation



The recommendation values in the table above accommodate errors of the clock source and the baud generator. The following figure gives an example for a baud rate of 3Mbps:

Figure 29-8. USART Rx Error Calculation Example



Related Links

[28.6.2.3. Clock Generation – Baud-Rate Generator](#)

29.6.3 Additional Features

29.6.3.1 Parity

Even or odd parity can be selected for error checking by writing 0x1 to the Frame Format bit field in the Control A register (CTRLA.FORM).

If **even parity** is selected (CTRLB.PMODE=0), the Parity bit of an outgoing frame is '1' if the data contains an odd number of bits that are '1', making the total number of '1' even.

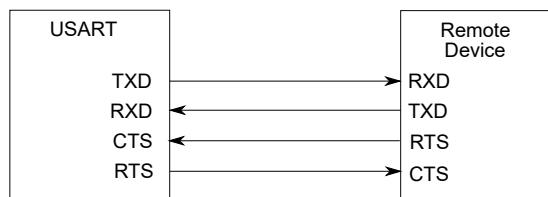
If **odd parity** is selected (CTRLB.PMODE=1), the Parity bit of an outgoing frame is '1' if the data contains an even number of bits that are '0', making the total number of '1' odd.

When parity checking is enabled, the parity checker calculates the parity of the data bits in incoming frames and compares the result with the Parity bit of the corresponding frame. If a parity error is detected, the Parity Error bit in the Status register (STATUS.PERR) is set.

29.6.3.2 Hardware Handshaking

The USART features an out-of-band hardware handshaking flow control mechanism, implemented by connecting the RTS and CTS pins with the remote device, as shown in the figure below.

Figure 29-9. Connection with a Remote Device for Hardware Handshaking

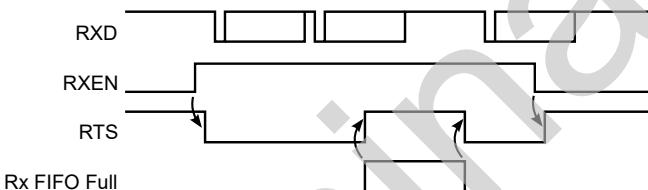


Hardware handshaking is only available in the following configuration:

- USART with internal clock (CTRLA.MODE=1),
- Asynchronous mode (CTRLA.CMODE=0), and
- Flow control pinout (CTRLA.TXPO=2).

When the receiver is disabled or the receive FIFO is full, the receiver will drive the RTS pin high. This notifies the remote device to stop transfer after the ongoing transmission. Enabling and disabling the receiver by writing to CTRLB.RXEN will set/clear the RTS pin after a synchronization delay. When the receive FIFO goes full, RTS will be set immediately and the frame being received will be stored in the Shift register until the receive FIFO is no longer full.

Figure 29-10. Receiver Behavior when Operating with Hardware Handshaking



The current CTS Status is in the STATUS register (STATUS.CTS). Character transmission will start only if STATUS.CTS=0. When CTS is set, the transmitter will complete the ongoing transmission and stop transmitting.

Figure 29-11. Transmitter Behavior when Operating with Hardware Handshaking



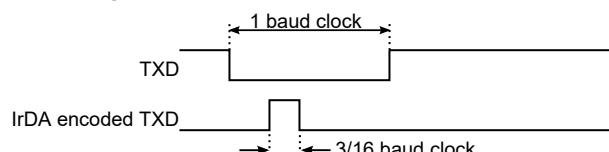
29.6.3.3 IrDA Modulation and Demodulation

Transmission and reception can be encoded IrDA compliant up to 115.2 kb/s. IrDA modulation and demodulation work in the following configuration:

- IrDA encoding enabled (CTRLB.ENC=1),
- Asynchronous mode (CTRLA.CMODE=0),
- and 16x sample rate (CTRLA.SAMPR[0]=0).

During transmission, each low bit is transmitted as a high pulse. The pulse width is 3/16 of the baud rate period, as illustrated in the figure below.

Figure 29-12. IrDA Transmit Encoding



The reception decoder has two main functions.

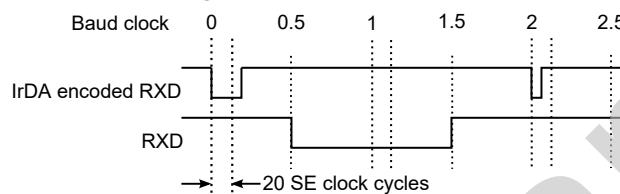
The first is to synchronize the incoming data to the IrDA baud rate counter. Synchronization is performed at the start of each zero pulse.

The second main function is to decode incoming Rx data. If a pulse width meets the minimum length set by configuration (RXPL.RXPL), it is accepted. When the baud rate counter reaches its middle value (1/2 bit length), it is transferred to the receiver.

Note: Note that the polarity of the transmitter and receiver are opposite: During transmission, a '0' bit is transmitted as a '1' pulse. During reception, an accepted '0' pulse is received as a '0' bit.

Example: The figure below illustrates reception where RXPL.RXPL is set to 19. This indicates that the pulse width should be at least 20 SE clock cycles. When using BAUD=0xE666 or 160 SE cycles per bit, this corresponds to 2/16 baud clock as minimum pulse width required. In this case the first bit is accepted as a '0', the second bit is a '1', and the third bit is also a '1'. A low pulse is rejected since it does not meet the minimum requirement of 2/16 baud clock.

Figure 29-13. IrDA Receive Decoding



29.6.3.4 Break Character Detection and Auto-Baud/LIN Slave

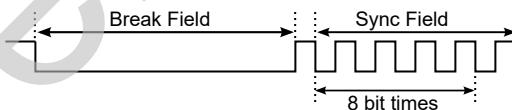
Break character detection and auto-baud are available in this configuration:

- Auto-baud frame format (CTRLA.FORM = 0x04 or 0x05),
- Asynchronous mode (CTRLA.CMODE = 0),
- and 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1).

The USART uses a break detection threshold of greater than 11 nominal bit times at the configured baud rate. At any time, if more than 11 consecutive dominant bits are detected on the bus, the USART detects a Break Field. When a break field has been detected, the Receive Break Interrupt Flag (INTFLAG.RXBRK) is set and the USART expects the sync field character to be 0x55. This field is used to update the actual baud rate in order to stay synchronized. If the received sync character is not 0x55, then the Inconsistent Sync Field error flag (STATUS.ISF) is set along with the Error Interrupt Flag (INTFLAG.ERROR), and the baud rate is unchanged.

The auto-baud follows the LIN format. All LIN Frames start with a Break Field followed by a Sync Field.

Figure 29-14. LIN Break and Sync Fields



After a break field is detected and the Start bit of the sync field is detected, a counter is started. The counter is then incremented for the next 8 bit times of the sync field. At the end of these 8 bit times, the counter is stopped. At this moment, the 13 Most Significant bits of the counter (value divided by 8) give the new clock divider (BAUD.BAUD), and the 3 Least Significant bits of this value (the remainder) give the new Fractional Part (BAUD.FP).

When the sync field has been received, the clock divider (BAUD.BAUD) and the Fractional Part (BAUD.FP) are updated after a synchronization delay. After the break and sync fields are received, multiple characters of data can be received.

29.6.3.5 LIN Master

LIN master is available with the following configuration:

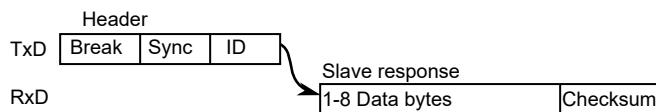
- LIN master format (CTRLA.FORM = 0x02)
- Asynchronous mode (CTRLA.CMODE = 0)
- 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1)

LIN frames start with a header transmitted by the master. The header consists of the break, sync, and identifier fields. After the master transmits the header, the addressed slave will respond with 1-8 bytes of data plus checksum.

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Figure 29-15. LIN Frame Format



Using the LIN command field (CTRLB.LINCMD), the complete header can be automatically transmitted, or software can control transmission of the various header components.

When CTRLB.LINCMD=0x1, software controls transmission of the LIN header. In this case, software uses the following sequence.

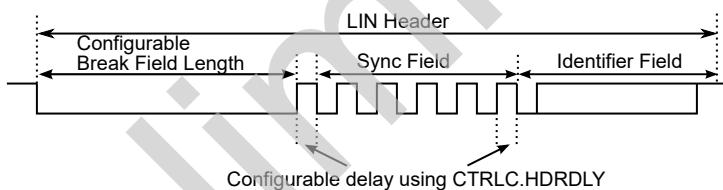
- CTRLB.LINCMD is written to 0x1.
- DATA register written to 0x00. This triggers transmission of the break field by hardware. Note that writing the DATA register with any other value will also result in the transmission of the break field by hardware.
- DATA register written to 0x55. The 0x55 value (sync) is transmitted.
- DATA register written to the identifier. The identifier is transmitted.

When CTRLB.LINCMD=0x2, hardware controls transmission of the LIN header. In this case, software uses the following sequence.

- CTRLB.LINCMD is written to 0x2.
- DATA register written to the identifier. This triggers transmission of the complete header by hardware. First the break field is transmitted. Next, the sync field is transmitted, and finally the identifier is transmitted.

In LIN master mode, the length of the break field is programmable using the break length field (CTRLC.BRKLEN). When the LIN header command is used (CTRLB.LINCMD=0x2), the delay between the break and sync fields, in addition to the delay between the sync and ID fields are configurable using the header delay field (CTRLC.HDRDLY). When manual transmission is used (CTRLB.LINCMD=0x1), software controls the delay between break and sync.

Figure 29-16. LIN Header Generation



After header transmission is complete, the slave responds with 1-8 data bytes plus checksum.

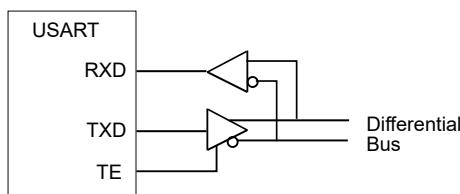
29.6.3.6 RS485

RS485 is available with the following configuration:

- USART frame format (CTRLA.FORM = 0x00 or 0x01)
- RS485 pinout (CTRLA.TXPO=0x3).

The RS485 feature enables control of an external line driver as shown in the figure below. While operating in RS485 mode, the transmit enable pin (TE) is driven high when the transmitter is active.

Figure 29-17. RS485 Bus Connection



The TE pin will remain high for the complete frame including stop bit(s). If a Guard Time is programmed in the Control C register (CTRLC.GTIME), the line will remain driven after the last character completion. The following figure shows a transfer with one stop bit and CTRLC.GTIME=3.

Figure 29-18. Example of TE Drive with Guard Time



The Transmit Complete interrupt flag (INTFLAG.TXC) will be raised after the guard time is complete and TE goes low.

29.6.3.7 ISO 7816 for Smart Card Interfacing

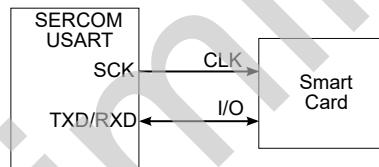
The SERCOM USART features an ISO/IEC 7816-compatible operating mode. This mode permits interfacing with smart cards and Security Access Modules (SAM) communicating through an ISO 7816 link. Both T=0 and T=1 protocols defined by the ISO 7816 specification are supported.

ISO 7816 is available with the following configuration:

- ISO 7816 format (CTRLA.FORM = 0x07)
- Inverse transmission and reception (CTRLA.RXINV=1 and CTRLA.TXINV=1)
- Single bidirectional data line (CTRLA.TXPO and CTRLA.RXPO configured to use the same data pin)
- Even parity (CTRLB.PMODE=0)
- 8-bit character size (CTRLB.CHSIZE=0)
- T=0 (CTRLA.CMODE=1) or T=1 (CTRLA.CMODE=0)

ISO 7816 is a half duplex communication on a single bidirectional line. The USART connects to a smart card as shown below. The output is only driven when the USART is transmitting. The USART is considered as the master of the communication as it generates the clock.

Figure 29-19. Connection of a Smart Card to the SERCOM USART



ISO 7816 characters are specified as 8 bits with even parity. The USART must be configured accordingly.

The USART cannot operate concurrently in both receiver and transmitter modes as the communication is unidirectional. It has to be configured according to the required mode by enabling or disabling either the receiver or the transmitter as desired. Enabling both the receiver and the transmitter at the same time in ISO 7816 mode may lead to unpredictable results.

The ISO 7816 specification defines an inverse transmission format. Data bits of the character must be transmitted on the I/O line at their negative value (CTRLA.RXINV=1 and CTRLA.TXINV=1).

Protocol T=0

In T=0 protocol, a character is made up of:

- one start bit,
- eight data bits,
- one parity bit
- and one guard time, which lasts two bit times.

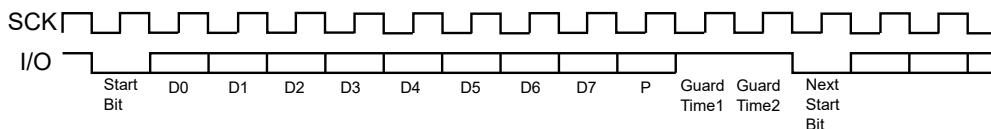
To transmit data in ISO7816, T=0 protocol mode, the USART is configured in CTRLA.CMODE =1 communication mode. The transmitter shifts out the bits and does not drive the I/O line during the guard time. Additional guard time can be added by programming the Guard Time (CTRLC.GTIME).

If no parity error is detected, the I/O line remains during the guard time and the transmitter can continue with the transmission of the next character, as shown in the figure below.

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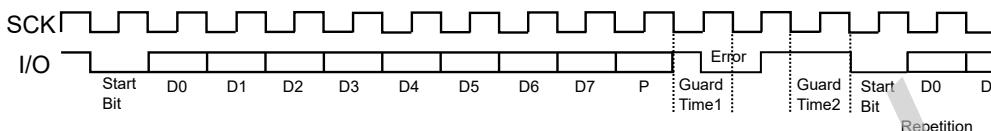
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Figure 29-20. T=0 Protocol without Parity Error



If a parity error is detected by the receiver, it drives the I/O line to 0 during the guard time, as shown in the next figure. This error bit is also named NACK, for Non Acknowledge. In this case, the character lasts 1 bit time more, as the guard time length is the same and is added to the error bit time, which lasts 1 bit time.

Figure 29-21. T=0 Protocol with Parity Error



When the USART is the receiver and it detects a parity error, the parity error bit in the Status Register (STATUS.PERR) is set and the character is not written to the receive FIFO.

Receive Error Counter

The receiver also records the total number of errors (receiver parity errors and NACKs from the remote transmitter) up to a maximum of 255. This can be read in the Receive Error Count (RXERRCNT) register. RXERRCNT is automatically cleared on read.

Receive NACK Inhibit

The receiver can also be configured to inhibit error generation. This can be achieved by setting the Inhibit Not Acknowledge (CTRLC.INACK) bit. If CTRLC.INACK is 1, no error signal is driven on the I/O line even if a parity error is detected. Moreover, if CTRLC.INACK is set, the erroneous received character is stored in the receive FIFO, and the STATUS.PERR bit is set. Inhibit not acknowledge (CTRLC.INACK) takes priority over disable successive receive NACK (CTRLC.DSNACK).

Transmit Character Repetition

When the USART is transmitting a character and gets a NACK, it can automatically repeat the character before moving on to the next character. Repetition is enabled by writing the Maximum Iterations register (CTRLC.MAXITER) to a non-zero value. The USART repeats the character the number of times specified in CTRLC.MAXITER.

When the USART repetition number reaches the programmed value in CTRLC.MAXITER, the STATUS.ITER bit is set and the internal iteration counter is reset. If the repetition of the character is acknowledged by the receiver before the maximum iteration is reached, the repetitions are stopped and the iteration counter is cleared.

Disable Successive Receive NACK

The receiver can limit the number of successive NACKs sent back to the remote transmitter. This is programmed by setting the Disable Successive NACK bit (CTRLC.DSNACK). The maximum number of NACKs transmitted is programmed in the CTRLC.MAXITER field. As soon as the maximum is reached, the character is considered as correct, an acknowledge is sent on the line, the STATUS.ITER bit is set and the internal iteration counter is reset.

Protocol T=1

To transmit data in ISO7816, T=1 protocol mode, the USART is configured in CTRLA.CMODE =0 communication mode with one or two stop bits. After the stop bits are sent, the transmitter does not drive the I/O line.

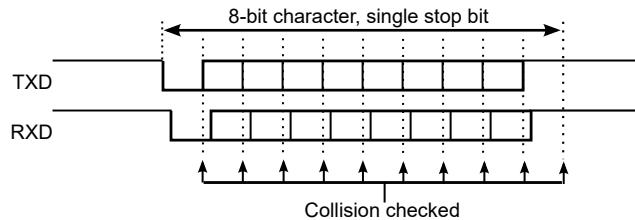
Parity is generated when transmitting and checked when receiving. Parity error detection sets the STATUS.PERR bit, and the erroneous character is written to the receive FIFO. When using T=1 protocol, the receiver does not signal errors on the I/O line and the transmitter does not retransmit.

29.6.3.8 Collision Detection

When the receiver and transmitter are connected either through pin configuration or externally, transmit collision can be detected after selecting the Collision Detection Enable bit in the CTRLB register (CTRLB.COLDEN=1). To detect collision, the receiver and transmitter must be enabled (CTRLB.RXEN=1 and CTRLB.TXEN=1).

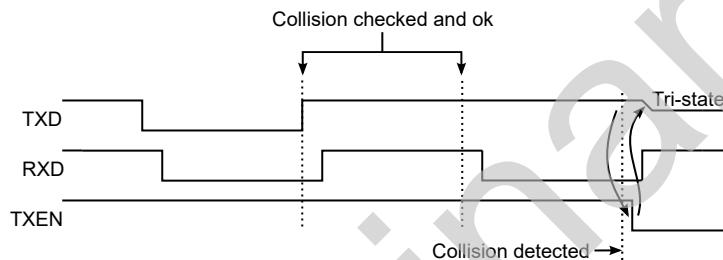
Collision detection is performed for each bit transmitted by comparing the received value with the transmit value, as shown in the figure below. While the transmitter is idle (no transmission in progress), characters can be received on RxD without triggering a collision.

Figure 29-22. Collision Checking



The next figure shows the conditions for a collision detection. In this case, the Start bit and the first Data bit are received with the same value as transmitted. The second received Data bit is found to be different than the transmitted bit at the detection point, which indicates a collision.

Figure 29-23. Collision Detected



When a collision is detected, the USART follows this sequence:

1. Abort the current transfer.
2. Flush the transmit buffer.
3. Disable transmitter (CTRLB.TXEN=0)
 - This is done after a synchronization delay. The CTRLB Synchronization Busy bit (SYNCBUSY.CTRLB) will be set until this is complete.
 - After disabling, the TxD pin will be tri-stated.
4. Set the Collision Detected bit (STATUS.COLL) along with the Error Interrupt Flag (INTFLAG.ERROR).
5. Set the Transmit Complete Interrupt Flag (INTFLAG.TXC), since the transmit buffer no longer contains data.

After a collision, software must manually enable the transmitter again before continuing, after assuring that the CTRLB Synchronization Busy bit (SYNCBUSY.CTRLB) is not set.

29.6.3.9 Loop-Back Mode

For Loop-Back mode, configure the Receive Data Pinout (CTRLA.RXPO) and Transmit Data Pinout (CTRLA.TXPO) to use the same data pins for transmit and receive. The loop-back is through the pad, so the signal is also available externally.

29.6.3.10 Start-of-Frame Detection

The USART start-of-frame detector can wake-up the CPU when it detects a Start bit. In Standby Sleep mode, the internal fast start-up oscillator must be selected as the GCLK_SERCOMx_CORE source.

When a 1-to-0 transition is detected on RxD, the 8 MHz Internal Oscillator is powered up and the USART clock is enabled. After start-up, the rest of the data frame can be received, provided that the baud rate is slow enough in relation to the fast start-up internal oscillator start-up time. Refer to the Electrical Specifications chapters for details. The start-up time of this oscillator varies with supply voltage and temperature.

The USART start-of-frame detection works both in Asynchronous and Synchronous modes. It is enabled by writing '1' to the Start of Frame Detection Enable bit in the Control B register (CTRLB.SFDE).

If the Receive Start Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.RXS) is set, the Receive Start interrupt is generated immediately when a start is detected.

When using start-of-frame detection without the Receive Start interrupt, start detection will force the 8 MHz internal oscillator and USART clock active while the frame is being received. In this case, the CPU will not wake up until the receive complete interrupt is generated.

29.6.3.11 Sample Adjustment

In Asynchronous mode (CTRLA.CMODE=0), three samples in the middle are used to determine the value based on majority voting. The three samples used for voting can be selected using the Sample Adjustment bit field in Control A register (CTRLA.SAMPA). When CTRLA.SAMPA=0, samples 7-8-9 are used for 16x oversampling, and samples 3-4-5 are used for 8x oversampling.

29.6.3.12 32-bit Extension

For better system bus utilization, 32-bit data receive and transmit can be enabled separately by writing to the Data 32-bit bit field in the Control C register (CTRLC.DATA32B). When enabled, writes and/or reads to the DATA register are 32 bit in size.

If frames are not multiples of 4 Bytes, the length counter (LENGTH.LEN) and length enable (LENGTH.LENEN) must be configured before data transfer begins, LENGTH.LEN must be enabled only when CTRLC.DATA32B is enabled.

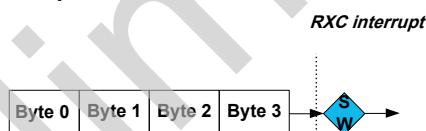
The figure below shows the order of transmit and receive when using 32-bit extension. Bytes are transmitted or received, and stored in order from 0 to 3. Only 8-bit and smaller character sizes are supported. If the character size is less than 8 bits, characters will still be 8-bit aligned within the 32-bit APB write or read. The unused bits within each byte will be zero for received data and unused for transmit data.

Figure 29-24. 32-bit Extension Ordering

APB Write/Read	BYTE3	BYTE2	BYTE1	BYTE0
Bit Position	31			0

A receive transaction using 32-bit extension is in the next figure. The Receive Complete flag (INTFLAG.RXC) is raised every four received Bytes. For transmit transactions, the Data Register Empty flag (INTFLAG.DRE) is raised instead of INTFLAG.RXC.

Figure 29-25. 32-bit Extension Receive Operation



Data Length Configuration

When the Data Length Enable bit field in the Length register (LENGTH.LENEN) is written to 0x1 or 0x2, the Data Length bit (LENGTH.LEN) determines the number of characters to be transmitted or received from 1 to 255.

Note: There is one internal length counter that can be used for either transmit (LENGTH.LENEN=0x1) or receive (LENGTH.LENEN=0x2), but not for both simultaneously.

The LENGTH register must be written before the frame begins. If LENGTH.LEN is not a multiple of 4 Bytes, the final INTFLAG.RXC/DRE interrupt will be raised when the last byte is received/sent. The internal length counter is reset when LENGTH.LEN is reached or when LENGTH.LENEN is written to 0x0.

Writing the LENGTH register while a frame is in progress will produce unpredictable results. If LENGTH.LENEN is not set and a frame is not a multiple of 4 Bytes, the remainder may be lost. Attempting to use the length counter for transmit and receive at the same time will produce unpredictable results.

29.6.4 DMA, Interrupts and Events

Table 29-5. Module Request for SERCOM USART

Condition	Request		
	DMA	Interrupt	Event
Data Register Empty (DRE)	Yes (request cleared when data is written)	Yes	NA
Receive Complete (RXC)	Yes (request cleared when data is read)	Yes	
Transmit Complete (TXC)	NA	Yes	
Receive Start (RXS)	NA	Yes	
Clear to Send Input Change (CTSIC)	NA	Yes	
Receive Break (RXBRK)	NA	Yes	
Error (ERROR)	NA	Yes	

29.6.4.1 DMA Operation

The USART generates the following DMA requests:

- Data received (RX): The request is set when data is available in the receive FIFO. The request is cleared when DATA is read.
- Data transmit (TX): The request is set when the transmit buffer (TX DATA) is empty. The request is cleared when DATA is written.

29.6.4.2 Interrupts

The USART has the following interrupt sources. These are asynchronous interrupts, and can wake-up the device from any Sleep mode:

- Data Register Empty (DRE)
- Receive Complete (RXC)
- Transmit Complete (TXC)
- Receive Start (RXS)
- Clear to Send Input Change (CTSIC)
- Received Break (RXBRK)
- Error (ERROR)

Each interrupt source has its own Interrupt flag. The Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the interrupt condition is met. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and if the corresponding interrupt is enabled. The interrupt request remains active until either the Interrupt flag is cleared, the interrupt is disabled, or the USART is reset. For details on clearing Interrupt flags, refer to the INTFLAG register description.

The value of INTFLAG indicates which interrupt is executed. Note that interrupts must be globally enabled for interrupt requests. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

29.6.4.3 Events

Not applicable.

29.6.5 Sleep Mode Operation

The behavior in Sleep mode is depending on the clock source and the Run In Standby bit in the Control A register (CTRLA.RUNSTDBY):

- Internal clocking, CTRLA.RUNSTDBY=1: GCLK_SERCOMx_CORE can be enabled in all Sleep modes. Any interrupt can wake-up the device.
- External clocking, CTRLA.RUNSTDBY=1: The Receive Complete interrupt(s) can wake-up the device.
- Internal clocking, CTRLA.RUNSTDBY=0: Internal clock will be disabled, after any ongoing transfer was completed. The Receive Complete interrupt(s) can wake-up the device.
- External clocking, CTRLA.RUNSTDBY=0: External clock will be disconnected, after any ongoing transfer was completed. All reception will be dropped.

29.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in the CTRLA register (CTRLA.SWRST)
- Enable bit in the CTRLA register (CTRLA.ENABLE)
- Receiver Enable bit in the CTRLB register (CTRLB.RXEN)
- Transmitter Enable bit in the Control B register (CTRLB.TXEN)

Note: CTRLB.RXEN is write-synchronized somewhat differently. See also [29.8.2. CTRLB](#) for details.

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

29.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
		15:8		SAMPR[2:0]				RXINV	TXINV	IBON
		23:16	SAMPA[1:0]		RXPO[1:0]					TXPO[1:0]
		31:24		DORD	CPOL	CMODE		FORM[3:0]		
0x04	CTRLB	7:0		SBMODE				CHSIZE[2:0]		
		15:8			PMODE			ENC	SFDE	COLDEN
		23:16							RXEN	TXEN
		31:24						LINCMD[1:0]		
0x08	CTRLC	7:0						GTIME[2:0]		
		15:8					HDRDLY[1:0]		BRKLEN[1:0]	
		23:16		MAXITER[2:0]					DSNACK	INACK
		31:24								DATA32B[1:0]
0x0C	BAUD	7:0				BAUD[7:0]				
		15:8				BAUD[15:8]				
0x0E	RXPL	7:0				RXPL[7:0]				
0x0F ...	Reserved									
0x14	INTENCLR	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x15	Reserved									
0x16	INTENSET	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
0x19	Reserved									
0x1A	STATUS	7:0	ITER	TXE	COLL	ISF	CTS	BUFOVF	FERR	PERR
		15:8								
0x1C	SYNCBUSY	7:0				LENGTH	RXERRCNT	CTRLB	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20	RXERRCNT	7:0				RXERRCNT[7:0]				
0x21	Reserved									
0x22	LENGTH	7:0				LEN[7:0]				
		15:8							LENEN[1:0]	
0x24 ...	Reserved									
0x28	DATA	7:0				DATA[7:0]				
		15:8				DATA[15:8]				
		23:16				DATA[23:16]				
		31:24				DATA[31:24]				
0x2C ...	Reserved									
0x30	DBGCTRL	7:0								DBGSTOP

29.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

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Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

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29.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access		DORD	CPOL	CMODE		FORM[3:0]		
Reset		R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W			RXINV	TXINV	IBON
Reset	0	0	0			0	0	0
Bit	7	6	5	4	3	2	1	0
Access	RUNSTDBY			MODE[2:0]		ENABLE	SWRST	
Reset	0			0	0	0	0	0

Bit 30 – DORD Data Order

This bit selects the data order when a character is shifted out from the Data register.
This bit is not synchronized.

Value	Description
0	MSB is transmitted first.
1	LSB is transmitted first.

Bit 29 – CPOL Clock Polarity

This bit selects the relationship between data output change and data input sampling in synchronous mode.
This bit is not synchronized.

CPOL	TxD Change	RxD Sample
0x0	Rising XCK edge	Falling XCK edge
0x1	Falling XCK edge	Rising XCK edge

Bit 28 – CMODE Communication Mode

This bit selects asynchronous or synchronous communication.
This bit is not synchronized.

Value	Description
0	Asynchronous communication.
1	Synchronous communication.

Bits 27:24 – FORM[3:0] Frame Format

These bits define the frame format.
These bits are not synchronized.

FORM[3:0]	Description
0x0	USART frame
0x1	USART frame with parity

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.....continued

FORM[3:0]	Description
0x2	LIN Master - Break and sync generation. See LIN Command (CTRLB.LINCMD).
0x3	Reserved
0x4	Auto-baud (LIN Slave) - break detection and auto-baud.
0x5	Auto-baud - break detection and auto-baud with parity
0x6	Reserved
0x7	ISO 7816
0x8-0xF	Reserved

Bits 23:22 – SAMPA[1:0] Sample Adjustment

These bits define the sample adjustment.

These bits are not synchronized.

SAMPA[1:0]	16x Over-sampling (CTRLA.SAMPR=0 or 1)	8x Over-sampling (CTRLA.SAMPR=2 or 3)
0x0	7-8-9	3-4-5
0x1	9-10-11	4-5-6
0x2	11-12-13	5-6-7
0x3	13-14-15	6-7-8

Bits 21:20 – RXPO[1:0] Receive Data Pinout

These bits define the receive data (RxD) pin configuration.

These bits are not synchronized.

RXPO[1:0]	Name	Description
0x0	PAD[0]	SERCOM PAD[0] is used for data reception
0x1	PAD[1]	SERCOM PAD[1] is used for data reception
0x2	PAD[2]	SERCOM PAD[2] is used for data reception
0x3	PAD[3]	SERCOM PAD[3] is used for data reception

Bits 17:16 – TXPO[1:0] Transmit Data Pinout

These bits define the transmit data (TxD) and XCK pin configurations.

This bit is not synchronized.

TXPO	TxD Pin Location	XCK Pin Location (When Applicable)	RTS/TE	CTS
0x0	SERCOM PAD[0]	SERCOM PAD[1]	N/A	N/A
0x1	Reserved			
0x2	SERCOM PAD[0]	N/A	SERCOM PAD[2]	SERCOM PAD[3]
0x3	SERCOM_PAD[0]	SERCOM_PAD[1]	SERCOM_PAD[2]	N/A

Bits 15:13 – SAMPR[2:0] Sample Rate

These bits select the sample rate.

These bits are not synchronized.

SAMPR[2:0]	Description
0x0	16x over-sampling using arithmetic baud rate generation.
0x1	16x over-sampling using fractional baud rate generation.
0x2	8x over-sampling using arithmetic baud rate generation.
0x3	8x over-sampling using fractional baud rate generation.
0x4	3x over-sampling using arithmetic baud rate generation.
0x5-0x7	Reserved

Bit 10 – RXINV Receive Data Invert

This bit controls whether the receive data (RxD) is inverted or not.

Note: Start, parity and stop bit(s) are unchanged. When enabled, parity is calculated on the inverted data.

This bit is not synchronized.

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Value	Description
0	RxD is not inverted.
1	RxD is inverted.

Bit 9 – TXINV Transmit Data Invert

This bit controls whether the transmit data (TxD) is inverted or not.

Note: Start, parity and stop bit(s) are unchanged. When enabled, parity is calculated on the inverted data.

This bit is not synchronized.

Value	Description
0	TxD is not inverted.
1	TxD is inverted.

Bit 8 – IBON Immediate Buffer Overflow Notification

This bit controls when the buffer overflow status bit (STATUS.BUFOVF) is asserted when a buffer overflow occurs.

This bit is not synchronized.

Value	Description
0	STATUS.BUFOVF is asserted when it occurs in the data stream.
1	STATUS.BUFOVF is asserted immediately upon buffer overflow.

Bit 7 – RUNSTDBY Run In Standby

This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

RUNSTDBY	External Clock	Internal Clock
0x0	External clock is disconnected when ongoing transfer is finished. All reception is dropped.	Generic clock is disabled when ongoing transfer is finished. The device will not wake up on Transfer Complete interrupt unless the appropriate ONDEMAND bits are set in the clocking chain.
0x1	Wake on Receive Complete interrupt.	Generic clock is enabled in all sleep modes. Any interrupt can wake up the device.

Bits 4:2 – MODE[2:0] Operating Mode

These bits select the USART serial communication interface of the SERCOM.

These bits are not synchronized.

Value	Description
0x0	USART with external clock
0x1	USART with internal clock

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable Synchronization Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

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Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

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29.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24	
							LINCMD[1:0]		
Access							R/W	R/W	
Reset							0	0	
Bit	23	22	21	20	19	18	17	16	
							RXEN	TXEN	
Access							R/W	R/W	
Reset							0	0	
Bit	15	14	13	12	11	10	9	8	
			PMODE			ENC	SFDE	COLDEN	
Access				R/W		R/W	R/W	R/W	
Reset				0		0	0	0	
Bit	7	6	5	4	3	2	1	0	
		SBMODE					CHSIZE[2:0]		
Access		R/W				R/W	R/W	R/W	
Reset		0				0	0	0	

Bits 25:24 – LINCMD[1:0] LIN Command

These bits define the LIN header transmission control. This field is only valid in LIN master mode (CTRLA.FORM= LIN Master).

These are strobe bits and will always read back as zero.

These bits are not enable-protected.

Value	Description
0x0	Normal USART transmission.
0x1	Break field is transmitted when DATA is written.
0x2	Break, sync and identifier are automatically transmitted when DATA is written with the identifier.
0x3	Reserved

Bit 17 – RXEN Receiver Enable

Writing '0' to this bit will disable the USART receiver. Disabling the receiver will flush the receive buffer and clear the FERR, PERR and BUFOVF bits in the STATUS register.

Writing '1' to CTRLB.RXEN when the USART is disabled will set CTRLB.RXEN immediately. When the USART is enabled, CTRLB.RXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the receiver is enabled. When the receiver is enabled, CTRLB.RXEN will read back as '1'.

Writing '1' to CTRLB.RXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.RXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The receiver is disabled or being enabled.
1	The receiver is enabled or will be enabled when the USART is enabled.

Bit 16 – TXEN Transmitter Enable

Writing '0' to this bit will disable the USART transmitter. Disabling the transmitter will not become effective until ongoing and pending transmissions are completed.

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Writing '1' to CTRLB.TXEN when the USART is disabled will set CTRLB.TXEN immediately. When the USART is enabled, CTRLB.TXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the transmitter is enabled. When the transmitter is enabled, CTRLB.TXEN will read back as '1'.

Writing '1' to CTRLB.TXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the transmitter is enabled, and CTRLB.TXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The transmitter is disabled or being enabled.
1	The transmitter is enabled or will be enabled when the USART is enabled.

Bit 13 – PMODE Parity Mode

This bit selects the type of parity used when parity is enabled (CTRLA.FORM is '1'). The transmitter will automatically generate and send the parity of the transmitted data bits within each frame. The receiver will generate a parity value for the incoming data and parity bit, compare it to the parity mode and, if a mismatch is detected, STATUS.PERR will be set.

This bit is not synchronized.

Value	Description
0	Even parity.
1	Odd parity.

Bit 10 – ENC Encoding Format

This bit selects the data encoding format.

This bit is not synchronized.

Value	Description
0	Data is not encoded.
1	Data is IrDA encoded.

Bit 9 – SFDE Start of Frame Detection Enable

This bit controls whether the start-of-frame detector will wake up the device when a start bit is detected on the RxD line.

This bit is not synchronized.

SFDE	INTENSET.RXS	INTENSET.RXC	Description
0	X	X	Start-of-frame detection disabled.
1	0	0	Reserved
1	0	1	Start-of-frame detection enabled. RXC wakes up the device from all sleep modes.
1	1	0	Start-of-frame detection enabled. RXS wakes up the device from all sleep modes.
1	1	1	Start-of-frame detection enabled. Both RXC and RXS wake up the device from all sleep modes.

Bit 8 – COLDEN Collision Detection Enable

This bit enables collision detection.

This bit is not synchronized.

Value	Description
0	Collision detection is not enabled.
1	Collision detection is enabled.

Bit 6 – SBMODE Stop Bit Mode

This bit selects the number of stop bits transmitted.

This bit is not synchronized.

Value	Description
0	One stop bit.
1	Two stop bits.

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Bits 2:0 – CHSIZE[2:0] Character Size

These bits select the number of bits in a character.

These bits are not synchronized.

CHSIZE[2:0]	Description
0x0	8 bits
0x1	9 bits
0x2-0x4	Reserved
0x5	5 bits
0x6	6 bits
0x7	7 bits

Preliminary

29.8.3 Control C

Name: CTRLC
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
							DATA32B[1:0]	
Access							R/W	R/W
Reset							0	0
Bit	23	22	21	20	19	18	17	16
			MAXITER[2:0]				DSNACK	INACK
Access		R/W	R/W	R/W			R/W	R/W
Reset		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8
				HDRDLY[1:0]			BRKLEN[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
					GTIME[2:0]			
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 25:24 – DATA32B[1:0] Data 32 Bit

These bits configure 32-bit Extension for read and write transactions to the DATA register.
When disabled, access is according to CTRLB.CHSIZE.

Value	Description
0x0	DATA reads (for received data) and writes (for transmit data) according to CTRLB.CHSIZE.
0x1	DATA reads according to CTRLB.CHSIZE. DATA writes using 32-bit Extension.
0x2	DATA reads using 32-bit Extension. DATA writes according to CTRLB.CHSIZE.
0x3	DATA reads and writes using 32-bit Extension.

Bits 22:20 – MAXITER[2:0] Maximum Iterations

These bits define the maximum number of retransmit iterations.
These bits also define the successive NACKs sent to the remote transmitter when CTRLC.DSNACK is set.
This field is only valid when using ISO7816 T = 0 mode (CTRLA.MODE = 0x7).

Bit 17 – DSNACK Disable Successive Not Acknowledge

This bit controls how many times NACK will be sent on parity error reception.
This bit is only valid in ISO7816 T=0 mode and when CTRLC.INACK=0.

Value	Description
0	NACK is sent on the ISO line for every parity error received.
1	Successive parity errors are counted up to the value specified in CTRLC.MAXITER. These parity errors generate a NACK on the ISO line. As soon as this value is reached, no additional NACK is sent on the ISO line.

Bit 16 – INACK Inhibit Not Acknowledge

This bit controls whether a NACK is transmitted when a parity error is received.
This bit is only valid in ISO7816 T = 0 mode.

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Value	Description
0	NACK is transmitted when a parity error is received.
1	NACK is not transmitted when a parity error is received.

Bits 11:10 – HDRDLY[1:0] LIN Master Header Delay

These bits define the delay between break and sync transmission in addition to the delay between the sync and identifier (ID) fields when in LIN master mode (CTRLA.FORM=0x2).

This field is only valid when using the LIN header command (CTRLB.LINCMD=0x2).

Value	Description
0x0	Delay between break and sync transmission is 1 bit time.
	Delay between sync and ID transmission is 1 bit time.
0x1	Delay between break and sync transmission is 4 bit time.
	Delay between sync and ID transmission is 4 bit time.
0x2	Delay between break and sync transmission is 8 bit time.
	Delay between sync and ID transmission is 4 bit time.
0x3	Delay between break and sync transmission is 14 bit time.
	Delay between sync and ID transmission is 4 bit time.

Bits 9:8 – BRKLEN[1:0] LIN Master Break Length

These bits define the length of the break field transmitted when in LIN master mode (CTRLA.FORM=0x2).

Value	Description
0x0	Break field transmission is 13 bit times
0x1	Break field transmission is 17 bit times
0x2	Break field transmission is 21 bit times
0x3	Break field transmission is 26 bit times

Bits 2:0 – GTIME[2:0] Guard Time

These bits define the guard time when using RS485 mode (CTRLA.FORM = 0x0 or CTRLA.FORM = 0x1, and CTRLA.TXPO = 0x3) or ISO7816 mode (CTRLA.FORM = 0x7).

For RS485 mode, the guard time is programmable from 0-7 bit times and defines the time that the transmit enable pin (TE) remains high after the last stop bit is transmitted and there is no remaining data to be transmitted.

For ISO7816 T = 0 mode, the guard time is programmable from 2-9 bit times and defines the guard time between each transmitted byte.

29.8.4 Baud

Name: BAUD
Offset: 0x0C
Reset: 0x0000
Property: Enable-Protected, PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
BAUD[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
BAUD[7:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BAUD[15:0]: Baud Value

Arithmetic Baud Rate Generation (CTRLA.SAMPR[0]=0):

These bits control the clock generation, as described in the SERCOM Baud Rate section.

If Fractional Baud Rate Generation (CTRLA.SAMPR[0]=1 or =3) bit positions 15 to 13 are replaced by FP[2:0]

Fractional Part:

- **Bits 15:13 - FP[2:0]: Fractional Part**

These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator* section.

- **Bits 12:0 - BAUD[12:0]: Baud Value**

These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator* section.

29.8.5 Receive Pulse Length Register

Name: RXPL
Offset: 0x0E
Reset: 0x00
Property: Enable-Protected, PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
RXPL[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RXPL[7:0] Receive Pulse Length

When the encoding format is set to IrDA (CTRLB.ENC=1), these bits control the minimum pulse length that is required for a pulse to be accepted by the IrDA receiver with regards to the serial engine clock period SE_{per} .

$$PULSE \geq (RXPL + 1) \cdot SE_{per}$$

29.8.6 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 5 – RXBRK Receive Break Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Break Interrupt Enable bit, which disables the Receive Break interrupt.

Value	Description
0	Receive Break interrupt is disabled.
1	Receive Break interrupt is enabled.

Bit 4 – CTSIC Clear to Send Input Change Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Clear To Send Input Change Interrupt Enable bit, which disables the Clear To Send Input Change interrupt.

Value	Description
0	Clear To Send Input Change interrupt is disabled.
1	Clear To Send Input Change interrupt is enabled.

Bit 3 – RXS Receive Start Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Start Interrupt Enable bit, which disables the Receive Start interrupt.

Value	Description
0	Receive Start interrupt is disabled.
1	Receive Start interrupt is enabled.

Bit 2 – RXC Receive Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Complete Interrupt Enable bit, which disables the Receive Complete interrupt.

Value	Description
0	Receive Complete interrupt is disabled.
1	Receive Complete interrupt is enabled.

Bit 1 – TXC Transmit Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Transmit Complete Interrupt Enable bit, which disables the Receive Complete interrupt.

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Value	Description
0	Transmit Complete interrupt is disabled.
1	Transmit Complete interrupt is enabled.

Bit 0 – DRE Data Register Empty Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Register Empty Interrupt Enable bit, which disables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

29.8.7 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset 0 0 0 0 0 0 0 0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 5 – RXBRK Receive Break Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Receive Break Interrupt Enable bit, which enables the Receive Break interrupt.

Value	Description
0	Receive Break interrupt is disabled.
1	Receive Break interrupt is enabled.

Bit 4 – CTSIC Clear to Send Input Change Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Clear To Send Input Change Interrupt Enable bit, which enables the Clear To Send Input Change interrupt.

Value	Description
0	Clear To Send Input Change interrupt is disabled.
1	Clear To Send Input Change interrupt is enabled.

Bit 3 – RXS Receive Start Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Receive Start Interrupt Enable bit, which enables the Receive Start interrupt.

Value	Description
0	Receive Start interrupt is disabled.
1	Receive Start interrupt is enabled.

Bit 2 – RXC Receive Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Receive Complete Interrupt Enable bit, which enables the Receive Complete interrupt.

Value	Description
0	Receive Complete interrupt is disabled.
1	Receive Complete interrupt is enabled.

Bit 1 – TXC Transmit Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Transmit Complete Interrupt Enable bit, which enables the Transmit Complete interrupt.

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Value	Description
0	Transmit Complete interrupt is disabled.
1	Transmit Complete interrupt is enabled.

Bit 0 – DRE Data Register Empty Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Register Empty Interrupt Enable bit, which enables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

29.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
Access	R/W		R/W	R/W	R/W	R	R/W	R
Reset	0		0	0	0	0	0	0

Bit 7 – ERROR Error

This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. Errors that will set this flag are COLL, ISF, BUFOVF, FERR, and PERR. Writing '0' to this bit has no effect. Writing '1' to this bit will clear the flag.

Bit 5 – RXBRK Receive Break

This flag is cleared by writing '1' to it.

This flag is set when auto-baud is enabled (CTRLA.FORM) and a break character is received.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 4 – CTSIC Clear to Send Input Change

This flag is cleared by writing a '1' to it.

This flag is set when a change is detected on the CTS pin.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – RXS Receive Start

This flag is cleared by writing '1' to it.

This flag is set when a Start condition is detected on the RxD line and start-of-frame detection is enabled (CTRLB.SFDE is '1').

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Start Interrupt flag.

Bit 2 – RXC Receive Complete

This flag is cleared by reading the Data register (DATA) or by disabling the receiver.

This flag is set when there are unread data in DATA.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 1 – TXC Transmit Complete

This flag is cleared by writing '1' to it or by writing new data to DATA.

This flag is set when the entire frame in the Transmit Shift register has been shifted out and there are no new data in DATA.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 0 – DRE Data Register Empty

This flag is cleared by writing new data to DATA.

This flag is set when DATA is empty and ready to be written.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

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29.8.9 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – ITER Maximum Number of Repetitions Reached

This bit is set when the maximum number of NACK repetitions or retransmissions is met in ISO7816 T=0 mode.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 6 – TXE Transmitter Empty

When CTRLA.FORM is set to LIN Master mode, this bit is set when any ongoing transmission is complete and TxDATA is empty.

When CTRLA.FORM is not set to LIN Master mode, this bit will always read back as zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 5 – COLL Collision Detected

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when collision detection is enabled (CTRLB.COLDEN) and a collision is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 4 – ISF Inconsistent Sync Field

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when the frame format is set to auto-baud (CTRLA.FORM) and a sync field not equal to 0x55 is received.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 3 – CTS Clear to Send

This bit indicates the current level of the CTS pin when flow control is enabled (CTRLA.TXPO).

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 2 – BUFOVF Buffer Overflow

Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a buffer overflow condition is detected. A buffer overflow occurs when the receive buffer is full, there is a new character waiting in the receive shift register and a new start bit is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

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Bit 1 – FERR Frame Error

Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if the received character had a frame error, i.e., when the first stop bit is zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 0 – PERR Parity Error

Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if parity checking is enabled (CTRLA.FORM is 0x1, 0x5, or 0x7) and a parity error is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

29.8.10 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit 4 – LENGTH LENGTH Synchronization Busy

Writing to the LENGTH register requires synchronization. When writing to LENGTH, SYNCBUSY.LENGTH will be set until synchronization is complete. If the LENGTH register is written to while SYNCBUSY.LENGTH is asserted, an APB error is generated.

Value	Description
0	LENGTH synchronization is not busy.
1	LENGTH synchronization is busy.

Bit 3 – RXERRCNT Receive Error Count Synchronization Busy

The RXERRCNT register is automatically synchronized to the APB domain upon error. When returning from sleep, this bit will be raised until the new value is available to be read.

Value	Description
0	RXERRCNT synchronization is not busy.
1	RXERRCNT synchronization is busy.

Bit 2 – CTRLB CTRLB Synchronization Busy

Writing to the CTRLB register when the SERCOM is enabled requires synchronization. When writing to CTRLB the SYNCBUSY.CTRLB bit will be set until synchronization is complete. If CTRLB is written while SYNCBUSY.CTRLB is asserted, an APB error will be generated.

Value	Description
0	CTRLB synchronization is not busy.
1	CTRLB synchronization is busy.

Bit 1 – ENABLE SERCOM Enable Synchronization Busy

Enabling and disabling the SERCOM (CTRLA.ENABLE) requires synchronization. When written, the SYNCBUSY.ENABLE bit will be set until synchronization is complete.

Value	Description
0	Enable synchronization is not busy.
1	Enable synchronization is busy.

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Bit 0 – SWRST Software Reset Synchronization Busy

Resetting the SERCOM (CTRLA.SWRST) requires synchronization. When written, the SYNCBUSY.SWRST bit will be set until synchronization is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

29.8.11 Receive Error Count

Name: RXERRCNT
Offset: 0x20
Reset: 0x00
Property: Read-Synchronized

Bit	7	6	5	4	3	2	1	0
RXERRCNT[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RXERRCNT[7:0] Receive Error Count

This register records the total number of parity errors and NACK errors combined in ISO7816 mode (CTRLA.FORM=0x7).

This register is automatically cleared on read.

29.8.12 Length

Name: LENGTH
Offset: 0x22
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
							LENEN[1:0]	
Access						R/W		R/W
Reset						0		0
Bit	7	6	5	4	3	2	1	0
				LEN[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – LENEN[1:0] Data Length Enable

In 32-bit Extension mode, this bit field configures the length counter either for transmit or receive transactions.

Value	Description
0x0	Length counter disabled
0x1	Length counter enabled for transmit
0x2	Length counter enabled for receive
0x3	Reserved

Bits 7:0 – LEN[7:0] Data Length

In 32-bit Extension mode, this bit field configures the data length after which the flags INTFLAG.RXC or INTFLAG.DRE are raised.

Value	Description
0x00	Reserved if LENEN=0x1 or LENEN=0x2
0x01-0xF	Data Length
F	

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29.8.13 Data

Name: DATA
Offset: 0x28
Reset: 0x0000
Property: -

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data

Reading these bits will return the contents of the Receive Data register. The register should be read only when the Receive Complete Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set. The status bits in STATUS should be read before reading the DATA value in order to get any corresponding error.

Writing these bits will write the Transmit Data register. This register should be written only when the Data Register Empty Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is set.

Reads and writes are 32-bit or CTLB.CHSIZE based on the CTRLC.DATA32B setting.

29.8.14 Debug Control

Name: DBGCTRL
Offset: 0x30
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGSTOP 0

Bit 0 – DBGSTOP Debug Stop Mode

This bit controls the baud-rate generator functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.

30. SERCOM SPI – SERCOM Serial Peripheral Interface

30.1 Overview

The Serial Peripheral Interface (SPI) is one of the available modes in the Serial Communication Interface (SERCOM).

The SPI uses the SERCOM transmitter and receiver configured as shown in Block Diagram (see *Full-Duplex SPI Master Slave Interconnection* in the *Block Diagram* from Related Links. Each side, master and slave, depicts a separate SPI containing a Shift register, a transmit buffer and a two-level receive buffer. In addition, the SPI master uses the SERCOM baud-rate generator, while the SPI Slave can use the SERCOM address match logic. Labels in capital letters are synchronous to PBx_CLK and accessible by the CPU, while labels in lowercase letters are synchronous to the SCK clock.

Related Links

[30.3. Block Diagram](#)

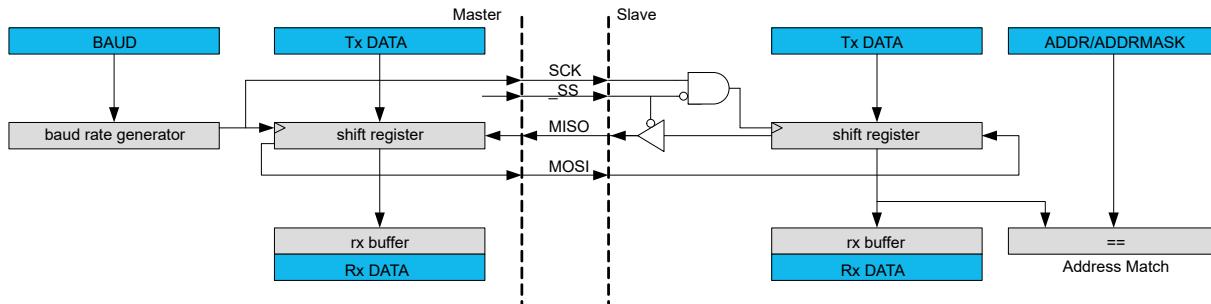
30.2 Features

SERCOM SPI includes the following features:

- Full-duplex, four-wire interface (MISO, MOSI, SCK, SS)
- One-level transmit buffer, two-level receive buffer
- Supports all four SPI modes of operation
- Single data direction operation allows alternate function on MISO or MOSI pin
- Selectable LSB- or MSB-first data transfer
- Can be used with DMA
- 32-bit Extension for better system bus utilization
- Master Operation:
 - Serial clock speed up to half the system clock
 - 8-bit clock generator
 - Hardware controlled SS
 - Optional inter-character spacing
- Slave Operation:
 - Serial clock speed up to half the system clock
 - Optional 8-bit address match operation
 - Operation in all sleep modes
 - Wake on SS transition

30.3 Block Diagram

Figure 30-1. Full-Duplex SPI Host Client Interconnection



30.4 Signal Description

Table 30-1. SERCOM SPI Signals

Signal Name	Type	Description
PAD[3:0]	Digital I/O	General SERCOM pins

One signal can be mapped to one of several pins.

30.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

30.5.1 I/O Lines

In order to use the SERCOM's I/O lines, the I/O pins must be configured using the System Configuration registers or PPS registers.

When the SERCOM is configured for SPI operation, the SERCOM controls the direction and value of the I/O pins according to the following table. Both PORT Control bits PINCFGn.PULLEN and PINCFGn.DRVSTR are still effective. If the receiver is disabled, the data input pin can be used for other purposes. In Master mode, the Slave Select line (\overline{SS}) is hardware controlled when the Master Slave Select Enable bit in the Control B register (CTRLB.MSSEN) is '1'.

Table 30-2. SPI Pin Configuration

Pin	Master SPI	Slave SPI
MOSI	Output	Input
MISO	Input	Output
SCK	Output	Input
\overline{SS}	Output (CTRLB.MSSEN = 1)	Input

The combined configuration of PORT, the Data In Pinout and the Data Out Pinout bit groups in the Control A register (CTRLA.DIPO and CTRLA.DOPO) define the physical position of the SPI signals in the table above.

30.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake-up the device from Sleep modes.

30.5.3 Clocks

A generic clock (GCLK_SERCOMx_CORE) is required to clock the SPI. This clock must be configured and enabled in the Clock and Reset Unit (CRU) and Configuration (CFG.CFGPCLKGEN1) registers before using the SPI.

This generic clock is asynchronous to the bus clock (PBx_CLK). Therefore, writes to certain registers will require synchronization to the clock domains.

30.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

[21. Direct Memory Access Controller \(DMAC\)](#)

30.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

30.5.6 Events

Not applicable.

30.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

30.5.8 Register Access Protection

Registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC).

PAC write protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)

Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

30.5.9 Analog Connections

Not applicable.

30.6 Functional Description

30.6.1 Principle of Operation

The SPI is a high-speed synchronous data transfer interface. It allows high-speed communication between the device and peripheral devices.

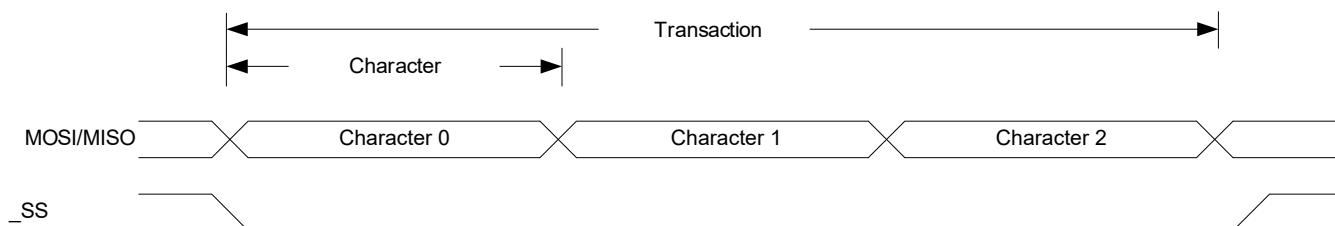
The SPI can operate as host or client. As host, the SPI initiates and controls all data transactions. The SPI is single buffered for transmitting and double buffered for receiving.

When transmitting data, the Data register can be loaded with the next character to be transmitted during the current transmission.

When receiving, the data is transferred to the two-level receive buffer, and the receiver is ready for a new character.

The SPI transaction format is shown in [SPI Transaction Format](#). Each transaction can contain one or more characters. The character size is configurable, and can be either 8 or 9 bits.

Figure 30-2. SPI Transaction Format



The SPI host must pull the SPI select line (SS) of the desired client low to initiate a transaction if multiple clients are connected to the bus. The SPI select line can be wired low if there is only one SPI client on the bus. The host and client prepare data to send via their respective Shift registers, and the host generates the serial clock on the SCK line.

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Data is always shifted from host to client on the Host Output Client Input line (MOSI); data is shifted from client to host on the Host Input Client Output line (MISO).

Each time character is shifted out from the host, a character will be shifted out from the client simultaneously. To signal the end of a transaction, the host will pull the SS line high.

30.6.2 Basic Operation

30.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the SPI is disabled (CTRLA.ENABLE=0):

- Control A register (CTRLA), except Enable (CTRLA.ENABLE) and Software Reset (CTRLA.SWRST)
- Control B register (CTRLB), except Receiver Enable (CTRLB.RXEN)
- Baud register (BAUD)
- Address register (ADDR)

When the SPI is enabled or is being enabled (CTRLA.ENABLE=1), any writing to these registers will be discarded.

When the SPI is being disabled, writing to these registers will be completed after the disabling.

Enable-protection is denoted by the Enable-Protection property in the register description.

Initialize the SPI by following these steps:

1. Select SPI mode in host/client operation in the Operating Mode bit group in the CTRLA register (CTRLA.MODE= 0x2 or 0x3).
2. Select Transfer mode for the Clock Polarity bit and the Clock Phase bit in the CTRLA register (CTRLA.CPOL and CTRLA.CPHA) if desired.
3. Select the Frame Format value in the CTRLA register (CTRLA.FORM).
4. Configure the Data In Pinout field in the Control A register (CTRLA.DIPO) for SERCOM pads of the receiver.
5. Configure the Data Out Pinout bit group in the Control A register (CTRLA.DOPO) for SERCOM pads of the transmitter.
6. Select the Character Size value in the CTRLB register (CTRLB.CHSIZE).
7. Write the Data Order bit in the CTRLA register (CTRLA.DORD) for data direction.
8. If the SPI is used in Host mode:
 - a. Select the desired baud rate by writing to the Baud register (BAUD).
 - b. If Hardware SS control is required, write '1' to the Host SPI Select Enable bit in CTRLB register (CTRLB.MSSEN).
9. Enable the receiver by writing the Receiver Enable bit in the CTRLB register (CTRLB.RXEN=1).

30.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

Refer to the CTRLA register description for details.

30.6.2.3 Clock Generation

In the SPI master operation (CTRLA.MODE = 0x3), the serial clock (SCK) is generated internally by the SERCOM Baud Rate Generator (BRG).

In SPI mode, the BRG is set to Synchronous mode. The 8-bit Baud register (BAUD) value is used for generating SCK and clocking the Shift register, see *Clock Generation – Baud-Rate Generator* from Related Links.

In the SPI slave operation (CTRLA.MODE = 0x2), the clock is provided by an external master on the SCK pin. This clock is used to clock the SPI Shift register.

Related Links

[28.6.2.3. Clock Generation – Baud-Rate Generator](#)

30.6.2.4 Data Register

The SPI Transmit Data register (TxDATA) and SPI Receive Data register (RxDATA) share the same I/O address, referred to as the SPI Data register (DATA). Writing DATA register will update the Transmit Data register. Reading the DATA register will return the contents of the Receive Data register.

30.6.2.5 SPI Transfer Modes

There are four combinations of SCK phase and polarity to transfer serial data. The SPI Data Transfer modes are shown in [SPI Transfer Modes \(Table\)](#) and [SPI Transfer Modes \(Figure\)](#).

SCK phase is configured by the Clock Phase bit in the CTRLA register (CTRLA.CPHA). SCK polarity is programmed by the Clock Polarity bit in the CTRLA register (CTRLA.CPOL). Data bits are shifted out and latched in on opposite edges of the SCK signal. This ensures sufficient time for the data signals to stabilize.

Table 30-3. SPI Transfer Modes

Mode	CPOL	CPHA	Leading Edge	Trailing Edge
0	0	0	Rising, sample	Falling, setup
1	0	1	Rising, setup	Falling, sample
2	1	0	Falling, sample	Rising, setup
3	1	1	Falling, setup	Rising, sample

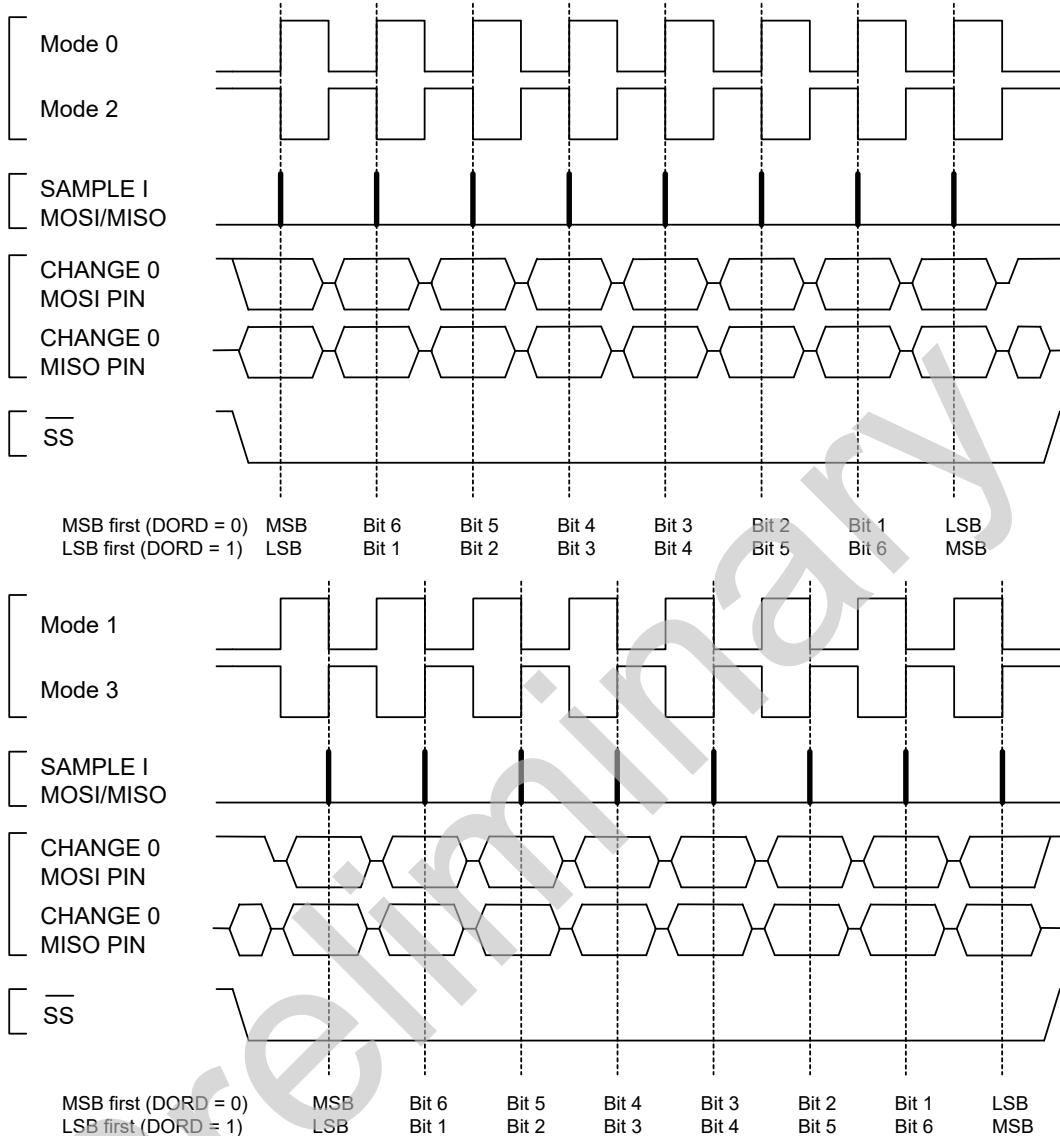
Note:

Leading edge is the first clock edge in a clock cycle.

Trailing edge is the second clock edge in a clock cycle.

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Figure 30-3. SPI Transfer Modes



30.6.2.6 Transferring Data

30.6.2.6.1 Master

In Master mode (CTRLA.MODE=0x3), when Master Slave Enable Select (CTRLB.MSSEN) is '1', hardware will control the SS line.

When Master Slave Select Enable (CTRLB.MSSEN) is '0', the SS line must be configured as an output. SS can be assigned to any general purpose I/O pin. When the SPI is ready for a data transaction, software must pull the SS line low.

When writing a character to the Data register (DATA), the character will be transferred to the Shift register. Once the content of TxDATA has been transferred to the Shift register, the Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) will be set, and a new character can be written to DATA.

Each time one character is shifted out from the master, another character will be shifted in from the slave simultaneously. If the receiver is enabled (CTRLA.RXEN=1), the contents of the Shift register will be transferred to the two-level receive buffer. The transfer takes place in the same clock cycle as the last data bit is shifted in. Then the Receive Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) will be set. The received data can be retrieved by reading DATA.

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When the last character has been transmitted and there is no valid data in DATA, the Transmit Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.TXC) will be set. When the transaction is finished, the master must pull the SS line high to notify the slave. If Master Slave Select Enable (CTRLB.MSSEN) is set to '0', the software must pull the SS line high.

30.6.2.6.2 Slave

In Slave mode (CTRLA.MODE = 0x2), the SPI interface will remain inactive with the MISO line tri-stated as long as the SS pin is pulled high. Software may update the contents of DATA at any time as long as the Data Register Empty flag in the Interrupt Status and Clear register (INTFLAG.DRE) is set.

When SS is pulled low and SCK is running, the slave will sample and shift out data according to the Transaction mode set. When the content of TxDATA has been loaded into the Shift register, INTFLAG.DRE will be set, and new data can be written to DATA.

Similar to the master, the slave will receive one character for each character transmitted. A character will be transferred into the two-level receive buffer within the same clock cycle its last data bit is received. The received character can be retrieved from DATA when the Receive Complete interrupt flag (INTFLAG.RXC) is set.

When the master pulls the SS line high, the transaction is done and the Transmit Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.TXC) will be set.

After DATA is written it takes up to three SCK clock cycles until the content of DATA is ready to be loaded into the Shift register on the next character boundary. As a consequence, the first character transferred in a SPI transaction will not be the content of DATA. This can be avoided by using the preloading feature, see *Preloading of the Slave Shift Register* from Related Links.

When transmitting several characters in one SPI transaction, the data has to be written into DATA register with at least three SCK clock cycles left in the current character transmission. If this criteria is not met, the previously received character will be transmitted.

Once the DATA register is empty, it takes three CLK_SERCOM_APB cycles for INTFLAG.DRE to be set.

Related Links

[30.6.3.2. Preloading of the Slave Shift Register](#)

30.6.2.7 Receiver Error Bit

The SPI receiver has one error bit: the Buffer Overflow bit (BUFOVF), which can be read from the Status register (STATUS). Once an error happens, the bit will stay set until it is cleared by writing '1' to it. The bit is also automatically cleared when the receiver is disabled.

There are two methods for buffer overflow notification, selected by the immediate Buffer Overflow Notification bit in the Control A register (CTRLA.IBON):

If CTRLA.IBON=1, STATUS.BUFOVF is raised immediately upon buffer overflow. Software can then empty the receive FIFO by reading RxDATA until the receiver complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) goes low.

If CTRLA.IBON=0, the Buffer Overflow condition travels with data through the receive FIFO. After the received data is read, STATUS.BUFOVF and INTFLAG.ERROR will be set along with INTFLAG.RXC, and RxDATA will be zero.

30.6.3 Additional Features

30.6.3.1 Address Recognition

When the SPI is configured for client operation (CTRLA.MODE=0x2) with address recognition (CTRLA.FORM is 0x2), the SERCOM address recognition logic is enabled: the first character in a transaction is checked for an address match.

If there is a match, the Receive Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set, the MISO output is enabled, and the transaction is processed. If the device is in Sleep mode, an address match can wake-up the device in order to process the transaction.

If there is no match, the complete transaction is ignored.

If a 9-bit frame format is selected, only the lower 8 bits of the Shift register are checked against the Address register (ADDR).

Preload must be disabled (CTRLB.PLOADEN=0) in order to use this mode.

Related Links

[28.6.3.1. Address Match and Mask](#)

30.6.3.2 Preloading of the Slave Shift Register

When starting a transaction, the slave will first transmit the contents of the shift register before loading new data from DATA. The first character sent can be either the reset value of the shift register (if this is the first transmission since the last reset) or the last character in the previous transmission.

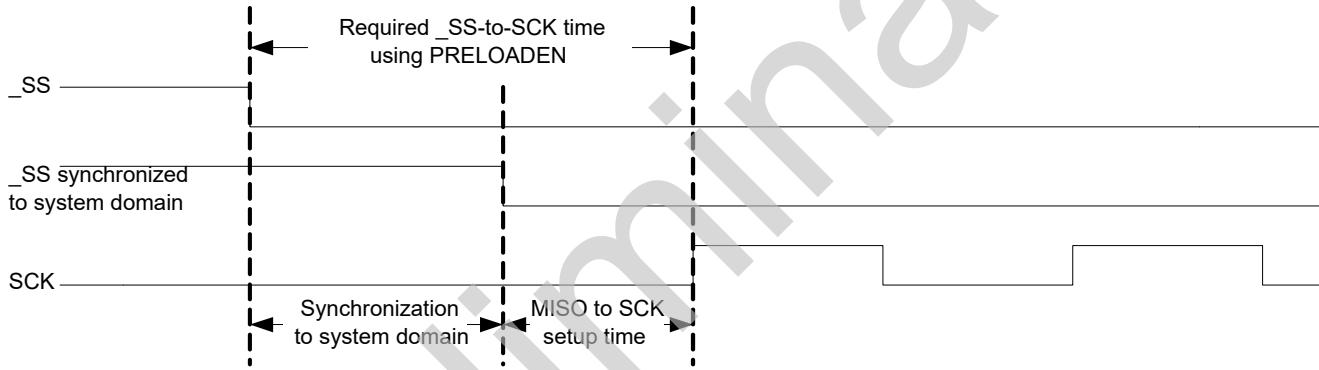
Preloading can be used to preload data into the shift register while \overline{SS} is high: this eliminates sending a dummy character when starting a transaction. If the shift register is not preloaded, the current contents of the shift register will be shifted out.

Only one data character will be preloaded into the shift register while the synchronized \overline{SS} signal is high. If the next character is written to DATA before \overline{SS} is pulled low, the second character will be stored in DATA until transfer begins.

For proper preloading, sufficient time must elapse between \overline{SS} going low and the first SCK sampling edge, as shown in the following figure. For timing details, see Electrical Specifications.

Preloading is enabled by writing ‘1’ to the Slave Data Preload Enable bit in the CTRLB register (CTRLB.PLOADEN).

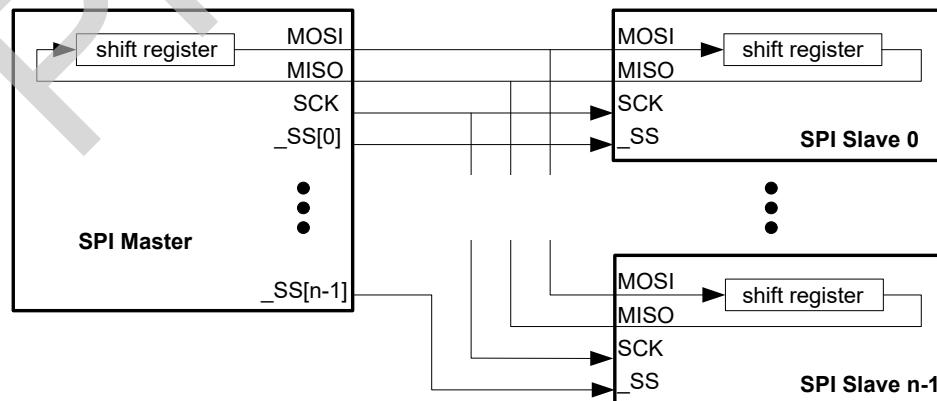
Figure 30-4. Timing Using Preloading



30.6.3.3 Host with Several Clients

Host with multiple clients in parallel is only available when Host SPI Select Enable (CTRLB.MSEN) is set to zero and hardware \overline{SS} control is disabled. If the bus consists of several SPI clients, a SPI host can use general purpose I/O pins to control the \overline{SS} line to each of the clients on the bus, as shown in the following figure. In this configuration, the single selected SPI client will drive the tri-state MISO line.

Figure 30-5. Multiple Clients in Parallel

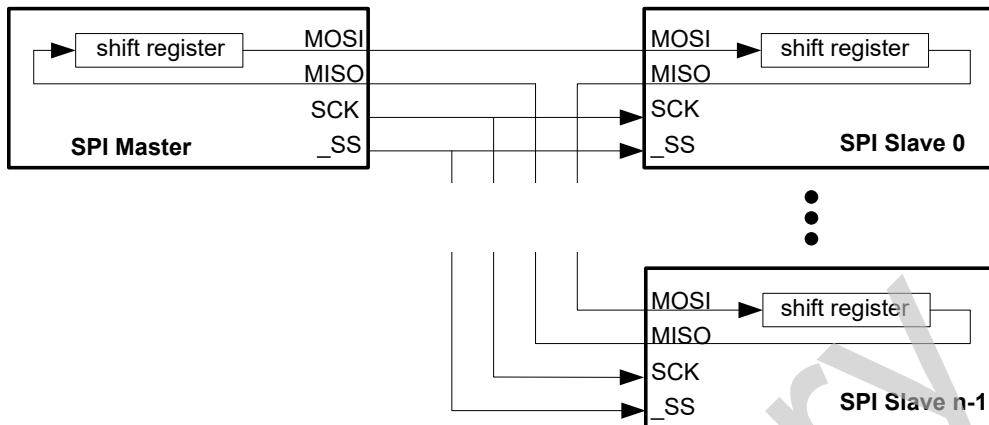


Another configuration is multiple clients in series, as shown in the following figure. In this configuration, all n attached clients are connected in series. A common \overline{SS} line is provided to all clients, enabling them simultaneously. The host

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must shift n characters for a complete transaction. Depending on the Host SPI Select Enable bit (CTRLB.MSSEN), the SS line can be controlled either by hardware or user software and normal GPIO.

Figure 30-6. Multiple Clients in Series



30.6.3.4 Loop-Back Mode

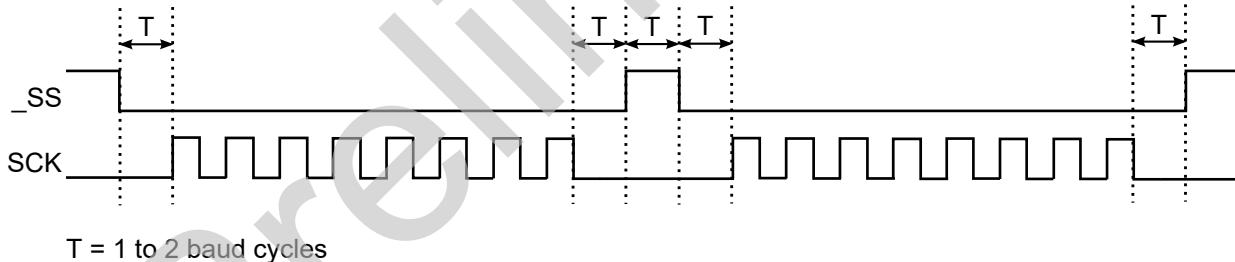
For Loop-back mode, configure the Data In Pinout (CTRLA.DIPO) and Data Out Pinout (CTRLA.DOPO) to use the same data pins for transmit and receive. The loop-back is through the pad, so the signal is also available externally.

30.6.3.5 Hardware Controlled SS

In Host mode, a single SS chip select can be controlled by hardware by writing the Host SPI Select Enable (CTRLB.MSSEN) bit to '1'. In this mode, the SS pin is driven low for a minimum of one baud cycle before transmission begins, and stays low for a minimum of one baud cycle after transmission completes. If back-to-back frames are transmitted, the SS pin will always be driven high for a minimum of one baud cycle between frames.

In [Hardware Controlled SS](#), the time T is between one and two baud cycles depending on the SPI Transfer mode.

Figure 30-7. Hardware Controlled SS



$T = 1 \text{ to } 2 \text{ baud cycles}$

When CTRLB.MSSEN=0, the SS pin(s) is/are controlled by user software and normal GPIO.

30.6.3.6 SPI Select Low Detection

In Client mode, the SPI can wake the CPU when the SPI Select (SS) goes low. When the SPI Select Low Detect is enabled (CTRLB.SSDE=1), a high-to-low transition will set the SPI Select Low Interrupt flag (INTFLAG.SSL) and the device will wake-up if applicable.

30.6.3.7 Master Inter-Character Spacing

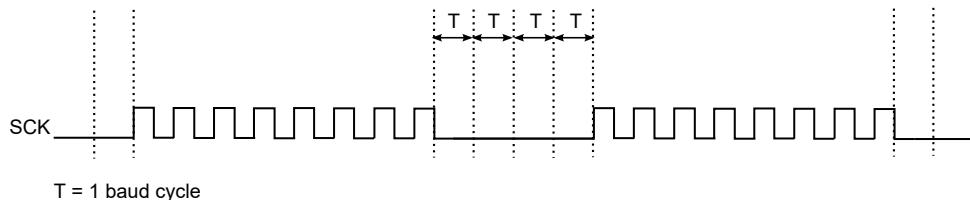
When configured as master, inter-character spacing can be increased by writing a non-zero value to the Inter-Character Spacing bit field in the Control C register (CTRLC.ICSPACE). When non-zero, CTRLC.ICSPACE represents the minimum number of baud cycles that the SCK clock line does not toggle and the next character is stalled.

The figure gives an example for CTRLC.ICSPACE=4; In this case, the SCK is inactive for 4 baud cycles.

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Figure 30-8. Four Cycle Inter-Character Spacing Example



30.6.3.8 32-bit Extension

For better system bus utilization, 32-bit data receive and transmit can be enabled by writing to the Data 32-bit bit field in the Control C register (CTRLC.DATA32B=1). When enabled, write and read transaction to/from the DATA register are 32 bit in size.

If frames are not multiples of 4 Bytes, the Length Counter (LENGTH.LEN) and Length Enable (LENGTH.LENEN) must be configured before data transfer begins. LENGTH.LEN must be enabled only when CTRLC.DATA32B is enabled.

The figure below shows the order of transmit and receive when using 32-bit mode. Bytes are transmitted or received and stored in order from 0 to 3.

Only 8-bit character size is supported.

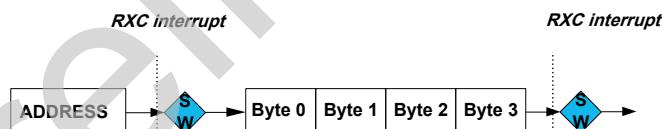
Figure 30-9. 32-bit Extension Byte Ordering



32-bit Extension Slave Operation

The figure below shows a transaction with 32-bit Extension enabled (CTRLC.DATA32B=1). When address recognition is enabled (CTRLA.FORM=0x2) and there is an address match, the address is loaded into the FIFO as Byte zero and data begins with Byte 1. INTFLAGS.RXC will then be raised for every 4 Bytes transferred. For transmit, there is a 32-bit holding buffer in the core domain. Once DATA has been registered in the core domain, INTFLAG.DRE will be raised, so that the next 32 bits can be written to the DATA register.

Figure 30-10. 32-bit Extension Slave Operation



When utilizing the length counter, the LENGTH register must be written before the frame begins. If the frame length while \overline{SS} is low is not a multiple of LENGTH.LEN Bytes, the Length Error Status bit (STATUS.LENERR) is raised. If LENGTH.LEN is not a multiple of 4 Bytes, the final INTFLAG.RXC interrupt will be raised when the last Byte is received.

The length count is based on the received Bytes, or the number of clocks if the receiver is not enabled. If pre-loading is disabled and DATA is written to for transmit before SCK starts, transmitted data will be delayed by one Byte, but the length counter will still increment for the first (empty) Byte transmission. When the counter reaches LENGTH.LEN, the internal length counter, Rx Byte counter, and Tx Byte counter are reset. If multiple lengths are to be transmitted, INTFLAG.TXC must go high before writing DATA for subsequent lengths.

If there is a Length Error (STATUS.LENERR), the remaining Bytes in the length will be transmitted at the beginning of the next frame. If this is not desired, the SERCOM must be disabled and re-enabled in order to flush the Tx and Rx pipelines.

Writing the LENGTH register while a frame is in progress will produce unpredictable results. If LENGTH.LENEN is not configured and a frame is not a multiple of 4 Bytes (while \overline{SS} is low), the remainder will be transmitted in the next frame.

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32-bit Extension Master Operation

When using the SPI configured as Master, the Length and the Length Enable bit fields (LENGTH.LEN and LENGTH.LENEN) must be written before the frame begins. When LENGTH.LENEN is written to '1', the value of LENGTH.LEN determines the number of data bytes in the transaction from 1 to 255.

For receive data, INTFLAG.RXC is raised every 4 Bytes received. If LENGTH.LEN is not a multiple of 4 Bytes, the final INTFLAG.RXC is set when the final byte is received.

For transmit, there is a holding buffer for the 32-bit data in the core domain. Once DATA has been registered in the core domain, INTFLAG.DRE will be raised so that the next 32 bits can be written to the DATA register.

If multiple lengths are to be transmitted, INTFLAG.TXC must go high before writing DATA for subsequent lengths.

30.6.4 DMA, Interrupts, and Events

Table 30-4. Module Request for SERCOM SPI

Condition	Request		
		Interrupt	Event
Data Register Empty (DRE)	Yes (request cleared when data is written)	Yes	NA
Receive Complete (RXC)	Yes (request cleared when data is read)	Yes	
Transmit Complete (TXC)	NA	Yes	
Slave Select low (SSL)	NA	Yes	
Error (ERROR)	NA	Yes	

30.6.4.1 DMA Operation

The SPI generates the following DMA requests:

- Data received (RX): The request is set when data is available in the receive FIFO. The request is cleared when DATA is read.
- Data transmit (TX): The request is set when the transmit buffer (TX DATA) is empty. The request is cleared when DATA is written.

30.6.4.2 Interrupts

The SPI has the following interrupt sources. These are asynchronous interrupts, and can wake-up the device from any Sleep mode:

- Data Register Empty (DRE)
- Receive Complete (RXC)
- Transmit Complete (TXC)
- Slave Select Low (SSL)
- Error (ERROR)

Each interrupt source has its own Interrupt flag. The Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the Interrupt condition is met. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and if the corresponding interrupt is enabled. The interrupt request remains active until either the Interrupt flag is cleared, the interrupt is disabled, or the SPI is reset. For details on clearing Interrupt flags, see INTFLAG register description.

The value of INTFLAG indicates which interrupt is executed. Note that interrupts must be globally enabled for interrupt requests. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

30.6.4.3 Events

Not applicable.

30.6.5 Sleep Mode Operation

The behavior in Sleep mode is depending on the host/client configuration and the Run In Standby bit in the Control A register (CTRLA.RUNSTDBY):

- Host operation, CTRLA.RUNSTDBY=1: The peripheral clock GCLK_SERCOMx_CORE will continue to run in Idle Sleep mode and in Standby Sleep mode. Any interrupt can wake-up the device.
- Host operation, CTRLA.RUNSTDBY=0: GLK_SERCOMx_CORE will be disabled after the ongoing transaction is finished. Any interrupt can wake up the device.
- Client operation, CTRLA.RUNSTDBY=1: The Receive Complete interrupt can wake-up the device.
- Client operation, CTRLA.RUNSTDBY=0: All reception will be dropped, including the ongoing transaction.

30.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in the CTRLA register (CTRLA.SWRST)
- Enable bit in the CTRLA register (CTRLA.ENABLE)
- Receiver Enable bit in the CTRLB register (CTRLB.RXEN)

Note: CTRLB.RXEN is write-synchronized somewhat differently. See *CTRLB* register from Related Links.

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

[30.8.2. CTRLB](#)

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30.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
		15:8								IBON
		23:16			DIPO[1:0]					DOPO[1:0]
		31:24		DORD	CPOL	CPHA		FORM[3:0]		
0x04	CTRLB	7:0		PLOADEN					CHSIZE[2:0]	
		15:8	AMODE[1:0]		MSSEN				SSDE	
		23:16							RXEN	
		31:24					ICSPACE[5:0]			
0x08	CTRLC	7:0								
		15:8								
		23:16								
		31:24								DATA32B
0x0C	BAUD	7:0				BAUD[7:0]				
0x0D	Reserved									
0x13										
0x14	INTENCLR	7:0	ERROR				SSL	RXC	TXC	DRE
0x15	Reserved									
0x16	INTENSET	7:0	ERROR				SSL	RXC	TXC	DRE
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR				SSL	RXC	TXC	DRE
0x19	Reserved									
0x1A	STATUS	7:0						BUFOVF		
0x1B		15:8					LENERR			
0x1C	SYNCBUSY	7:0			LENGTH			CTRLB	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20	Reserved									
0x21										
0x22	LENGTH	7:0				LEN[7:0]				
0x23		15:8								LENEN
0x24	ADDR	7:0				ADDR[7:0]				
		15:8								
		23:16				ADDRMASK[7:0]				
		31:24								
0x28	DATA	7:0				DATA[7:0]				
		15:8				DATA[15:8]				
		23:16				DATA[23:16]				
		31:24				DATA[31:24]				
0x2C	Reserved									
0x2F										
0x30	DBGCTRL	7:0								DBGSTOP

30.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

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Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

See *Peripheral Access Controller (PAC)* from Related Links.

Related Links

[25. Peripheral Access Controller \(PAC\)](#)

Preliminary

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30.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		DORD	CPOL	CPHA			FORM[3:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
			DIPO[1:0]				DOPO[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0
Bit	15	14	13	12	11	10	9	8
								IBON
Access								R/W
Reset								0
Bit	7	6	5	4	3	2	1	0
	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – DORD Data Order

This bit selects the data order when a character is shifted out from the shift register.
This bit is not synchronized.

Value	Description
0	MSB is transferred first.
1	LSB is transferred first.

Bit 29 – CPOL Clock Polarity

In combination with the Clock Phase bit (CPHA), this bit determines the SPI transfer mode.
This bit is not synchronized.

Value	Description
0	SCK is low when idle. The leading edge of a clock cycle is a rising edge, while the trailing edge is a falling edge.
1	SCK is high when idle. The leading edge of a clock cycle is a falling edge, while the trailing edge is a rising edge.

Bit 28 – CPHA Clock Phase

In combination with the Clock Polarity bit (CPOL), this bit determines the SPI transfer mode.
This bit is not synchronized.

Mode	CPOL	CPHA	Leading Edge	Trailing Edge
0x0	0	0	Rising, sample	Falling, change
0x1	0	1	Rising, change	Falling, sample
0x2	1	0	Falling, sample	Rising, change
0x3	1	1	Falling, change	Rising, sample

Value	Description
0	The data is sampled on a leading SCK edge and changed on a trailing SCK edge.
1	The data is sampled on a trailing SCK edge and changed on a leading SCK edge.

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Bits 27:24 – FORM[3:0] Frame Format

This bit field selects the various frame formats supported by the SPI in client mode. When the 'SPI frame with address' format is selected, the first byte received is checked against the ADDR register.

FORM[3:0]	Name	Description
0x0	SPI	SPI frame
0x1	-	Reserved
0x2	SPI_ADDR	SPI frame with address
0x3-0xF	-	Reserved

Bits 21:20 – DIPO[1:0] Data In Pinout

These bits define the data in (DI) pad configurations.

In host operation, DI is MISO.

In client operation, DI is MOSI.

These bits are not synchronized.

DIPO[1:0]	Name	Description
0x0	PAD[0]	SERCOM PAD[0] is used as data input
0x1	PAD[1]	SERCOM PAD[1] is used as data input
0x2	PAD[2]	SERCOM PAD[2] is used as data input
0x3	PAD[3]	SERCOM PAD[3] is used as data input

Bits 17:16 – DOPO[1:0] Data Out Pinout

This bit defines the available pad configurations for data out (DO), the serial clock (SCK) and the SPI Select (\overline{SS}). In Client operation, the SPI Select line (\overline{SS}) is controlled by DOPO. In host operation, the SPI Select line (\overline{SS}) is either controlled by DOPO when CTRLB.MSEN = 1, or by a GPIO driven by the application when CTRLB.MSEN = 0.

In host operation, DO is MOSI.

In client operation, DO is MISO.

These bits are not synchronized.

DOPO	DO	SCK	Client \overline{SS}	Host \overline{SS} (MSEN = 1)	Host \overline{SS} (MSEN = 0)
0x0	PAD[0]	PAD[1]	PAD[2]	PAD[2]	Any GPIO configured by the application
0x1				Reserved	
0x2	PAD[3]	PAD[1]	PAD[2]	PAD[2]	Any GPIO configured by the application
0x3				Reserved	

Bit 8 – IBON Immediate Buffer Overflow Notification

This bit controls when the Buffer Overflow Status bit (STATUS.BUFOVF) is set when a buffer overflow occurs.

This bit is not synchronized.

Value	Description
0	STATUS.BUFOVF is set when it occurs in the data stream.
1	STATUS.BUFOVF is set immediately upon buffer overflow.

Bit 7 – RUNSTDBY Run In Standby

This bit defines the functionality in Standby mode.

These bits are not synchronized.

RUNSTDBY	Client	Host
0x0	Disabled. All reception is dropped, including the ongoing transaction.	Generic clock is disabled when ongoing transaction is finished. All interrupts can wake up the device.
0x1	Ongoing transaction continues, wake on Receive Complete interrupt.	Generic clock is enabled while in sleep modes. All interrupts can wake up the device.

Bits 4:2 – MODE[2:0] Operating Mode

These bits must be written to 0x2 or 0x3 to select the SPI serial communication interface of the SERCOM.

0x2: SPI client operation

0x3: SPI host operation

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These bits are not synchronized.

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing "1" to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

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30.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access							R/W	
Reset							0	
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W				R/W	
Reset	0	0	0				0	
Bit	7	6	5	4	3	2	1	0
Access		PLOADEN					CHSIZE[2:0]	
Reset		R/W				R/W	R/W	R/W
		0				0	0	0

Bit 17 – RXEN Receiver Enable

Writing '0' to this bit will disable the SPI receiver immediately. The receive buffer will be flushed, data from ongoing receptions will be lost and STATUS.BUFOVF will be cleared.

Writing '1' to CTRLB.RXEN when the SPI is disabled will set CTRLB.RXEN immediately. When the SPI is enabled, CTRLB.RXEN will be cleared, SYNCBUSY.CTRLB will be set and remain set until the receiver is enabled. When the receiver is enabled CTRLB.RXEN will read back as '1'.

Writing '1' to CTRLB.RXEN when the SPI is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.RXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The receiver is disabled.
1	The receiver is enabled or it will be enabled when SPI is enabled.

Bits 15:14 – AMODE[1:0] Address Mode

These bits set the Slave Addressing mode when the frame format (CTRLA.FORM) with address is used. They are unused in Master mode.

These bits are not synchronized.

AMODE[1:0]	Name	Description
0x0	MASK	ADDRMASK is used as a mask to the ADDR register
0x1	2_ADDRS	The slave responds to the two unique addresses in ADDR and ADDRMASK
0x2	RANGE	The slave responds to the range of addresses between and including ADDR and ADDRMASK. ADDR is the upper limit
0x3	-	Reserved

Bit 13 – MSSEN Master Slave Select Enable

This bit enables hardware Slave Select (SS) control.

This bit is not synchronized.

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Value	Description
0	Hardware SS control is disabled.
1	Hardware \bar{SS} control is enabled.

Bit 9 – SSDE Slave Select Low Detect Enable

This bit enables wake-up when the Slave Select (\bar{SS}) pin transitions from high-to-low.

This bit is not synchronized.

Value	Description
0	SS low detector is disabled.
1	\bar{SS} low detector is enabled.

Bit 6 – PLOADEN Slave Data Preload Enable

Setting this bit will enable preloading of the Slave Shift register when there is no transfer in progress. If the \bar{SS} line is high when DATA is written, it will be transferred immediately to the Shift register.

This bit is not synchronized.

Bits 2:0 – CHSIZE[2:0] Character Size

These bits are not synchronized.

CHSIZE[2:0]	Name	Description
0x0	8BIT	8 bits
0x1	9BIT	9 bits
0x2-0x7	-	Reserved

30.8.3 Control C

Name: CTRLC
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24	
									DATA32B
Access									R/W
Reset									0
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	3	2	1	0	
									ICSPACE[5:0]
Access			R/W	R/W	R/W	R/W	R/W	R/W	
Reset			0	0	0	0	0	0	

Bit 24 – DATA32B Data 32 Bit

This bit enables 32-bit Extension for read and write transactions to the DATA register.
When disabled, access is according to CTRLB.CHSIZE.

Value	Description
0	Transactions from and to DATA register are 8-bit
1	Transactions from and to DATA register are 32-bit

Bits 5:0 – ICSPACE[5:0] Inter-Character Spacing

When non-zero, CTRLC.ICSPACE selects the minimum number of baud cycles the SCK line will not toggle between characters.

Value	Description
0x00	Inter-Character Spacing is disabled
0x01–0x3F	The minimum Inter-Character Spacing

30.8.4 Baud Rate

Name: BAUD
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
BAUD[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BAUD[7:0] Baud Register

These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator*.

30.8.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 3 – SSL Slave Select Low Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Slave Select Low Interrupt Enable bit, which disables the Slave Select Low interrupt.

Value	Description
0	Slave Select Low interrupt is disabled.
1	Slave Select Low interrupt is enabled.

Bit 2 – RXC Receive Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Complete Interrupt Enable bit, which disables the Receive Complete interrupt.

Value	Description
0	Receive Complete interrupt is disabled.
1	Receive Complete interrupt is enabled.

Bit 1 – TXC Transmit Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Transmit Complete Interrupt Enable bit, which disable the Transmit Complete interrupt.

Value	Description
0	Transmit Complete interrupt is disabled.
1	Transmit Complete interrupt is enabled.

Bit 0 – DRE Data Register Empty Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Register Empty Interrupt Enable bit, which disables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

30.8.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 3 – SSL Slave Select Low Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Slave Select Low Interrupt Enable bit, which enables the Slave Select Low interrupt.

Value	Description
0	Slave Select Low interrupt is disabled.
1	Slave Select Low interrupt is enabled.

Bit 2 – RXC Receive Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Receive Complete Interrupt Enable bit, which enables the Receive Complete interrupt.

Value	Description
0	Receive Complete interrupt is disabled.
1	Receive Complete interrupt is enabled.

Bit 1 – TXC Transmit Complete Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Transmit Complete Interrupt Enable bit, which enables the Transmit Complete interrupt.

Value	Description
0	Transmit Complete interrupt is disabled.
1	Transmit Complete interrupt is enabled.

Bit 0 – DRE Data Register Empty Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Register Empty Interrupt Enable bit, which enables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

30.8.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R	R/W	R
Reset	0				0	0	0	0

Bit 7 – ERROR Error

This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding Status flags in the STATUS register. The BUFOVF error and the LENERR error will set this Interrupt flag.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – SSL SPI Select Low

This flag is cleared by writing '1' to it.

This bit is set when a high to low transition is detected on the SS pin in Client mode and SPI Select Low Detect (CTRLB.SSDE) is enabled.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 2 – RXC Receive Complete

This flag is cleared by reading the Data (DATA) register or by disabling the receiver.

This flag is set when there are unread data in the receive buffer. If address matching is enabled, the first data received in a transaction will be an address.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 1 – TXC Transmit Complete

This flag is cleared by writing '1' to it or by writing new data to DATA.

In Host mode, this flag is set when the data have been shifted out and there are no new data in DATA.

In Client mode, this flag is set when the SS pin is pulled high. If address matching is enabled, this flag is only set if the transaction was initiated with an address match.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 0 – DRE Data Register Empty

This flag is cleared by writing new data to DATA.

This flag is set when DATA is empty and ready for new data to transmit.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

30.8.8 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: –

Bit	15	14	13	12	11	10	9	8
Access					LENERR			
Reset					R/W			
					0			
Bit	7	6	5	4	3	2	1	0
Access					BUFOVF			
Reset					R/W			
					0			

Bit 11 – LENERR Transaction Length Error

This bit is set in slave mode when the length counter is enabled (LENGTH.LENEN=1) and the transfer length while SS is low is not a multiple of LENGTH.LEN.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Length Error has occurred.
1	A Length Error has occurred.

Bit 2 – BUFOVF Buffer Overflow

Reading this bit before reading DATA will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a Buffer Overflow condition is detected. See CTRLA from Related Links for overflow handling. When set, the corresponding RxDATA will be zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Buffer Overflow has occurred.
1	A Buffer Overflow has occurred.

Related Links

[30.8.1. CTRLA](#)

30.8.9 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access				R		R	R	R
Reset				0		0	0	0

Bit 4 – LENGTH LENGTH Synchronization Busy

Writing to the LENGTH register requires synchronization. When writing to LENGTH, SYNCBUSY.LENGTH will be set until synchronization is complete. If the LENGTH register is written to while SYNCBUSY.LENGTH is asserted, an APB error is generated.

Note: In slave mode, the clock is only running during data transfer, so SYNCBUSY.LENGTH will remain asserted until the next data transfer begins.

Value	Description
0	LENGTH synchronization is not busy.
1	LENGTH synchronization is busy.

Bit 2 – CTRLB CTRLB Synchronization Busy

Writing to the CTRLB when the SERCOM is enabled requires synchronization. Ongoing synchronization is indicated by SYNCBUSY.CTRLB=1 until synchronization is complete. If CTRLB is written while SYNCBUSY.CTRLB=1, an APB error will be generated.

Value	Description
0	CTRLB synchronization is not busy.
1	CTRLB synchronization is busy.

Bit 1 – ENABLE SERCOM Enable Synchronization Busy

Enabling and disabling the SERCOM (CTRLA.ENABLE) requires synchronization. Ongoing synchronization is indicated by SYNCBUSY.ENABLE=1 until synchronization is complete.

Value	Description
0	Enable synchronization is not busy.
1	Enable synchronization is busy.

Bit 0 – SWRST Software Reset Synchronization Busy

Resetting the SERCOM (CTRLA.SWRST) requires synchronization. Ongoing synchronization is indicated by SYNCBUSY.SWRST=1 until synchronization is complete.

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Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

Preliminary

30.8.10 Length

Name: LENGTH
Offset: 0x22
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
Access								LENEN
Reset								0
Bit	7	6	5	4	3	2	1	0
	LEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 8 – LENEN Data Length Enable

In 32-bit Extension mode, this bit field enables the length counter.

Value	Description
0	Length counter disabled
1	Length counter enabled

Bits 7:0 – LEN[7:0] Data Length

In 32-bit Extension mode, this bit field configures the data length after which the flags INTFLAG.RCX or INTFLAG.DRE are raised.

Value	Description
0x00	Reserved if LENEN=0x1
0x01-0xF	Data Length
F	

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30.8.11 Address

Name: ADDR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	ADDRMASK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – ADDRMASK[7:0] Address Mask

These bits hold the address mask when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

Bits 7:0 – ADDR[7:0] Address

These bits hold the address when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

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30.8.12 Data

Name: DATA
Offset: 0x28
Reset: 0x0000
Property: –

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data

Reading these bits will return the contents of the receive data buffer. The register should be read only when the Receive Complete Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set.

Writing these bits will write the transmit data buffer. This register should be written only when the Data Register Empty Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is set.

Reads and writes are 32-bit or CTLB.CHSIZE based on the CTRLC.DATA32B setting.

30.8.13 Debug Control

Name: DBGCTRL
Offset: 0x30
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGSTOP 0

Bit 0 – DBGSTOP Debug Stop Mode

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.

31. SERCOM I²C – Inter-Integrated Circuit

31.1 Overview

The inter-integrated circuit (I²C) interface is one of the available modes in the serial communication interface (SERCOM).

The I²C interface uses the SERCOM transmitter and receiver configured as shown in [Figure 31-1](#). Labels in capital letters are registers accessible by the CPU, while lowercase labels are internal to the SERCOM.

A SERCOM instance can be configured to be either an I²C host or an I²C client. Both host and client have an interface containing a shift register, a transmit buffer and a receive buffer. In addition, the I²C host uses the SERCOM baud-rate generator, while the I²C client uses the SERCOM address match logic.

Related Links

[28. SERCOM – Serial Communication Interface](#)

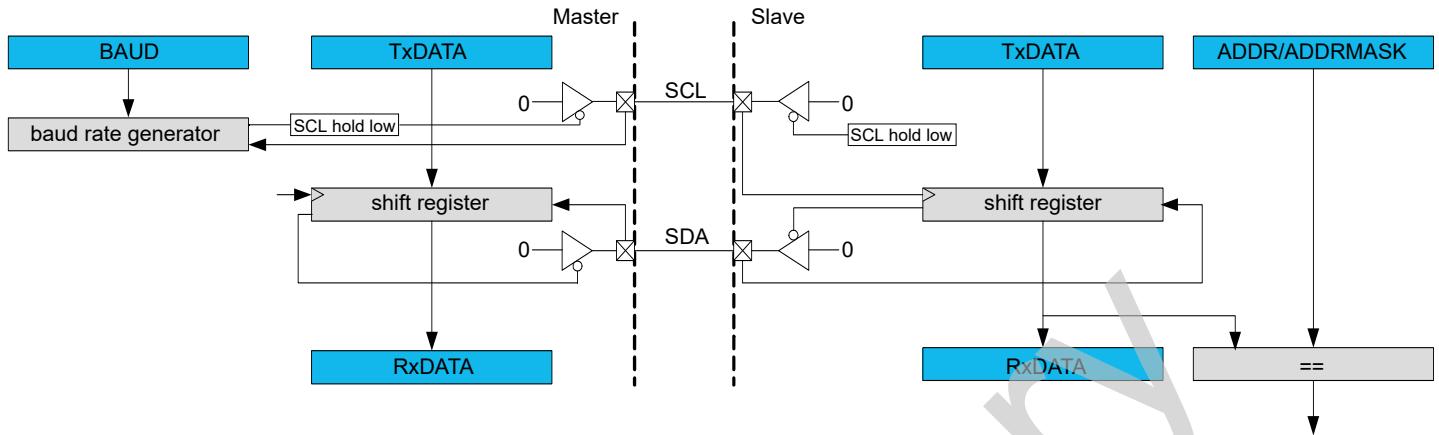
31.2 Features

SERCOM I²C includes the following features:

- Master or Slave Operation
- Can be used with DMA
- Philips I²C Compatible
- SMBus Compatible
- PMBus™ Compatible
- Support of 100 kHz and 400 kHz, 1 MHz I²C mode
- 32-bit Data Extension for better system bus utilization
- 4-Wire Operation Supported
- Physical interface includes:
 - Slew-rate limited outputs
 - Filtered inputs
- Slave Operation:
 - Operation in all Sleep modes
 - Wake-up on address match
 - 7-bit Address match in hardware for:
 - Unique address and/or 7-bit general call address
 - Address range
 - Two unique addresses can be used with DMA

31.3 Block Diagram

Figure 31-1. I²C Single-Master Single-Slave Interconnection



31.4 Signal Description

Signal Name	Type	Description
PAD[0]	Digital I/O	SDA
PAD[1]	Digital I/O	SCL
PAD[2]	Digital I/O	SDA_OUT (4-wire operation)
PAD[3]	Digital I/O	SCL_OUT (4-wire operation)

One signal can be mapped on several pins.

Not all the pins are I²C pins.

Related Links

[31.6.3.3. 4-Wire Mode](#)

31.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

31.5.1 I/O Lines

In order to use the SERCOM's I/O lines, the I/O pins must be configured using the System Configuration registers only. I²C does not operate through PPS. See DEVCFG1 configuration bits SCOMn_HSEN in Configuration Bits Fuses and also CFGCON1 SCOMn_HSEN in CFGCON1(L) register. See *CFGCON1(L)* register from Related Links.

When the SERCOM is used in I²C mode, the SERCOM controls the direction and value of the I/O pins. In I²C mode pull-up resistors are disabled. External pull-up resistors are required for proper function.

Related Links

[17.4.2. CFGCON1\(L\)](#)

31.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake-up the device from Sleep modes.

31.5.3 Clocks

Two generic clocks are used by SERCOM, GCLK_SERCOMx_CORE and GCLK_SERCOMx_SLOW. The core clock (GCLK_SERCOMx_CORE) can clock the I²C when working as a master. The slow clock (GCLK_SERCOMx_SLOW) is required only for certain functions, e.g. SMBus timing. These two clocks must be configured and enabled in the CRU registers before using the I²C.

These generic clocks are asynchronous to the bus clock (PBx_CLK). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains.

31.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

[21. Direct Memory Access Controller \(DMAC\)](#)

31.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

31.5.6 Events

Not applicable.

31.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

31.5.8 Register Access Protection

Registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC).

PAC write protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)
- Address register (ADDR)

Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

31.5.9 Analog Connections

Not applicable.

31.6 Functional Description

31.6.1 Principle of Operation

The I²C interface uses two physical lines for communication:

- Serial Data Line (SDA) for data transfer
- Serial Clock Line (SCL) for the bus clock

A transaction starts with the I²C master sending the Start condition, followed by a 7-bit address and a direction bit (read or write to/from the slave).

The addressed I²C slave will then Acknowledge (ACK) the address, and data packet transactions can begin. Every 9-bit data packet consists of 8 data bits followed by a one-bit reply indicating whether the data was acknowledged or not.

If a data packet is Not Acknowledged (NACK), whether by the I²C slave or master, the I²C master takes action by either terminating the transaction by sending the Stop condition, or by sending a repeated start to transfer more data.

The figure below illustrates the possible transaction formats and [Transaction Diagram Symbols](#) explains the transaction symbols. These symbols will be used in the following descriptions.

Figure 31-2. Transaction Diagram Symbols

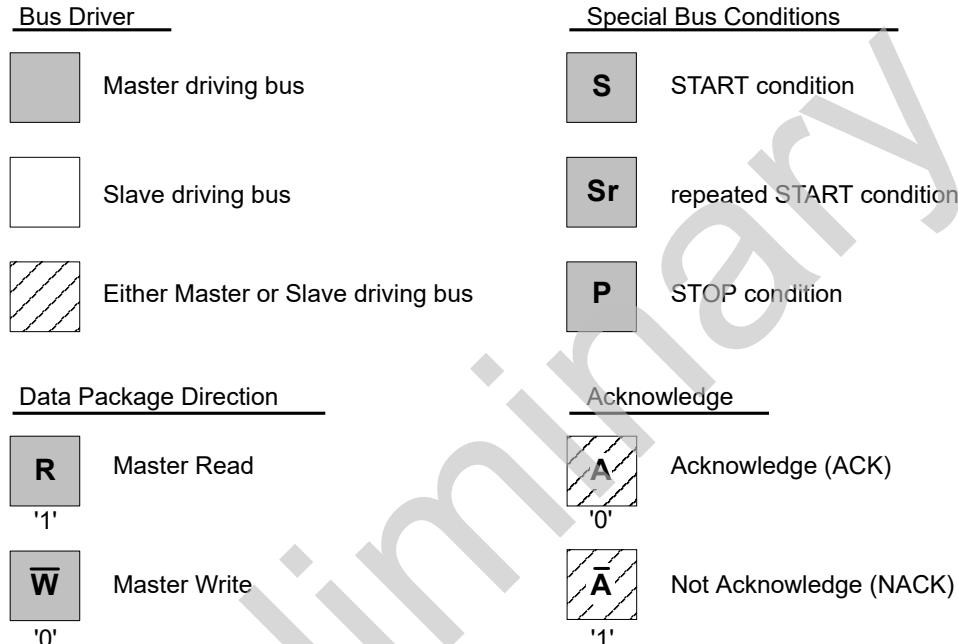
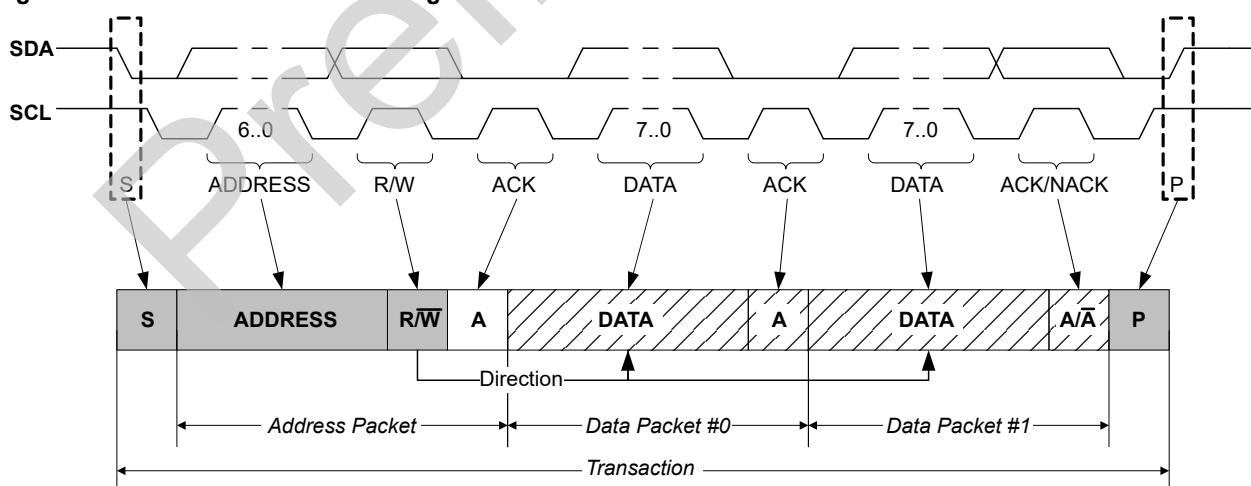


Figure 31-3. Basic I²C Transaction Diagram



31.6.2 Basic Operation

31.6.2.1 Initialization

The following registers are enable-protected, meaning they can be written only when the I²C interface is disabled (CTRLA.ENABLE is '0'):

- Control A register (CTRLA), except Enable (CTRLA.ENABLE) and Software Reset (CTRLA.SWRST) bits
- Control B register (CTRLB), except Acknowledge Action (CTRLB.ACKACT) and Command (CTRLB.CMD) bits
- Baud register (BAUD) in master operation
- Address register (ADDR) in slave operation

When the I²C is enabled or is being enabled (CTRLA.ENABLE=1), writing to these registers will be discarded. If the I²C is being disabled, writing to these registers will be completed after the disabling.

Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the I²C is enabled it must be configured as outlined by the following steps:

1. Select I²C Master or Slave mode by writing 0x4 (Slave mode) or 0x5 (Master mode) to the Operating Mode bits in the CTRLA register (CTRLA.MODE).
2. If desired, select the SDA Hold Time value in the CTRLA register (CTRLA.SDAHOLD).
3. In Slave mode, the minimum slave setup time for the SDA can be selected in the SDA Setup Time bit group in the Control C register (CTRLC.SDASETUP).
4. If desired, enable smart operation by setting the Smart Mode Enable bit in the CTRLB register (CTRLB.SMEN).
5. If desired, enable SCL low time-out by setting the SCL Low Time-Out bit in the Control A register (CTRLA.LOWTOUT).
6. In Master mode:
 - a. Select the inactive bus time-out in the Inactive Time-Out bit group in the CTRLA register (CTRLA.INACTOUT).
 - b. Write the Baud Rate register (BAUD) to generate the desired baud rate.

In Slave mode:

- a. Configure the address match configuration by writing the Address Mode value in the CTRLB register (CTRLB.AMODE).
- b. Set the Address and Address Mask value in the Address register (ADDR.ADDR and ADDR.ADDRMASK) according to the address configuration.

31.6.2.2 Enabling, Disabling, and Resetting

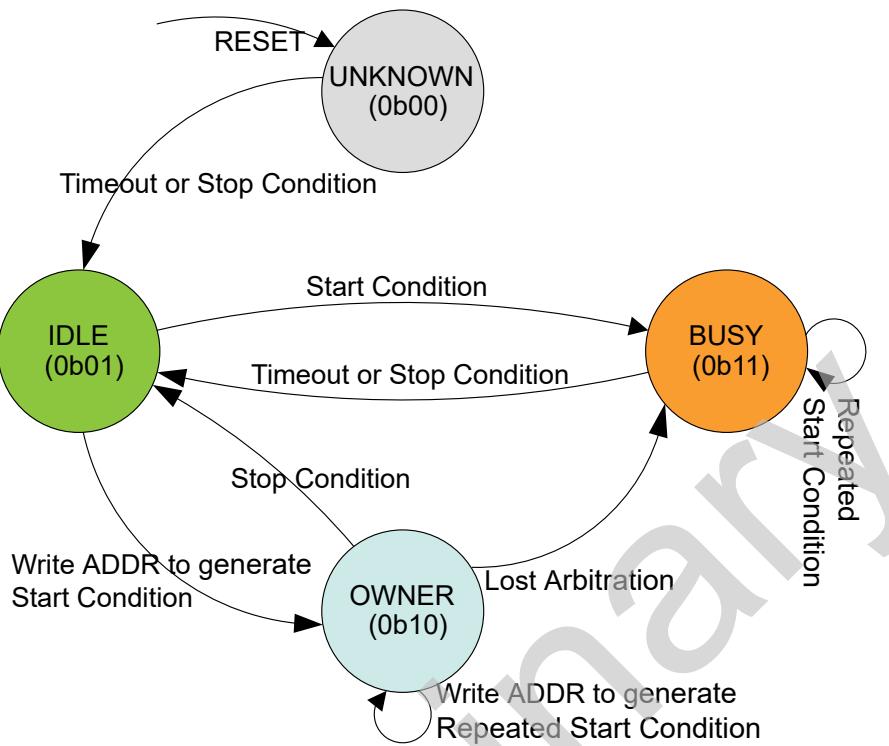
This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

31.6.2.3 I²C Bus State Logic

The Bus state logic includes several logic blocks that continuously monitor the activity on the I²C bus lines in all Sleep modes with running GCLK_SERCOM_x clocks. The start and stop detectors and the bit counter are all essential in the process of determining the current Bus state. The Bus state is determined according to [Bus State Diagram](#). Software can get the current Bus state by reading the Master Bus State bits in the Status register (STATUS.BUSSTATE). The value of STATUS.BUSSTATE in the figure is shown in binary.

Figure 31-4. Bus State Diagram



The Bus state machine is active when the I²C master is enabled.

After the I²C master has been enabled, the Bus state is UNKNOWN (0b00). From the UNKNOWN state, the bus will transition to IDLE (0b01) by either:

- Forcing by writing 0b01 to STATUS.BUSSTATE
- A Stop condition is detected on the bus
- If the inactive bus time-out is configured for SMBus compatibility (CTRLA.INACTOUT) and a time-out occurs.

Note: Once a known Bus state is established, the Bus state logic will not re-enter the UNKNOWN state.

When the bus is IDLE it is ready for a new transaction. If a Start condition is issued on the bus by another I²C master in a multi-master setup, the bus becomes BUSY (0b11). The bus will re-enter IDLE either when a Stop condition is detected, or when a time-out occurs (inactive bus time-out needs to be configured).

If a Start condition is generated internally by writing the Address bit group in the Address register (ADDR.ADDR) while IDLE, the OWNER state (0b10) is entered. If the complete transaction was performed without interference, i.e., arbitration was not lost, the I²C master can issue a Stop condition, which will change the Bus state back to IDLE.

However, if a packet collision is detected while in OWNER state, the arbitration is assumed lost and the Bus state becomes BUSY until a Stop condition is detected. A repeated Start condition will change the Bus state only if arbitration is lost while issuing a repeated start.

Note: Violating the protocol may cause the I²C to hang. If this happens it is possible to recover from this state by a software Reset (CTRLA.SWRST='1').

31.6.2.4 I²C Master Operation

The I²C master is byte-oriented and interrupt based. The number of interrupts generated is kept at a minimum by automatic handling of most incidents. The software driver complexity and code size are reduced by auto-triggering of operations, and a Special Smart mode, which can be enabled by the Smart Mode Enable bit in the Control A register (CTRLA.SMEN).

The I²C master has two interrupt strategies.

When SCL Stretch Mode (CTRLA.SCLSM) is '0', SCL is stretched before or after the Acknowledge bit. In this mode the I²C master operates according to *I²C Master Behavioral Diagram (SCLSM=0)* as shown in the following figure.

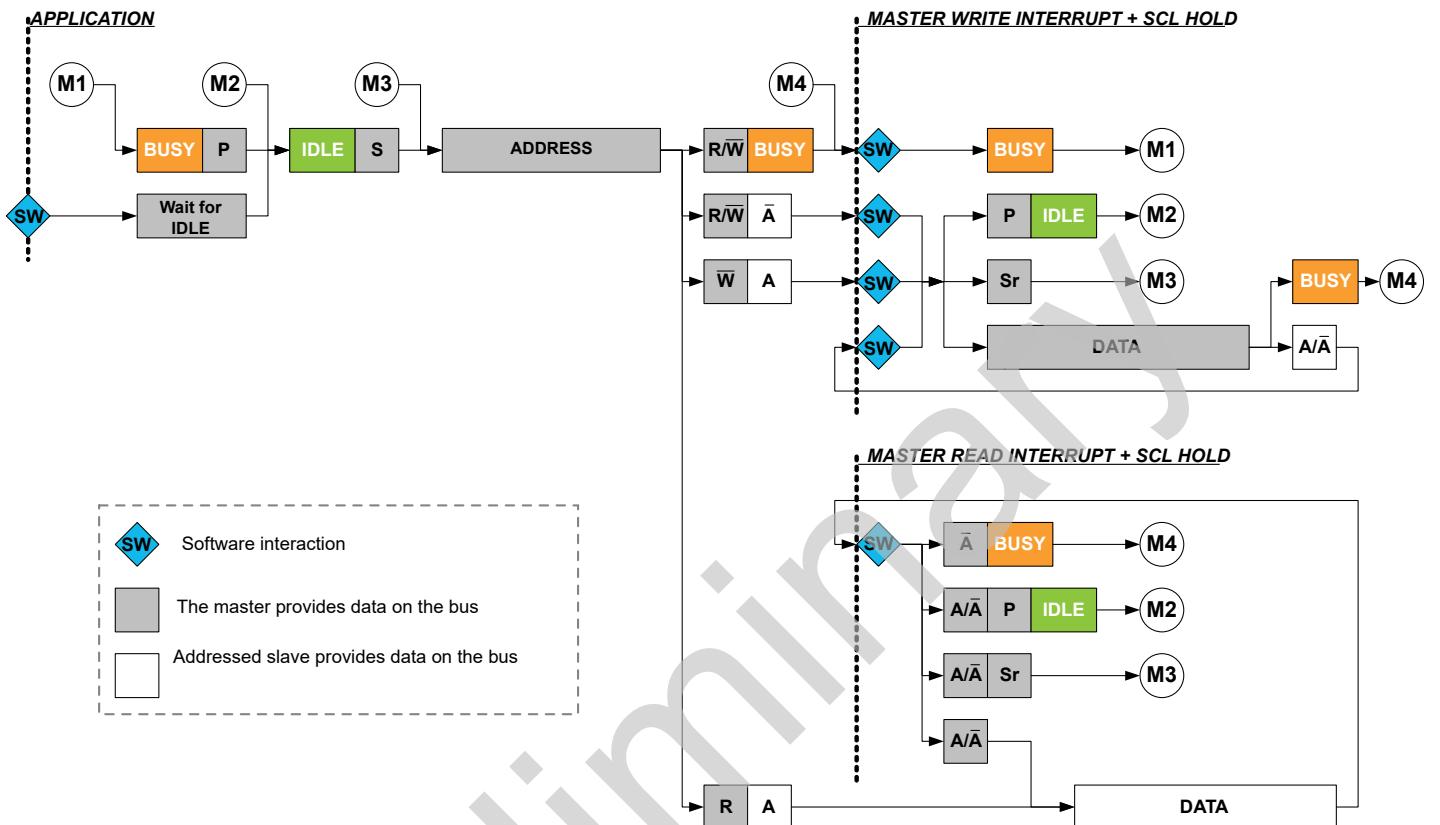
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The circles labeled "Mn" (M1, M2..) indicate the nodes the bus logic can jump to, based on software or hardware interaction.

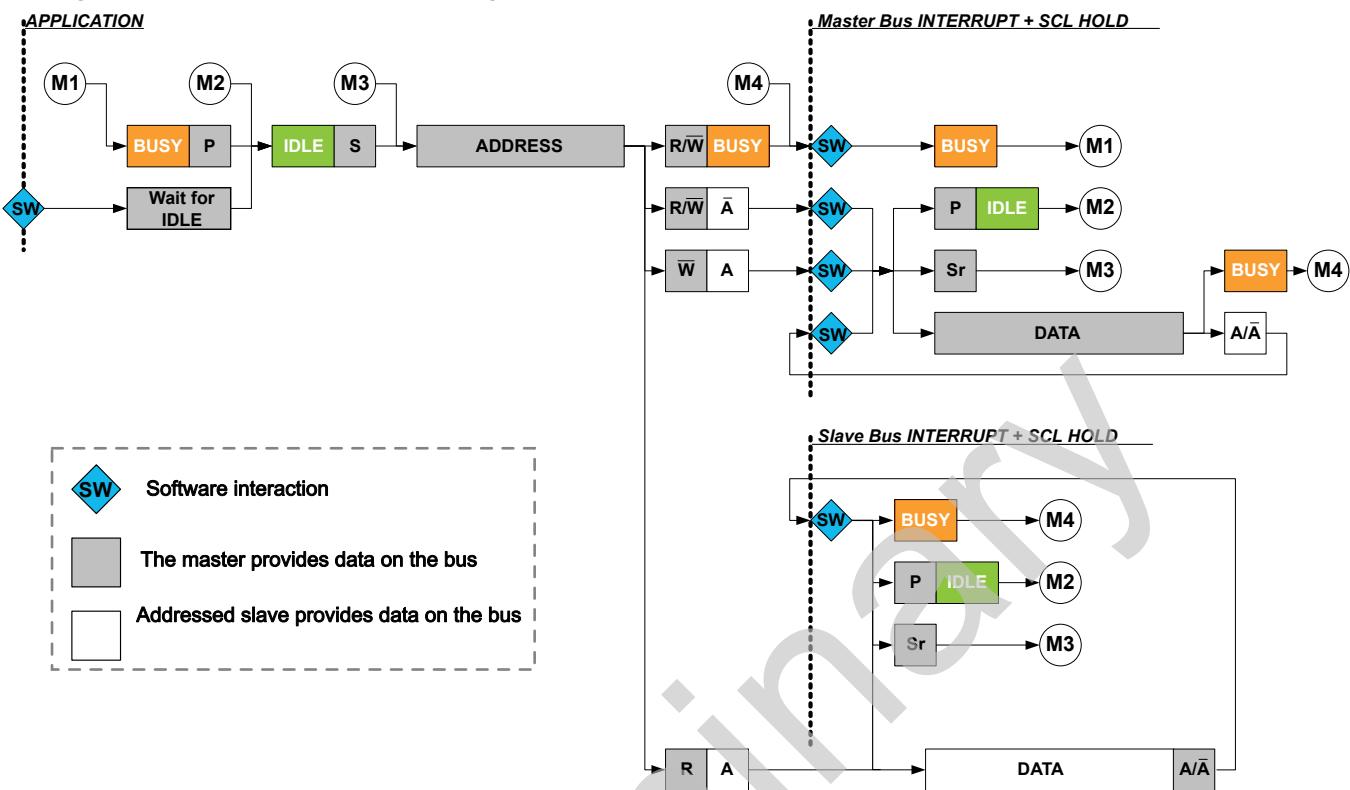
This diagram is used as reference for the description of the I²C master operation throughout the document.

Figure 31-5. I²C Master Behavioral Diagram (SCLSM=0)



In the second strategy (CTRLA.SCLSM=1), interrupts only occur after the ACK bit, as in *Master Behavioral Diagram (SCLSM=1)* shown in the following figure. This strategy can be used when it is not necessary to check DATA before acknowledging.

Figure 31-6. I²C Master Behavioral Diagram (SCLSM=1)



31.6.2.4.1 Master Clock Generation

The SERCOM peripheral supports several I²C bidirectional modes:

- Standard mode (*Sm*) up to 100 kHz
- Fast mode (*Fm*) up to 400 kHz
- Fast mode Plus (*Fm+*) up to 1 MHz

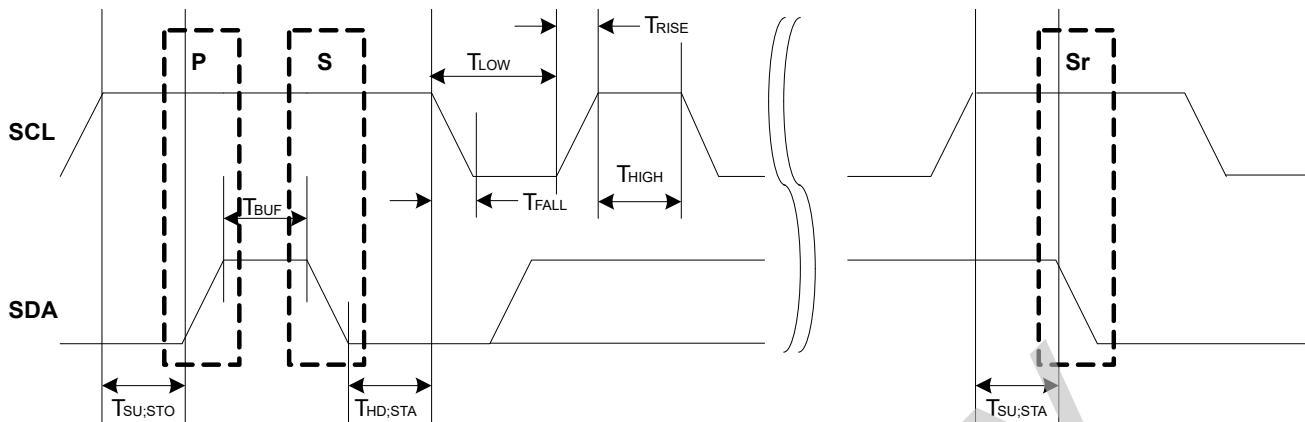
The Master clock configuration for *Sm*, *Fm*, and *Fm+* are described in *Clock Generation (Standard-Mode, Fast-Mode, and Fast-Mode Plus)* as follows.

Clock Generation (Standard-Mode, Fast-Mode, and Fast-Mode Plus)

In I²C *Sm*, *Fm*, and *Fm+* mode, the Master clock (SCL) frequency is determined as described in this section:

The low (T_{LOW}) and high (T_{HIGH}) times are determined by the Baud Rate register (BAUD), while the rise (T_{RISE}) and fall (T_{FALL}) times are determined by the bus topology. Because of the wired-AND logic of the bus, T_{FALL} will be considered as part of T_{LOW} . Likewise, T_{RISE} will be in a state between T_{LOW} and T_{HIGH} until a high state has been detected.

Figure 31-7. SCL Timing



The following parameters are timed using the SCL low time period T_{LOW} . This comes from the Master Baud Rate Low bit group in the Baud Rate register (BAUD.BAUDLOW). When BAUD.BAUDLOW=0, or the Master Baud Rate bit group in the Baud Rate register (BAUD.BAUD) determines it.

- T_{LOW} – Low period of SCL clock
- TSU,STA – Set-up time for stop condition
- T_{BUF} – Bus free time between stop and start conditions
- THD,STA – Hold time (repeated) start condition
- TSU,STA – Set-up time for repeated start condition
- T_{HIGH} is timed using the SCL high time count from BAUD.BAUD
- T_{RISE} is determined by the bus impedance; for internal pull-ups.
- T_{FALL} is determined by the open-drain current limit and bus impedance; can typically be regarded as zero.

The SCL frequency is given by:

$$f_{SCL} = \frac{1}{T_{LOW} + T_{HIGH} + T_{RISE}}$$

When BAUD.BAUDLOW is zero, the BAUD.BAUD value is used to time both SCL high and SCL low. In this case the following formula will give the SCL frequency:

$$f_{SCL} = \frac{f_{GCLK}}{10 + 2BAUD + f_{GCLK} \cdot T_{RISE}}$$

When BAUD.BAUDLOW is non-zero, the following formula determines the SCL frequency:

$$f_{SCL} = \frac{f_{GCLK}}{10 + BAUD + BAUDLOW + f_{GCLK} \cdot T_{RISE}}$$

The following formulas can determine the SCL T_{LOW} and T_{HIGH} times:

$$T_{LOW} = \frac{BAUDLOW + 5}{f_{GCLK}}$$

$$T_{HIGH} = \frac{BAUD + 5}{f_{GCLK}}$$

Note: The I²C standard Fm+ (Fast-mode plus) requires a nominal high to low SCL ratio of 1:2, and BAUD should be set accordingly. At a minimum, BAUD.BAUD and/or BAUD.BAUDLOW must be non-zero.

Startup Timing The minimum time between SDA transition and SCL rising edge is 6 APB cycles when the DATA register is written in smart mode. If a greater startup time is required due to long rise times, the time between DATA write and IF clear must be controlled by software.

Note: When timing is controlled by user, the Smart Mode cannot be enabled.

31.6.2.4.2 Transmitting Address Packets

The I²C master starts a bus transaction by writing the I²C slave address to ADDR.ADDR and the direction bit, as described in [31.6.1. Principle of Operation](#). If the bus is busy, the I²C master will wait until the bus becomes idle before continuing the operation. When the bus is idle, the I²C master will issue a start condition on the bus. The I²C master will then transmit an address packet using the address written to ADDR.ADDR. After the address packet has been transmitted by the I²C master, one of four cases will arise according to arbitration and transfer direction.

Case 1: Arbitration lost or bus error during address packet transmission

If arbitration was lost during transmission of the address packet, the Master on Bus bit in the Interrupt Flag Status and Clear register (INTFLAG.MB) and the Arbitration Lost bit in the Status register (STATUS.ARBLOST) are both set. Serial data output to SDA is disabled, and the SCL is released, which disables clock stretching. In effect the I²C master is no longer allowed to execute any operation on the bus until the bus is idle again. A bus error will behave similarly to the Arbitration Lost condition. In this case, the MB Interrupt flag and Master Bus Error bit in the Status register (STATUS.BUSERR) are both set in addition to STATUS.ARBLOST.

The Master Received Not Acknowledge bit in the Status register (STATUS.RXNACK) will always contain the last successfully received acknowledge or not acknowledge indication.

In this case, software will typically inform the application code of the condition and then clear the interrupt flag before exiting the interrupt routine. No other flags have to be cleared at this moment, because all flags will be cleared automatically the next time the ADDR.ADDR register is written.

Case 2: Address packet transmit complete – No ACK received

If there is no I²C slave device responding to the address packet, then the INTFLAG.MB Interrupt flag and STATUS.RXNACK will be set. The clock hold is active at this point, preventing further activity on the bus.

The missing ACK response can indicate that the I²C slave is busy with other tasks or sleeping. Therefore, it is not able to respond. In this event, the next step can be either issuing a Stop condition (recommended) or resending the address packet by a repeated Start condition. When using SMBus logic, the slave must ACK the address. If there is no response, it means that the slave is not available on the bus.

Case 3: Address packet transmit complete – Write packet, Master on Bus set

If the I²C master receives an acknowledge response from the I²C slave, INTFLAG.MB will be set and STATUS.RXNACK will be cleared. The clock hold is active at this point, preventing further activity on the bus.

In this case, the software implementation becomes highly protocol dependent. Three possible actions can enable the I²C operation to continue:

- Initiate a data transmit operation by writing the data byte to be transmitted into DATA.DATA.
- Transmit a new address packet by writing ADDR.ADDR. A repeated Start condition will automatically be inserted before the address packet.
- Issue a Stop condition, consequently terminating the transaction.

Case 4: Address packet transmit complete – Read packet, Slave on Bus set

If the I²C master receives an ACK from the I²C slave, the I²C master proceeds to receive the next byte of data from the I²C slave. When the first data byte is received, the Slave on Bus bit in the Interrupt Flag register (INTFLAG.SB) will be set and STATUS.RXNACK will be cleared. The clock hold is active at this point, preventing further activity on the bus.

In this case, the software implementation becomes highly protocol dependent. Three possible actions can enable the I²C operation to continue:

- Let the I²C master continue to read data by acknowledging the data received. ACK can be sent by software, or automatically in Smart mode.
- Transmit a new address packet.
- Terminate the transaction by issuing a Stop condition.

Note: An ACK or NACK will be automatically transmitted if Smart mode is enabled. The Acknowledge Action bit in the Control B register (CTRLB.ACKACT) determines whether ACK or NACK should be sent.

31.6.2.4.3 Transmitting Data Packets

When an address packet with direction Master Write (see [Figure 31-3](#)) was transmitted successfully, INTFLAG.MB will be set. The I²C master will start transmitting data via the I²C bus by writing to DATA.DATA, and monitor continuously for packet collisions.

If a collision is detected, the I²C master will lose arbitration and STATUS.ARBLOST will be set. If the transmit was successful, the I²C master will receive an ACK bit from the I²C slave, and STATUS.RXNACK will be cleared. INTFLAG.MB will be set in both cases, regardless of arbitration outcome.

It is recommended to read STATUS.ARBLOST and handle the arbitration lost condition in the beginning of the I²C Master on Bus interrupt. This can be done as there is no difference between handling address and data packet arbitration.

STATUS.RXNACK must be checked for each data packet transmitted before the next data packet transmission can commence. The I²C master is not allowed to continue transmitting data packets if a NACK is received from the I²C slave.

31.6.2.4.4 Receiving Data Packets (SCLSM=0)

When INTFLAG.SB is set, the I²C master will already have received one data packet. The I²C master must respond by sending either an ACK or NACK. Sending a NACK may be unsuccessful when arbitration is lost during the transmission. In this case, a lost arbitration will prevent setting INTFLAG.SB. Instead, INTFLAG.MB will indicate a change in arbitration. Handling of lost arbitration is the same as for data bit transmission.

31.6.2.4.5 Receiving Data Packets (SCLSM=1)

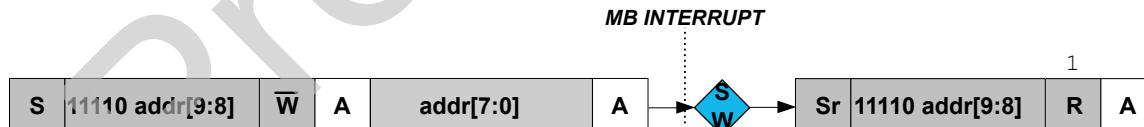
When INTFLAG.SB is set, the I²C master will already have received one data packet and transmitted an ACK or NACK, depending on CTRLB.ACKACT. At this point, CTRLB.ACKACT must be set to the correct value for the next ACK bit, and the transaction can continue by reading DATA and issuing a command if not in the Smart mode.

31.6.2.4.6 10-Bit Addressing

When 10-bit addressing is enabled by the Ten Bit Addressing Enable bit in the Address register (ADDR.TENBITEN=1) and the Address bit field ADDR.ADDR is written, the two address bytes will be transmitted, see [10-bit Address Transmission for a Read Transaction](#). The addressed slave acknowledges the two address bytes, and the transaction continues. Regardless of whether the transaction is a read or write, the master must start by sending the 10-bit address with the direction bit (ADDR.ADDR[0]) being zero.

If the master receives a NACK after the first byte, the Write Interrupt flag will be raised and the STATUS.RXNACK bit will be set. If the first byte is acknowledged by one or more slaves, then the master will proceed to transmit the second address byte and the master will first see the Write Interrupt flag after the second byte is transmitted. If the transaction direction is read-from-slave, the 10-bit address transmission must be followed by a repeated start and the first 7 bits of the address with the read/write bit equal to '1'.

Figure 31-8. 10-bit Address Transmission for a Read Transaction



This implies the following procedure for a 10-bit read operation:

1. Write the 10-bit address to ADDR.ADDR[10:1]. ADDR.TENBITEN must be '1', the direction bit (ADDR.ADDR[0]) must be '0' (can be written simultaneously with ADDR).
2. Once the Master on Bus interrupt is asserted, Write ADDR[7:0] register to '11110 address [9:8] 1'. ADDR.TENBITEN must be cleared (can be written simultaneously with ADDR).
3. Proceed to transmit data.

31.6.2.5 I²C Slave Operation

The I²C slave is byte-oriented and interrupt-based. The number of interrupts generated is kept at a minimum by automatic handling of most events. The software driver complexity and code size are reduced by auto-triggering of operations, and a special smart mode, which can be enabled by the Smart Mode Enable bit in the Control A register (CTRLA.SMEN).

The I²C slave has two interrupt strategies.

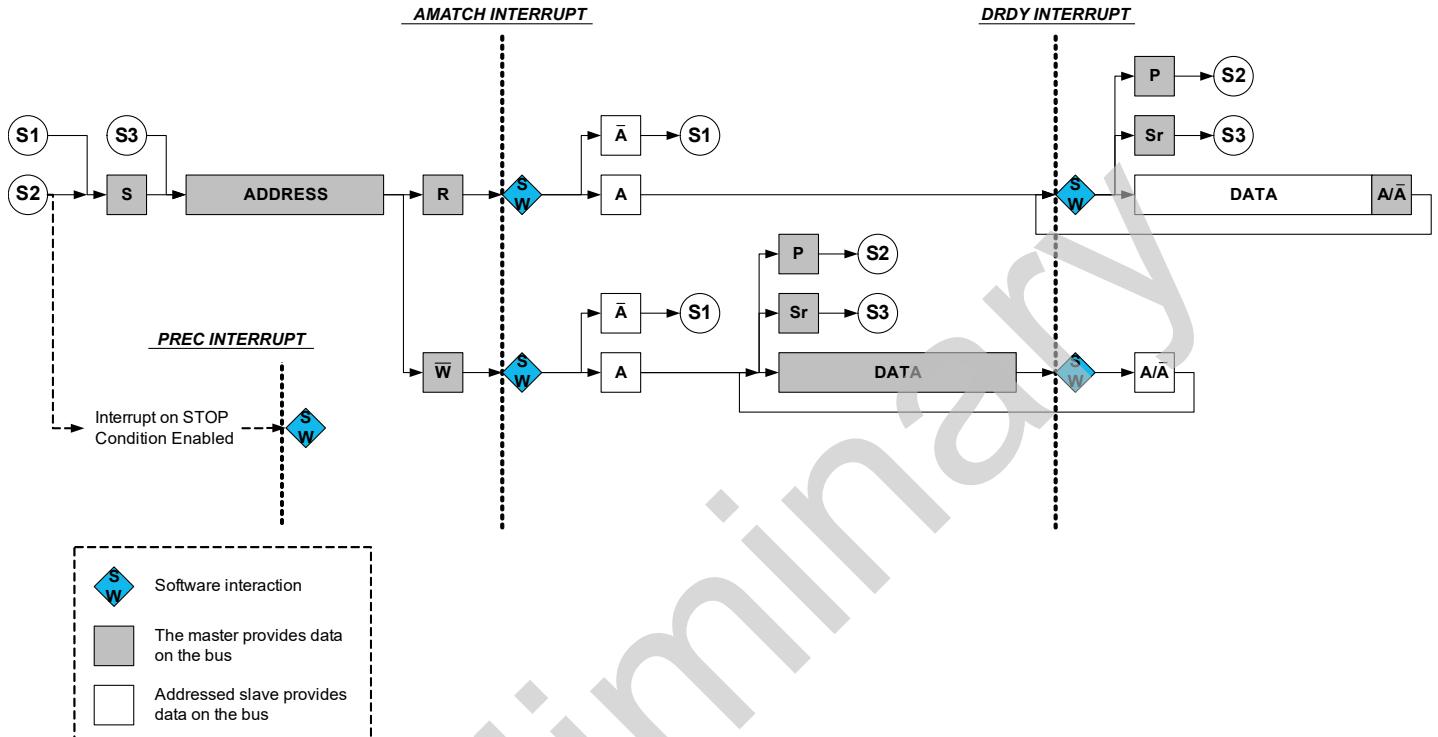
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When SCL Stretch Mode bit (CTRLA.SCLSM) is '0', SCL is stretched before or after the acknowledge bit. In this mode, the I²C slave operates according to *I²C Slave Behavioral Diagram (SCLSM=0)* as shown in the following figure. The circles labelled "Sn" (S1, S2..) indicate the nodes the bus logic can jump to, based on software or hardware interaction.

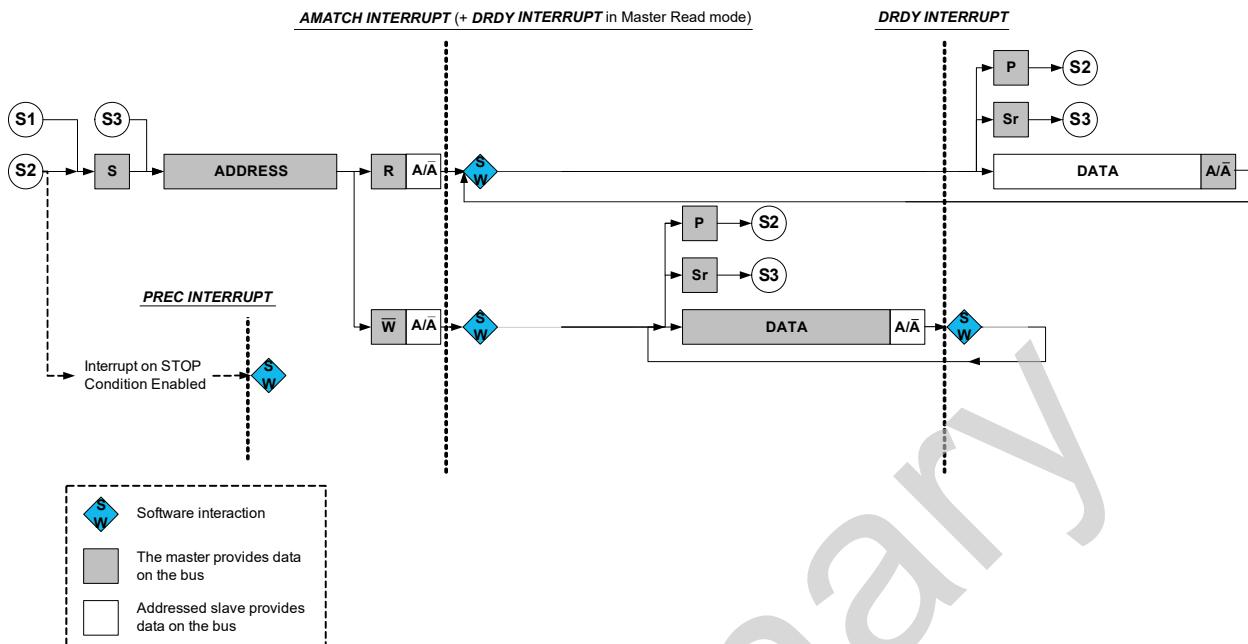
This diagram is used as reference for the description of the I²C slave operation throughout the document.

Figure 31-9. I²C Slave Behavioral Diagram (SCLSM=0)



In the second strategy (CTRLA.SCLSM=1), interrupts only occur after the ACK bit is sent as shown in the following figure *I²C Slave Behavioral Diagram (SCLSM=1)*. This strategy can be used when it is not necessary to check DATA before acknowledging. For master reads, an address and data interrupt will be issued simultaneously after the address acknowledge. However, for master writes, the first data interrupt will be seen after the first data byte has been received by the slave and the acknowledge bit has been sent to the master.

Figure 31-10. I²C Slave Behavioral Diagram (SCLSM=1)



31.6.2.5.1 Receiving Address Packets (SCLSM=0)

When CTRLA.SCLSM=0, the I²C slave stretches the SCL line according to Figure 31-9. When the I²C slave is properly configured, it will wait for a Start condition.

When a Start condition is detected, the successive address packet will be received and checked by the address match logic. If the received address is not a match, the packet will be rejected, and the I²C slave will wait for a new Start condition. If the received address is a match, the Address Match bit in the Interrupt Flag register (INTFLAG.AMATCH) will be set.

SCL will be stretched until the I²C slave clears INTFLAG.AMATCH. As the I²C slave holds the clock by forcing SCL low, the software has unlimited time to respond.

The direction of a transaction is determined by reading the Read/Write Direction bit in the Status register (STATUS.DIR). This bit will be updated only when a valid address packet is received.

If the Transmit Collision bit in the Status register (STATUS.COLL) is set, this indicates that the last packet addressed to the I²C slave had a packet collision. A collision causes the SDA and SCL lines to be released without any notification to software. Therefore, the next AMATCH interrupt is the first indication of the previous packet's collision. Collisions are intended to follow the SMBus Address Resolution Protocol (ARP).

After the address packet has been received from the I²C master, one of two cases will arise based on transfer direction.

Case 1: Address packet accepted – Read flag set

The STATUS.DIR bit is '1', indicating an I²C master read operation. The SCL line is forced low, stretching the bus clock. If an ACK is sent, I²C slave hardware will set the Data Ready bit in the Interrupt Flag register (INTFLAG.DRDY), indicating data are needed for transmit. If a NACK is sent, the I²C slave will wait for a new Start condition and address match.

Typically, software will immediately acknowledge the address packet by sending an ACK/NACK bit. The I²C slave Command bit field in the Control B register (CTRLB.CMD) can be written to '0x3' for both read and write operations as the command execution is dependent on the STATUS.DIR bit. Writing '1' to INTFLAG.AMATCH will also cause an ACK/NACK to be sent corresponding to the CTRLB.ACCKT bit.

Case 2: Address packet accepted – Write flag set

The STATUS.DIR bit is cleared, indicating an I²C master write operation. The SCL line is forced low, stretching the bus clock. If an ACK is sent, the I²C slave will wait for data to be received. Data, repeated start or stop can be received.

If a NACK is sent, the I²C slave will wait for a new Start condition and address match. Typically, software will immediately acknowledge the address packet by sending an ACK/NACK. The I²C slave command CTRLB.CMD = 3 can be used for both read and write operation as the command execution is dependent on STATUS.DIR.

Writing '1' to INTFLAG.AMATCH will also cause an ACK/NACK to be sent corresponding to the CTRLB.ACKACT bit.

31.6.2.5.2 Receiving Address Packets (SCLSM=1)

When SCLSM=1, the I²C slave will stretch the SCL line only after an ACK, see [I²C Slave Behavioral Diagram \(SCLSM=0\)](#) Slave Behavioral Diagram (SCLSM=1). When the I²C slave is properly configured, it will wait for a Start condition to be detected.

When a Start condition is detected, the successive address packet will be received and checked by the address match logic.

If the received address is not a match, the packet will be rejected and the I²C slave will wait for a new Start condition.

If the address matches, the acknowledge action as configured by the Acknowledge Action bit Control B register (CTRLB.ACKACT) will be sent and the Address Match bit in the Interrupt Flag register (INTFLAG.AMATCH) is set. SCL will be stretched until the I²C slave clears INTFLAG.AMATCH. As the I²C slave holds the clock by forcing SCL low, the software is given unlimited time to respond to the address.

The direction of a transaction is determined by reading the Read/Write Direction bit in the Status register (STATUS.DIR). This bit will be updated only when a valid address packet is received.

If the Transmit Collision bit in the Status register (STATUS.COLL) is set, the last packet addressed to the I²C slave had a packet collision. A collision causes the SDA and SCL lines to be released without any notification to software. The next AMATCH interrupt is, therefore, the first indication of the previous packet's collision. Collisions are intended to follow the SMBus Address Resolution Protocol (ARP).

After the address packet has been received from the I²C master, INTFLAG.AMATCH be set to '1' to clear it.

31.6.2.5.3 Receiving and Transmitting Data Packets

After the I²C slave has received an address packet, it will respond according to the direction either by waiting for the data packet to be received or by starting to send a data packet by writing to DATA.DATA. When a data packet is received or sent, INTFLAG.DRDY will be set. After receiving data, the I²C slave will send an acknowledge according to CTRLB.ACKACT.

Case 1: Data received

INTFLAG.DRDY is set, and SCL is held low, pending for SW interaction.

Case 2: Data sent

When a byte transmission is successfully completed, the INTFLAG.DRDY Interrupt flag is set. If NACK is received, indicated by STATUS.RXNACK=1, the I²C slave must expect a stop or a repeated start to be received. The I²C slave must release the data line to allow the I²C master to generate a stop or repeated start. Upon detecting a Stop condition, the Stop Received bit in the Interrupt Flag register (INTFLAG.PREC) will be set and the I²C slave will return to IDLE state.

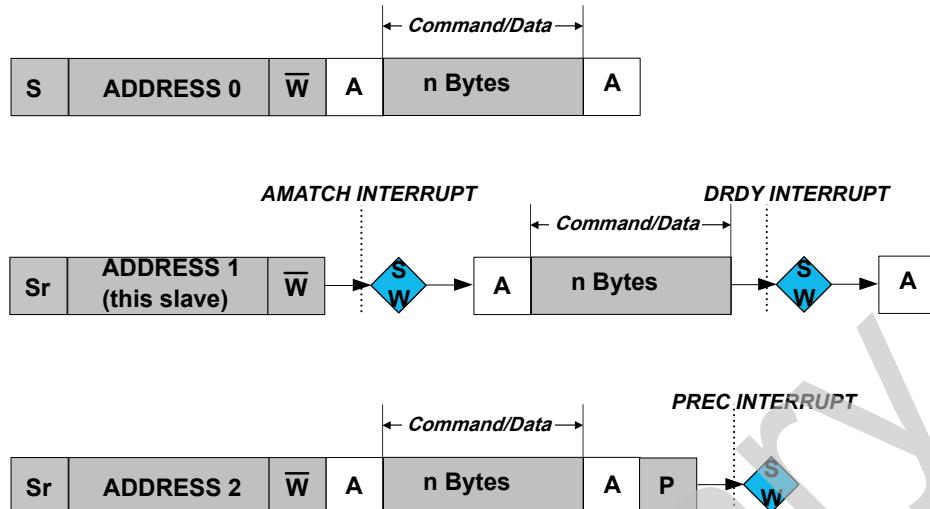
31.6.2.5.4 PMBus Group Command

When the PMBus Group Command bit in the CTRLB register is set (CTRLB.GCMD=1) and 7-bit addressing is used, INTFLAG.PREC will be set if the slave has been addressed since the last STOP condition. When CTRLB.GCMD=0, a STOP condition without address match will not be set INTFLAG.PREC.

The group command protocol is used to send commands to more than one device. The commands are sent in one continuous transmission with a single STOP condition at the end. When the STOP condition is detected by the slaves addressed during the group command, they all begin executing the command they received.

[PMBus Group Command Example](#) shows an example where this slave, bearing ADDRESS 1, is addressed after a repeated START condition. There can be multiple slaves addressed before and after this slave. Eventually, at the end of the group command, a single STOP is generated by the master. At this point a STOP interrupt is asserted.

Figure 31-11. PMBus Group Command Example



31.6.3 Additional Features

31.6.3.1 SMBus

The I²C includes three hardware SCL low time-outs, which allow a time-out to occur for SMBus SCL low time-out, master extend time-out, and slave extend time-out. This allows for SMBus functionality. These time-outs are driven by the GCLK_SERCOM_SLOW clock. The GCLK_SERCOM_SLOW clock is used to accurately time the time-out and must be configured to use a 32.768 kHz oscillator. The I²C interface also allows for a SMBus compatible SDA hold time.

- $T_{TIMEOUT}$: SCL low time of 25..35ms – Measured for a single SCL low period. It is enabled by CTRLA.LOWTOUTEN.
- $T_{LOW:SEXT}$: Cumulative clock low extend time of 25 ms – Measured as the cumulative SCL low extend time by a slave device in a single message from the initial START to the STOP. It is enabled by CTRLA.SEXTTOEN.
- $T_{LOW:MEXT}$: Cumulative clock low extend time of 10 ms – Measured as the cumulative SCL low extend time by the master device within a single byte from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is enabled by CTRLA.MEXTTOEN.

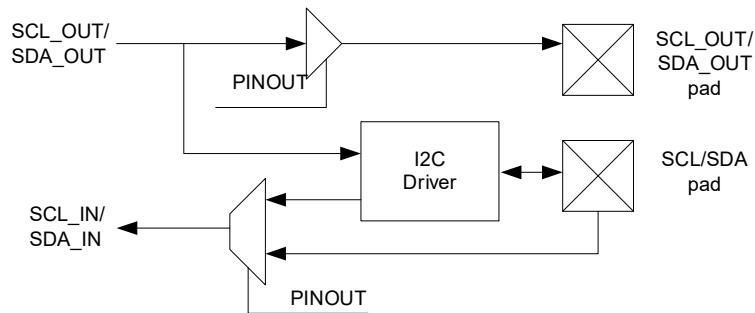
31.6.3.2 Smart Mode

The I²C interface has a Smart mode that simplifies application code and minimizes the user interaction needed to adhere to the I²C protocol. The Smart mode accomplishes this by automatically issuing an ACK or NACK (based on the content of CTRLB.ACKACT) as soon as DATA.DATA is read.

31.6.3.3 4-Wire Mode

Writing a '1' to the Pin Usage bit in the Control A register (CTRLA.PINOUT) will enable 4-Wire mode operation. In this mode, the internal I²C tri-state drivers are bypassed, and an external I²C compliant tri-state driver is needed when connecting to an I²C bus.

Figure 31-12. I²C Pad Interface



31.6.3.4 Quick Command

Setting the Quick Command Enable bit in the Control B register (CTRLB.QCEN) enables quick command. When quick command is enabled, the corresponding Interrupt flag (INTFLAG.SB or INTFLAG.MB) is set immediately after the slave acknowledges the address. At this point, the software can either issue a Stop command or a repeated start by writing CTRLB.CMD or ADDR.ADDR.

31.6.3.5 32-bit Extension

For better system bus utilization, 32-bit data receive and transmit can be enabled by writing to the Data 32-bit bit field in the Control C register (CTRLC.DATA32B=1). When enabled, write and read transaction to/from the DATA register are 32 bit in size.

If frames are not multiples of 4 Bytes, the Length Counter (LENGTH.LEN) and Length Enable (LENGTH.LENEN) must be configured before data transfer begins. LENGTH.LEN must be enabled only when CTRLC.DATA32B is enabled.

The figure below shows the order of transmit and receive when using 32-bit mode. Bytes are transmitted or received and stored in order from 0 to 3.

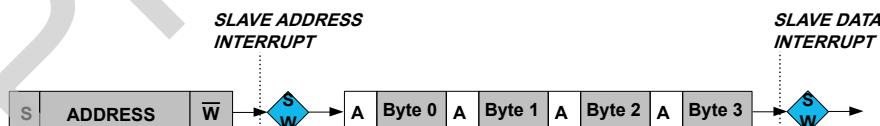
Figure 31-13. 32-bit Extension Byte Ordering



32-bit Extension Slave Operation

The figure below shows a transaction with 32-bit Extension enabled (CTRLC.DATA32B=1). In slave operation, the Address Match interrupt in the Interrupt Flag Status and Clear register (INTFLAG.AMATCH) is set after the address is received and available in the DATA register. The Data Ready interrupt (INTFLAG.DRDY) will then be raised for every 4 Bytes transferred.

Figure 31-14. 32-bit Extension Slave Operation



The LENGTH register can be written before the frame begins, or when the AMATCH interrupt is set. If the frame size is not LENGTH.LEN Bytes, the Length Error status bit (STATUS.LENERR) is raised. If LENGTH.LEN is not a multiple of 4 Bytes, the final INTFLAG.DRDY interrupt is raised when the last Byte is received for master reads. For master writes, the last data byte will be automatically NACKed. On address recognition, the internal length counter is reset in preparation for the incoming frame.

High Speed transactions start with a Full Speed Master Code. When a Master Code is detected, no data is received and the next expected operation is a repeated start. For this reason, the length is not counted after a Master Code is received. In this case, no Length Error (STATUS.LENERR) is registered, regardless of the LENGTH.LENEN setting.

When SCL clock stretch mode is selected (CTRLA.SCLSM=1) and the transaction is a master write, the selected Acknowledge Action (CTRLB.ACKACT) will only be used to ACK/NACK each 4th byte. All other bytes are ACKed. This allows the user to write CTRLB.ACKACT=1 in the final interrupt, so that the last byte in a 32-bit word will be NACKed.

Writing to the LENGTH register while a frame is in progress will produce unpredictable results. If LENGTH.LENEN is not set and a frame is not a multiple of 4 Bytes, the remainder will be lost.

32-bit Extension Master Operation

When using the I²C configured as Master, the Address register must be written with the desired address (ADDR.ADDR), and optionally, the transaction Length and transaction Length Enable bits (ADDR.LEN and ADDR.LENEN) can be written. When ADDR.LENEN is written to '1' along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. Then, the ADDR.LEN bytes are transferred, followed by an automatically generated NACK (for master reads) and a STOP.

The INTFLAG.SB or INTFLAG.MB are raised for every 4 Bytes transferred. If the transaction is a master read and ADDR.LEN is not a multiple of 4 Bytes, the final INTFLAG.SB is set when the last byte is received.

When SCL clock stretch mode is enabled (CTRLA.SCLSM=1) and the transaction is a master read, the selected Acknowledge Action (CTRLB.ACKACT) will only be used to ACK/NACK each 4th Byte. All other bytes are ACKed. This allows the user to set CTRLB.ACKACT=1 in the final interrupt, so that the last byte in a 32-bit word will be NACKed.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated, and the length error (STATUS.LENERR) is raised along with the INTFLAG.ERROR interrupt.

31.6.4 DMA, Interrupts and Events

Each interrupt source has its own Interrupt flag. The Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the Interrupt condition is met. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request is active until the Interrupt flag is cleared, the interrupt is disabled or the I²C is reset. See the [INTFLAG](#) (Slave) or [INTFLAG](#) (Master) register for details on how to clear Interrupt flags.

Table 31-1. Module Request for SERCOM I²C Slave

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Slave Transmit mode)	Yes (request cleared when data is written)		NA
Data received (RX) (Slave Receive mode)	Yes (request cleared when data is read)		
Data Ready (DRDY)		Yes	
Address Match (AMATCH)		Yes	
Stop received (PREC)		Yes	
Error (ERROR)		Yes	

Table 31-2. Module Request for SERCOM I²C Master

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Master Transmit mode)	Yes (request cleared when data is written)		NA
Data needed for transmit (RX) (Master Transmit mode)	Yes (request cleared when data is read)		
Master on Bus (MB)		Yes	
Stop received (SB)		Yes	
Error (ERROR)		Yes	

31.6.4.1 DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

31.6.4.1.1 Slave DMA

When using the I²C slave with DMA, an address match will cause the address Interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

31.6.4.1.2 Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

31.6.4.2 Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any Sleep mode:

- Error (ERROR)
- Data Ready (DRDY)
- Address Match (AMATCH)
- Stop Received (PREC)

The I²C master has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any Sleep mode:

- Error (ERROR)
- Slave on Bus (SB)
- Master on Bus (MB)

Each interrupt source has its own Interrupt flag. The Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the Interrupt condition is met. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

The status of enabled interrupts can be read from either INTENSET or INTENCLR. An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request active until the Interrupt flag is cleared, the interrupt is disabled or the I²C is reset. For details on how to clear Interrupt flags, see INTFLAG register from Related Links.

The value of INTFLAG indicates which interrupt is executed. Note that interrupts must be globally enabled for interrupt requests. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

- 9.2. Nested Vector Interrupt Controller (NVIC)
- 31.10.7. INTFLAG

31.6.4.3 Events

Not applicable.

31.6.5 Sleep Mode Operation

I²C Master Operation

The generic clock (GCLK_SERCOMx_CORE) will continue to run in idle sleep mode. If the Run In Standby bit in the Control A register (CTRLA.RUNSTDBY) is '1', the GLK_SERCOMx_CORE will also run in Standby Sleep mode. Any interrupt can wake-up the device.

If CTRLA.RUNSTDBY=0, the GLK_SERCOMx_CORE will be disabled after any ongoing transaction is finished. Any interrupt can wake-up the device.

I²C Slave Operation

Writing CTRLA.RUNSTDBY=1 will allow the Address Match interrupt to wake-up the device.

When CTRLA.RUNSTDBY=0, all receptions will be dropped.

31.7 Register Summary - I2C Slave

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
		15:8								
		23:16	SEXTTOEN		SDAHOLD[1:0]					PINOUT
		31:24		LOWTOUT			SCLSM		SPEED[1:0]	
0x04	CTRLB	7:0								
		15:8		AMODE[1:0]				AACKEN	GCMD	SMEN
		23:16					ACKACT		CMD[1:0]	
		31:24								
0x08	CTRLC	7:0					SDASETUP[3:0]			
		15:8								
		23:16								
		31:24								DATA32B
0x0C ...	Reserved									
0x14	INTENCLR	7:0	ERROR					DRDY	AMATCH	PREC
0x15	Reserved									
0x16	INTENSET	7:0	ERROR					DRDY	AMATCH	PREC
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR					DRDY	AMATCH	PREC
0x19	Reserved									
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
		15:8					LENERR		SEXTTOUT	
0x1C	SYNCBUSY	7:0				LENGTH			ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20 ...	Reserved									
0x22	LENGTH	7:0				LEN[7:0]				
		15:8								LENEN
0x24	ADDR	7:0				ADDR[6:0]				GENCEN
		15:8								
		23:16				ADDRMASK[6:0]				
		31:24								ADDRMASK[9:7]
0x28	DATA	7:0				DATA[7:0]				
		15:8				DATA[15:8]				
		23:16				DATA[23:16]				
		31:24				DATA[31:24]				

31.8 Register Description - I2C Slave

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

31.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		LOWTOUT			SCLSM		SPEED[1:0]	
Access		R/W			R/W		R/W	R/W
Reset		0			0		0	0
Bit	23	22	21	20	19	18	17	16
	SEXTTOEN		SDAHOLD[1:0]				PINOUT	
Access	R/W		R/W	R/W			R/W	
Reset	0		0	0			0	
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]		ENABLE	SWRST	
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – LOWTOUT SCL Low Time-Out

This bit enables the SCL low time-out. If SCL is held low for 25ms-35ms, the slave will release its clock hold, if enabled, and reset the internal state machine. Any interrupt flags set at the time of time-out will remain set.

This bit is not synchronized.

Value	Description
0	Time-out disabled.
1	Time-out enabled.

Bit 27 – SCLSM SCL Clock Stretch Mode

This bit controls when SCL will be stretched for software interaction.

This bit is not synchronized.

Value	Description
0	SCL stretch according to Figure 31-9
1	SCL stretch only after ACK bit according to Figure 31-10

Bits 25:24 – SPEED[1:0] Transfer Speed

These bits define bus speed.

These bits are not synchronized.

Value	Description
0x0	Standard-mode (Sm) up to 100 kHz and Fast-mode (Fm) up to 400 kHz
0x1	Fast-mode Plus (Fm+) up to 1 MHz
0x2	Reserved
0x3	Reserved

Bit 23 – SEXTTOEN Slave SCL Low Extend Time-Out

This bit enables the slave SCL low extend time-out. If SCL is cumulatively held low for greater than 25ms from the initial START to a STOP, the slave will release its clock hold if enabled and reset the internal state machine. Any interrupt flags set at the time of time-out will remain set. If the address was recognized, PREC will be set when a STOP is received.

This bit is not synchronized.

Value	Description
0	Time-out disabled
1	Time-out enabled

Bits 21:20 – SDAHOLD[1:0] SDA Hold Time

These bits define the SDA hold time with respect to the negative edge of SCL.

These bits are not synchronized.

Value	Name	Description
0x0	DIS	Disabled
0x1	75	50-100ns hold time
0x2	450	300-600ns hold time
0x3	600	400-800ns hold time

Bit 16 – PINOUT Pin Usage

This bit sets the pin usage to either two- or four-wire operation:

This bit is not synchronized.

Value	Description
0	4-wire operation disabled
1	4-wire operation enabled

Bit 7 – RUNSTDBY Run in Standby

This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

Value	Description
0	Disabled – All reception is dropped.
1	Wake on address match, if enabled.

Bits 4:2 – MODE[2:0] Operating Mode

These bits must be written to 0x04 to select the I²C slave serial communication interface of the SERCOM.

These bits are not synchronized.

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled.

The value written to CTRLA.ENABLE will read back immediately and the Enable Synchronization Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

31.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access						ACKACT	CMD[1:0]	
Reset						R/W	W	W
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W			AACKEN	GCMD	SMEN	
Reset	0	0			R/W	R/W	R/W	
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 18 – ACKACT Acknowledge Action

This bit defines the slave's acknowledge behavior after an address or data byte is received from the master.

The acknowledge action is executed when a command is written to the CMD bits. If smart mode is enabled (CTRLB.SMEN=1), the acknowledge action is performed when the DATA register is read.

ACKACT shall not be updated more than once between each peripheral interrupts request.

This bit is not enable-protected.

Value	Description
0	Send ACK
1	Send NACK

Bits 17:16 – CMD[1:0] Command

This bit field triggers the slave operation as the below. The CMD bits are strobe bits, and always read as zero.

The operation is dependent on the slave interrupt flags, INTFLAG.DRDY and INTFLAG.AMATCH, in addition to STATUS.DIR.

All interrupt flags (INTFLAG.DRDY, INTFLAG.AMATCH and INTFLAG.PREC) are automatically cleared when a command is given.

This bit is not enable-protected.

Table 31-3. Command Description

CMD[1:0]	DIR	Action
0x0	X	(No action)
0x1	X	(Reserved)
0x2		Used to complete a transaction in response to a data interrupt (DRDY)
	0 (Master write)	Execute acknowledge action succeeded by waiting for any start (S/Sr) condition
	1 (Master read)	Wait for any start (S/Sr) condition

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.....continued

CMD[1:0]	DIR	Action
0x3		Used in response to an address interrupt (AMATCH)
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute acknowledge action succeeded by slave data interrupt
		Used in response to a data interrupt (DRDY)
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute a byte read operation followed by ACK/NACK reception

Bits 15:14 – AMODE[1:0] Address Mode

These bits set the addressing mode.

Value	Name	Description
0x0	MASK	The slave responds to the address written in ADDR.ADDR masked by the value in ADDR.ADDRMASK.
0x1	2_ADDRS	The slave responds to the two unique addresses in ADDR.ADDR and ADDR.ADDRMASK.
0x2	RANGE	The slave responds to the range of addresses between and including ADDR.ADDR and ADDR.ADDRMASK. ADDR.ADDR is the upper limit.
0x3	-	Reserved.

Bit 10 – AACKEN Automatic Acknowledge Enable

This bit enables the address to be automatically acknowledged if there is an address match.

Value	Description
0	Automatic acknowledge is disabled.
1	Automatic acknowledge is enabled.

Bit 9 – GCMD PMBus Group Command

This bit enables PMBus group command support. When enabled, the Stop Received interrupt flag (INTFLAG.PREC) will be set when a STOP condition is detected if the slave has been addressed since the last STOP condition on the bus.

Value	Description
0	Group command is disabled.
1	Group command is enabled.

Bit 8 – SMEN Smart Mode Enable

When smart mode is enabled, data is acknowledged automatically when DATA.DATA is read.

Value	Description
0	Smart mode is disabled.
1	Smart mode is enabled.

31.8.3 Control C

Name: CTRLC
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24	DATA32B
Access								R/W	
Reset								0	
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	3	2	1	0	SDASETUP[3:0]
Access					R/W	R/W	R/W	R/W	
Reset					0	0	0	0	

Bit 24 – DATA32B Data 32 Bit

This bit enables 32-bit data writes and reads to/from the DATA register.

Value	Description
0	Data transaction to/from DATA are 8-bit in size
1	Data transaction to/from DATA are 32-bit in size

Bits 3:0 – SDASETUP[3:0] SDA Setup Time

These bits select the minimum SDA-to-SCL setup time, measured from the release of SDA to the release of SCL:

$$t_{SU:DAT} = (GCLK_SERCOMx \times APP\ period(PBx_CLK)) \times (6 + 16 \times SDASETUP)$$

31.8.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 2 – DRDY Data Ready Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Ready bit, which disables the Data Ready interrupt.

Value	Description
0	The Data Ready interrupt is disabled.
1	The Data Ready interrupt is enabled.

Bit 1 – AMATCH Address Match Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Address Match Interrupt Enable bit, which disables the Address Match interrupt.

Value	Description
0	The Address Match interrupt is disabled.
1	The Address Match interrupt is enabled.

Bit 0 – PREC Stop Received Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Stop Received Interrupt Enable bit, which disables the Stop Received interrupt.

Value	Description
0	The Stop Received interrupt is disabled.
1	The Stop Received interrupt is enabled.

31.8.5 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 2 – DRDY Data Ready Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Ready bit, which enables the Data Ready interrupt.

Value	Description
0	The Data Ready interrupt is disabled.
1	The Data Ready interrupt is enabled.

Bit 1 – AMATCH Address Match Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Address Match Interrupt Enable bit, which enables the Address Match interrupt.

Value	Description
0	The Address Match interrupt is disabled.
1	The Address Match interrupt is enabled.

Bit 0 – PREC Stop Received Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Stop Received Interrupt Enable bit, which enables the Stop Received interrupt.

Value	Description
0	The Stop Received interrupt is disabled.
1	The Stop Received interrupt is enabled.

31.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR Error

This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. The corresponding bits in STATUS are LENERR, SEXTTOUT, LOWTOUT, COLL, and BUSERR.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 2 – DRDY Data Ready

This flag is set when a I²C slave byte transmission is successfully completed.

The flag is cleared by hardware when either:

- Writing to the DATA register.
- Reading the DATA register with Smart mode enabled.
- Writing a valid command to the CMD register.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Ready Interrupt flag.

Bit 1 – AMATCH Address Match

This flag is set when the I²C slave address match logic detects that a valid address has been received.

The flag is cleared by hardware when CTRL.CMD is written.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Address Match Interrupt flag. When cleared, an ACK/NACK will be sent according to CTRLB.ACKACT.

Bit 0 – PREC Stop Received

This flag is set when a Stop condition is detected for a transaction being processed. A Stop condition detected between a bus master and another slave will not set this flag, unless the PMBus Group Command is enabled in the Control B register (CTRLB.GCMD=1).

This flag is cleared by hardware after a command is issued on the next address match.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Stop Received Interrupt flag.

31.8.7 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
Access					LENERR		SEXTTOUT	
Reset					0		0	
Bit	7	6	5	4	3	2	1	0
Access	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
Reset	R	R/W		R	R	R	R/W	R/W
	0	0		0	0	0	0	0

Bit 11 – LENERR Transaction Length Error

This bit is set when the length counter is enabled (LENGTH.LENEN) and a STOP or repeated START is received before or after the length in LENGTH.LEN is reached.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No length error has occurred.
1	Length error has occurred.

Bit 9 – SEXTTOUT Slave SCL Low Extend Time-Out

This bit is set if a slave SCL low extend time-out occurs.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No SCL low extend time-out has occurred.
1	SCL low extend time-out has occurred.

Bit 7 – CLKHOLD Clock Hold

The slave Clock Hold bit (STATUS.CLKHOLD) is set when the slave is holding the SCL line low, stretching the I2C clock. Software should consider this bit a read-only status flag that is set when INTFLAG.DRDY or INTFLAG.AMATCH is set.

This bit is automatically cleared when the corresponding interrupt is also cleared.

Bit 6 – LOWTOUT SCL Low Time-out

This bit is set if an SCL low time-out occurs.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No SCL low time-out has occurred.
1	SCL low time-out has occurred.

Bit 4 – SR Repeated Start

When INTFLAG.AMATCH is raised due to an address match, SR indicates a repeated start or start condition.

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This flag is only valid while the INTFLAG.AMATCH flag is one.

Value	Description
0	Start condition on last address match
1	Repeated start condition on last address match

Bit 3 – DIR Read / Write Direction

The Read/Write Direction (STATUS.DIR) bit stores the direction of the last address packet received from a master.

Value	Description
0	Master write operation is in progress.
1	Master read operation is in progress.

Bit 2 – RXNACK Received Not Acknowledge

This bit indicates whether the last data packet sent was acknowledged or not.

Value	Description
0	Master responded with ACK.
1	Master responded with NACK.

Bit 1 – COLL Transmit Collision

If set, the I2C slave was not able to transmit a high data or NACK bit, the I2C slave will immediately release the SDA and SCL lines and wait for the next packet addressed to it.

This flag is intended for the SMBus address resolution protocol (ARP). A detected collision in non-ARP situations indicates that there has been a protocol violation, and should be treated as a bus error.

Note that this status will not trigger any interrupt, and should be checked by software to verify that the data were sent correctly. This bit is cleared automatically if responding to an address match with an ACK or a NACK (writing 0x3 to CTRLB.CMD), or INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No collision detected on last data byte sent.
1	Collision detected on last data byte sent.

Bit 0 – BUSERR Bus Error

The Bus Error bit (STATUS.BUSERR) indicates that an illegal bus condition has occurred on the bus, regardless of bus ownership. An illegal bus condition is detected if a protocol violating start, repeated start or stop is detected on the I2C bus lines. A start condition directly followed by a stop condition is one example of a protocol violation. If a time-out occurs during a frame, this is also considered a protocol violation, and will set STATUS.BUSERR.

This bit is cleared automatically if responding to an address match with an ACK or a NACK (writing 0x3 to CTRLB.CMD) or INTFLAG.AMATCH is cleared.

Writing a '1' to this bit will clear the status.

Writing a '0' to this bit has no effect.

Value	Description
0	No bus error detected.
1	Bus error detected.

31.8.8 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access				R			R	R
Reset				0			0	0

Bit 4 – LENGTH LENGTH Synchronization Busy

Writing LENGTH requires synchronization. When written, this bit will be set until synchronization is complete. If LENGTH is written while SYNCBUSY.LENGTH is asserted, an APB error will be generated.

Note: In client mode, the clock is only running during data transfer, so SYNCBUSY.LENGTH will remain asserted until the next data transfer begins.

Value	Description
0	LENGTH synchronization is not busy.
1	LENGTH synchronization is busy.

Bit 1 – ENABLE SERCOM Enable Synchronization Busy

Enabling and disabling the SERCOM (CTRLA.ENABLE) requires synchronization. When written, the SYNCBUSY.ENABLE bit will be set until synchronization is complete.

Value	Description
0	Enable synchronization is not busy.
1	Enable synchronization is busy.

Bit 0 – SWRST Software Reset Synchronization Busy

Resetting the SERCOM (CTRLA.SWRST) requires synchronization. When written, the SYNCBUSY.SWRST bit will be set until synchronization is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

31.8.9 Length

Name: LENGTH
Offset: 0x22
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
Access								LENEN
Reset								R/W 0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 8 – LENEN Data Length Enable

In 32-bit Extension mode (CTRLC.DATA32B=1), this bit field enables the length counter.

Value	Description
0	Length counter is disabled.
1	Length counter is enabled.

Bits 7:0 – LEN[7:0] Data Length

In 32-bit Extension mode (CTRLC.DATA32B=1) with Data Length counting enabled (LENGTH.LENEN), this bit field configures the data length from 0 to 255 Bytes after which the flag INTFLAG.DRDY is raised.

31.8.10 Address

Name: ADDR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
							ADDRMASK[9:7]	
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	23	22	21	20	19	18	17	16
				ADDRMASK[6:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8
							ADDR[9:7]	
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	7	6	5	4	3	2	1	0
				ADDR[6:0]				GENCEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 26:17 – ADDRMASK[9:0] Address Mask

These bits act as a second address match register, an address mask register or the lower limit of an address range, depending on the CTRLB.AMODE setting.

Bits 10:1 – ADDR[9:0] Address

These bits contain the I²C slave address used by the slave address match logic to determine if a master has addressed the slave.

When using 7-bit addressing, the slave address is represented by ADDR[6:0].

When the address match logic detects a match, INTFLAG.AMATCH is set and STATUS.DIR is updated to indicate whether it is a read or a write transaction.

Bit 0 – GENCEN General Call Address Enable

A general call address is an address consisting of all-zeroes, including the direction bit (master write).

Value	Description
0	General call address recognition disabled.
1	General call address recognition enabled.

31.8.11 Data

Name: DATA
Offset: 0x28
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data

The slave data register I/O location (DATA.DATA) provides access to the master transmit and receive data buffers. Reading valid data or writing data to be transmitted can be successfully done only when SCL is held low by the slave (STATUS.CLKHOLD is set). An exception occurs when reading the last data byte after the stop condition has been received.

Accessing DATA.DATA auto-triggers I²C bus operations. The operation performed depends on the state of CTRLB.ACKACT, CTRLB.SMEN and the type of access (read/write).

When CTRLC.DATA32B=1, read and write transactions from/to the DATA register are 32 bit in size. Otherwise, reads and writes are 8 bit.

31.9 Register Summary - I2C Master

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
		15:8								
		23:16	SEXTTOEN	MEXTTOEN		SDAHOLD[1:0]				PINOUT
		31:24		LOWTOUT		INACTOUT[1:0]	SCLSM			SPEED[1:0]
0x04	CTRLB	7:0								
		15:8							QCEN	SMEN
		23:16						ACKACT		CMD[1:0]
		31:24								
0x08	CTRLC	7:0								
		15:8								
		23:16								
		31:24								DATA32B
0x0C	BAUD	7:0				BAUD[7:0]				
		15:8				BAUDLOW[7:0]				
		23:16								
		31:24								
0x10	Reserved									
0x13										
0x14	INTENCLR	7:0	ERROR						SB	MB
0x15	Reserved									
0x16	INTENSET	7:0	ERROR						SB	MB
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR						SB	MB
0x19	Reserved									
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT		BUSSTATE[1:0]			RXNACK	ARBLOST
		15:8							LENERR	MEXTTOUT
0x1C	SYNCBUSY	7:0							SYSOP	ENABLE
		15:8								SWRST
		23:16								
		31:24								
0x20	Reserved									
0x23										
0x24	ADDR	7:0				ADDR[7:0]				
		15:8	TENBITEN		LENEN				ADDR[10:8]	
		23:16				LEN[7:0]				
		31:24								
0x28	DATA	7:0				DATA[7:0]				
		15:8				DATA[15:8]				
		23:16				DATA[23:16]				
		31:24				DATA[31:24]				
0x2C	Reserved									
0x2F										
0x30	DBGCTRL	7:0								DBGSTOP

31.10 Register Description - I²C Master

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

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Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Preliminary

31.10.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		LOWTOUT		INACTOUT[1:0]		SCLSM		SPEED[1:0]
Access		R/W	R/W	R/W	R/W		R/W	R/W
Reset		0	0	0	0		0	0
Bit	23	22	21	20	19	18	17	16
	SEXTTOEN	MEXTTOEN		SDAHOLD[1:0]				PINOUT
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	RUNSTDBY				MODE[2:0]		ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – LOWTOUT SCL Low Time-Out

This bit enables the SCL low time-out. If SCL is held low for 25ms-35ms, the master will release its clock hold, if enabled, and complete the current transaction. A stop condition will automatically be transmitted.

INTFLAG.SB or INTFLAG.MB will be set as normal, but the clock hold will be released. The STATUS.LOWTOUT and STATUS.BUSERR status bits will be set.

This bit is not synchronized.

Value	Description
0	Time-out disabled.
1	Time-out enabled.

Bits 29:28 – INACTOUT[1:0] Inactive Time-Out

If the inactive bus time-out is enabled and the bus is inactive for longer than the time-out setting, the bus state logic will be set to idle. An inactive bus arise when either an I²C master or slave is holding the SCL low.

Enabling this option is necessary for SMBus compatibility, but can also be used in a non-SMBus set-up.

Calculated time-out periods are based on a 100kHz baud rate.

These bits are not synchronized.

Value	Name	Description
0x0	DIS	Disabled
0x1	55US	5-6 SCL cycle time-out (50-60μs)
0x2	105US	10-11 SCL cycle time-out (100-110μs)
0x3	205US	20-21 SCL cycle time-out (200-210μs)

Bit 27 – SCLSM SCL Clock Stretch Mode

This bit controls when SCL will be stretched for software interaction.

This bit is not synchronized.

Value	Description
0	SCL stretch according to Figure 31-5
1	SCL stretch only after ACK bit, Figure 31-6

Bits 25:24 – SPEED[1:0] Transfer Speed

These bits define bus speed.

These bits are not synchronized.

Value	Description
0x0	Standard-mode (Sm) up to 100 kHz and Fast-mode (Fm) up to 400 kHz
0x1	Fast-mode Plus (Fm+) up to 1 MHz
0x2	Reserved
0x3	Reserved

Bit 23 – SEXTTOEN Slave SCL Low Extend Time-Out

This bit enables the slave SCL low extend time-out. If SCL is cumulatively held low for greater than 25ms from the initial START to a STOP, the master will release its clock hold if enabled, and complete the current transaction. A STOP will automatically be transmitted.

SB or MB will be set as normal, but CLKHOLD will be released. The MEXTTOUT and BUSERR status bits will be set.

This bit is not synchronized.

Value	Description
0	Time-out disabled
1	Time-out enabled

Bit 22 – MEXTTOEN Master SCL Low Extend Time-Out

This bit enables the master SCL low extend time-out. If SCL is cumulatively held low for greater than 10ms from START-to-ACK, ACK-to-ACK, or ACK-to-STOP the master will release its clock hold if enabled, and complete the current transaction. A STOP will automatically be transmitted.

SB or MB will be set as normal, but CLKHOLD will be released. The MEXTTOUT and BUSERR status bits will be set.

This bit is not synchronized.

Value	Description
0	Time-out disabled
1	Time-out enabled

Bits 21:20 – SDAHOLD[1:0] SDA Hold Time

These bits define the SDA hold time with respect to the negative edge of SCL.

These bits are not synchronized.

Value	Name	Description
0x0	DIS	Disabled
0x1	75NS	50-100ns hold time
0x2	450NS	300-600ns hold time
0x3	600NS	400-800ns hold time

Bit 16 – PINOUT Pin Usage

This bit set the pin usage to either two- or four-wire operation:

This bit is not synchronized.

Value	Description
0	4-wire operation disabled.
1	4-wire operation enabled.

Bit 7 – RUNSTDBY Run in Standby

This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

Value	Description
0	GCLK_SERCOMx_CORE is disabled and the I ² C master will not operate in standby sleep mode.
1	GCLK_SERCOMx_CORE is enabled in all sleep modes.

Bits 4:2 – MODE[2:0] Operating Mode

These bits must be written to 0x5 to select the I²C master serial communication interface of the SERCOM.

These bits are not synchronized.

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Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

31.10.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access						ACKACT	CMD[1:0]	
Reset						R/W	W	W
Bit	15	14	13	12	11	10	9	8
Access						QCEN	SMEN	
Reset						R/W	R/W	
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 18 – ACKACT Acknowledge Action

This bit defines the I²C master's acknowledge behavior after a data byte is received from the I²C slave. The acknowledge action is executed when a command is written to CTRLB.CMD, or if Smart mode is enabled (CTRLB.SMEN is written to one), when DATA.DATA is read.

This bit is not enable-protected.

This bit is not write-synchronized.

Value	Description
0	Send ACK.
1	Send NACK.

Bits 17:16 – CMD[1:0] Command

Writing these bits triggers a master operation as described below. The CMD bits are strobe bits, and always read as zero. The acknowledge action is only valid in Master Read mode. In Master Write mode, a command will only result in a repeated Start or Stop condition. The CTRLB.ACKACT bit and the CMD bits can be written at the same time, and then the acknowledge action will be updated before the command is triggered.

Commands can only be issued when either the Slave on Bus Interrupt flag (INTFLAG.SB) or Master on Bus Interrupt flag (INTFLAG.MB) is '1'.

If CMD 0x1 is issued, a repeated start will be issued followed by the transmission of the current address in ADDR.ADDR. If another address is desired, ADDR.ADDR must be written instead of the CMD bits. This will trigger a repeated start followed by transmission of the new address.

Issuing a command will set the System Operation bit in the Synchronization Busy register (SYNCBUSY.SYSOP).

Table 31-4. Command Description

CMD[1:0]	Direction	Action
0x0	X	(No action)
0x1	X	Execute acknowledge action succeeded by repeated Start
0x2	0 (Write)	No operation
	1 (Read)	Execute acknowledge action succeeded by a byte read operation
0x3	X	Execute acknowledge action succeeded by issuing a Stop condition

These bits are not enable-protected.

Bit 9 – QCEN Quick Command Enable

This bit is not write-synchronized.

Value	Description
0	Quick Command is disabled.
1	Quick Command is enabled.

Bit 8 – SMEN Smart Mode Enable

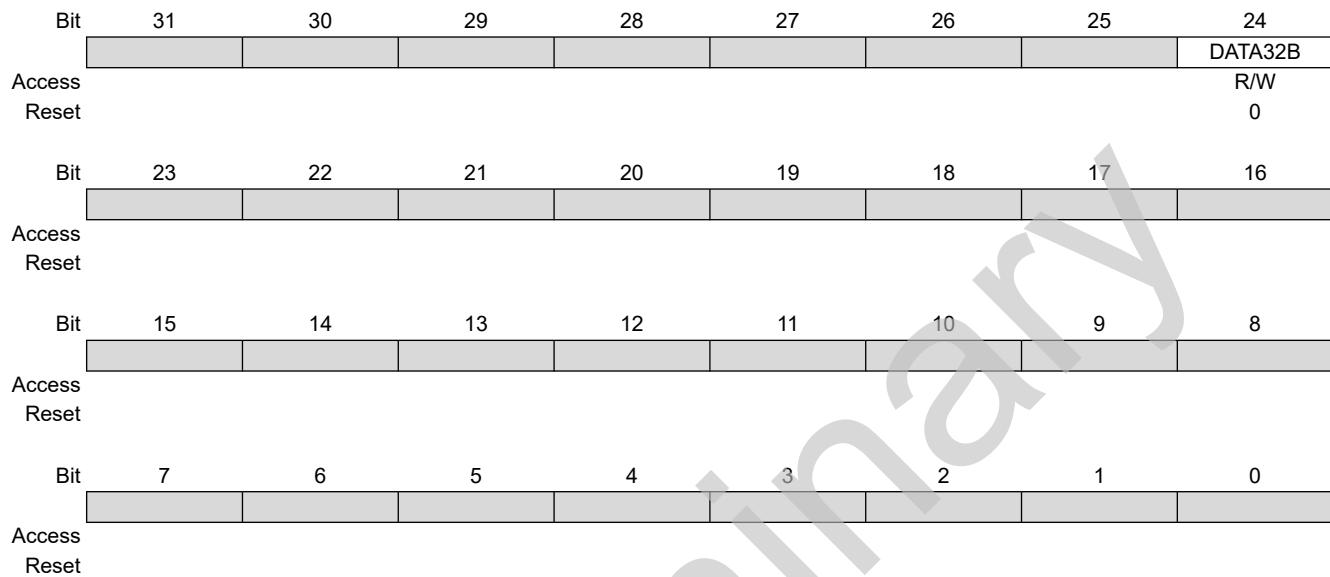
When Smart mode is enabled, acknowledge action is sent when DATA.DATA is read.

This bit is not write-synchronized.

Value	Description
0	Smart mode is disabled.
1	Smart mode is enabled.

31.10.3 Control C

Name: CTRLC
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected



Bit 24 – DATA32B Data 32 Bit

This bit enables 32-bit data writes and reads to/from the DATA register.

Value	Description
0	Data transactions to/from DATA are 8-bit in size
1	Data transactions to/from DATA are 32-bit in size

31.10.4 Baud Rate

Name: BAUD
Offset: 0x0C
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
				BAUDLOW[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				BAUD[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – BAUDLOW[7:0] Master Baud Rate Low

If this bit field is non-zero, the SCL low time will be described by the value written.

For more details on how to calculate the frequency, see *Clock Generation – Baud-Rate Generator* from Related Links.

Bits 7:0 – BAUD[7:0] Master Baud Rate

This bit field is used to derive the SCL high time if BAUD.BAUDLOW is non-zero. If BAUD.BAUDLOW is zero, BAUD will be used to generate both high and low periods of the SCL.

For more details on how to calculate the frequency, see *Clock Generation – Baud-Rate Generator* from Related Links.

Related Links

[28.6.2.3. Clock Generation – Baud-Rate Generator](#)

31.10.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 1 – SB Slave on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Slave on Bus Interrupt Enable bit, which disables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

Bit 0 – MB Master on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Master on Bus Interrupt Enable bit, which disables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

31.10.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 1 – SB Slave on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Slave on Bus Interrupt Enable bit, which enables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

Bit 0 – MB Master on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Master on Bus Interrupt Enable bit, which enables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

31.10.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR Error

This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status bits in the STATUS register. These status bits are LENERR, SEXTTOUT, MEXTTOUT, LOWTOUT, ARBLOST, and BUSERR.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 1 – SB Client on Bus

The Client on Bus flag (SB) is set when a byte is successfully received in Host Read mode, for example, no arbitration lost or bus error occurred during the operation. When this flag is set, the host forces the SCL line low, stretching the I²C clock period. The SCL line will be released and SB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when Smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the SB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

Bit 0 – MB Host on Bus

This flag is set when a byte is transmitted in Host Write mode. The flag is set regardless of the occurrence of a bus error or an Arbitration Lost condition. MB is also set when arbitration is lost during sending of NACK in Host Read mode, or when issuing a Start condition if the bus state is unknown. When this flag is set and arbitration is not lost, the host forces the SCL line low, stretching the I²C clock period. The SCL line will be released and MB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when Smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the MB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

31.10.8 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
Access						LENERR	SEXTTOUT	MEXTTOUT
Reset						0	0	0
Bit	7	6	5	4	3	2	1	0
Access	CLKHOLD	LOWTOUT	BUSSTATE[1:0]	R/W	R/W	RXNACK	ARBLOST	BUSERR
Reset	0	0	0	0	0	0	0	0

Bit 10 – LENERR Transaction Length Error

This bit is set when automatic length is used for a DMA and/or 32-bit transaction and the slave sends a NACK before ADDR.LEN bytes have been written by the master.

Writing '1' to this bit location will clear STATUS.LENERR. This flag is automatically cleared when writing to the ADDR register.

Writing '0' to this bit has no effect.

This bit is not write-synchronized.

Bit 9 – SEXTTOUT Slave SCL Low Extend Time-Out

This bit is set if a slave SCL low extend time-out occurs.

This bit is automatically cleared when writing to the ADDR register.

Writing '1' to this bit location will clear SEXTTOUT. Normal use of the I²C interface does not require the SEXTTOUT flag to be cleared by this method.

Writing '0' to this bit has no effect.

This bit is not write-synchronized.

Bit 8 – MEXTTOUT Master SCL Low Extend Time-Out

This bit is set if a master SCL low time-out occurs.

Writing '1' to this bit location will clear STATUS.MEXTTOUT. This flag is automatically cleared when writing to the ADDR register.

Writing '0' to this bit has no effect.

This bit is not write-synchronized.

Bit 7 – CLKHOLD Clock Hold

This bit is set when the master is holding the SCL line low, stretching the I²C clock. Software should consider this bit when INTFLAG.SB or INTFLAG.MB is set.

This bit is cleared when the corresponding Interrupt flag is cleared and the next operation is given.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

This bit is not write-synchronized.

Bit 6 – LOWTOUT SCL Low Time-Out

This bit is set if an SCL low time-out occurs.

Writing '1' to this bit location will clear this bit. This flag is automatically cleared when writing to the ADDR register.

Writing '0' to this bit has no effect.

This bit is not write-synchronized.

Bits 5:4 – BUSSTATE[1:0] Bus State

These bits indicate the current I²C Bus state.

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SERCOM I2C – Inter-Integrated Circuit

When in UNKNOWN state, writing 0x1 to BUSSTATE forces the bus state into the IDLE state. The bus state cannot be forced into any other state.

Writing BUSSTATE to idle will set SYNCBUSY.SYSOP.

Value	Name	Description
0x0	UNKNOWN	The Bus state is unknown to the I ² C master and will wait for a Stop condition to be detected or wait to be forced into an Idle state by software
0x1	IDLE	The Bus state is waiting for a transaction to be initialized
0x2	OWNER	The I ² C master is the current owner of the bus
0x3	BUSY	Some other I ² C master owns the bus

Bit 2 – RXNACK Received Not Acknowledge

This bit indicates whether the last address or data packet sent was acknowledged or not.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

This bit is not write-synchronized.

Value	Description
0	Slave responded with ACK.
1	Slave responded with NACK.

Bit 1 – ARBLOST Arbitration Lost

This bit is set if arbitration is lost while transmitting a high data bit or a NACK bit, or while issuing a Start or Repeated Start condition on the bus. The Master on Bus Interrupt flag (INTFLAG.MB) will be set when STATUS.ARBLOST is set.

Writing the ADDR.ADDR register will automatically clear STATUS.ARBLOST.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

This bit is not write-synchronized.

Bit 0 – BUSERR Bus Error

This bit indicates that an illegal Bus condition has occurred on the bus, regardless of bus ownership. An illegal Bus condition is detected if a protocol violating start, repeated start or stop is detected on the I²C bus lines. A Start condition directly followed by a Stop condition is one example of a protocol violation. If a time-out occurs during a frame, this is also considered a protocol violation, and will set BUSERR.

If the I²C master is the bus owner at the time a bus error occurs, STATUS.ARBLOST and INTFLAG.MB will be set in addition to BUSERR.

Writing the ADDR.ADDR register will automatically clear the BUSERR flag.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

This bit is not write-synchronized.

31.10.9 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	SYSOP	ENABLE	SWRST
Access					R	R	R	
Reset					0	0	0	

Bit 2 – SYSOP System Operation Synchronization Busy

Writing CTRLB.CMD, STATUS.BUSSTATE, ADDR, or DATA when the SERCOM is enabled requires synchronization. When written, the SYNCBUSY.SYSOP bit will be set until synchronization is complete.

Value	Description
0	System operation synchronization is not busy.
1	System operation synchronization is busy.

Bit 1 – ENABLE SERCOM Enable Synchronization Busy

Enabling and disabling the SERCOM (CTRLA.ENABLE) requires synchronization. When written, the SYNCBUSY.ENABLE bit will be set until synchronization is complete.

Value	Description
0	Enable synchronization is not busy.
1	Enable synchronization is busy.

Bit 0 – SWRST Software Reset Synchronization Busy

Resetting the SERCOM (CTRLA.SWRST) requires synchronization. When written, the SYNCBUSY.SWRST bit will be set until synchronization is complete.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

31.10.10 Address

Name: ADDR
Offset: 0x24
Reset: 0x0000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit								
Access	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0
LEN[7:0]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit								
Access	15	14	13	12	11	10	9	8
Reset	TENBITEN		LENEN				ADDR[10:8]	
R/W								
Access	0			R/W		R/W	R/W	R/W
Reset	0			0		0	0	0
Bit								
Access	7	6	5	4	3	2	1	0
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR[7:0]								
Access	0	0	0	0	0	0	0	0

Bits 23:16 – LEN[7:0] Transaction Length

These bits define the transaction length of a DMA and/or 32-bit transaction from 0 to 255 bytes. The Transfer Length Enable (LENEN) bit must be written to '1' in order to use DMA.

Bit 15 – TENBITEN Ten Bit Addressing Enable

This bit enables 10-bit addressing. This bit can be written simultaneously with ADDR to indicate a 10-bit or 7-bit address transmission.

Value	Description
0	10-bit addressing disabled.
1	10-bit addressing enabled.

Bit 13 – LENEN Transfer Length Enable

Value	Description
0	Automatic transfer length disabled.
1	Automatic transfer length enabled.

Bits 10:0 – ADDR[10:0] Address

When ADDR is written, the consecutive operation will depend on the bus state:

UNKNOWN: INTFLAG.MB and STATUS.BUSERR are set, and the operation is terminated.

BUSY: The I²C master will await further operation until the bus becomes IDLE.

IDLE: The I²C master will issue a start condition followed by the address written in ADDR. If the address is acknowledged, SCL is forced and held low, and STATUS.CLKHOLD and INTFLAG.MB are set.

OWNER: A repeated start sequence will be performed. If the previous transaction was a read, the acknowledge action is sent before the repeated start bus condition is issued on the bus. Writing ADDR to issue a repeated start is performed while INTFLAG.MB or INTFLAG.SB is set.

STATUS.BUSERR, STATUS.ARBLOST, INTFLAG.MB and INTFLAG.SB will be cleared when ADDR is written.

The ADDR register can be read at any time without interfering with ongoing bus activity, as a read access does not trigger the master logic to perform any bus protocol related operations.

The I²C master control logic uses bit 0 of ADDR as the bus protocol's read/write flag (R/W); 0 for write and 1 for read.

31.10.11 Data

Name: DATA
Offset: 0x28
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data

The master data register I/O location (DATA) provides access to the master transmit and receive data buffers. Reading valid data or writing data to be transmitted can be successfully done only when SCL is held low by the master (STATUS.CLKHold is set). An exception is reading the last data byte after the stop condition has been sent. Accessing DATA.DATA auto-triggers I²C bus operations. The operation performed depends on the state of CTRLB.ACKACT, CTRLB.SMEN and the type of access (read/write). When CTRLC.DATA32B=1, read and write transactions from/to the DATA register are 32 bit in size. Otherwise, reads and writes are 8 bit.

31.10.12 Debug Control

Name: DBGCTRL
Offset: 0x30
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	Reset	R/W
											DBGSTOP 0

Bit 0 – DBGSTOP Debug Stop Mode

This bit controls functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.

32. QSPI - Quad Serial Peripheral Interface

32.1 Overview

The Quad SPI Interface (QSPI) circuit is a synchronous serial data link that provides communication with external devices in Master mode.

The QSPI can be used in "SPI mode" to interface serial peripherals, such as ADCs, DACs, LCD controllers and sensors, or in "Serial Memory Mode" to interface serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (XIP) without code shadowing to SRAM. The serial Flash memory mapping is seen in the system as other memories (ROM, SRAM, DRAM, embedded Flash memories, etc.,).

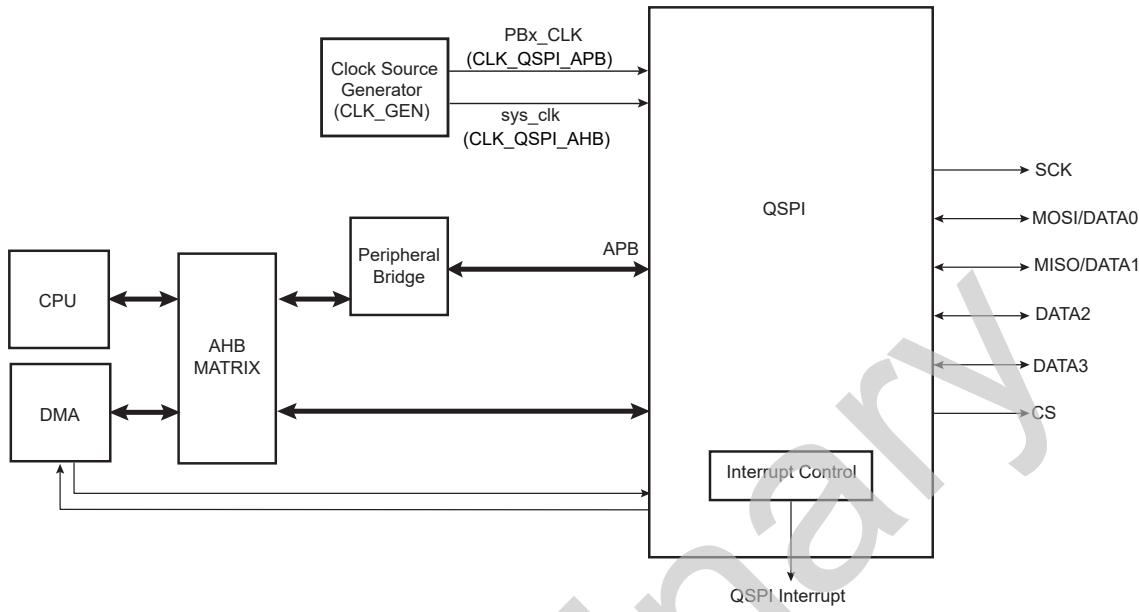
With the support of the quad-SPI protocol, the QSPI allows the system to use high performance serial Flash memories which are small and inexpensive, in place of larger and more expensive parallel Flash memories.

32.2 Features

- Master SPI Interface:
 - Programmable Clock Phase and Clock Polarity
 - Programmable transfer delays between consecutive transfers, between clock and data, between deactivation and activation of chip select (CS)
- SPI Mode:
 - To use serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers, and sensors
 - 8-bit, 16-bit, or 32-bit programmable data length
- Serial Memory Mode:
 - To use serial Flash memories operating in single-bit SPI, Dual SPI and Quad SPI
 - Supports "execute in place" (XIP). The system can execute code directly from a Serial Flash memory
 - Flexible Instruction register, to be compatible with all Serial Flash memories
 - 32-bit Address mode (default is 24-bit address) to support Serial Flash memories larger than 128 Mbit
 - Continuous Read mode
 - Scrambling/Unscrambling "On-the-Fly"
 - Double data rate support
- Connection to DMA Channel Capabilities Optimizes Data Transfers
 - One channel for the receiver and one channel for the transmitter
- Register Write Protection

32.3 Block Diagram

Figure 32-1. QSPI Block Diagram



32.4 Signal Description

Table 32-1. Quad-SPI Signals

Signal	Description	Type
SCK	Serial Clock	Output
CS	Chip Select	Output
MOSI(DATA0)	Data Output (Data Input Output 0)	Output (Input/Output)
MISO(DATA1)	Data Input (Data Input Output 1)	Input (Input/Output)
DATA2	Data Input Output 2	Input/Output
DATA3	Data Input Output 3	Input/Output

Notes:

1. MOSI and MISO are used for single-bit SPI operation
2. DATA0-DATA1 are used for Dual SPI operation
3. DATA0-DATA3 are used for Quad SPI operation

See *Pinout and Signal Description List* from Related Links for details on the pin mapping for QSPI peripheral.

32.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

32.5.1 I/O Lines

Using the QSPI I/O lines requires the I/O pins to be configured.

32.5.2 Power Management

The QSPI will continue to operate in any Sleep mode where the selected source clock is running. The QSPI interrupts can be used to wake up the device from sleep modes. See *Power Management Unit (PMU)* from Related Links for details on the different sleep modes.

Related Links

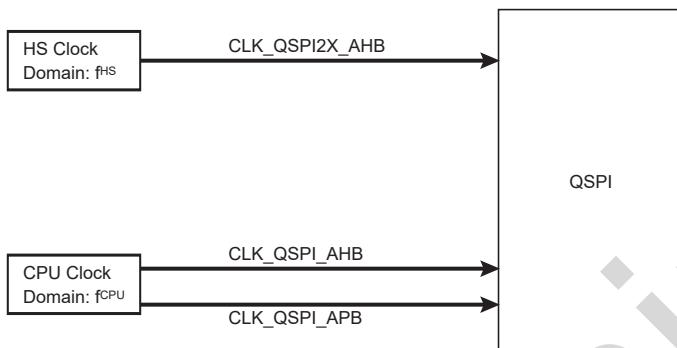
[14. Power Management Unit \(PMU\)](#)

32.5.3 Clocks

An AHB clock (CLK_QSPI_AHB) is required to clock the QSPI. This clock can be enabled and disabled in the CRU.

A FAST clock (CLK_QSPI2X_AHB) is required to clock the QSPI. This clock can be enabled and disabled in the CFGCON1 register, bit 29 (CFGCON1.QSPIDDRM). When using QSPI DDR Mode, the System Clock (sys_clk) must be $\leq 48\text{MHz}$.

Figure 32-2. QSPI Clock Organization



Important: The CLK_QSPI2x_AHB must be 2 times faster to CLK_QSPI_AHB when the QSPI is operated in DDR mode. In SDR, the CLK_QSPI2x_AHB is not used.

CLK_QSPI_APB, CLK_QSPI_AHB, and CLK_QSPI2X_AHB, respectively, are all synchronous, but can be divided by a prescaler and may run even when the module clock is turned off.

32.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). Using the QSPI DMA requests requires the DMA Controller to be configured first.

Note: DMAC write access must be 32-bit aligned. If a single byte is to be written in a 32-bit word, the rest of the word must be filled with 'ones'.

32.5.5 Interrupts

The interrupt request lines are connected to the interrupt controller. Using the QSPI interrupts requires the interrupt controller to be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

32.5.6 Events

Not applicable.

32.5.7 Debug Operation

When the CPU is halted in debug mode the QSPI continues normal operation. If the QSPI is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

32.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the peripheral access controller (PAC), except the following registers:

- Control A (CTRLA) register
- Transmit Data (TXDATA) register
- Interrupt Flag Status and Clear (INTFLAG) register
- Interrupt Flag Status and Clear (INTFLAG) register
- Scrambling Key (SCRAMBKEY) register

PAC write-protection is denoted by the 'PAC Write-Protection' property in the register description.

Write-protection does not apply to accesses through an external debugger.

32.6 Functional Description

32.6.1 Principle of Operation

The QSPI is a high-speed synchronous data transfer interface. It allows high-speed communication between the device and peripheral or serial memory devices.

The QSPI operates as a master. It initiates and controls all data transactions.

When transmitting, the TXDATA register can be loaded with the next character to be transmitted during the current transmission.

When receiving, the data is transferred to the RXDATA register, and the receiver is ready for a new character.

32.6.2 Basic Operation

32.6.2.1 Initialization

After Power-On Reset, this peripheral is enabled.

32.6.2.2 Enabling, Disabling, and Resetting

The peripheral is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE).

The peripheral is disabled by writing a '0' to CTRLA.ENABLE.

The peripheral is reset by writing a '1' to the Software Reset bit (CTRLA.SWRST).

32.6.3 Transfer Data Rate

By default, the QSPI module is enabled in single data rate mode. In this operating mode, the CLK_QSPI2X_AHB clock is not used and must be disabled.

The dual data rate operating mode is enabled by writing a '1' to the Double Data Rate Enable bit in the CFGCON1 register (CFGCON.QSPIDDRM). This operating mode requires the CLK_QSPI2X_AHB clock and must be enabled before writing the DDREN bit.

32.6.4 Serial Clock Baud Rate

The QSPI Baud rate clock is generated by dividing the module clock (CLK_QSPI_AHB) by a value between 1 and 255.

This allows a maximum operating baud rate at up to Master Clock and a minimum operating baud rate of CLK_QSPI_AHB divided by 255.

32.6.5 Serial Clock Phase and Polarity

Four combinations of polarity and phase are available for data transfers. Writing the Clock Polarity bit in the QSPI Baud register (BAUD.CPOL) selects the polarity. The Clock Phase bit in the BAUD register programs the clock phase (BAUD.CPHA). These two parameters determine the edges of the clock signal on which data is driven and sampled. Each of the two parameters has two possible states, resulting in four possible combinations

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QSPI - Quad Serial Peripheral Interface

Note: The polarity/phase combinations are incompatible. Thus, the interfaced slave must use the same parameter values to communicate.

Table 32-2. SPI Transfer Mode

Clock Mode	BAUD.CPOL	BAUD.CPHA	Shift SCK Edge	Capture SCK Edge	SCK Inactive Level
0	0	0	Falling	Rising	Low
1	0	1	Rising	Falling	Low
2	1	0	Rising	Falling	High
3	1	1	Falling	Rising	High

Figure 32-3. QSPI Transfer Modes (BAUD.CPHA = 0, 8-bit transfer)

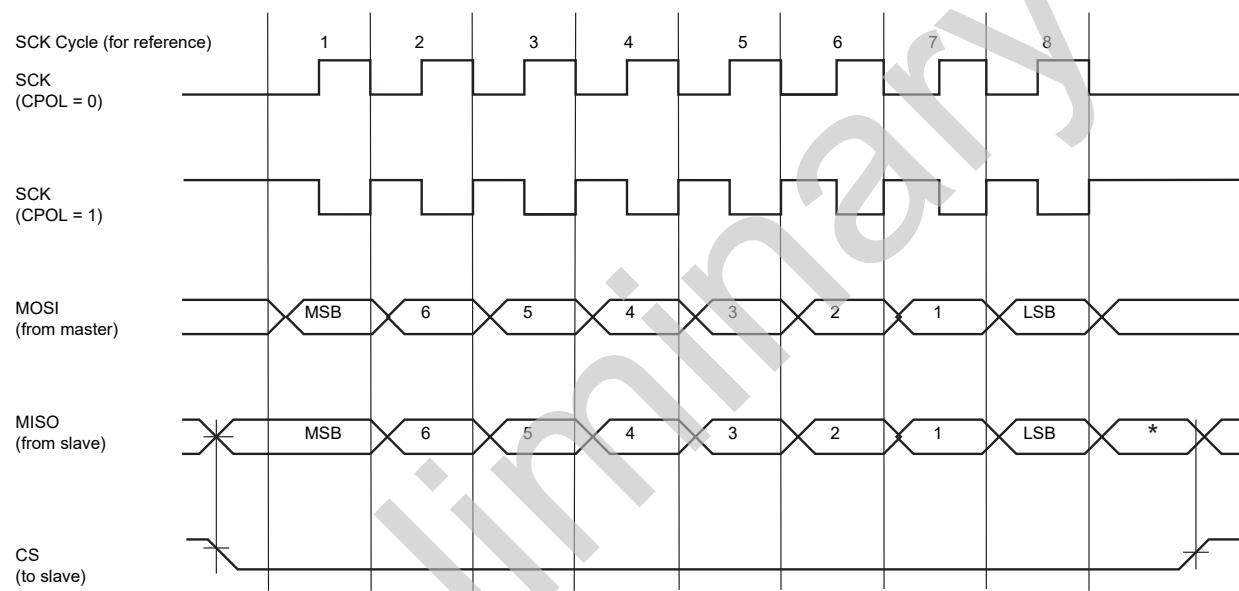
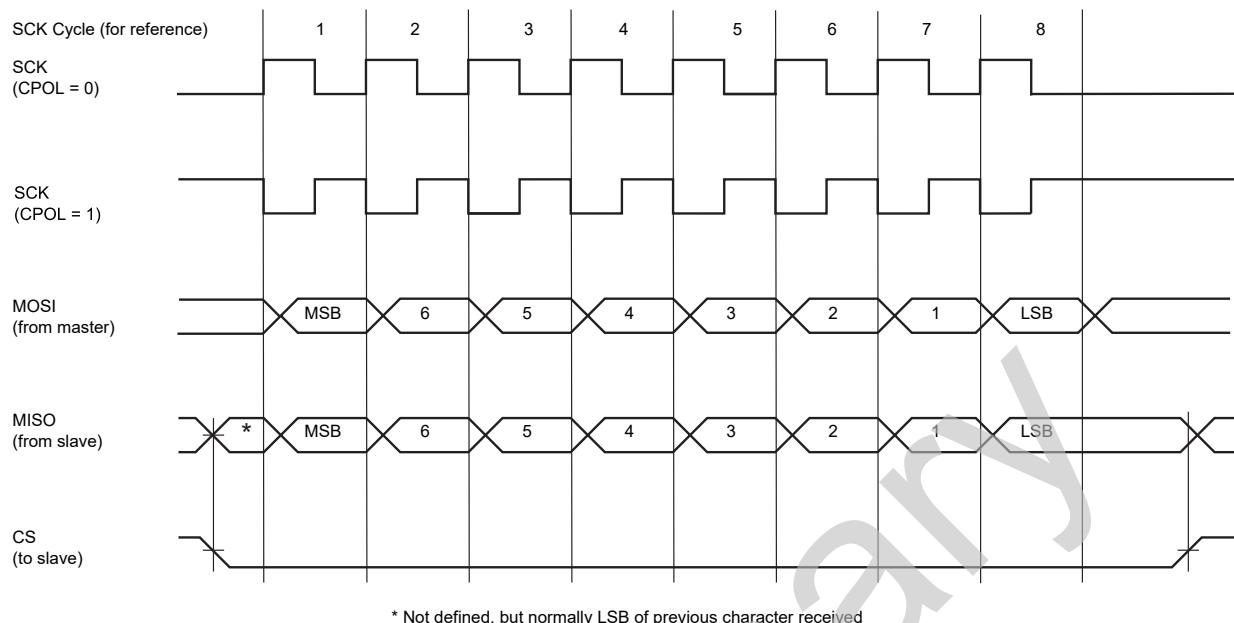


Figure 32-4. QSPI Transfer Modes (BAUD.CPHA = 1, 8-bit transfer)



* Not defined, but normally LSB of previous character received

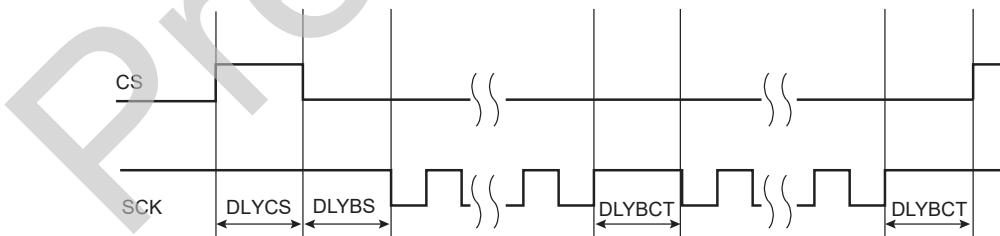
32.6.6 Transfer Delays

The QSPI supports several consecutive transfers while the chip select is active. Three delays can be programmed to modify the transfer waveforms:

- The delay between the inactivation and the activation of CS is programmed by writing the Minimum Inactive CS Delay bit field in the Control B register (CTRLB.DLYCS), allowing to tune the minimum time of CS at high level.
- The delay between consecutive transfers is programmed by writing the Delay Between Consecutive Transfers bit field in the Control B register (CTRLB.DLYBCT), allowing to insert a delay between two consecutive transfers. In Serial Memory mode, this delay is not programmable and DLYBCT settings are ignored.
- The delay before SCK is programmed by writing the Delay Before SCK bit field in the BAUD register (BAUD.DLYBS), allowing to delay the start of SPCK after the chip select has been asserted.

These delays allow the QSPI to be adapted to the interfaced peripherals and their speed and bus release time.

Figure 32-5. Programmable Delay



32.6.7 QSPI SPI Mode

In this mode, the QSPI acts as a regular SPI Master.

To activate this mode, the MODE bit in Control B register must be cleared (CTRLB.MODE=0).

32.6.7.1 SPI Mode Operations

The QSPI in standard SPI mode operates on the clock generated by the internal programmable baud rate generator. It fully controls the data transfers to and from the slave connected to the SPI bus. The QSPI drives the chip select line to the slave (CS) and the serial clock signal (SCK).

The QSPI features a single internal shift register and two holding registers: the Transmit Data Register (TXDATA) and the Receive Data Register (RXDATA). The holding registers maintain the data flow at a constant rate.

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After enabling the QSPI, a data transfer begins when the processor writes to the TXDATA. The written data is immediately transferred into the internal shift register and transfer on the SPI bus starts. While the data in the internal shift register is shifted on the MOSI line, the MISO line is sampled and shifted into the internal shift register. Receiving data cannot occur without transmitting data.

If new data is written in TXDATA during the transfer, it stays in TXDATA until the current transfer is completed. Then, the received data is transferred from the internal shift register to the RXDATA, the data in TXDATA is loaded into the internal shift register, and a new transfer starts.

The transfer of data written in TXDATA in the internal shift register is indicated by the Transmit Data Register Empty (DRE) bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE). When new data is written in TXDATA, this bit is cleared. The DRE bit is used to trigger the Transmit DMA channel.

The end of transfer is indicated by the Transmission Complete flag (INTFLAG.TXC). If the transfer delay for the last transfer was configured to be greater than 0 (CTRLB.DLYBCT), TXC is set after the completion of the delay. The module clock (CLK_QSPI_AHB) can be switched off at this time.

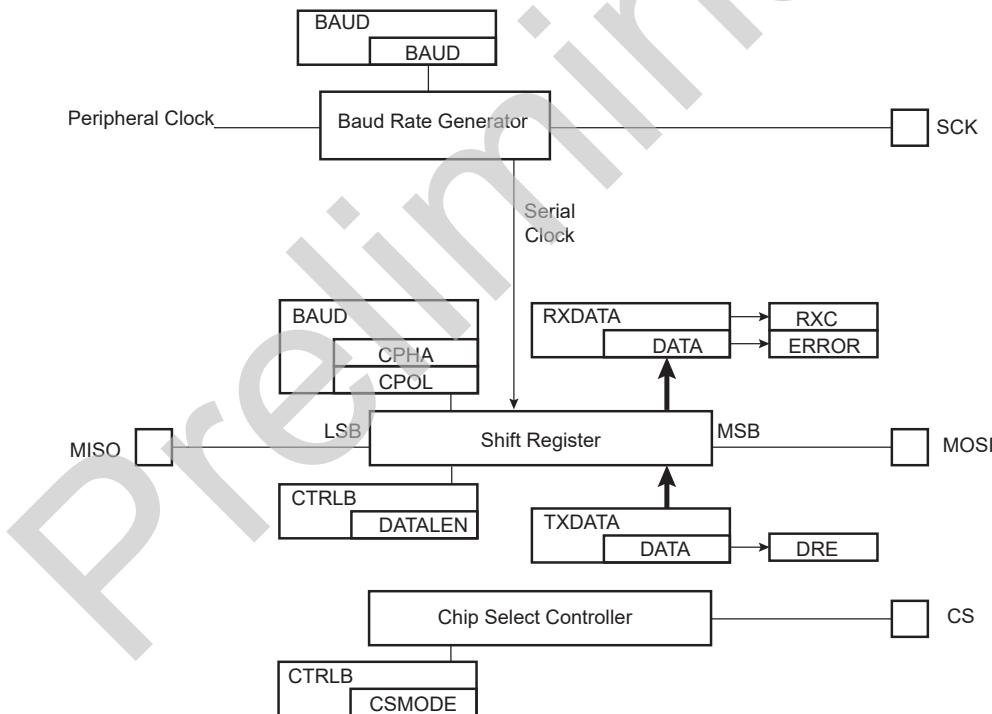
Ongoing transfer of received data from the internal shift register into RXDATA is indicated by the Receive Data Register Full flag (INTFLAG.RXC). When the received data is read, the RXC bit is cleared.

If the RXDATA has not been read before new data is received, the Overrun Error flag in INTFLAG register (INTFLAG.ERROR) is set. As long as this flag is set, data is loaded in RXDATA.

The SPI Mode Block Diagram shows a flow chart describing how transfers are handled.

32.6.7.2 SPI Mode Block Diagram

Figure 32-6. SPI Mode Block Diagram



32.6.7.3 SPI Mode Flow Diagram

Figure 32-7. SPI Mode Flow Diagram

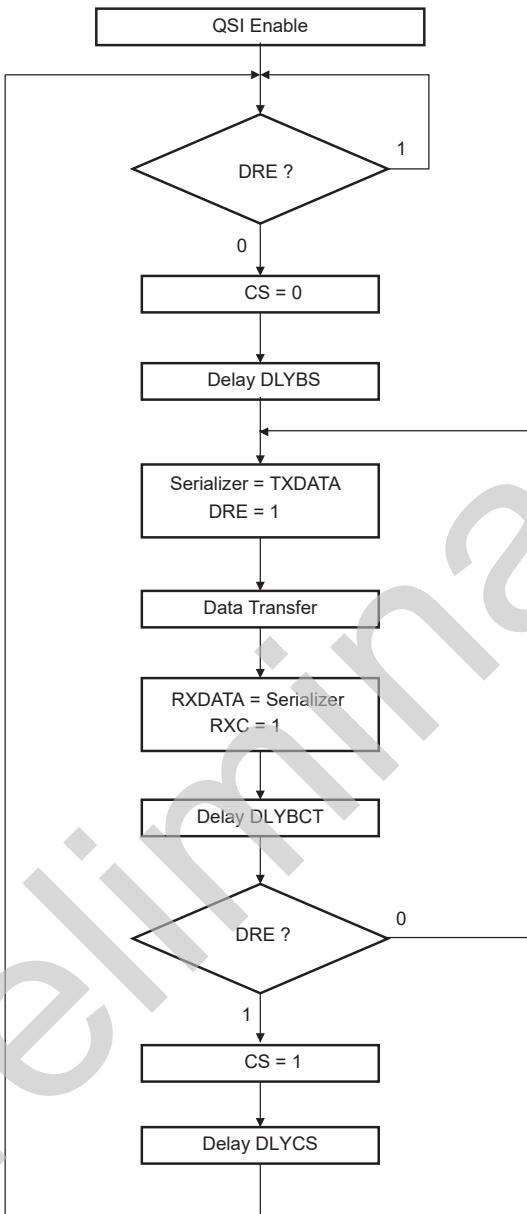
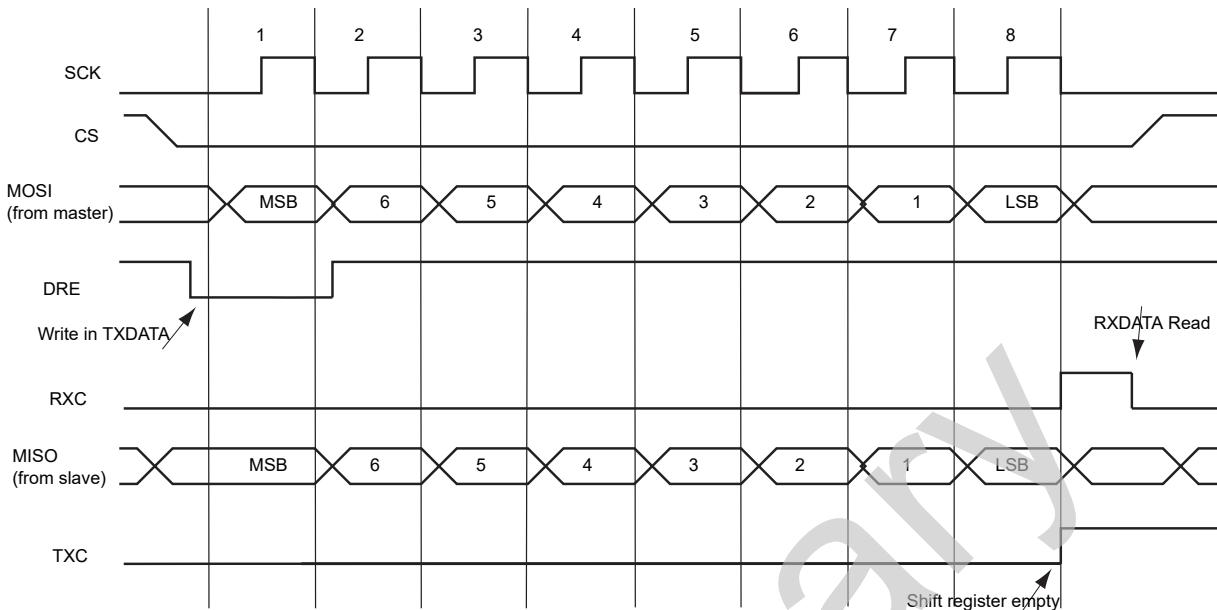


Figure 32-8. Interrupt Flags Behaviour



32.6.7.4 Peripheral Deselection with DMA

When the Direct Memory Access Controller is used, the Chip Select line will remain low during the whole transfer since the Transmit Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is managed by the DMA itself. The reloading of the TXDATA by the DMA is done as soon as INTFLAG.DRE flag is set. In this case, setting the Chip Select Mode bit field in the Control B register (CTRLB.CSMODE) to 0x1 is not mandatory.

However, it may happen that when other DMA channels connected to other peripherals are in use as well, the QSPI DMA could be delayed by another DMA transfer with a higher priority on the bus. Having DMA buffers in slower memories like flash memory or SDRAM (compared to fast internal SRAM), may lengthen the reload time of the TXDATA by the DMA as well. This means that TXDATA might not be reloaded in time to keep the Chip Select line low. In this case the Chip Select line may toggle between data transfer and according to some SPI Slave devices, and the communication might get lost. Writing CTRLB.CSMODE=0x1 can prevent this loss.

When CTRLB.CSMODE=0x0, the CS does not rise in all cases between two transfers on the same peripheral. During a transfer on a Chip Select, the INTFLAG.DRE flag is raised as soon as the content of the TXDATA is transferred into the internal shifter. When this flag is detected the TXDATA can be reloaded. If this reload occurs before the end of the current transfer and if the next transfer is performed on the same Chip Select as the current transfer, the Chip Select is not de-asserted between the two transfers. This may lead to difficulties for interfacing with some serial peripherals requiring the Chip Select to be de-asserted after each transfer. To facilitate interfacing with such devices, it is recommended to write CTRLB.CSMODE to 0x2.

32.6.7.5 Peripheral Deselection without DMA

During multiple data transfers on a Chip Select without the DMA, the TXDATA is loaded by the processor, and the Transmit Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) rises as soon as the content of the RXDATA is transferred into the internal shift register. When this flag is detected high, the TXDATA can be reloaded. If this reload-by-processor occurs before the end of the current transfer and if the next transfer is performed on the same Chip Select as the current transfer, the Chip Select is not de-asserted between the two transfers.

Depending on the application software handling the flags or servicing other interrupts or other tasks, the processor may not reload the TXDATA in time to keep the Chip Select active (low). A null Delay Between Consecutive Transfer bit field value in the CTRLB register (CTRLB.DLYBCT) will give even less time for the processor to reload the TXDATA. With some SPI slave peripherals, requiring the Chip Select line to remain active (low) during a full set of transfers might lead to communication errors.

To facilitate interfacing with such devices, the Chip Select Mode bit field in the CTRLB register (CTRLB.CSMODE) can be written to 0x1. This allows the Chip Select lines to remain in their current state (low = active) until the end of transfer is indicated by the Last Transfer bit in the CTROLA register (CTROLA.LASTXFER). Even if the TXDATA is not reloaded the Chip Select will remain active. To have the Chip Select line rise at the end of the last data transfer, the LASTXFER bit in the CTROLA must be set before writing the last data to transmit into the TXDATA.

32.6.8 QSPI Serial Memory Mode

In this mode the QSPI acts as a serial flash memory controller. The QSPI can be used to read data from the serial flash memory allowing the CPU to execute code from it (XIP execute in place). The QSPI can also be used to control the serial flash memory (Program, Erase, Lock, etc.) by sending specific commands. In this mode, the QSPI is compatible with single-bit SPI, Dual SPI and Quad SPI protocols.

To activate this mode, the MODE bit in Control B register must be set to one (CTRLB.MODE = 1).

In serial memory mode, data cannot be transferred by the TXDATA and the RXDATA, but by writing or reading the QSPI memory space (0x0400 0000 – 0x0500 0000).

32.6.8.1 Instruction Frame

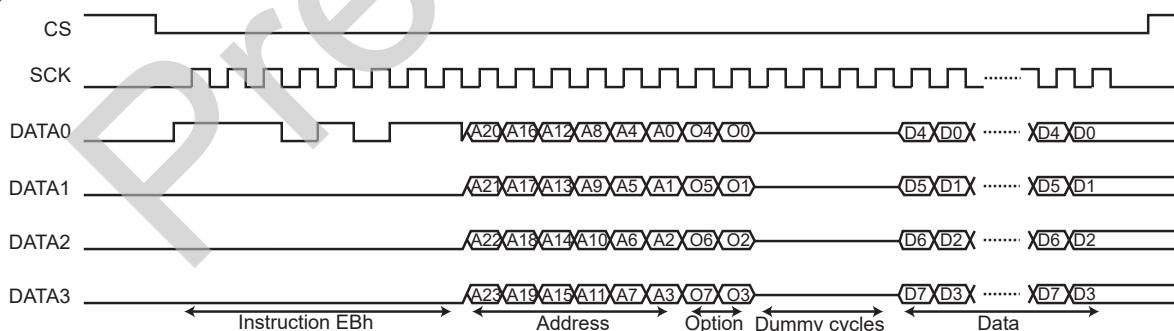
In order to control serial flash memories, the QSPI is able to sent instructions by the SPI bus (ex: READ, PROGRAM, ERASE, LOCK, etc.). Because instruction set implemented in serial flash memories is memory vendor dependant, the QSPI includes a complete instruction registers, which makes it very flexible and compatible with all serial flash memories.

An instruction frame includes:

- An instruction code (size: 8 bits). The instruction can be optional in some cases.
- An address (size: 24 bits or 32 bits). The address is optional but is required by instructions such as READ, PROGRAM, ERASE, LOCK. By default the address is 24 bits long, but it can be 32 bits long to support serial flash memories larger than 128 Mbit (16 Mbyte).
- An option code (size: 1/2/4/8 bits). The option code is optional but is useful for activate the “XIP mode” or the “Continuous Read Mode” for READ instructions, in some serial flash memory devices. These modes allow to improve the data read latency.
- Dummy cycles. Dummy cycles are optional but required by some READ instructions.
- Data bytes are optional. Data bytes are present for data transfer instructions such as READ or PROGRAM.

The instruction code, the address(option and the data can be sent with Single-bit SPI, Dual SPI or Quad SPI protocols.

Figure 32-9. Instruction Frame



32.6.8.2 Instruction Frame Sending

To send an instruction frame, the user must first configure the address to send by writing the field ADDR in the Instruction Address Register (INSTRADDR.ADDR). This step is required if the instruction frame includes an address and no data. When data is present, the address of the instruction is defined by the address of the data accesses in the QSPI memory space, and not by the INSTRADDR register.

If the instruction frame includes the instruction code and/or the option code, the user must configure the instruction code and/or the option code to send by writing the fields INST and OPTCODE bit fields in the Instruction Control Register (INSTRCTRL.OPTCODE, INSTRCTRL.INSTR).

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Then, the user must write the Instruction Frame Register (INSTRFRAME) to configure the instruction frame depending on which instruction must be sent. If the instruction frame does not include data, writing in this register triggers the send of the instruction frame in the QSPI. If the instruction frame includes data, the send of the instruction frame is triggered by the first data access in the QSPI memory space.

The instruction frame is configured by the following bits and fields of INSTRFRAME:

- WIDTH field is used to configure which data lanes are used to send the instruction code, the address, the option code and to transfer the data. It is possible to use two unidirectional data lanes (MISO-MOSI Single-bit SPI), two bidirectional data lanes (DATA0 - DATA1 Dual SPI) or four bidirectional data lanes (DATA0 - DATA3).

Table 32-3. WIDTH Encoding

INSTRFRAME	Instruction	Address/Option	Data
0	Single-bit SPI	Single-bit SPI	Single-bit SPI
1	Single-bit SPI	Single-bit SPI	Dual SPI
2	Single-bit SPI	Single-bit SPI	Quad SPI
3	Single-bit SPI	Dual SPI	Dual SPI
4	Single-bit SPI	Quad SPI	Quad SPI
5	Dual SPI	Dual SPI	Dual SPI
6	Quad SPI	Quad SPI	Quad SPI
7	Reserved		

- INSTREN bit enables sending an instruction code.
- ADDREN bit enables sending of an address after the instruction code.
- OPTCODEEN bit enables sending of an option code after the address.
- DATAEN bit enables the transfer of data (READ or PROGRAM instruction).
- OPTCODELEN field configures the option code length (0 → 1-bit / 1 → 2-bit / 2 → 4-bit / 3 → 8-bit). The value written in OPTCODELEN must be consistent with value written in the field WIDTH. For example: OPTCODELEN = 0 (1-bit option code) is not coherent with WIDTH = 6 (option code sent with QuadSPI protocol, thus the minimum length of the option code is 4-bit).
- ADDRLEN bit configures the address length (0 → 24 bits / 1 → 32 bits)
- TFRTYPE field defines which type of data transfer must be performed.
- DUMMYLEN field configures the number of dummy cycles when reading data from the serial flash memory. Between the address/options and the data, with some instructions, dummy cycles are inserted by the serial flash memory.

If data transfer is enabled, the user can access the serial memory by reading or writing the QSPI memory space following these rules:

- Reading from the serial memory, but not memory data (for example reading the JEDEC-ID or the STATUS), requires TFRTYPE to be written to 0x0.
- Reading from the serial memory, and particularly memory data, requires TFRTYPE to be written to '1'.
- Writing to the serial memory, but not memory data (for example writing the configuration or STATUS), requires TFRTYPE to be written to 0x2.
- Writing to the serial memory, and particularly memory data, requires TFRTYPE to be written to 0x3.

If TFRTYP has a value other than 0x1 and CTRLB.SMEMREG=0, the address sent in the instruction frame is the address of the first system bus accesses. The addresses of the subsequent access actions are not used by the QSPI. At each system bus access, an SPI transfer is performed with the same size. For example, a half-word system bus access leads to a 16-bit SPI transfer, and a byte system bus access leads to an 8-bit SPI transfer.

If CTRLB.SMEMREG=1, accesses are made via the QSPI registers and the address sent in the instruction frame is the address defined in the INSTRADDR register. Each time the INSTRFRAME or TXDATA registers are written, an SPI transfer is performed with a byte size. Another byte is read each time RXDATA register is read or written

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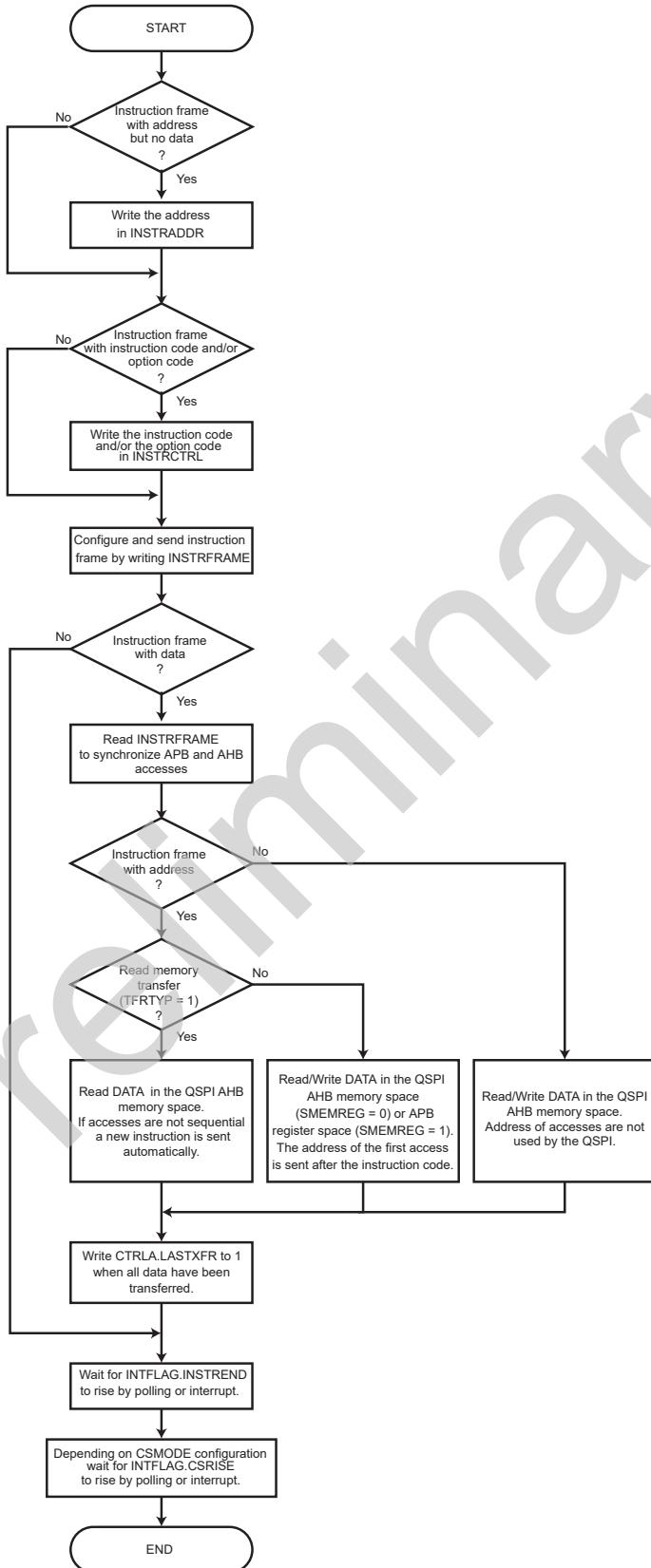
each time TXDATA register is written. The SPI transfer ends by writing the LASTXFER bit in Control A register (CTRLA.LASTXFER).

If TFRTYP=0x1, the address of the first instruction frame is the one of the first read access in the QSPI memory space. Each time the read accesses become non-sequential (addresses are not consecutive), a new instruction frame is sent with the last system bus access address. In this way, the system can read data at a random location in the serial memory. The size of the SPI transfers may differ from the size of the system bus read accesses.

When data transfer is not enabled, the end of the instruction frame is indicated when the INSTREND interrupt flag in the INTFLAG register is set. When data transfer is enabled, the user must indicate when data transfer is completed in the QSPI memory space by setting the bit LASTXFR in the CTRLA. The end of the instruction frame is indicated when the INSTREND interrupt flag in the INTFLAG register is set.

Preliminary

Figure 32-10. Instruction Transmission Flow Diagram



32.6.8.3 Read Memory Transfer

The user can access the data of the serial memory by sending an instruction with DATAEN=1 and TFRTYP=0x1 in the Instruction Frame register (INSTRFRAME).

In this mode the QSPI is able to read data at random address into the serial flash memory, allowing the CPU to execute code directly from it (XIP execute-in-place).

In order to fetch data, the user must first configure the instruction frame by writing the INSTRFRAME. Then data can be read at any address in the QSPI address space mapping. The address of the system bus read accesses match the address of the data inside the serial Flash memory.

When Fetch Mode is enabled, several instruction frames can be sent before writing the bit LASTXFR in the CTRLA. Each time the system bus read accesses become non-sequential (addresses are not consecutive), a new instruction frame is sent with the corresponding address.

32.6.8.4 Continuous Read Mode

The QSPI is compatible with Continuous Read Mode (CRM) which is implemented in some Serial Flash memories.

The CRM allows to reduce the instruction overhead by excluding the instruction code from the instruction frame. When CRM is activated in a Serial Flash memory (by a specific option code), the instruction code is stored in the memory. For the next instruction frames, the instruction code is not required, as the memory uses the stored one.

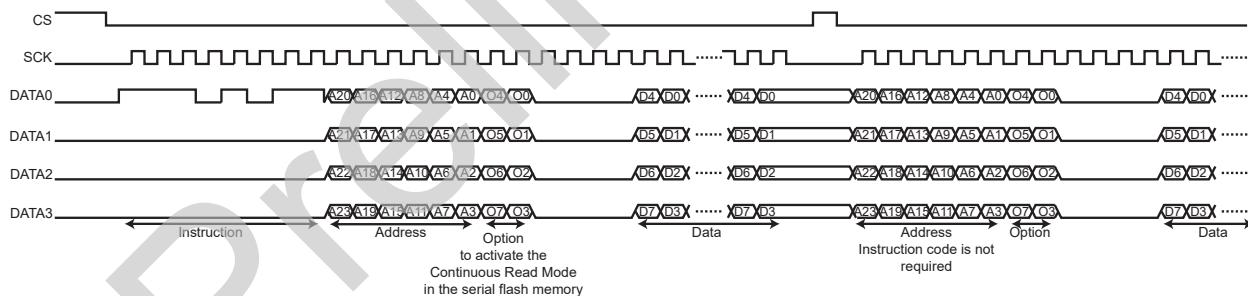
In the QSPI, CRM is used when reading data from the memory (INSTFRAME.TFRTYPE=0x1). The addresses of the system bus read accesses are often non-sequential, this leads to many instruction frames with always the same instruction code. By disabling the sending of the instruction code, the CRM reduces the access time of the data.

To be functional, this mode must be enabled in both the QSPI and the Serial Flash memory. The CRM is enabled in the QSPI by setting the CRM bit in the INSTRFRAME register (INSTFRAME.CRMODE=1, INSTFRAME.TFRTYPE must be 0x1). The CRM is enabled in the Serial Flash memory by sending a specific option code.



If CRM is not supported by the Serial Flash memory or disabled, the CRMODE bit must not be set. Otherwise, data read out the Serial Flash memory is not valid.

Figure 32-11. Continuous Read Mode



32.6.8.5 Instruction Frame Transmission Examples

All waveforms in the following examples describe SPI transfers in SPI Clock mode 0 (BAUD.CPOL=0 and BAUD.CPHA=0). All system bus accesses described below refer to the system bus address phase. System bus wait cycles and system bus data phases are not shown.

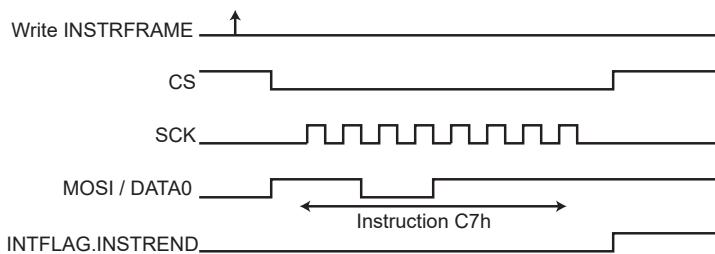
Example 32-1. Example 1

Instruction in Single-bit SPI, without address, without option, without data.

Command: CHIP ERASE (C7h).

- Write 0x0000_00C7 to INSTRCTRL register.
- Write 0x0000_0010 to INSTRFRAME register.
- Wait for INTFLAG.INSTREND to rise.

Figure 32-12. Instruction Transmission Waveform 1



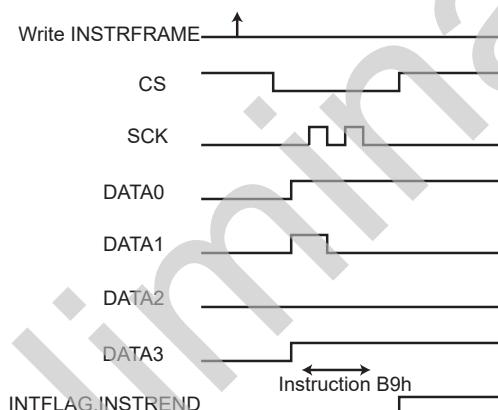
Example 32-2. Example 2

Instruction in Quad SPI, without address, without option, without data.

Command: POWER DOWN (B9h)

- Write 0x0000_00B9 to INSTRCTRL register.
- Write 0x0000_0016 to INSTRFRAME register.
- Wait for INTFLAG.INSTREND to rise.

Figure 32-13. Instruction Transmission Waveform 2



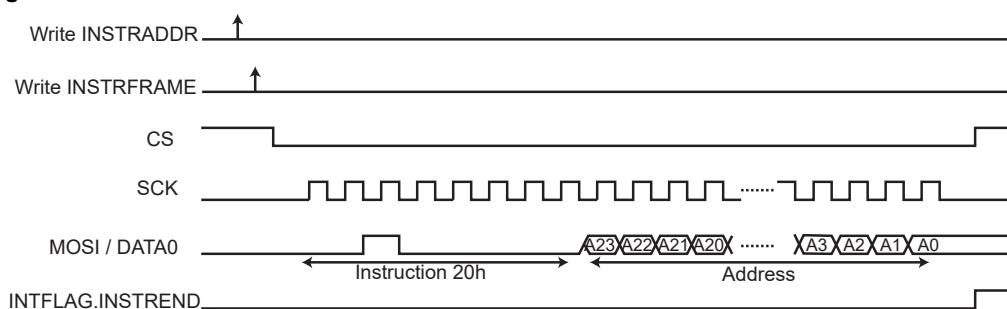
Example 32-3. Example 3

Instruction in Single-bit SPI, with address in Single-bit SPI, without option, without data.

Command: BLOCK ERASE (20h)

- Write the address (of the block to erase) to QSPI_AR.
- Write 0x0000_0020 to INSTRCTRL register.
- Write 0x0000_0030 to INSTRFRAME register.
- Wait for INTFLAG.INSTREND to rise.

Figure 32-14. Instruction Transmission Waveform 3



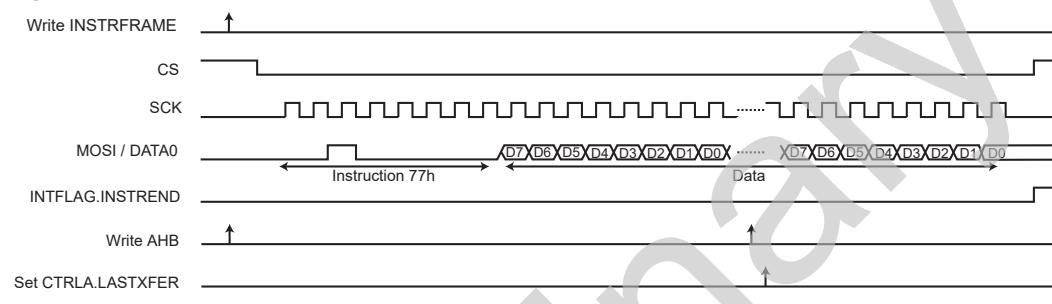
Example 32-4. Example 4

Instruction in Single-bit SPI, without address, without option, with data write in Single-bit SPI.

Command: SET BURST (77h)

- Write 0x0000_0077 to INSTRCTRL register.
- Write 0x0000_2090 to INSTRFRAME register.
- Read INSTRFRAME register (dummy read) to synchronize system bus accesses.
- Write data to the system bus memory space (0x0400_0000–0x0500_0000). The address of the system bus write accesses is not used.
- Write the LASTXFR bit in CTRLA register to '1'.
- Wait for INTFLAG.INSTREND to rise.

Figure 32-15. Instruction Transmission Waveform 4



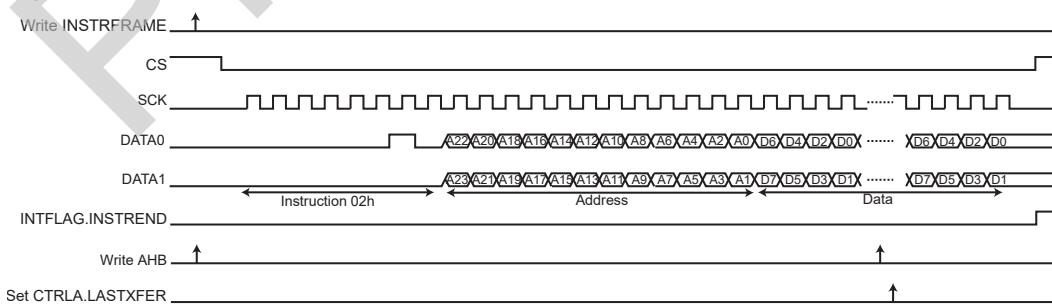
Example 32-5. Example 5

Instruction in Single-bit SPI, with address in Dual SPI, without option, with data write in Dual SPI.

Command: BYTE/PAGE PROGRAM (02h)

- Write 0x0000_0002 to INSTRCTRL register.
 - Write 0x0000_30B3 to INSTRFRAME register.
 - Read INSTRFRAME register (dummy read) to synchronize system bus accesses.
 - Write data to the QSPI system bus memory space (0x040 00000–0x0500_0000).
- The address of the first system bus write access is sent in the instruction frame.
- The address of the next system bus write accesses is not used.
- Write LASTXFR bit in CTRLA register to '1'.
 - Wait for INTFLAG.INSTREND to rise.

Figure 32-16. Instruction Transmission Waveform 5



Example 32-6. Example 6

Instruction in Single-bit SPI, with address in Single-bit SPI, without option, with data read in Quad SPI, with eight dummy cycles.

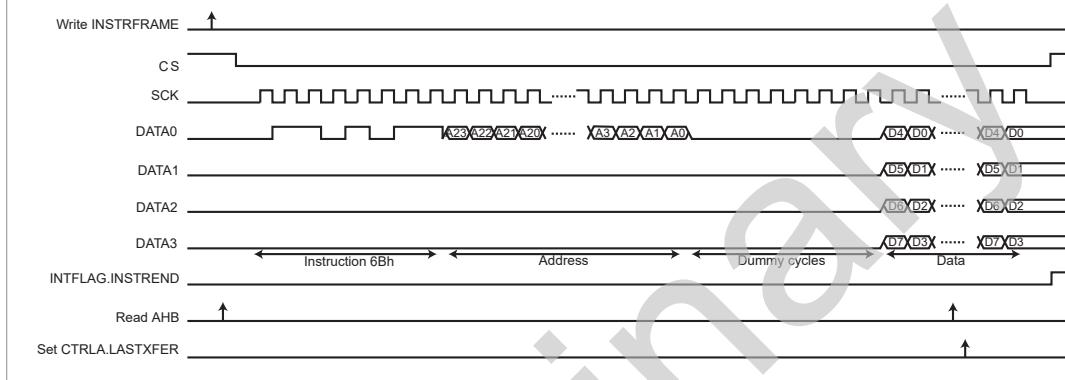
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Command: QUAD_OUTPUT READ ARRAY (6Bh)

- Write 0x0000_006B to INSTRCTRL register.
 - Write 0x0008_10B2 to INSTRFRAME register.
 - Read QSPI_IR (dummy read) to synchronize system bus accesses.
 - Read data from the QSPI system bus memory space (0x040 00000–0x0500_0000).
- The address of the first system bus read access is sent in the instruction frame.
- The address of the next system bus read accesses is not used.
- Write the LASTXFR bit in CTRLA register to '1'.
 - Wait for INTFLAG.INSTREND to rise.

Figure 32-17. Instruction Transmission Waveform 6



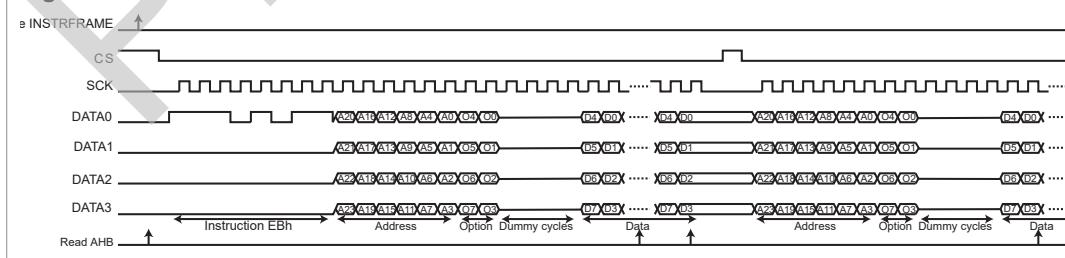
Example 32-7. Example 7

Instruction in Single-bit SPI, with address and option in Quad SPI, with data read from Quad SPI, with four dummy cycles, with fetch and continuous read.

Command: FAST READ QUAD I/O (EBh) - 8-BIT OPTION (0x30h)

- Write 0x0030_00EB to INSTRCTRL register.
 - Write 0x0004_33F4 to INSTRFRAME register.
 - Read INSTRFRAME register (dummy read) to synchronize system bus accesses.
 - Read data from the QSPI system bus memory space (0x040 00000–0x0500_0000).
- Fetch is enabled, the address of the system bus read accesses is always used.
- Write LASTXFR bit in CTRLA register to '1'.
 - Wait for INTFLAG.INSTREND to rise.

Figure 32-18. Instruction Transmission Waveform 7



Example 32-8. Example 8

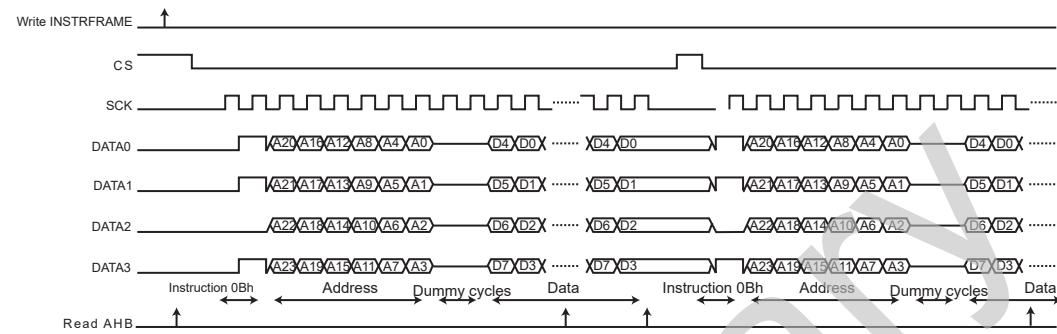
Instruction in Quad SPI, with address in Quad SPI, without option, with data read from Quad SPI, with two dummy cycles, with fetch.

Command: HIGH-SPEED READ (0Bh)

- Write 0x0000_000B to INSTRCTRL register.

- Write 0x0002_20B6 to INSTRFRAME register.
 - Read INSTRFRAME register (dummy read) to synchronize system bus accesses.
 - Read data in the QSPI system bus memory space (0x040 00000–0x0500_0000).
- Fetch is enabled, the address of the system bus read accesses is always used.
- Write LASTXFR bit in CTRLA register to '1'.
 - Wait for INTFLAG.INSTREND to rise.

Figure 32-19. Instruction Transmission Waveform 8



32.6.9 Scrambling/Unscrambling Function

The scrambling/unscrambling function cannot be performed on devices other than memories. Data is scrambled when written to memory and unscrambled when data is read.

The external data lines can be scrambled in order to prevent intellectual property data located in off-chip memories from being easily recovered by analyzing data at the package pin level of either the micro-controller or the QSPI slave device (e.g. memory).

The scrambling/unscrambling function can be enabled by writing a '1' to the ENABLE bit in the Scrambling Control register (SCRAMBCTRL.ENABLE).

The scrambling and unscrambling are performed on-the-fly without impacting the throughput.

The scrambling method depends on the user-configurable Scrambling User Key in the Scrambling Key register (SCRAMBKEY.KEY). This register is only accessible in write mode.

By default, the scrambling and unscrambling algorithm includes the scrambling user key, plus a device-dependent random value. This random value is not included when the Scrambling/Unscrambling Random Value Disable bit in the Scrambling Mode register (SCRAMBCTRL.RANDOMDIS) is written to '1'.

The random value is neither user configurable nor readable. If SCRAMBCTRL.RANDOMDIS=0, data scrambled by a given circuit cannot be unscrambled by a different circuit.

If SCRAMBCTRL.RANDOMDIS=1, the scrambling/unscrambling algorithm includes only the scrambling user key, making it possible to manage data by different circuits.

The scrambling user key must be securely stored in a reliable non-volatile memory in order to recover data from the off-chip memory. Any data scrambled with a given key cannot be recovered if the key is lost.

32.6.10 DMA Operation

The QSPI generates the following DMA requests:

- Data received (RX): The request is set when data is available in the RXDATA register, and cleared when RXDATA is read.
- Data transmit (TX): The request is set when the transmit buffer (TXDATA) is empty, and cleared when TXDATA is written.

Note: If DMA and RX memory modes are selected, a QSPI memory space read operation is required to force the first triggering.

If the CPU accesses the registers which are source of DMA request set/clear condition, the DMA request can be lost or the DMA transfer can be corrupted.

32.6.11 Interrupts

The QSPI has the following interrupt source:

- Interrupt Request (INTREQ): Indicates that at least one bit in the Interrupt Flag Status and Clear register (INTFLAG) is set to '1'.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the QSPI is reset. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated.

32.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0							ENABLE	SWRST
		15:8								
		23:16								
		31:24								LASTXFER
0x04	CTRLB	7:0			CSMODE[1:0]	SMEMREG	WDRBT	LOOPEN	MODE	
		15:8								DATALEN[3:0]
		23:16			DLYBCT[7:0]					
		31:24			DLYCS[7:0]					
0x08	BAUD	7:0							CPHA	CPOL
		15:8			BAUD[7:0]					
		23:16			DLYBS[7:0]					
		31:24								
0x0C	RXDATA	7:0			DATA[7:0]					
		15:8			DATA[15:8]					
		23:16								
		31:24								
0x10	TXDATA	7:0			DATA[7:0]					
		15:8			DATA[15:8]					
		23:16								
		31:24								
0x14	INTENCLR	7:0				ERROR	TXC	DRE	RXC	
		15:8					INSTREND			CSRISE
		23:16								
		31:24								
0x18	INTENSET	7:0				ERROR	TXC	DRE	RXC	
		15:8					INSTREND			CSRISE
		23:16								
		31:24								
0x1C	INTFLAG	7:0				ERROR	TXC	DRE	RXC	
		15:8					INSTREND			CSRISE
		23:16								
		31:24								
0x20	STATUS	7:0						ENABLE		
		15:8						CSSTATUS		
		23:16								
		31:24								
0x24 ... 0x2F	Reserved									
0x30	INSTRADDR	7:0			ADDR[7:0]					
		15:8			ADDR[15:8]					
		23:16			ADDR[23:16]					
		31:24			ADDR[31:24]					
0x34	INSTRCTRL	7:0			INSTR[7:0]					
		15:8								
		23:16			OPTCODE[7:0]					
		31:24								
0x38	INSTRFRAME	7:0	DATAEN	OPTCODEEN	ADDREN	INSTREN			WIDTH[2:0]	
		15:8	DDREN	CRMODE	TFRTYPE[1:0]			ADDRLEN	OPTCODELEN[1:0]	
		23:16						DUMMYLEN[4:0]		
		31:24								
0x3C ... 0x3F	Reserved									

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x40	SCRAMBCTRL	7:0							RANDOMDIS	ENABLE
		15:8								
		23:16								
		31:24								
0x44	SCRAMBKEY	7:0					KEY[7:0]			
		15:8					KEY[15:8]			
		23:16					KEY[23:16]			
		31:24					KEY[31:24]			

32.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

See *Peripheral Access Controller (PAC)* from Related Links.

Some registers are enable-protected, meaning they can only be written when the QSPI is disabled. Enable-protection is denoted by the Enable-Protected property in each individual register description.

Related Links

- 25. Peripheral Access Controller (PAC)

32.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: -

Control A

Bit	31	30	29	28	27	26	25	24	
Access								LASTXFER	
Reset								W	0
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
Access									
Reset									
Bit	7	6	5	4	3	2	1	0	
Access							ENABLE	SWRST	
Reset							R/W	W	0

Bit 24 – LASTXFER Last Transfer

0: No effect.

1: The chip select will be de-asserted after the character written in TD has been transferred.

Bit 1 – ENABLE Enable

Writing a '0' to this bit disables the QSPI.

Writing a '1' to this bit enables the QSPI to transfer and receive data.

As soon as ENABLE is reset, QSPI finishes its transfer.

All pins are set in input mode and no data is received or transmitted.

If a transfer is in progress, the transfer is finished before the QSPI is disable.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the QSPI. A software-triggered hardware reset of the QSPI interface is performed.

DMAC channels are not affected by software reset.

32.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Control B

Bit	31	30	29	28	27	26	25	24
DLYCS[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DLYBCT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DATALEN[3:0]								
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
CSMODE[1:0] SMEMREG WDRBT LOOPEN MODE								
Access		R/W						
Reset		0	0	0	0	0	0	0

Bits 31:24 – DLYCS[7:0] Minimum Inactive CS Delay

This bit field defines the minimum delay between the inactivation and the activation of CS. The DLYCS time guarantees the slave minimum deselect time.

If DLYCS is 0x00, one CLK_QSPI_AHB period will be inserted by default.

Otherwise, the following equation determines the delay:

$$\text{DLYCS} = \text{Minimum inactive} \times \text{fperipheral clock}$$

Bits 23:16 – DLYBCT[7:0] Delay Between Consecutive Transfers

This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT=0x00, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers. In Serial Memory mode (MODE=1), DLYBCT is ignored and no delay is inserted. Otherwise, the following equation determines the delay:

$$\text{DLYBCT} = (\text{Delay Between Consecutive Transfers} \times \text{fperipheral clock}) / 32$$

Bits 11:8 – DATALEN[3:0] Data Length

The DATALEN field determines the number of data bits transferred. Reserved values should not be used.

Value	Name	Description
0x0	8BITS	8-bits transfer
0x1	9BITS	9-bits transfer
0x2	10BITS	10-bits transfer
0x3	11BITS	11-bits transfer
0x4	12BITS	12-bits transfer
0x5	13BITS	13-bits transfer
0x6	14BITS	14-bits transfer
0x7	15BITS	15-bits transfer
0x8	16BITS	16-bits transfer
0x9–0xFF		Reserved

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Bits 5:4 – CSMODE[1:0] Chip Select Mode

The CSMODE field determines how the chip select is de-asserted.

Value	Name	Description
0x0	NORELOAD	The chip select is de-asserted if TD has not been reloaded before the end of the current transfer.
0x1	LASTXFER	The chip select is de-asserted when the bit LASTXFER is written at 1 and the character written in TD has been transferred.
0x2	SYSTEMATICALLY	The chip select is de-asserted systematically after each transfer.
0x3		Reserved

Bit 3 – SMEMREG Serial Memory Register Mode

Value	Description
0	Serial memory registers are written via AHB access.
1	Serial memory registers are written via APB access. Reset the QSPI.

Bit 2 – WDRBT Wait Data Read Before Transfer

This bit determines the Wait Data Read Before Transfer option.

Bit 1 – LOOPEN Local Loopback Enable

This bit defines if the Local Loopback is enabled or disabled.

LOOPEN controls the local loopback on the data serializer for testing in SPI Mode only. (MISO is internally connected on MOSI).

Value	Description
0	Local Loopback is disabled.
1	Local Loopback is enabled.

Bit 0 – MODE Serial Memory Mode

This bit defines if the QSPI is in SPI Mode or Serial Memory Mode.

Value	Name	Description
0	SPI	SPI operating mode
1	MEMORY	Serial Memory operating mode

32.8.3 Baud Rate

Name: BAUD
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit								
Access	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0
Bit								
Access	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0
Bit								
Access	7	6	5	4	3	2	1	0
Reset							R/W	R/W
							0	0

Bits 23:16 – DLYBS[7:0] Delay Before SCK

This field defines the delay from CS valid to the first valid SCK transition.

When DLYBS equals zero, the CS valid to SCK transition is 1/2 the SCK clock period.

Otherwise, the following equation determines the delay:

Equation 32-1. Delay Before SCK

$$\text{Delay Before SCK} = \frac{\text{DLYBS}}{\text{MCK}}$$

Bits 15:8 – BAUD[7:0] Serial Clock Baud Rate

The QSPI uses a modulus counter to derive the SCK baud rate from the module clock (MCK) CLK_QSPI_AHB. The Baud rate is selected by writing a value from 1 to 255 in the BAUD field. The following equation determines the SCK baud rate:

Equation 32-2. SCK Baud Rate

$$\text{SCK Baud Rate} = \frac{\text{MCK}}{(\text{BAUD} + 1)}$$

Bit 1 – CPHA Clock Phase

CPHA determines which edge of SCK causes data to change and which edge causes data to be captured. CPHA is used with CPOL to produce the required clock/data relationship between master and slave devices.

Value	Description
0	Data is captured on the leading edge of SCK and changed on the following edge of SCK.
1	Data is changed on the leading edge of SCK and captured on the following edge of SCK.

Bit 0 – CPOL Clock Polarity

CPOL is used to determine the inactive state value of the serial clock (SCK). It is used with CPHA to produce the required clock/data relationship between master and slave devices.

Value	Description
0	The inactive state value of SCK is logic level zero.

PIC32CX-BZ2 and WBZ45 Family

QSPI - Quad Serial Peripheral Interface

Value	Description
0	The inactive state value of SCK is logic level 'one'.

Preliminary

32.8.4 Receive Data

Name: RXDATA
Offset: 0x0C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
				DATA[15:8]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				DATA[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] Receive Data

Data received by the QSPI is stored in this register right-justified. Unused bits read zero.

32.8.5 Transmit Data

Name: TXDATA
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
				DATA[15:8]				
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				DATA[7:0]				
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] Transmit Data

Data to be transmitted by the QSPI is stored in this register. Information to be transmitted must be written to the transmit data register in a right-justified format.

32.8.6 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					INSTREND			
Reset					R/W		R/W	
Bit	7	6	5	4	3	2	1	0
Access					ERROR	TXC	DRE	RXC
Reset					R/W	R/W	R/W	R/W

Bit 10 – INSTREND Instruction End Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The INSTREND interrupt is disabled.
1	The INSTREND interrupt is enabled.

Bit 8 – CSRise Chip Select Rise Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The CSRise interrupt is disabled.
1	The CSRise interrupt is enabled.

Bit 3 – ERROR Overrun Error Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The ERROR interrupt is disabled.
1	The ERROR interrupt is enabled.

Bit 2 – TXC Transmission Complete Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The TXC interrupt is disabled.
1	The TXC interrupt is enabled.

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Bit 1 – DRE Transmit Data Register Empty Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The DRE interrupt is disabled.
1	The DRE interrupt is enabled.

Bit 0 – RXC Receive Data Register Full Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' will clear the corresponding interrupt request.

Value	Description
0	The RXC interrupt is disabled.
1	The RXC interrupt is enabled.

32.8.7 Interrupt Enable Set

Name: INTENSET
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection

Access	Bit 31	30	29	28	27	26	25	24
Reset								
Access	Bit 23	22	21	20	19	18	17	16
Reset								
Access	Bit 15	14	13	12	11	10	9	8
Reset					INSTREND	R/W	R/W	
Access	Bit 7	6	5	4	3	ERROR	TXC	DRE
Reset					R/W	R/W	R/W	R/W

Bit 10 – INSTREND Instruction End Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value Description

0	The INSTREND interrupt is disabled.
1	The INSTREND interrupt is enabled.

Bit 8 – CSRise Chip Select Rise Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value Description

0	The CSRise interrupt is disabled.
1	The CSRise interrupt is enabled.

Bit 3 – ERROR Overrun Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value Description

0	The ERROR interrupt is disabled.
1	The ERROR interrupt is enabled.

Bit 2 – TXC Transmission Complete Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value Description

0	The TXC interrupt is disabled.
1	The TXC interrupt is enabled.

PIC32CX-BZ2 and WBZ45 Family

QSPI - Quad Serial Peripheral Interface

Bit 1 – DRE Transmit Data Register Empty Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value	Description
0	The DRE interrupt is disabled.
1	The DRE interrupt is enabled.

Bit 0 – RXC Receive Data Register Full Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' will set the corresponding interrupt request.

Value	Description
0	The RXC interrupt is disabled.
1	The RXC interrupt is enabled.

32.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					INSTREND	R/W	R/W	
Reset					0	0	0	
Bit	7	6	5	4	3	2	1	0
Access				ERROR	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 10 – INSTREND Instruction End

This bit is set when an Instruction End has been detected.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 8 – CSRISE Chip Select Rise

The bit is set when a Chip Select Rise has been detected.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 3 – ERROR Overrun Error

This bit is set when an ERROR has occurred.

An ERROR occurs when RXDATA is loaded at least twice from the serializer.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the flag.

Bit 2 – TXC Transmission Complete

0: As soon as data is written in TXDATA.

1: TXDATA and internal shifter are empty. If a transfer delay has been defined, TXC is set after the completion of such delay.

Bit 1 – DRE Transmit Data Register Empty

0: Data has been written to TXDATA and not yet transferred to the serializer.

1: The last data written in the TXDATA has been transferred to the serializer.

This bit is '0' when the QSPI is disabled or at reset.

The bit is set as soon as ENABLE bit is set.

Bit 0 – RXC Receive Data Register Full

0: No data has been received since the last read of RXDATA.

PIC32CX-BZ2 and WBZ45 Family

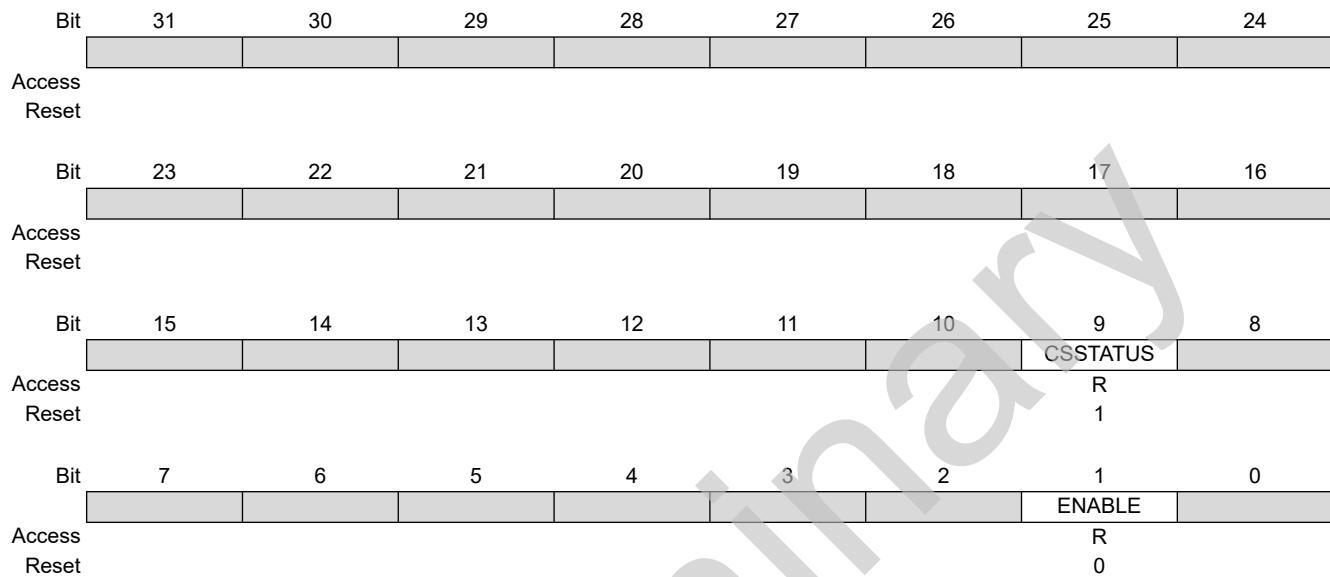
QSPI - Quad Serial Peripheral Interface

1: Data has been received and the received data has been transferred from the serializer to RXDATA since the last read of RXDATA.

Preliminary

32.8.9 Status

Name: STATUS
Offset: 0x20
Reset: 0x00000200
Property: -



Bit 9 – CSSTATUS Chip Select

Value	Description
0	Chip Select is asserted.
1	Chip Select is not asserted.

Bit 1 – ENABLE Enable

Value	Description
0	QSPI is disabled.
1	QSPI is enabled.

32.8.10 Instruction Address

Name: INSTRADDR
Offset: 0x30
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
ADDR[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ADDR[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Instruction Address

Address to send to the serial flash memory in the instruction frame.

32.8.11 Instruction Code

Name: INSTRCTRL
Offset: 0x34
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – OPTCODE[7:0] Option Code

These bits define the option code to send to the serial flash memory.

Bits 7:0 – INSTR[7:0] Instruction Code

Instruction code to send to the serial flash memory.

32.8.12 Instruction Frame

Name: INSTRFRAME
Offset: 0x38
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					DUMMYLEN[4:0]			
Reset				R/W	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	DDREN	CRMODE	TFRTYPE[1:0]		ADDRLEN	OPTCODELEN[1:0]		
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	0	0	0	0	0	0	0	0
Access	DATAEN	OPTCODEEN	ADDREN	INSTREN		WIDTH[2:0]		
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 20:16 – DUMMYLEN[4:0] Dummy Cycles Length

The DUMMYLEN field defines the number of dummy cycles required by the serial Flash memory before data transfer.

Bit 15 – DDREN Double Data Rate Enable

Value	Description
0	Double Data Rate operating mode is disabled.
1	Double Data Rate operating mode is enabled.

Bit 14 – CRMODE Continuous Read Mode

This bit defines if the Continuous Read Mode is enabled or disabled.

Value	Description
0	Continuous Read Mode is disabled.
1	Continuous Read Mode is enabled.

Bits 13:12 – TFRTYPE[1:0] Data Transfer Type

These bits define the data type transfer.

Value	Name	Description
0x0	READ	Read transfer from the serial memory.Scrambling is not performed.Read at random location (fetch) in the serial flash memory is not possible.
0x1	READMEMORY	Read data transfer from the serial memory.If enabled, scrambling is performed.Read at random location (fetch) in the serial flash memory is possible.
0x2	WRITE	Write transfer into the serial memory.Scrambling is not performed.
0x3	WRITEMEMORY	Write data transfer into the serial memory. If enabled, scrambling is performed.

Bit 10 – ADDRLEN Address Length

The ADDRLEN bit determines the length of the address.

Value	Name	Description
0x0	24BITS	24-bits address length
0x1	32BITS	32-bits address length

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Bits 9:8 – OPTCODELEN[1:0] Option Code Length

The OPTCODELEN field determines the length of the option code. The value written in OPTCODELEN must be coherent with value written in the field WIDTH. For example: OPTCODELEN=0 (1-bit option code) is not coherent with WIDTH=6 (option code sent with QuadSPI protocol, thus the minimum length of the option code is 4-bit).

Value	Name	Description
0x0	1BIT	1-bit length option code
0x1	2BITS	2-bits length option code
0x2	4BITS	4-bits length option code
0x3	8BITS	8-bits length option code

Bit 7 – DATAEN Data Enable

Value	Description
0	No data is sent/received to/from the serial flash memory.
1	Data is sent/received to/from the serial flash memory.

Bit 6 – OPTCODEEN Option Enable

Value	Description
0	The option is not sent to the serial flash memory
1	The option is sent to the serial flash memory.

Bit 5 – ADDREN Address Enable

Value	Description
0	The transfer address is not sent to the serial flash memory.
1	The transfer address is sent to the serial flash memory.

Bit 4 – INSTREN Instruction Enable

Value	Description
0	The instruction is not sent to the serial flash memory.
1	The instruction is sent to the serial flash memory.

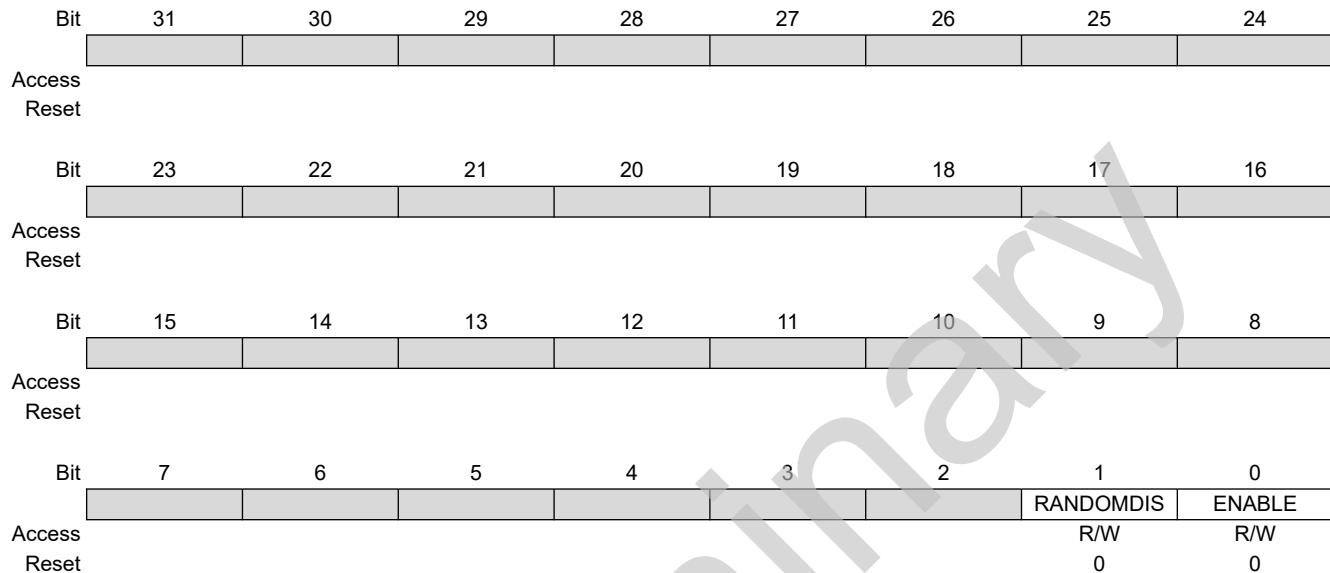
Bits 2:0 – WIDTH[2:0] Instruction Code, Address, Option Code and Data Width

This field defines the width of the instruction code, the address, the option and the data.

Value	Name	Description
0x0	SINGLE_BIT_SPI	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Single-bit SPI
0x1	DUAL_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Dual SPI
0x2	QUAD_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Quad SPI
0x3	DUAL_IO	Instruction: Single-bit SPI / Address-Option: Dual SPI / Data: Dual SPI
0x4	QUAD_IO	Instruction: Single-bit SPI / Address-Option: Quad SPI / Data: Quad SPI
0x5	DUAL_CMD	Instruction: Dual SPI / Address-Option: Dual SPI / Data: Dual SPI
0x6	QUAD_CMD	Instruction: Quad SPI / Address-Option: Quad SPI / Data: Quad SPI
0x7		Reserved

32.8.13 Scrambling Mode

Name: SCRAMBCTRL
Offset: 0x40
Reset: 0x00000000
Property: PAC Write-Protection



Bit 1 – RANDOMDIS Scrambling/Unscrambling Random Value Disable

Value	Description
0	The scrambling/unscrambling algorithm includes the scrambling user key plus a random value that may differ from chip to chip.
1	The scrambling/unscrambling algorithm includes only the scrambling user key.

Bit 0 – ENABLE Scrambling/Unscrambling Enable

This bit defines if the scrambling/unscrambling is enabled or disabled.

Value	Description
0	Scrambling/unscrambling is disabled.
1	Scrambling/unscrambling is enabled.

32.8.14 Scrambling Key

Name: SCRAMBKEY
Offset: 0x44
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
KEY[31:24]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEY[23:16]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEY[15:8]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEY[7:0]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – KEY[31:0] Scrambling User Key
 This field defines the user key value.

33. Configurable Custom Logic (CCL)

33.1 Overview

The Configurable Custom Logic (CCL) is a programmable logic peripheral which can be connected to the device pins, to events, or to other internal peripherals. This allows the user to eliminate logic gates for simple glue logic functions on the PCB.

Each LookUp Table (LUT) consists of three inputs, a truth table, an optional synchronizer/filter, and an optional edge detector. Each LUT can generate an output as a user programmable logic expression with three inputs. Inputs can be individually masked.

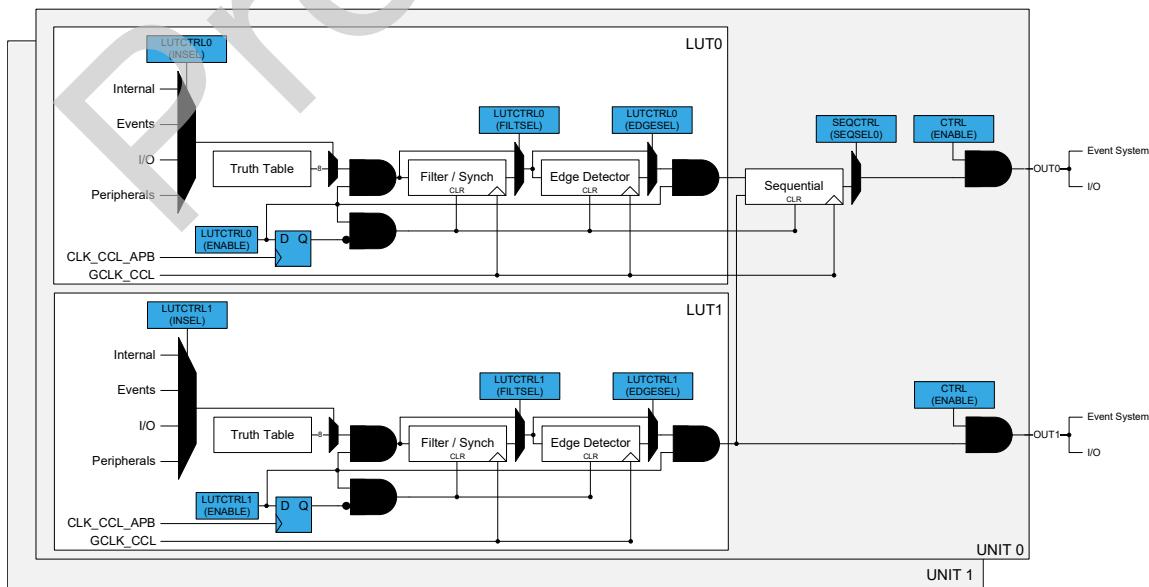
The output can be combinatorially generated from the inputs, and can be filtered to remove spikes. Optional sequential logic can be used. The inputs of the sequential module are individually controlled by two independent, adjacent LUT (LUT0/LUT1) outputs, enabling complex waveform generation.

33.2 Features

- Glue logic for general purpose PCB design
- Two programmable LookUp Tables (LUTs)
- Combinatorial logic functions: AND, NAND, OR, NOR, XOR, XNOR, NOT
- Sequential logic functions: Gated D Flip-Flop, JK Flip-Flop, gated D Latch, RS Latch
- Flexible LUT inputs selection:
 - I/Os
 - Events
 - Internal peripherals
 - Subsequent LUT output
- Output can be connected to the I/O pins or the Event System
- Optional synchronizer, filter, or edge detector available on each LUT output

33.3 Block Diagram

Figure 33-1. Configurable Custom Logic



33.4 Signal Description

Pin Name	Type	Description
OUT[1:0]	Digital output	Output from lookup table
IN[5:0]	Digital input	Input to lookup table

For details on the pin mapping for this peripheral, see *I/O Ports and Peripheral Pin Select (PPS)* from Related Links. One signal can be mapped on several pins.

Related Links

- 5. [I/O Ports and Peripheral Pin Select \(PPS\)](#)

33.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

33.5.1 I/O Lines

The CCL can take inputs and generate output through I/O pins. For this to function properly, the I/O pins must be configured to be used by a Look Up Table (LUT).

33.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. Events connected to the event system can trigger other operations in the system without exiting Sleep modes.

33.5.3 Clocks

A generic clock (GCLK_CCL) is optionally required to clock the CCL. This clock must be configured and enabled in the Generic Clock Controller (GCLK) before using input events, filter, edge detection or sequential logic. GCLK_CCL is required when input events, a filter, an edge detector, or a sequential sub-module is enabled.

This generic clock is asynchronous to the user interface clock (PB2_CLK).

33.5.4 DMA

Not applicable.

33.5.5 Interrupts

Not applicable.

33.5.6 Events

The CCL can use events from other peripherals and generate events that can be used by other peripherals. For this feature to function, the events have to be configured properly. Refer to the Related Links below for more information about the event users and event generators.

Related Links

- 27. [Event System \(EVSYS\)](#)

33.5.7 Debug Operation

When the CPU is halted in Debug mode the CCL continues normal operation. However, the CCL cannot be halted when the CPU is halted in Debug mode. If the CCL is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

33.5.8 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC). See *Peripheral Access Controller (PAC)* from Related Links.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

PAC write protection does not apply to accesses through an external debugger.

Related Links

[25. Peripheral Access Controller \(PAC\)](#)

33.5.9 Analog Connections

Not applicable.

33.6 Functional Description

33.6.1 Principle of Operation

Configurable Custom Logic (CCL) is a programmable logic block that can use the device port pins, internal peripherals, and the internal Event System as both input and output channels. The CCL can serve as glue logic between the device and external devices. The CCL can eliminate the need for external logic component and can also help the designer overcome challenging real-time constraints by combining core independent peripherals in clever ways to handle the most time critical parts of the application independent of the CPU.

33.6.2 Operation

33.6.2.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the corresponding even LUT is disabled (LUTCTRLx.ENABLE=0):

- Sequential Selection bits in the Sequential Control x (SEQCTRLx.SEQSEL) register

The following registers are enable-protected, meaning that they can only be written when the corresponding LUT is disabled (LUTCTRLx.ENABLE=0):

- LUT Control x (LUTCTRLx) register, except the ENABLE bit

Enable-protected bits in the LUTCTRLx registers can be written at the same time as LUTCTRLx.ENABLE is written to '1', but not at the same time as LUTCTRLx.ENABLE is written to '0'.

Enable-protection is denoted by the Enable-Protected property in the register description.

33.6.2.2 Enabling, Disabling, and Resetting

The CCL is enabled by writing a '1' to the Enable bit in the Control register (CTRL.ENABLE). The CCL is disabled by writing a '0' to CTRL.ENABLE.

Each LUT is enabled by writing a '1' to the Enable bit in the LUT Control x register (LUTCTRLx.ENABLE). Each LUT is disabled by writing a '0' to LUTCTRLx.ENABLE.

The CCL is reset by writing a '1' to the Software Reset bit in the Control register (CTRL.SWRST). All registers in the CCL will be reset to their initial state, and the CCL will be disabled. Refer to [33.8.1. CTRL](#) for details.

33.6.2.3 Lookup Table Logic

The lookup table in each LUT unit can generate any logic expression OUT as a function of three inputs (IN[2:0]), as shown in [Figure 33-2](#). One or more inputs can be masked. The truth table for the expression is defined by TRUTH bits in LUT Control x register (LUTCTRLx.TRUTH).

Figure 33-2. Truth Table Output Value Selection

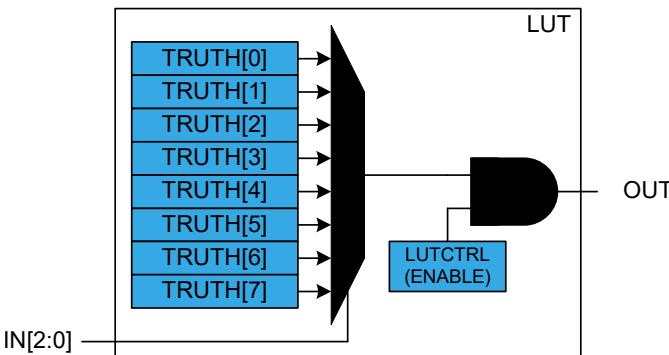


Table 33-1. Truth Table of LUT

IN[2]	IN[1]	IN[0]	OUT
0	0	0	TRUTH[0]
0	0	1	TRUTH[1]
0	1	0	TRUTH[2]
0	1	1	TRUTH[3]
1	0	0	TRUTH[4]
1	0	1	TRUTH[5]
1	1	0	TRUTH[6]
1	1	1	TRUTH[7]

33.6.2.4 Truth Table Inputs Selection

Input Overview

The inputs can be individually:

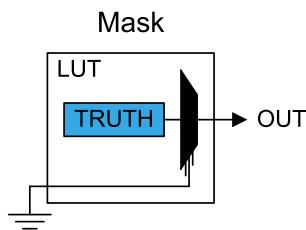
- Masked
- Driven by peripherals:
 - Analog comparator output (AC)
 - Timer/Counters waveform outputs (TC)
 - Serial Communication output transmit interface (SERCOM)
- Driven by internal events from Event System
- Driven by other CCL sub-modules

The Input Selection for each input 'y' of LUT x is configured by writing the Input 'y' Source Selection bit in the LUT x Control register (LUTCTRLx.INSELy).

Masked Inputs (MASK)

When a LUT input is masked (LUTCTRLx.INSELy = MASK), the corresponding TRUTH input (IN) is internally tied to zero, as shown in this figure:

Figure 33-3. Masked Input Selection



Internal Feedback Inputs (FEEDBACK)

When selected (LUTCTRLx.INSEL_y = FEEDBACK), the Sequential (SEQ) output is used as input for the corresponding LUT.

The output from an internal sequential sub-module can be used as input source for the LUT, see figure below for an example for LUT0 and LUT1. The sequential selection for each LUT follows the formula:

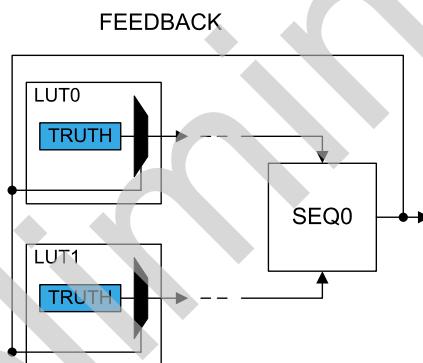
$$IN[2N][i] = SEQ[N]$$

$$IN[2N+1][i] = SEQ[N]$$

With N representing the sequencer number and $i=0,1,2$ representing the LUT input index.

See *Sequential Logic* from Related Links.

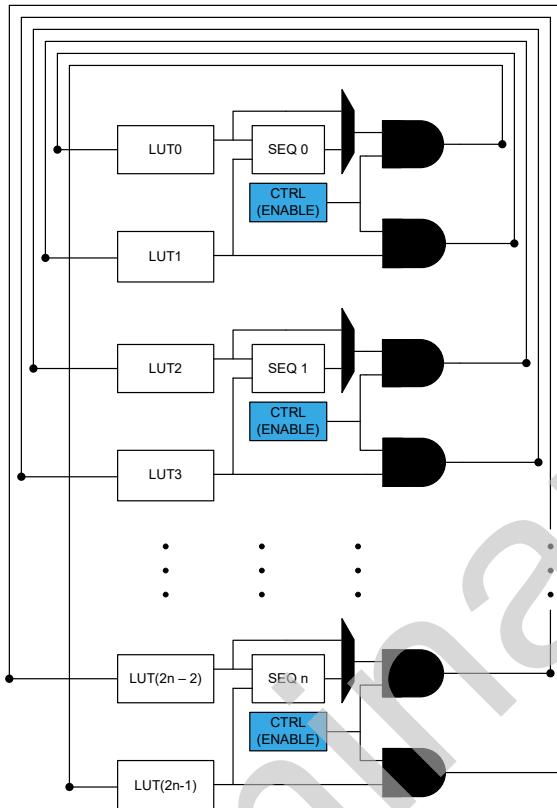
Figure 33-4. Feedback Input Selection



Linked LUT (LINK)

When selected (LUTCTRLx.INSEL_y=LINK), the subsequent LUT output is used as the LUT input (for example, LUT2 is the input for LUT1), as shown in the figure below:

Figure 33-5. Linked LUT Input Selection



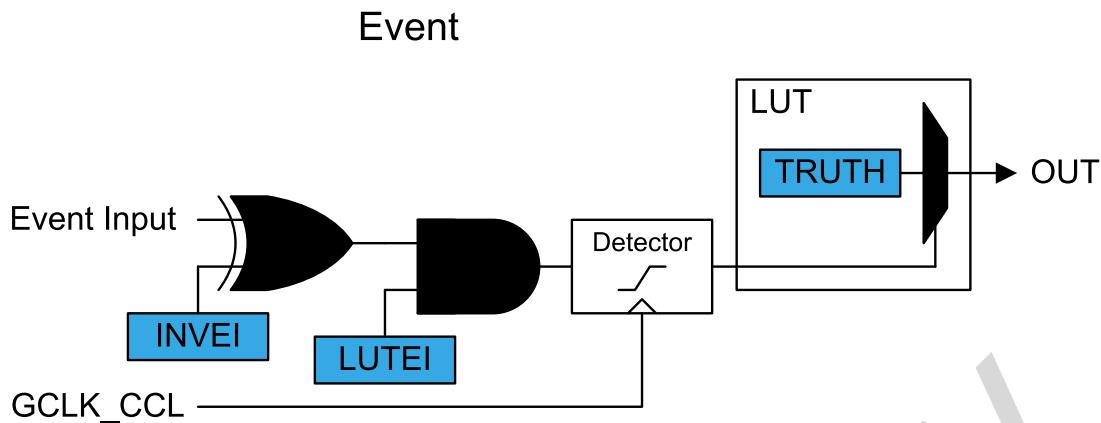
Internal Events Inputs Selection (EVENT)

Asynchronous events from the Event System can be used as input selection, as shown in the following figure. For each LUT, one event input line is available and can be selected on each LUT input. Before enabling the event selection by writing `LUTCTRLx.INSEL=EVENT`, the Event System must be configured first.

By default, CCL includes an edge detector. When the event is received, an internal strobe is generated when a rising edge is detected. The pulse duration is one `GCLK_CCL` clock cycle. Writing the `LUTCTRLx.INSEL=ASYNCEVENT` will disable the edge detector. In this case, it is possible to combine an asynchronous event input with any other input source. This is typically useful with event levels inputs for example, (external I/O pin events). The following steps ensure proper operation:

1. Enable the `GCLK_CCL` clock.
2. Configure the Event System to route the event asynchronously.
3. Select the event input type (`LUTCTRLx.INSEL = ASYNCEVENT`).
4. If a strobe must be generated on the event input falling edge, write a '1' to the Inverted Event Enable bit in the LUT Control register (`LUTCTRLx.INVEI`) .
5. Enable the event input by writing the Event Input Enable bit in the LUT Control register (`LUTCTRLx.LUTEI`) to '1'.

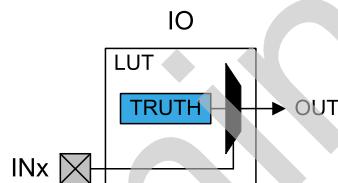
Figure 33-6. Event Input Selection



I/O Pin Inputs (IO)

When the I/O pin is selected as LUT input (LUTCTRLx.INSELy = IO), the corresponding LUT input will be connected to the pin, as shown in the figure below.

Figure 33-7. I/O Pin Input Selection



Analog Comparator Inputs (AC)

The AC outputs can be used as input source for the LUT (LUTCTRLx.INSELy=AC).

The analog comparator outputs are distributed following the formula:

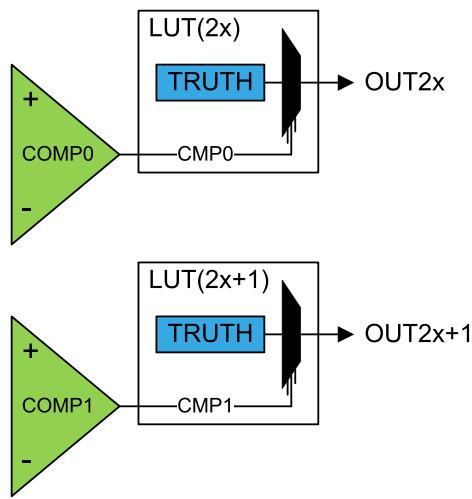
$$IN[N][i] = AC[N \% \text{ ComparatorOutput_Number}]$$

With N representing the LUT number and $i=[0,1,2]$ representing the LUT input index.

Before selecting the comparator output, the AC must be configured first.

The output of comparator 0 is available on even LUTs ("LUT(2x)": LUT0) and the comparator 1 output is available on odd LUTs ("LUT(2x+1)": LUT1), as shown in the figure below.

Figure 33-8. AC Input Selection



Timer/Counter Inputs (TC)

The TC waveform output $WO[0]$ can be used as input source for the LUT ($LUTCTRLx.INSEL_y = TC$). Only consecutive instances of the TC, that is, TC_x and the subsequent $TC_{(x+1)}$, are available as default and alternative TC selections (for example, TC_0 and TC_1 are sources for LUT_0 , TC_1 and TC_2 are sources for LUT_1). See the figure below for an example for LUT_0 . More general, the Timer/Counter selection for each LUT follows the formula:

$$IN[N][i] = DefaultTC[N \% TC_Instance_Number]$$

$$IN[N][i] = AlternativeTC[(N + 1) \% TC_Instance_Number]$$

Where N represents the LUT number and i represents the LUT input index ($i=0,1,2$).

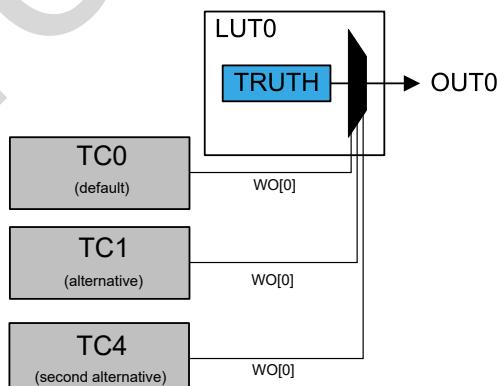
It is also possible to enable a second alternative option ($LUTCTRLx.INSEL = ALT2TC$). This option is intended to relax the alternative pin function or PCB design constraints when the default or the alternative TC instances are used for other purposes. When enabled, the Timer/Counter selection for each LUT follows the formula:

$$IN[N][i] = SecondAlternativeTC[(N + 4) \% TC_Instance_Number]$$

Note that for not implemented $TC_Instance_Number$, the corresponding input is tied to ground.

Before selecting the waveform outputs, the TC must be configured first.

Figure 33-9. TC Input Selection



Timer/Counter for Control Application Inputs (TCC)

The TCC waveform outputs can be used as input source for the LUT. Only $WO[2:0]$ outputs can be selected and routed to the respective LUT input (that is, IN_0 is connected to WO_0 , IN_1 to WO_1 , and IN_2 to WO_2), as shown in the figure below.

Note:

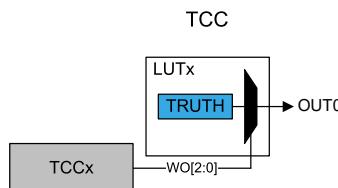
The TCC selection for each LUT follows the formula:

$$\text{IN}[N][i] = \text{TCC}[N \% \text{TCC_Instance_Number}].\text{WO}[i]$$

Where N represents the LUT number and i represents the LUT input index ($i=0,1,2$).

Before selecting the waveform outputs, the TCC must be configured first.

Figure 33-10. TCC Input Selection



Serial Communication Output Transmit Inputs (SERCOM)

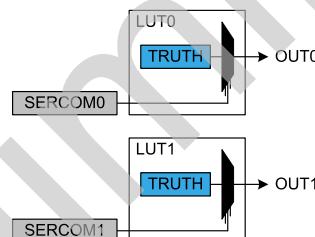
The serial engine transmitter output from Serial Communication Interface (SERCOM TX, TXd for USART, MOSI for SPI) can be used as input source for the LUT. The figure below shows an example for LUT0 and LUT1. The SERCOM selection for each LUT follows the formula:

$$\text{IN}[N][i] = \text{SERCOM}[N \% \text{SERCOM_Instance_Number}]$$

With N representing the LUT number and $i=0,1,2$ representing the LUT input index.

Before selecting the SERCOM as input source, the SERCOM must be configured first: the SERCOM TX signal must be output on SERCOMn/pad[0], which serves as input pad to the CCL.

Figure 33-11. SERCOM Input Selection



Related Links

[33.6.2.7. Sequential Logic](#)

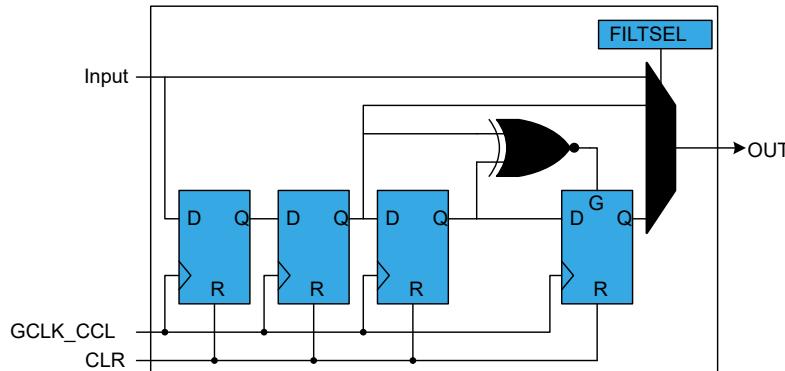
33.6.2.5 Filter

By default, the LUT output is a combinatorial function of the LUT inputs. This may cause some short glitches when the inputs change value. These glitches can be removed by clocking through filters, if demanded by application needs.

The Filter Selection bits in LUT Control register (LUTCTRLx.FILTSEL) define the synchronizer or digital filter options. When a filter is enabled, the OUT output will be delayed by two to five GCLK cycles. One APB clock after the corresponding LUT is disabled, all internal filter logic is cleared.

Note: Events used as LUT input will also be filtered, if the filter is enabled.

Figure 33-12. Filter



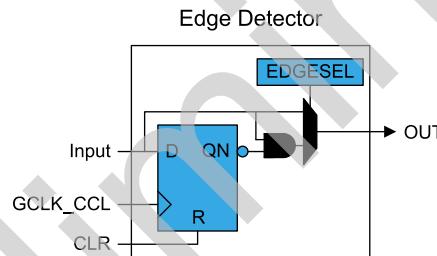
33.6.2.6 Edge Detector

The edge detector can be used to generate a pulse when detecting a rising edge on its input. To detect a falling edge, the TRUTH table should be inverted.

The edge detector is enabled by writing '1' to the Edge Selection bit in LUT Control register (LUTCTRLx.EDGESEL). In order to avoid unpredictable behavior, either the filter or synchronizer must be enabled.

Edge detection is disabled by writing a '0' to LUTCTRLx.EDGESEL. After disabling a LUT, the corresponding internal Edge Detector logic is cleared one APB clock cycle later.

Figure 33-13. Edge Detector



33.6.2.7 Sequential Logic

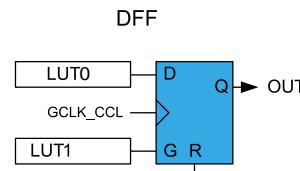
Each LUT pair can be connected to the internal sequential logic which can be configured to work as D flip flop, JK flip flop, gated D-latch or RS-latch by writing the Sequential Selection bits on the corresponding Sequential Control x register (SEQCTRLx.SEQSEL). Before using sequential logic, the GCLK_CCL clock and optionally each LUT filter or edge detector must be enabled.

Note: While configuring the sequential logic, the even LUT must be disabled. When configured the even LUT must be enabled.

Gated D Flip-Flop (DFF)

When the DFF is selected, the D-input is driven by the even LUT output LUT0, and the G-input is driven by the odd LUT output LUT1, as shown in the following figure.

Figure 33-14. D Flip Flop



When the even LUT is disabled LUTCTRL0.ENABLE=0, the flip-flop is asynchronously cleared. The reset command (R) is kept enabled for one APB clock cycle. In all other cases, the flip-flop output (OUT) is refreshed on rising edge of the GCLK_CCL, as shown in the following table.

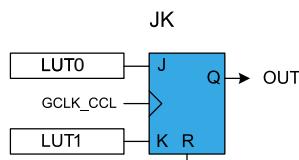
Table 33-2. DFF Characteristics

R	G	D	OUT
1	X	X	Clear
0	1	1	Set
		0	Clear
0	X		Hold state (no change)

JK Flip-Flop (JK)

When this configuration is selected, the J-input is driven by the even LUT output LUT0, and the K-input is driven by the odd LUT output LUT1, as shown in the following figure.

Figure 33-15. JK Flip Flop



When the even LUT is disabled LUTCTRL0.ENABLE=0, the flip-flop is asynchronously cleared. The reset command (R) is kept enabled for one APB clock cycle. In all other cases, the flip-flop output (OUT) is refreshed on rising edge of the GCLK_CCL, as shown in the following table.

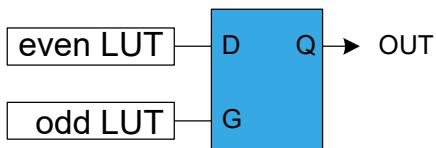
Table 33-3. JK Characteristics

R	J	K	OUT
1	X	X	Clear
0	0	0	Hold state (no change)
0	0	1	Clear
0	1	0	Set
0	1	1	Toggle

Gated D-Latch (DLATCH)

When the DLATCH is selected, the D-input is driven by the even LUT output LUT0, and the G-input is driven by the odd LUT output LUT1, as shown in the following figure.

Figure 33-16. D-Latch



When the even LUT is disabled LUTCTRL0.ENABLE=0, the latch output will be cleared. The G-input is forced enabled for one more APB clock cycle, and the D-input to zero. In all other cases, the latch output (OUT) is refreshed as shown in the following table.

Table 33-4. D-Latch Characteristics

G	D	OUT
0	X	Hold state (no change)
1	0	Clear

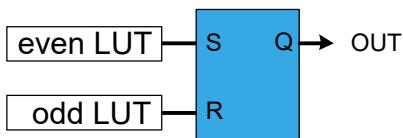
.....continued

G	D	OUT
1	1	Set

RS Latch (RS)

When this configuration is selected, the S-input is driven by the even LUT output LUT0, and the R-input is driven by the odd LUT output LUT1, as shown in the following figure.

Figure 33-17. RS-Latch



When the even LUT is disabled LUTCTRL0.ENABLE=0, the latch output will be cleared. The R-input is forced enabled for one more APB clock cycle and S-input to zero. In all other cases, the latch output (OUT) is refreshed as shown in the following table.

Table 33-5. RS-Latch Characteristics

S	R	OUT
0	0	Hold state (no change)
0	1	Clear
1	0	Set
1	1	Forbidden state

33.6.3 Events

The CCL can generate the following output events:

- LUTn where n=0-1: Lookup Table Output Value

Writing a '1' to the LUT Control Event Output Enable bit (LUTCTRL.LUTE0) enables the corresponding output event. Writing a '0' to this bit disables the corresponding output event.

The CCL can take the following actions on an input event:

- INSELx where x=0-2: The event is used as input for the TRUTH table. For additional information, refer to [33.5.6. Events](#).

Writing a '1' to the LUT Control Event Input Enable bit (LUTCTRL.LUTEI) enables the corresponding action on input event. Writing a '0' to this bit disables the corresponding action on input event.

Related Links

[27. Event System \(EVSYS\)](#)

33.6.4 Sleep Mode Operation

When using the GCLK_CCL internal clocking, writing the Run In Standby bit in the Control register (CTRL.RUNSTDBY) to '1' will allow GCLK_CCL to be enabled in Standby Sleep mode.

If CTRL.RUNSTDBY=0, the GCLK_CCL will be disabled in Standby Sleep mode. If the Filter, Edge Detector or Sequential logic are enabled, the LUT output will be forced to zero in STANDBY mode. In all other cases, the TRUTH table decoder will continue operation and the LUT output will be refreshed accordingly.

33.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRL	7:0		RUNSTDBY					ENABLE	SWRST
0x01	...	Reserved								
0x03										
0x04	SEQCTRLX	7:0							SEQSEL[3:0]	
0x05	...	Reserved								
0x07										
0x08	LUTCTRL0	7:0	EDGESEL		FILTSEL[1:0]				ENABLE	
		15:8		INSEL1[3:0]					INSEL0[3:0]	
		23:16	LUTE0	LUTEI	INVEI				INSEL2[3:0]	
		31:24			TRUTH[7:0]					
0x0C	LUTCTRL1	7:0	EDGESEL		FILTSEL[1:0]				ENABLE	
		15:8		INSEL1[3:0]					INSEL0[3:0]	
		23:16	LUTE0	LUTEI	INVEI				INSEL2[3:0]	
		31:24			TRUTH[7:0]					

33.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

[33.5.8. Register Access Protection](#)

33.8.1 Control

Name: CTRL
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Note: CTRL register (except the bits ENABLE & SWRST) is Enable Protected when CCL.CTRL.ENABLE = 1.

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	W
Reset		0					0	0

Bit 6 – RUNSTDBY Run in Standby

This bit indicates if the GCLK_CCL clock must be kept running in standby mode. The setting is ignored for configurations where the generic clock is not required. For details refer to [33.6.4. Sleep Mode Operation](#).



Important: This bit must be written before enabling the CCL.

Value	Description
0	Generic clock is not required in standby sleep mode.
1	Generic clock is required in standby sleep mode.

Bit 1 – ENABLE Enable

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the CCL to their initial state.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

33.8.2 Sequential Control X

Name: SEQCTRLX
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Enable-protected

Note: SEQCTRLX register is Enable-protected when CCL.LUTCTRL0.ENABLE = 1.

Bit	7	6	5	4	3	2	1	0
SEQSEL[3:0]								
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – SEQSEL[3:0] Sequential Selection

These bits select the sequential configuration:

Sequential Selection

Value	Name	Description
0x0	DISABLE	Sequential logic is disabled
0x1	DFF	D flip flop
0x2	JK	JK flip flop
0x3	LATCH	D latch
0x4	RS	RS latch
0x5 - 0xF		Reserved

33.8.3 LUT Control n

Name: LUTCTRL
Offset: 0x08 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-protected

Note: The LUTCTRLn register is Enable Protected when CCL.LUTCTRLn.ENABLE = 1.

Bit	31	30	29	28	27	26	25	24
TRUTH[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
INSEL2[3:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
INSEL1[3:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
FILTSEL[1:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
ENABLE								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – TRUTH[7:0] Truth Table

These bits define the value of truth logic as a function of inputs IN[2:0].

Bit 22 – LUTE0 LUT Event Output Enable

Value	Description
0	LUT event output is disabled.
1	LUT event output is enabled.

Bit 21 – LUTEI LUT Event Input Enable

Value	Description
0	LUT incoming event is disabled.
1	LUT incoming event is enabled.

Bit 20 – INVEI Inverted Event Input Enable

Value	Description
0	Incoming event is not inverted.
1	Incoming event is inverted.

Bits 8:11, 12:15, 16:19 – INSELx LUT Input x Source Selection

These bits select the LUT input x source:

Value	Name	Description
0x0	MASK	Masked input
0x1	FEEDBACK	Feedback input source
0x2	LINK	Linked LUT input source
0x3	EVENT	Event input source
0x4	IO	I/O pin input source
0x5	AC	AC input source: CMP[0] (LUT0) / CMP[1] (LUT1)

PIC32CX-BZ2 and WBZ45 Family

Configurable Custom Logic (CCL)

Value	Name	Description
0x6	TC	TC input source: TC0 WO[0] (LUT0) / TC1 WO[0] (LUT1)
0x7	ALTTC	Alternative TC input source: TC1 WO[0] (LUT0) / TC2 WO[0] (LUT1)
0x8	TCC	TCC input source: TCC0 (LUT0) / TCC1 (LUT1)
0x9	SERCOM	SERCOM input source: SERCOM0 PAD0 (LUT0) / SERCOM1 PAD0 (LUT1)
0xA	ALT2TC	1'b0
0xB	ASYNCEVENT	1'b0
0xC - 0xF	Reserved	Reserved

Bit 7 – EDGESEL Edge Selection

Value	Description
0	Edge detector is disabled.
1	Edge detector is enabled.

Bits 5:4 – FILTSEL[1:0] Filter Selection

These bits select the LUT output filter options:

Filter Selection

Value	Name	Description
0x0	DISABLE	Filter disabled
0x1	SYNCH	Synchronizer enabled
0x2	FILTER	Filter enabled
0x3	-	Reserved

Bit 1 – ENABLE LUT Enable

Value	Description
0	The LUT is disabled.
1	The LUT is enabled.

34. TRNG – True Random Number Generator

34.1 Overview

The True Random Number Generator (TRNG) generates unpredictable random numbers that are not generated by an algorithm. It passes the American NIST Special Publication 800-22 and Diehard Random Tests Suites.

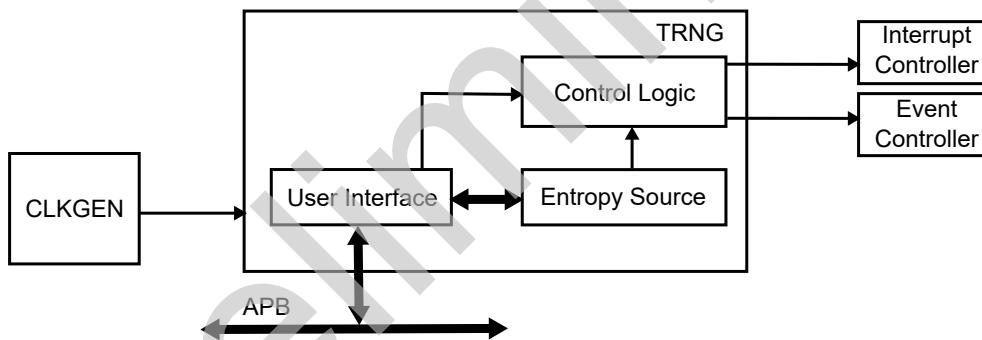
The TRNG may be used as an entropy source for seeding an NIST approved DRNG (Deterministic RNG) as required by FIPS PUB 140-2 and 140-3.

34.2 Features

- Passed NIST Special Publication 800-22 Tests Suite
- Passed Diehard Random Tests Suite
- May be used as Entropy Source for seeding an NIST approved DRNG (Deterministic RNG) as required by FIPS PUB 140-2 and 140-3
- Provides a 32-bit random number every 84 clock cycles

34.3 Block Diagram

Figure 34-1. TRNG Block Diagram.



34.4 Signal Description

Not applicable.

34.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

34.5.1 I/O Lines

Not applicable.

34.5.2 Power Management

The functioning of TRNG depends on the sleep mode of device.

The TRNG interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

Related Links

[34.6.5. Sleep Mode Operation](#)

34.5.3 Clocks

The TRNG bus clock () can be enabled and disabled in the CRU module or PMD3.RNGMD bit, see *Peripheral Module Disable Register (PMD)* from Related Links.

Related Links

[19. Peripheral Module Disable Register \(PMD\)](#)

34.5.4 DMA

Not applicable.

34.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the TRNG interrupt(s) requires the interrupt controller to be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

34.5.6 Events

TRNG can generate Events that are used by the Event System (EVSYS) and EVSYS users.

TRNG cannot use any Events from other peripherals, as it is not an Event User.

Related Links

[27. Event System \(EVSYS\)](#)

34.5.7 Debug Operation

When the CPU is halted in debug mode the TRNG continues normal operation. If the TRNG is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

34.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the Peripheral Access Controller (PAC), except the following register:

- Interrupt Flag Status and Clear (INTFLAG) register

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

34.5.9 Analog Connections

Not applicable.

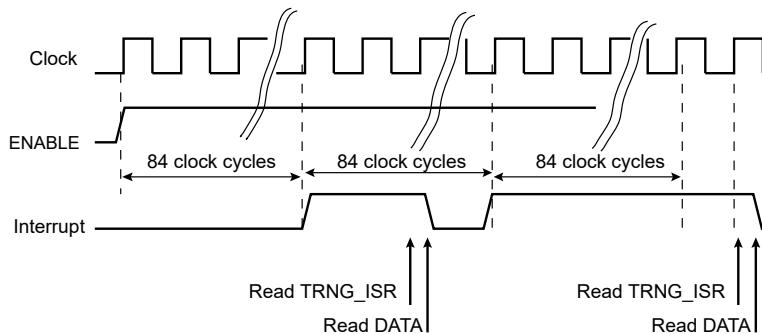
34.6 Functional Description

34.6.1 Principle of Operation

When the TRNG is enabled, the peripheral starts providing new 32-bit random numbers every 84 PB2_CLK clock cycles.

The TRNG can be configured to generate an interrupt or event when a new random number is available.

Figure 34-2. TRNG Data Generation Sequence



34.6.2 Basic Operation

34.6.2.1 Initialization

To operate the TRNG, do the following:

- Ensure PB2_CLK is enabled in the CRU and TRNG is enabled in the PMD3 register, PMD3.RNGMD bit.
- Optional: Enable the output event by writing a '1' to the EVCTRL.DATARDYEO bit.
- Optional: Enable the TRNG to Run in Standby sleep mode by writing a '1' to CTRLA.RUNSTDBY.
- Enable the TRNG operation by writing a '1' to CTRLA.ENABLE.

The following register is enable-protected, meaning that it can only be written when the TRNG is disabled (CTRLA.ENABLE is zero):

- Event Control register (EVCTRL)

Enable-protection is denoted by the Enable-Protected property in the register description.

34.6.2.2 Enabling, Disabling and Resetting

The TRNG is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TRNG is disabled by writing a zero to CTRLA.ENABLE.

34.6.3 Interrupts

The TRNG has the following interrupt source:

- Data Ready (DATARDY): Indicates that a new random number is available in the DATA register and ready to be read.
This interrupt is a synchronous wake-up source. See *Sleep Mode Controller* for details.

The interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.DATARDY) is set to '1' when the interrupt condition occurs. The interrupt can be enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET.DATARDY), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, or the interrupt is disabled. See *INTFLAG* register from Related Links for details on how to clear interrupt flags.

Note that interrupts must be globally enabled for interrupt requests to be generated.

Related Links

34.8.5. INTFLAG

34.6.4 Events

The TRNG can generate the following output event:

- Data Ready (DATARDY): Generated when a new random number is available in the DATA register.

Writing '1' to the Data Ready Event Output bit in the Event Control Register (EVCTRL.DATARDYEO) enables the DTARDY event. Writing a '0' to this bit disables the corresponding output event. Refer to *EVSYS – Event System* for details on configuring the Event System.

Related Links

[27. Event System \(EVSYS\)](#)

34.6.5 Sleep Mode Operation

The Run in Standby bit in Control A register (CTRLA.RUNSTDBY) controls the behavior of the TRNG during standby sleep mode:

When this bit is '0', the TRNG is disabled during sleep, but maintains its current configuration.

When this bit is '1', the TRNG continues to operate during sleep and any enabled TRNG interrupt source can wake up the CPU.

Preliminary

34.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0		RUNSTDBY					ENABLE	
0x01	...	Reserved								
0x03										
0x04	EVCTRL	7:0							DATARDYEO	
0x05	...	Reserved								
0x07										
0x08	INTENCLR	7:0							DATARDY	
0x09	INTENSET	7:0							DATARDY	
0x0A	INTFLAG	7:0							DATARDY	
0x0B	...	Reserved								
0x1F										
0x20	DATA	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							

34.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

34.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	
Access		R/W					R/W	
Reset		0					0	

Bit 6 – RUNSTDBY Run in Standby

This bit controls how the TRNG behaves during standby sleep mode:

Value	Description
0	The TRNG is halted during standby sleep mode.
1	The TRNG is not stopped in standby sleep mode.

Bit 1 – ENABLE Enable

Value	Description
0	The TRNG is disabled.
1	The TRNG is enabled.

34.8.2 Event Control

Name: EVCTRL
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0	Access	R/W
								DATARDYEO		0

Bit 0 – DATARDYEO Data Ready Event Output

This bit indicates whether the Data Ready event output is enabled and whether an output event will be generated when a new random value is ready.

Value	Description
0	Data Ready event output is disabled and an event will not be generated.
1	Data Ready event output is enabled and an event will be generated.

34.8.3 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	7	6	5	4	3	2	1	0	DATARDY
Access									R/W
Reset									0

Bit 0 – DATARDY Data Ready Interrupt Enable

Writing a '1' to this bit will clear the Data Ready Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The DATARDY interrupt is disabled.
1	The DATARDY interrupt is enabled.

34.8.4 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	7	6	5	4	3	2	1	0	DATARDY
Access									R/W
Reset									0

Bit 0 – DATARDY Data Ready Interrupt Enable

Writing a '1' to this bit will set the Data Ready Interrupt Enable bit, which enables the corresponding interrupt request.

Value	Description
0	The DATARDY interrupt is disabled.
1	The DATARDY interrupt is enabled.

34.8.5 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0	DATARDY
Access									R/W
Reset									0

Bit 0 – DATARDY Data Ready

This flag is set when a new random value is generated, and an interrupt will be generated if INTENCLR/SET.DATARDY=1.

This flag is cleared by writing a '1' to the flag or by reading the DATA register. Writing a '0' to this bit has no effect.

34.8.6 Output Data

Name: DATA
Offset: 0x20
Reset: -
Property: -

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-
DATA[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-
DATA[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-
DATA[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

Bits 31:0 – DATA[31:0] Output Data

These bits hold the 32-bit randomly generated output data.

35. AES – Advanced Encryption Standard

35.1 Overview

The Advanced Encryption Standard peripheral (AES) provides a means for symmetric-key encryption of 128-bit blocks, in compliance to NIST specifications.

The symmetric-key algorithm requires the same key for both encryption and decryption.

Different key sizes are supported. The key size determines the number of repetitions of transformation rounds that convert the input (called the "plaintext") into the final output ("ciphertext"). The number of rounds of repetition is as follows:

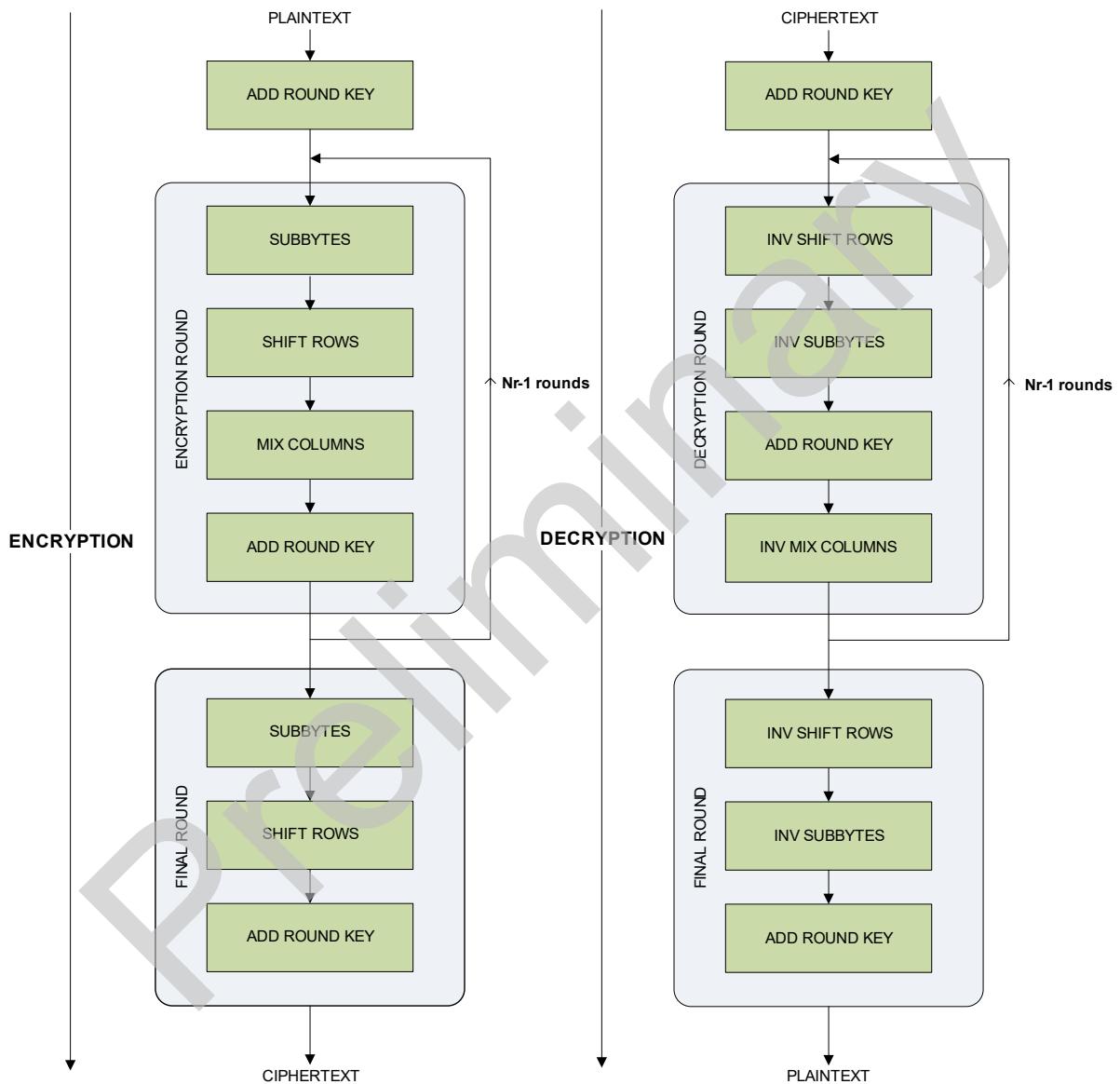
- 10 rounds of repetition for 128-bit keys
- 12 rounds of repetition for 192-bit keys
- 14 rounds of repetition for 256-bit keys

35.2 Features

- Compliant with FIPS Publication 197, Advanced Encryption Standard (AES)
- 128/192/256 bit cryptographic key supported
- Encryption time of 57/67/77 cycles with 128-bit/192-bit/256-bit cryptographic key
- Five confidentiality modes of operation as recommended in NIST Special Publication 800-38A
- Electronic Code Book (ECB)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Output Feedback (OFB)
- Counter (CTR)
- Supports Counter with CBC-MAC (CCM/CCM*) mode for authenticated encryption
- 8, 16, 32, 64, 128-bit data sizes possible in CFB mode
- Galois Counter mode (GCM) encryption and authentication

35.3 Block Diagram

Figure 35-1. AES Block Diagram



35.4 Signal Description

Not applicable.

35.5 Product Dependencies

In order to use this AES module, other parts of the system must be configured correctly, as described below.

35.5.1 I/O Lines

Not applicable.

35.5.2 Power Management

The AES will continue to operate in Standby sleep mode, if its source clock is running.

The AES interrupts can be used to wake up the device from Standby sleep mode. Refer to the Power Manager chapter for details on the different sleep modes.

AES is clocked only on the following conditions:

- When the DMA is enabled.
- Whenever there is an APB access for any read and write operation to the AES registers. (Not in Standby sleep mode.)
- When the AES is enabled & encryption/decryption is ongoing.

35.5.3 Clocks

The AES bus clock (PB2_CLK) can be enabled and disabled in the CRU module.

35.5.4 DMA

The AES has two DMA request lines; one for input data, and one for output data. They are both connected to the DMA Controller (DMAC). These DMA request triggers will be acknowledged by the DMAC ACK signals. Using the AES DMA requests requires the DMA Controller to be configured first. See *Direct Memory Access Controller (DMAC)* from Related Links.

Related Links

[21. Direct Memory Access Controller \(DMAC\)](#)

35.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the AES interrupt requires the interrupt controller to be configured first. Refer to the Processor and Architecture chapter for details.

All the AES interrupts are synchronous wake-up sources. See *Sleep Mode Controller* for details.

35.5.6 Events

Not applicable.

35.5.7 Debug Operation

When the CPU is halted in debug mode, the AES module continues normal operation. If the AES module is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging. The AES module can be forced to halt operation during debugging.

35.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the peripheral access controller (PAC), except the following register:

- Interrupt Flag Register (INTFLAG)

Write-protection is denoted by the Write-Protected property in the register description.

Write-protection does not apply to accesses through an external debugger. See *Peripheral Access Controller (PAC)* from Related Links.

Related Links

[25. Peripheral Access Controller \(PAC\)](#)

35.5.9 Analog Connections

Not applicable.

35.6 Functional Description

35.6.1 Principle of Operation

The following is a high level description of the algorithm. These are the steps:

- KeyExpansion: Round keys are derived from the cipher key using Rijndael's key schedule.
- InitialRound:
 - AddRoundKey: Each byte of the state is combined with the round key using bitwise XOR.
- Rounds:
 - SubBytes: A non-linear substitution step where each byte is replaced with another according to a lookup table.
 - ShiftRows: A transposition step where each row of the state is shifted cyclically a certain number of steps.
 - MixColumns: A mixing operation which operates on the columns of the state, combining the four bytes in each column.
 - AddRoundKey
- Final Round (no MixColumns):
 - SubBytes
 - ShiftRows
 - AddRoundKey

The relationship between the module's clock frequency and throughput (in bytes per second) is given by:

Clock Frequency = (Throughput/2) x (Nr+1) for 2 byte parallel processing

Clock Frequency = (Throughput/4) x (Nr+1) for 4 byte parallel processing

where Nr is the number of rounds, depending on the key length.

35.6.2 Basic Operation

35.6.2.1 Initialization

The following register is enable-protected:

- Control A (CTRLA)

Enable-protection is denoted by the Enable-Protected property in the register description.

35.6.2.2 Enabling, Disabling, and Resetting

The AES module is enabled by writing a one to the Enable bit in the Control A register (CTRLA.ENABLE). The module is disabled by writing a zero to CTRLA.ENABLE. The module is reset by writing a one to the Software Reset bit in the Control A register (CTRLA.SWRST).

35.6.2.3 Basic Programming

The CIPHER bit in the Control A Register (CTRLA.CIPHER) allows selection between the encryption and the decryption processes. The AES is capable of using cryptographic keys of 128/192/256 bits to encrypt and decrypt data in blocks of 128 bits. The Key Size (128/192/256) can be programmed in the KEYSIZE field in the Control A Register (CTRLA.KEYSIZE). This 128-bit/192-bit/256-bit key is defined in the Key Word Registers (KEYWORD). By

setting the XORKEY bit of CTRLA register, keyword can be updated with the resulting XOR value of user keyword and previous keyword content.

The input data for processing is written to a data buffer consisting of four 32-bit registers through the Data register address. The data buffer register (note that input and output data shares the same data buffer register) that is written to when the next write is performed is indicated by the Data Pointer in the Data Buffer Pointer (DATABUFPT) register. This field is incremented by one or wrapped by hardware when a write to the INDATA register address is performed. This field can also be programmed, allowing the user direct control over which input buffer register to write. Note that when AES module is in the CFB operation mode with the data segment size less than 128 bits, the input data must be written to the first (DATABUFPT = 0) and second (DATABUFPT = 1) input buffer registers (see [Table 35-1](#)).

The input to the encryption processes of the CBC, CFB and OFB modes includes, in addition to the plaintext, a 128-bit data block called the Initialization Vector (IV), which must be set in the Initialization Vector Registers (INTVECT). Additionally, the GCM mode 128-bit authentication data needs to be programmed. The Initialization Vector is used in the initial step in the encryption of a message and in the corresponding decryption of the message. The Initialization Vector Registers are also used by the Counter mode to set the counter value.

It is necessary to notify AES module whenever the next data block it is going to process is the beginning of a new message. This is done by writing a one to the New Message bit in the Control B register (CTRLB.NEWMSG).

The AES modes of operation are selected by setting the AESMODE field in the Control A Register (CTRLA.AESMODE). In Cipher Feedback Mode (CFB), five data sizes are possible (8, 16, 32, 64 or 128 bits), configurable by means of the CFBS field in the Control A Register (CTRLA.CFBS). In Counter mode, the size of the block counter embedded in the module is 16 bits. Therefore, there is a rollover after processing 1 megabyte of data. The data pre-processing, post-processing and data chaining for the concerned modes are automatically performed by the module.

When data processing has completed, the Encryption Complete bit in the Interrupt Flag register (INTFLAG.ENCCMP) is set by hardware (which triggers an interrupt request if the corresponding interrupt is enabled). The processed output data is read out through the Output Data register (INDATA) address from the data buffer consisting of four 32-bit registers. The data buffer register that is read when the next read is performed is indicated by the Data Pointer field in the Data Buffer Pointer register (DATABUFPT). This field is incremented by one or wrapped by hardware when a read from the INDATA register address is performed. This field can be programmed, giving the user direct control over which output buffer register to read from. Note that when AES module is in the CFB operation mode with the data segment size less than 128 bits, the output data must be read from the first (DATABUFPT = 0) and second (DATABUFPT = 1) output buffer registers (see [Table 35-1](#)). The Encryption Complete bit (INTFLAG.ENCCMP) is cleared by hardware after the processed data has been read from the relevant output buffer registers.

Table 35-1. Relevant Input/Output Data Registers for Different Confidentiality Modes

Confidentiality Mode	Relevant Input / Output Data Registers
ECB	All
CBC	All
OFB	All
128-bit CFB	All
64-bit CFB	First and Second
32-bit CFB	First
16-bit CFB	First
8-bit CFB	First
CTR	All

35.6.2.4 Start Modes

The Start mode field in the Control A Register (CTRLA.STARTMODE) allows the selection of encryption start mode.

1. Manual Start Mode

In the Manual Start Mode the sequence is as follows:

- a. Write the 128/192/256 bit key in the Key Register (KEYWORD)
 - b. Write the initialization vector or counter in the Initialization Vector Register (INTVECT). The initialization vector concerns all modes except ECB
 - c. Enable interrupts in Interrupt Enable Set Register (INTENSET), depending on whether an interrupt is required or not at the end of processing.
 - d. Write the data to be encrypted or decrypted in the Data Registers (INDATA).
 - e. Set the START bit in Control B Register (CTRLB.START) to begin the encryption or the decryption process.
 - f. When the processing completes, the Encryption Complete bit in the Interrupt Flag Register (INTFLAG.ENCCMP) raises. If Encryption Complete interrupt has been enabled, the interrupt line of the AES is activated.
 - g. When the software reads one of the Output Data Registers (INDATA), INTFLAG.ENCCMP bit is automatically cleared.
2. Auto start Mode
The Auto Start Mode is similar to the manual one, but as soon as the correct number of input data registers is written, processing is automatically started without setting the START bit in the Control B Register. DMA operation uses this mode.
 3. Last Output Data Mode (LOD)
This mode is used to generate message authentication code (MAC) on data in CCM mode of operation. The CCM mode combines counter mode for encryption and CBC-MAC generation for authentication.

When LOD is disabled in CCM mode then counter mode of encryption is performed on the input data block.

When LOD is enabled in CCM mode then CBC-MAC generation is performed. Zero block is used as the initialization vector by the hardware. Reading from the Output Data Register (INDATA) is not required to clear the ENCCMP flag. The ENCCMP flag is automatically cleared by writing into the Input Data Register (INDATA). This allows retrieval of only the last data in several encryption/decryption processes. No output data register reads are necessary between each block of encryption/decryption process.

Note that assembling message depending on the security level identifier in CCM* has to be done in software.

35.6.2.5 Computation of last Nk words of expanded key

The AES algorithm takes the cryptographic key provided by the user and performs a Key Expansion routine to generate an expanded key. The expanded key contains a total of $4(Nr + 1)$ 32-bit words, where the first Nk ($4/6/8$ for a 128-/192-/256-bit key) words are the user-provided key. For data encryption, the expanded key is used in the forward direction, i.e., the first four words are used in the initial round of data processing, the second four words in the first round, the third four words in the second round, and so on. On the other hand, for data decryption, the expanded key is used in the reverse direction, i.e., the last four words are used in the initial round of data processing, the last second four words in the first round, the last third four words in the second round, and so on.

To reduce gate count, the AES module does not generate and store the entire expanded key prior to data processing. Instead, it computes on-the-fly the round key (four 32-bit words) required for the current round of data processing. In general, the round key for the current round of data processing can be computed from the Nk words of the expanded key generated in the previous rounds. When AES module is operating in the encryption mode, the round key for the initial round of data processing is simply the user-provided key written to the KEY registers. On the other hand, when AES module is operating in the decryption mode, the round key for the initial round of data processing is the last four words of the expanded key, which is not available unless AES module has performed at least one encryption process prior to operating in the decryption mode.

In general, the last Nk words of the expanded key must be available before decryption can start. If desired, AES module can be instructed to compute the last Nk words of the expanded key in advance by writing a one to the Key Generate (KEYGEN) bit in the CTRLA register (CTRLA.KEYGEN). The computation takes Nr clock cycles. Alternatively, the last Nk words of the expanded key can be automatically computed by AES module when a decryption process is initiated if they have not been computed in advance or have become invalid. Note that this will introduce a latency of Nr clock cycles to the first decryption process.

35.6.2.6 Hardware Countermeasures against Differential Power Analysis Attacks

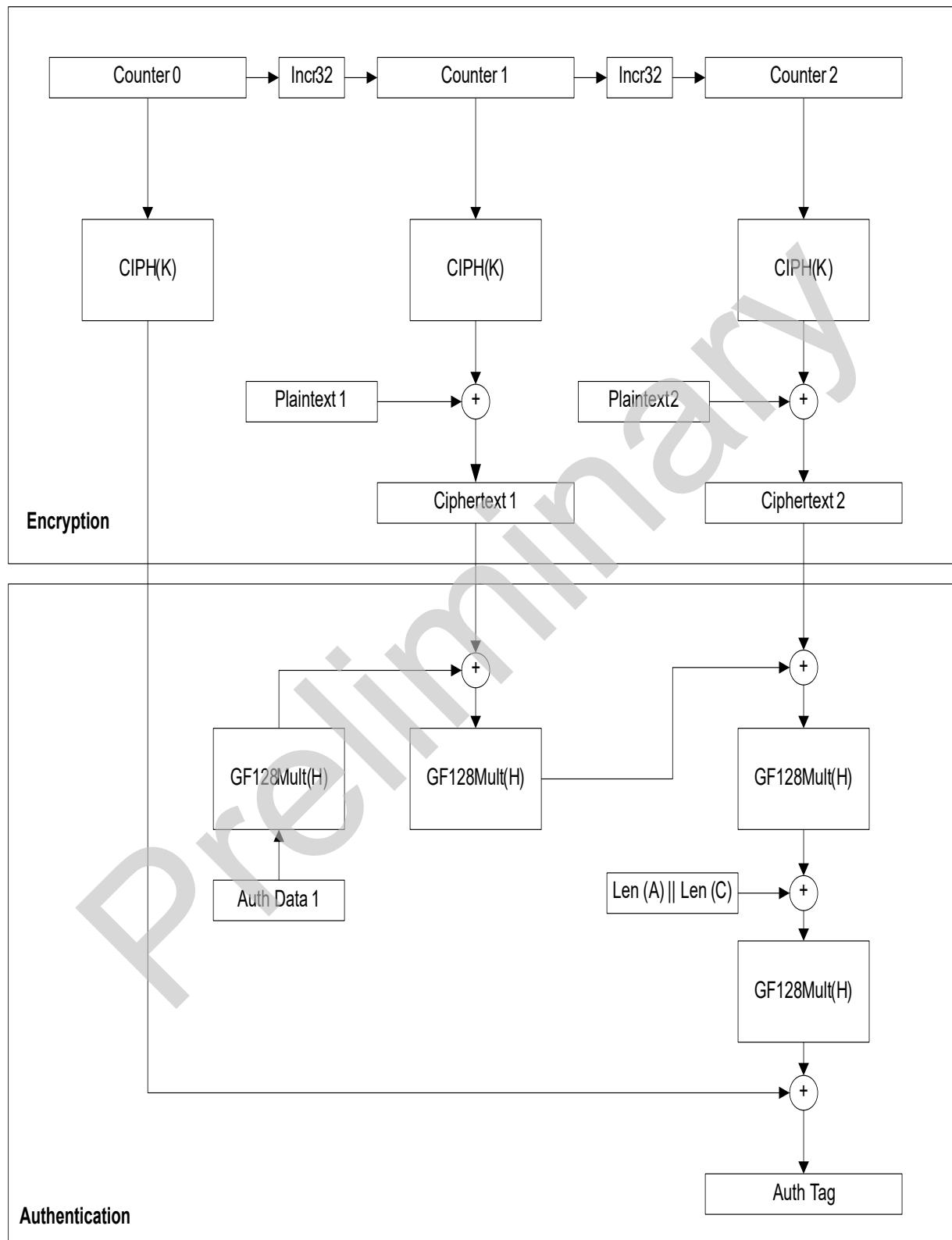
The AES module features four types of hardware countermeasures that are useful for protecting data against differential power analysis attacks:

- Type 1: Randomly add one cycle to data processing
- Type 2: Randomly add one cycle to data processing (other version)
- Type 3: Add a random number of clock cycles to data processing, subject to a maximum of 11/13/15 clock cycles for key sizes of 128/192/256 bits
- Type 4: Add random spurious power consumption during data processing

By default, all countermeasures are enabled, but require a write in DRNGSEED register to be effective. One or more of the countermeasures can be disabled by programming the Countermeasure Type field in the Control A (CTRLA.CTYPE) register. The countermeasures use random numbers generated by a deterministic random number generator embedded in AES module. The seed for the random number generator is written to the RANDSEED register. Note also that a new seed must be written after a change in the keysize. Note that enabling countermeasures reduces AES module's throughput. In short, the throughput is highest with all the countermeasures disabled. On the other hand, with all of the countermeasures enabled, the best protection is achieved but the throughput is worst.

35.6.3 Galois Counter Mode (GCM)

GCM is comprised of the AES engine in CTR mode along with a universal hash function (GHASH engine) that is defined over a binary Galois field to produce a message authentication tag. The GHASH engine processes data packets after the AES operation. GCM provides assurance of the confidentiality of data through the AES Counter mode of operation for encryption. Authenticity of the confidential data is assured through the GHASH engine. Refer to the NIST Special Publication 800-38D Recommendation for more information.



35.6.3.1 GCM Operation

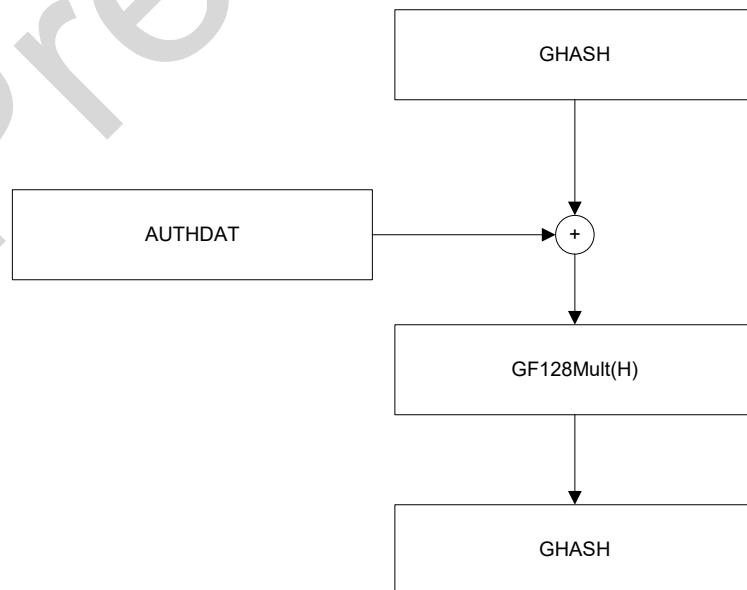
35.6.3.1.1 Hashkey Generation

- Configure CTRLA register as follows:
 - a. CTRLA.STARTMODE as Manual (Auto for DMAC)
 - b. CTRLA.CIPHER as Encryption
 - c. CTRLA.KEYSIZE as per the key used
 - d. CTRLA.AESMODE as ECB
 - e. CTRLA.CTYPE as per the countermeasures required.
- Set CTRLA.ENABLE
- Write zero to CIPLEN reg.
- Write the key in KEYWORD register
- Write the zeros to INDATA reg
- Set CTRLB.Start.
- Wait for INTFLAG.ENCCMP to be set
- AES Hardware generates Hash Subkey in HASHKEY register.

35.6.3.1.2 Authentication Header Processing

- Configure CTRLA register as follows:
 - a. CTRLA.STARTMODE as Manual
 - b. CTRLA.CIPHER as Encryption
 - c. CTRLA.KEYSIZE as per the key used
 - d. CTRLA.AESMODE as GCM
 - e. CTRLA.CTYPE as per the countermeasures required.
- Set CTRLA.ENABLE
- Write the key in KEYWORD register
- Set CTRLB.GFMUL
- Write the Authdata to INDATA reg
- Set CTRLB.START as1
- Wait for INTFLAG.GFMCMP to be set.
- AES Hardware generates output in GHASH register
- Continue steps 4 to 7 for remaining Authentication Header.

Note: If the Auth data is less than 128 bit, it has to be padded with zero to make it 128 bit aligned.



35.6.3.1.3 Plain text Processing

- Set CTRLB.NEWSMSG for the new set of plain text processing.
- Load CIPLEN reg.
- Load (J0+1) in INTVECT register.
- As described in NIST documentation $J_0 = IV \parallel 0 \ 31 \parallel 1$ when $\text{len}(IV)=96$ and $J_0 = \text{GHASH}_H(IV \parallel 0 \ s+64 \parallel [\text{len}(IV)] \ 64)$ (s is the minimum number of zeroes that should be padded with the Initialization Vector to make it a multiple of 128) if $\text{len}(IV) \neq 96$.
- Load plain text in INDATA register.
- Set CTRLB.START as 1.
- Wait for INTFLAG.ENCCMP to be set.
- AES Hardware generates output in INDATA register.
- Intermediate GHASH is stored in GHASH register and Cipher Text available in INDATA register.
- Continue 3 to 6 till the input of plain text to get the cipher text and the Hash keys.
- At the last input, set CTRLB.EOM.
- Write last in-data to INDATA reg.
- Set CTRLB.START as 1.
- Wait for INTFLAG.ENCCMP to be set.
- AES Hardware generates output in INDATA register and final Hash key in GHASH register.
- Load [LEN(A)]64|[LEN(C)]64 in INDATA register and set CTRLB.GFMUL and CTRLB.START as 1.
- Wait for INTFLAG.GFMCMP to be set.
- AES Hardware generates final GHASH value in GHASH register.

35.6.3.1.4 Plain text processing with DMAC

- Set CTRLB.NEWSMSG for the new set of plain text processing.
- Load CIPLEN reg.
- Load (J0+1) in INTVECT register.
- Load plain text in INDATA register.
- Wait for INTFLAG.ENCCMP to be set.
- AES Hardware generates output in INDATA register.
- Intermediate GHASH is stored in GHASH register and Cipher Text available in INDATA register.
- Continue 3 to 5 till the input of plain text to get the cipher text and the Hash keys.
- At the last input, set CTRLB.EOM.
- Write last in-data to INDATA reg.
- Wait for INTFLAG.ENCCMP to be set.
- AES Hardware generates output in INDATA register and final Hash key in GHASH register.
- Load [LEN(A)]64|[LEN(C)]64 in INDATA register and set CTRLB.GFMUL and CTRLB.START as 1.
- Wait for INTFLAG.GFMCMP to be set.
- AES Hardware generates final GHASH value in GHASH register.

35.6.3.1.5 Tag Generation

- Configure CTRLA
 - a. Set CTRLA.ENABLE to 0
 - b. Set CTRLA.AESMODE as CTR
 - c. Set CTRLA.ENABLE to 1
- Load J0 value to INITVECTV reg.
- Load GHASH value to INDATA reg.
- Set CTRLB.NEWSMSG and CTRLB.START to start the Counter mode operation.
- Wait for INTFLAG.ENCCMP to be set.
- AES Hardware generates the GCM Tag output in INDATA register.

35.6.4 Synchronization

Not applicable.

Preliminary

35.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	CFBS[2:0]			AESMODE[2:0]			ENABLE	SWRST
		15:8		XORKEY	KEYGEN	LOD	STARTMODE	CIPHER	KEYSIZE[1:0]	
		23:16					CTYPE[3:0]			
		31:24								
0x04	CTRLB	7:0					GFMUL	EOM	NEWMMSG	START
0x05	INTENCLR	7:0							GFMCMPP	ENCCMP
0x06	INTENSET	7:0							GFMCMPP	ENCCMP
0x07	INTFLAG	7:0							GFMCMPP	ENCCMP
0x08	DATABUFPTR	7:0							INDATA PTR[1:0]	
0x09	DBGCTRL	7:0								DBGRUN
0x0A	Reserved									
0x0B										
0C	KEYWORD0	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
10	KEYWORD1	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
14	KEYWORD2	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
18	KEYWORD3	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
1C	KEYWORD4	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
20	KEYWORD5	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
24	KEYWORD6	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
28	KEYWORD7	7:0	KEYWORD[7:0]							
		15:8	KEYWORD[15:8]							
		23:16	KEYWORD[23:16]							
		31:24	KEYWORD[31:24]							
0x2C	Reserved									
0x37										
0x38	INDATA	7:0	INDATA[7:0]							
		15:8	INDATA[15:8]							
		23:16	INDATA[23:16]							
		31:24	INDATA[31:24]							
3C	INTVECT0	7:0	INTVECTV[7:0]							
		15:8	INTVECTV[15:8]							
		23:16	INTVECTV[23:16]							
		31:24	INTVECTV[31:24]							

PIC32CX-BZ2 and WBZ45 Family

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
40	INTVECTV1	7:0								INTVECTV[7:0]
		15:8								INTVECTV[15:8]
		23:16								INTVECTV[23:16]
		31:24								INTVECTV[31:24]
44	INTVECTV2	7:0								INTVECTV[7:0]
		15:8								INTVECTV[15:8]
		23:16								INTVECTV[23:16]
		31:24								INTVECTV[31:24]
48	INTVECTV3	7:0								INTVECTV[7:0]
		15:8								INTVECTV[15:8]
		23:16								INTVECTV[23:16]
		31:24								INTVECTV[31:24]
0x4C ... 0x5B	Reserved									
0x5C	HASHKEY0	7:0								HASHKEY[7:0]
		15:8								HASHKEY[15:8]
		23:16								HASHKEY[23:16]
		31:24								HASHKEY[31:24]
0x60	HASHKEY1	7:0								HASHKEY[7:0]
		15:8								HASHKEY[15:8]
		23:16								HASHKEY[23:16]
		31:24								HASHKEY[31:24]
0x64	HASHKEY2	7:0								HASHKEY[7:0]
		15:8								HASHKEY[15:8]
		23:16								HASHKEY[23:16]
		31:24								HASHKEY[31:24]
0x68	HASHKEY3	7:0								HASHKEY[7:0]
		15:8								HASHKEY[15:8]
		23:16								HASHKEY[23:16]
		31:24								HASHKEY[31:24]
0x6C	GHASH0	7:0								GHASH[7:0]
		15:8								GHASH[15:8]
		23:16								GHASH[23:16]
		31:24								GHASH[31:24]
0x70	GHASH1	7:0								GHASH[7:0]
		15:8								GHASH[15:8]
		23:16								GHASH[23:16]
		31:24								GHASH[31:24]
0x74	GHASH2	7:0								GHASH[7:0]
		15:8								GHASH[15:8]
		23:16								GHASH[23:16]
		31:24								GHASH[31:24]
0x78	GHASH3	7:0								GHASH[7:0]
		15:8								GHASH[15:8]
		23:16								GHASH[23:16]
		31:24								GHASH[31:24]
0x7C ... 0x7F	Reserved									
80	CIPLEN	7:0								CIPLEN[7:0]
		15:8								CIPLEN[15:8]
		23:16								CIPLEN[23:16]
		31:24								CIPLEN[31:24]
0x84	RANDSEED	7:0								RANDSEED[7:0]
		15:8								RANDSEED[15:8]
		23:16								RANDSEED[23:16]
		31:24								RANDSEED[31:24]

35.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

[35.5.8. Register Access Protection](#)

Preliminary

35.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access						CTYPE[3:0]		
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access		XORKEY	KEYGEN	LOD	STARTMODE	CIPHER		
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
CFBS[2:0] AESMODE[2:0] ENABLE SWRST								

Bits 19:16 – CTYPE[3:0] Counter Measure Type

Value	Name	Description
XXX0	CTYPE1 disabled	Countermeasure1 disabled
XXX1	CTYPE1 enabled	Countermeasure1 enabled
XX0X	CTYPE2 disabled	Countermeasure2 disabled
XX1X	CTYPE2 enabled	Countermeasure2 enabled
X0XX	CTYPE3 disabled	Countermeasure3 disabled
X1XX	CTYPE3 enabled	Countermeasure3 enabled
0XXX	CTYPE4 disabled	Countermeasure4 disabled
1XXX	CTYPE4 enabled	Countermeasure4 enabled

Bit 14 – XORKEY XOR Key Operation

Value	Description
0	No effect
1	The user keyword gets XORed with the previous keyword register content.

Bit 13 – KEYGEN Last Key Generation

Value	Description
0	No effect
1	Start Computation of the last NK words of the expanded key

Bit 12 – LOD Last Output Data Mode

Value	Description
0	No effect
1	Start encryption in Last Output Data mode

Bit 11 – STARTMODE Start Mode Select

PIC32CX-BZ2 and WBZ45 Family

AES – Advanced Encryption Standard

Value	Name	Description
0	Manual Mode	Start Encryption / Decryption in Manual mode
1	Auto Mode	Start Encryption / Decryption in Auto mode

Bit 10 – CIPHER Cipher Mode Select

Value	Description
0	Decryption
1	Encryption

Bits 9:8 – KEYSIZE[1:0] Encryption Key Size

Value	Name	Description
0	128-bit Key	128-bit Key for Encryption / Decryption
1	192-bit Key	192-bit Key for Encryption / Decryption
2	256-bit Key	256-bit Key for Encryption / Decryption
3	Reserved	Reserved

Bits 7:5 – CFBS[2:0] Cipher Feedback Block Size

Value	Name	Description
0	128-bit data block	128-bit Input data block for Encryption/Decryption in Cipher Feedback mode
1	64-bit data block	64-bit Input data block for Encryption/Decryption in Cipher Feedback mode
2	32-bit data block	32-bit Input data block for Encryption/Decryption in Cipher Feedback mode
3	16-bit data block	16-bit Input data block for Encryption/Decryption in Cipher Feedback mode
4	8-bit data block	8-bit Input data block for Encryption/Decryption in Cipher Feedback mode
5–7	Reserved	Reserved

Bits 4:2 – AESMODE[2:0] AES Modes of Operation

Value	Name	Description
0	ECB	Electronic code book mode
1	CBC	Cipher block chaining mode
2	OFB	Output feedback mode
3	CFB	Cipher feedback mode
4	Counter	Counter mode
5	CCM	CCM mode
6	GCM	Galois counter mode
7	Reserved	Reserved

Bit 1 – ENABLE Enable

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the AES module to their initial state, and the module will be disabled.

Writing a '1' to SWRST will always take precedence, meaning that all other writes in the same write operation will be discarded.

Value	Description
0	There is no reset operation ongoing
1	The reset operation is ongoing

35.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access					GFMUL	EOM	NEWMMSG	START
Reset					R/W	R/W	R/W	R/W

Bit 3 – GFMUL GF Multiplication

This bit is applicable only to GCM mode.

Value	Description
0	No action
1	Setting this bit calculates GF multiplication with data buffer content and hashkey register content.

Bit 2 – EOM End of Message

This bit is applicable only to GCM mode.

Value	Description
0	No action
1	Setting this bit generates final GHASH value for the message.

Bit 1 – NEWMMSG New Message

This bit is used in cipher block chaining (CBC), cipher feedback (CFB) and output feedback (OFB), counter (CTR) modes to indicate the hardware to use Initialization vector for encrypting the first block of message.

Value	Description
0	No action
1	Setting this bit indicates start of new message to the module.

Bit 0 – START Start Encryption/Decryption

Value	Description
0	No action
1	Start encryption / decryption in manual mode.

35.8.3 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	7	6	5	4	3	2	1	0
Access							GFMCMPP	ENCCMP
Reset							R/W	R/W

Bit 1 – GFMCMPP GF Multiplication Complete Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the GF Multiplication Complete Interrupt Enable bit, which disables the GF Multiplication Complete interrupt.

Value	Description
0	The GF Multiplication Complete interrupt is disabled.
1	The GF Multiplication Complete interrupt is enabled.

Bit 0 – ENCCMP Encryption Complete Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Encryption Complete Interrupt Enable bit, which disables the Encryption Complete interrupt.

Value	Description
0	The Encryption Complete interrupt is disabled.
1	The Encryption Complete interrupt is enabled.

35.8.4 Interrupt Enable Set

Name: INTENSET
Offset: 0x06
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	7	6	5	4	3	2	1	0
Access							GFMCMPP	ENCCMP
Reset							R/W	R/W

Bit 1 – GFMCMPP GF Multiplication Complete Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the GF Multiplication Complete Interrupt Enable bit, which enables the GF Multiplication Complete interrupt.

Value	Description
0	The GF Multiplication Complete interrupt is disabled.
1	The GF Multiplication Complete interrupt is enabled.

Bit 0 – ENCCMP Encryption Complete Interrupt Enable

Writing a '0' to this bit has no effect. Writing a '1' to this bit will clear the Encryption Complete Interrupt Enable bit, which enables the Encryption Complete interrupt.

Value	Description
0	The Encryption Complete interrupt is disabled.
1	The Encryption Complete interrupt is enabled.

35.8.5 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x07
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
Access							GFMCMPI	ENCCMP
Reset							R/W	R/W

Bit 1 – GFMCMPI GF Multiplication Complete

This flag is cleared by writing a '1' to it.

This flag is set when GHASH value is available on the Galois Hash Registers (GHASH_x) in GCM mode.

Writing a '0' to this bit has no effect.

This flag is also automatically cleared in the following cases:

1. Manual encryption/decryption occurs (START in CTRLB register).
2. Reading from the GHASH_x register.

Bit 0 – ENCCMP Encryption Complete

This flag is cleared by writing a '1' to it.

This flag is set when encryption/decryption is complete and valid data is available on the Data Register.

Writing a '0' to this bit has no effect.

This flag is also automatically cleared in the following cases:

1. Manual encryption/decryption occurs (START in CTRLA register). (This feature is needed only if we do not support double buffering of INDATA registers).
2. Reading from the data register (INDATA_x) when LOD = 0.
3. Writing into the data register (INDATA_x) when LOD = 1.
4. Reading from the Hash Key register (HASHKEY_x).

35.8.6 Data Buffer Pointer

Name: DATABUFPTR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	INDATAPTR[1:0]							
Access							R/W	R/W
Reset							0	0

Bits 1:0 – INDATAPTR[1:0] Input Data Pointer

Writing to this field changes the value of the input data pointer, which determines which of the four data registers is written to/read from when the next write/read to the INDATA register address is performed.

35.8.7 Debug

Name: DBGCTRL
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	DBGRUN
Access									W
Reset									0

Bit 0 – DBGRUN Debug Run

Writing a '0' to this bit causes the AES to halt during debug mode.

Writing a '1' to this bit allows the AES to continue normal operation during debug mode. This bit can only be changed while the AES is disabled.

35.8.8 Keyword

Name: KEYWORD
Offset: 0x0C + n*0x04 [n=0..7]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
KEYWORD[31:24]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEYWORD[23:16]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEYWORD[15:8]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
KEYWORD[7:0]								
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – KEYWORD[31:0] Key Word Value

The four/six/eight 32-bit Key Word registers set the 128-bit/192-bit/256-bit cryptographic key used for encryption/decryption. KEYWORD0 .KEYWORD corresponds to the first word of the key and KEYWORD3 /KEYWORD5 /KEYWORD7 .KEYWORD to the last one.

Note: By setting the XORKEY bit of CTRLA register, keyword will update with the resulting XOR value of user keyword and previous keyword content.

35.8.9 Data

Name: INDATA
Offset: 0x38
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
INDATA[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
INDATA[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
INDATA[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
INDATA[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INDATA[31:0] Data Value

A write to or read from this register corresponds to a write to or read from one of the four data registers. The four 32-bit Data registers set the 128-bit data block used for encryption/decryption. The data register that is written to or read from is given by the **DATABUFPTC.R.INDATPTR** field.

Note: Both input and output shares the same data buffer. Reading INDATA register will return 0's when AES is performing encryption or decryption operation.

35.8.10 Initialization Vector Register

Name: INTVECTV
Offset: 0x3C + n*0x04 [n=0..3]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	INTVECTV[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	INTVECTV[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	INTVECTV[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	INTVECTV[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INTVECTV[31:0] Initialization Vector Value

The four 32-bit Initialization Vector registers INTVECTV_n set the 128-bit Initialization Vector data block that is used by some modes of operation as an additional initial input. INTVECTV0 . INTVECTV corresponds to the first word of the Initialization Vector, INTVECTV3 . INTVECTV to the last one. These registers are write-only to prevent the Initialization Vector from being read by another application. For CBC, OFB, and CFB modes, the Initialization Vector corresponds to the initialization vector. For CTR mode, it corresponds to the counter value.

35.8.11 Hash Key (GCM mode only)

Name: HASHKEY
Offset: 0x5C + n*0x04 [n=0..3]
Reset: 0x00000000
Property: PAC Write-protection

Bit	31	30	29	28	27	26	25	24
HASHKEY[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
HASHKEY[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
HASHKEY[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
HASHKEY[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HASHKEY[31:0] Hash Key Value

The four 32-bit HASHKEY registers contain the 128-bit Hash Key value computed from the AES KEY. The Hash Key value can also be programmed offering single GF128 multiplication possibilities.

35.8.12 Galois Hash (GCM mode only)

Name: GHASH
Offset: 0x6C + n*0x04 [n=0..3]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
GHASH[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GHASH[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GHASH[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
GHASH[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GHASH[31:0] Galois Hash Value

The four 32-bit Hash Word registers GHASH contain the GHASH value after GF128 multiplication in GCM mode. Writing a new key to KEYWORD registers causes GHASH to be initialized with zeroes. These registers can also be programmed.

35.8.13 Galois Hash x (GCM mode only)

Name: CIPLEN
Offset: 0X80
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
CIPLEN[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CIPLEN[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CIPLEN[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CIPLEN[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CIPLEN[31:0] Cipher Length

This register contains the length in bytes of the Cipher text that is to be processed. This is programmed by the user in GCM mode for Tag generation.

35.8.14 Random Seed

Name: RANDSEED
Offset: 0x84
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
RANDSEED[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RANDSEED[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RANDSEED[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
RANDSEED[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RANDSEED[31:0] Random Seed

A write to this register corresponds to loading a new seed into the Random number generator.

36. Analog-to-Digital Converter

The PIC32CX-BZ2 12-bit High Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) includes the following features:

- 12-bit resolution
- One ADC module, up to 2 Msps conversion rate
- Single-ended and/or differential input
- Supported in Sleep mode
- Two digital comparators
- Two digital filters supporting two modes:
 - Oversampling mode
 - Averaging mode
- Designed for motor control, power conversion, and general purpose applications

The PIC32CX-BZ2 has one shared ADC module. This ADC module incorporates a multiplexer on the input to facilitate a group of inputs, and provides flexible automated scanning option through the input scan logic.

For the ADC module, the analog inputs are connected to the Sample and Hold (S&H) capacitor. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample.

Equation 36-1. ADC Throughput Rate

$$FTP = \frac{T_{AD}}{T_{SAMP} + T_{CONV}}$$

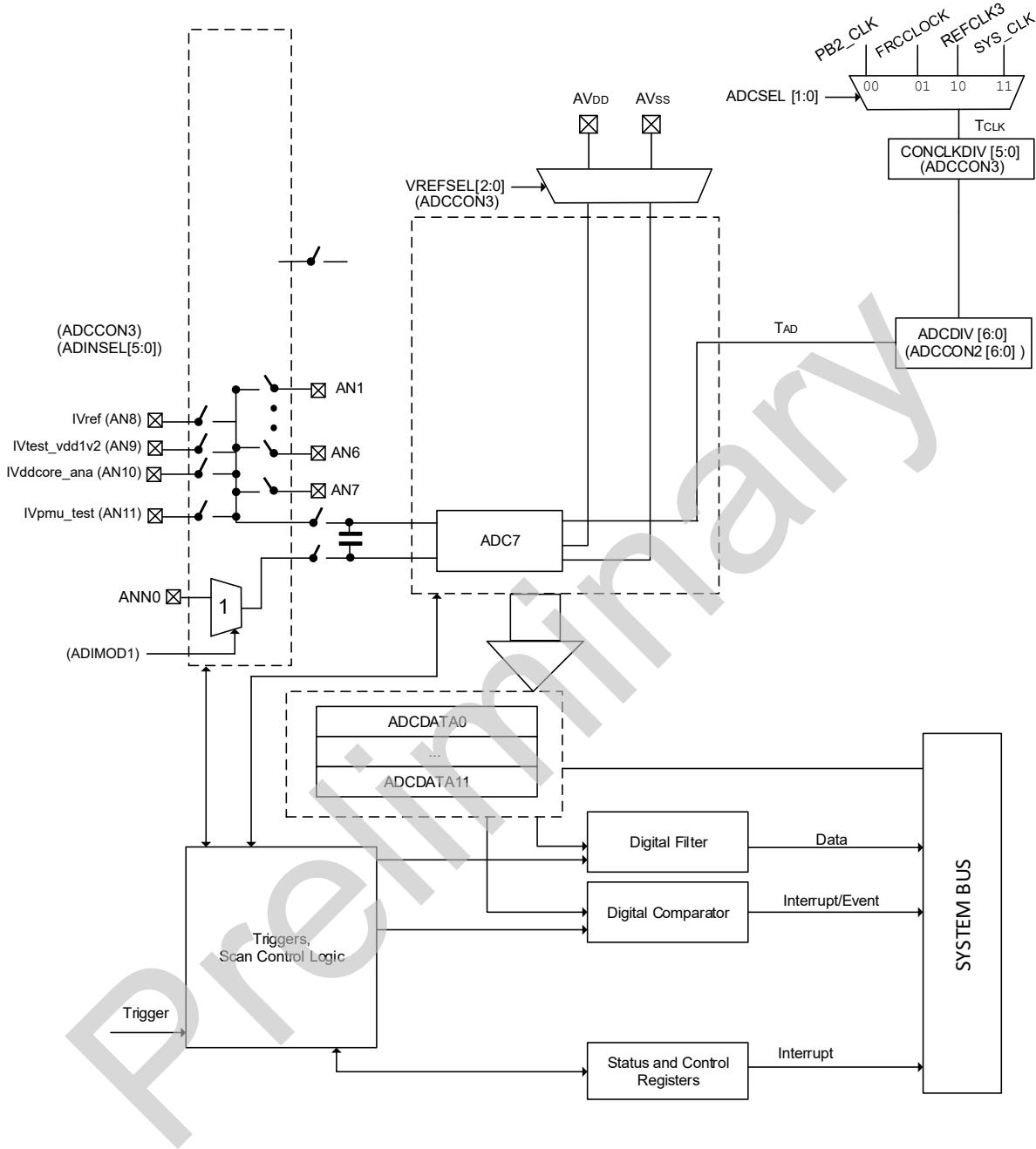
Where,

- T_{AD} = The frequency of the individual ADC module.

A block diagram of the ADC module is illustrated in the following figure.

PIC32CX-BZ2 and WBZ45 Family Analog-to-Digital Converter

Figure 36-1. ADC Block Diagram



36.1 ADC Operation

The High Speed Successive Approximation Register (SAR) ADC is designed to support power conversion and motor control applications and consists of one shared ADC module. The shared ADC module has multiple analog inputs connected to its S&H circuit through a multiplexer. Since multiple analog inputs share this ADC, it is termed the shared ADC module. The shared ADC module is used to measure analog signals of lower frequencies and signals which are static in nature (in other words, do not change significantly with time). However, this ADC module is capable of up to 2 Msps sample rate.

The analog inputs connected to the shared ADC module are Class 2 and Class 3 inputs. The number of inputs designated for each class depends on the specific device. For the PIC32CX-BZ2, the following arrangement is provided.

- Class 2 = AN0 to AN5
- Class 3 = AN6 to AN7

The property of each class of analog input is described in the following table.

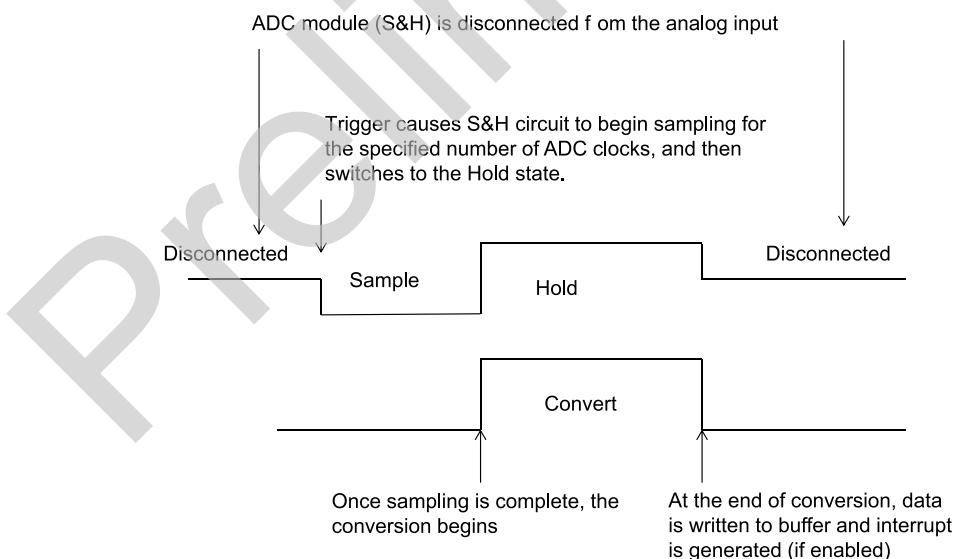
Table 36-1. Analog Input Class

ADC Module	Analog Input Class	Trigger	Trigger Action
Shared ADC module	Class 2	Individual trigger source or scan trigger	Starts sampling sequence or begins scan sequence
Shared ADC module with input scan	Class 3	Scan trigger	Starts scan sequence

Class 2 and Class 3 analog input properties:

- Class 2 inputs are used on the shared ADC module, either individually triggered or as part of a scan list. When used individually they are triggered by their unique trigger selected by the ADCTR_{Gx} register
- The analog inputs on the shared ADC have a natural order of priority (for example, AN6 has a higher priority than AN7)
- Class 3 inputs are used exclusively for scanning and share a common trigger source (scan trigger)
- Since Class 3 analog inputs share both the ADC module and the trigger source, the only method possible to convert them is to scan them sequentially for each incoming scan trigger event, where scanning occurs in the natural order of priority
- The arrival of a trigger in the shared ADC module only starts the sampling. When the trigger arrives, the ADC module goes into sampling mode for the sampling time decided by the SAMC[9:0]bits (ADCCON2[25:16]). At the end of sampling, the ADC starts conversion. Upon completion of conversion, the ADC module is used to convert the next in line Class 2 or Class 3 inputs, according to the natural order of priority. When a shared analog input (Class 2 or Class 3) has completed all conversion and no trigger is pending, the ADC module is disconnected from all analog inputs

Figure 36-2. Sample and Conversion Sequence for Shared ADC Modules

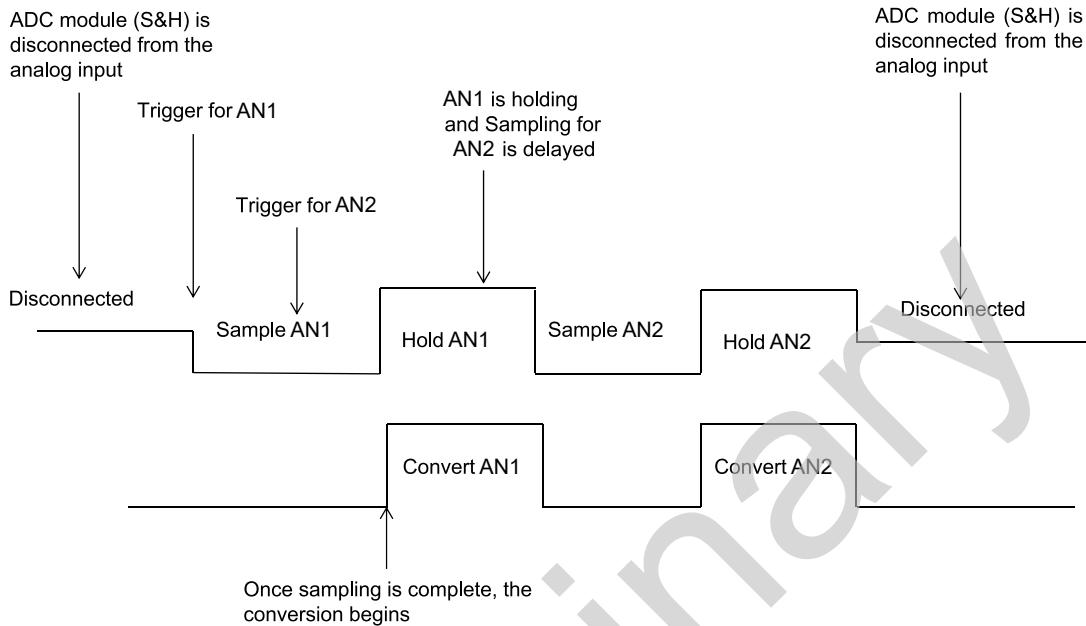


36.1.1 Class 2 Triggering

When a single Class 2 input is triggered, it is sampled and converted by the shared S&H using the sequence illustrated in Sample and Conversion Sequence for Shared ADC Modules figure, see *Sample and Conversion Sequence for Shared ADC Modules* figure in the *ADC Operation* from Related Links. When multiple Class 2 inputs are triggered, it is important to understand the consequences of trigger timing. If a conversion is underway and

another Class 2 trigger occurs then the sample-hold-conversion for the new trigger is stalled until the in-process sample-hold cycle is complete, as shown in the following figure.

Figure 36-3. Multiple Independent Class 2 Trigger Conversion Sequence



When multiple inputs to the shared S&H are triggered simultaneously, the processing order is determined by their natural priority (the lowest numbered input has the highest priority). As an example, if AN1, AN2, and AN3 are triggered simultaneously, AN1 is sampled and converted first, followed by AN2 and finally, AN3. When using the independent Class 2 triggering on the shared S&H, the SAMC[9:0] bits (ADCCON2[25:16]) determine the sample time for all inputs while the appropriate TRGSRC[4:0] bits in the ADCTRGx Register (see ADCTRG1 register from Related Links) determine the trigger source for each input.

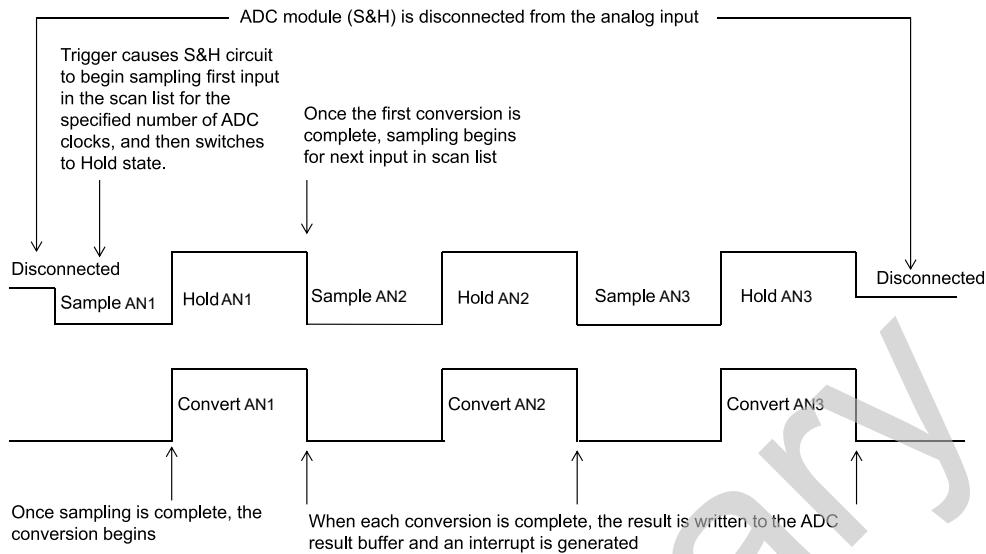
Related Links

- [36.10.15. ADCTRG1](#)
- [36.1. ADC Operation](#)

36.1.2 Input Scan

Input scanning is a feature that allows an automated scanning sequence of multiple Class 2 or Class 3 inputs. All Class 2 and Class 3 inputs are scanned using the single shared S&H. The selection of analog inputs for scanning is done with the CSSx bits of the ADCCSS1 registers. Class 2 inputs are triggered using STRIG selection in ADCTRGx register and Class 3 inputs are triggered using the STRGSRC[4:0] of ADCCON1[20:16] register. When a trigger occurs, for Class 2 or Class 3 inputs, the sampling and conversion occur in the natural input order is used; lower number inputs are sampled before higher number inputs.

Figure 36-4. Input Scan Conversion Sequence for Three Class 2 Inputs

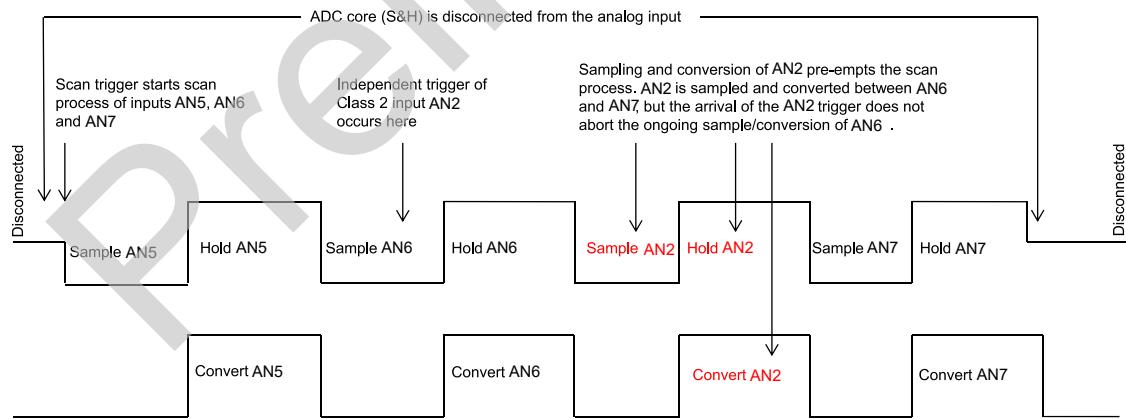


When using the shared analog inputs in scan mode, the SAMC[9:0] bits in the ADC Control Register 2 (ADCCON2[25:16]) determine the sample time for all inputs while the Scan Trigger Source Selection bits (STRGSRC[4:0]) in the ADC Control Register 1 (ADCCON1[20:16]), determine the trigger source.

To ensure predictable results, a scan should not be retriggered until sampling of all inputs has completed. Care should be taken in the system design to preclude retriggering a scan while a scan is in progress.

Individual Class 2 triggers that occur during a scan pre-empts the scan sequence if they are a higher priority than the sample currently being processed. In the following figure, a scan of AN5, AN6, and AN7 is underway when an independent trigger of Class 2 input AN2 takes place. The scan is interrupted for the sampling and conversion of AN2.

Figure 36-5. Scan Conversion Pre-empted by Class 2 Input Trigger



36.2 ADC Module Configuration

Operation of the ADC module is directed through bit settings in the specific registers. The following instructions summarize the actions and the settings. The options and details for each configuration step are provided in the subsequent sections.

To configure the ADC module, perform the following steps:

1. Configure the analog port pins, as described in [36.2.1. Configuring the Analog Port Pins](#).
2. Select the analog inputs to the ADC multiplexers, as described in [36.2.2. Selecting the ADC Multiplexer Analog Inputs](#).
3. Select the format of the ADC result, as described in [36.2.3. Selecting the Format of the ADC Result](#).
4. Select the conversion trigger source, as described in [36.2.4. Selecting the Conversion Trigger Source](#).
5. Select the voltage reference source, as described in [36.2.5. Selecting the Voltage Reference Source](#).
6. Select the scanned inputs, as described in [36.2.6. Selecting the Scanned Inputs](#).
7. Select the analog-to-digital conversion clock source and prescaler, as described in [36.2.7. Selecting the Analog-to-Digital Conversion Clock Source and Prescaler](#).
8. Specify any additional acquisition time, if required, as described in [36.8. ADC Sampling Requirements](#).
9. Turn on the ADC module, as described in [36.2.8. Turning ON the ADC](#).
10. Poll (or wait for the interrupt) for the voltage reference to be ready, as described in [36.2.5. Selecting the Voltage Reference Source](#).
11. Enable the analog and bias circuit for required ADC modules and after the ADC module wakes-up, enable the digital circuit, as described in [36.5.3. ADC Low-power Mode](#).
12. Configure the ADC interrupts (if required), as described in [36.4. Interrupts](#).

36.2.1 Configuring the Analog Port Pins

The ANSELx registers for the I/O ports associated with the analog inputs are used to configure the corresponding pin as an analog or a digital pin. A pin is configured as analog input when the corresponding ANSELx bit = '1'. When the ANSELx bit = '0', the pin is set to digital control. The ANSELx registers are set when the device comes out of Reset, causing the ADC input pins to be configured as analog inputs by default.

The TRISx registers control the digital function of the port pins. The port pins that are required as analog inputs must have their corresponding bit set in the specific TRISx register, configuring the pin as an input. If the I/O pin associated with an ADC input is configured as an output by clearing the TRISx bit, the port's digital output level (V_{OH} or V_{OL}) is converted. After a device Reset, all of the TRISx bits are set. For more information on port pin configuration, see [I/O Ports and Peripheral Pin Select \(PPS\)](#) from Related Links.

Note: When reading a PORT register that shares pins with the ADC, any pin configured as an analog input reads as a '0' when the PORT latch is read. Analog levels on any pin that is defined as a digital input but not configured as an analog input, may cause the input buffer to consume current that exceeds the device specification.

Related Links

[5. I/O Ports and Peripheral Pin Select \(PPS\)](#)

36.2.2 Selecting the ADC Multiplexer Analog Inputs

The ADC module has two inputs referred to as the positive and negative inputs. Input selection options vary as described in the following sections.

36.2.2.1 Selection of Positive Inputs

For the shared ADC module, the positive input is shared among all Class 2 and Class 3 inputs. Input connection of the analog input ANx to the shared ADC is automatic for either Class 2 input trigger or during a scan of Class 2 and or Class 3 inputs. Selecting inputs for scanning is described in [Selecting the Scanned Inputs](#), see [Selecting the Scanned Inputs](#) from Related Links.

Related Links

[36.2.6. Selecting the Scanned Inputs](#)

36.2.2.2 Selection of Negative Inputs

Negative input selection is determined by the setting of the DIFFx bit of the ADCIMCON1 register. The DIFFx bit allows the inputs to be rail-to-rail, and either single-ended or differential. The SIGNx and DIFFx bits in the ADCIMCON1 register scale the internal ADC analog inputs and reference voltages and configure the digital result to align with the expected full-scale output range.

For the shared ADC module, the analog inputs have individual settings for the DIFFx bit. Therefore, the user has the ability to select certain inputs as single-ended and others as differential, while being connected to the same

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shared ADC module. While sampling, the signal changes on-the-fly as single-ended or differential, according to its corresponding DIFFx bit setting.

Table 36-2. Negative Input Selection

ADCIMCON1		Input Configuration	Input Voltage			Output
DIFFx	SIGNx		Minimum input	$V_{INP} - V_{INN} = -V_{REF}$	-2048	
1	1	Differential 2's complement	Maximum input	$V_{INP} - V_{INN} = V_{REF}$	+2047	
			Minimum input	$V_{INP} - V_{INN} = -V_{REF}$	0	
1	0	Differential unipolar	Maximum input	$V_{INP} - V_{INN} = V_{REF}$	+4095	
			Minimum input	$V_{INP} - V_{INN} = -V_{REF}$	0	
0	1	Single-ended 2's complement	Minimum input	$V_{INP} = V_{REF}$	-2048	
			Maximum input	$V_{INP} - V_{INN} = V_{REF}$	+2047	
0	0	Single-ended unipolar	Minimum input	$V_{INP} = V_{REF}$	0	
			Maximum input	$V_{INP} - V_{INN} = V_{REF}$	+4095	

Legend:

- V_{INP} = Positive S&H input
- V_{INN} = Negative S&H input
- V_{REF} = $V_{REFH} - V_{REFL}$

Note: For proper operation and to prevent device damage, input voltage levels should not exceed the limits listed in the Electrical Specifications of the specific device data sheet.

36.2.3 Selecting the Format of the ADC Result

The data in the ADC Result register can be read in any of the four supported data formats. The user can select from unsigned integer, signed integer, unsigned fractional, or signed fractional. Integer data is right-justified and fractional data is left-justified.

- The integer or fractional data format selection is specified globally for all analog inputs using the Fractional Data Output Format bit, FRACT (ADCCON1[23])
- The signed or unsigned data format selection can be independently specified for each individual analog input using the SIGNx bits in the ADCIMCONx registers

The following table provides how a result is formatted.

Table 36-3. ADC Result Format

FRACT	SIGNx	Description	32-bit Output Data Format			
0	0	Unsigned integer	0000	0000	0000	0000
			0000	dddd	dddd	dddd
0	1	Signed integer	ssss	ssss	ssss	ssss
			ssss	sddd	ddd	ddd
1	0	Fractional	ddd	ddd	ddd	0000
			0000	0000	0000	0000

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.....continued

FRACT	SIGNx	Description	32-bit Output Data Format			
1	1	Signed fractional	sddd	dddd	dddd	dddd
			0000	0000	0000	0000

The following code is an example for ADC Class 2 configuration and fractional format.

```

int main(int argc, char** argv) {
    int result[3];

    /* Configure ADCCON1 */
    ADCCON1bits.FRACT = 1;      // use Fractional output format ADCCON1bits.SELRES = 3;    // ADC
    resolution is 12 bits ADCCON1bits.STRGSRC = 0; // No scan trigger.

    /* Configure ADCCON2 */
    ADCCON2bits.SAMC = 5;        // ADC sampling time = 5 * TAD7
    ADCCON2bits.ADCDIV = 1;       // ADC clock freq is half of control clock = TAD7

    /* Initialize warm up time register */ ADCANCON = 0;
    ADCANCONbits.WKUPCLKCNT = 5; // Wakeup exponent = 32 * TADx

    /* Clock setting */ ADCCON3 = 0;
    ADCCON3bits.ADCSEL = 0;      // Select input clock source
    ADCCON3bits.CONCLKDIV = 1;   // Control clock frequency is half of input clock
    ADCCON3bits.VREFSEL = 0;     // Select AVDD and AVSS as reference source

    /* No selection for dedicated ADC modules, no presync trigger, not sync sampling */
    ADCTRGMODEbits = 0;

    /* Select ADC input mode */
    ADCIMCON1bits.SIGN7 = 0;    // unsigned data format ADCIMCON1bits.DIFF7 = 0; // Single ended
    mode ADCIMCON1bits.SIGN8 = 0; // unsigned data format ADCIMCON1bits.DIFF8 = 0; // Single
    ended mode ADCIMCON1bits.SIGN9 = 0; // unsigned data format ADCIMCON1bits.DIFF9 = 0; // Single
    ended mode

    /* Configure ADCGIRQENx */
    ADCGIRQEN1 = 0;             // No interrupts are used
    ADCGIRQEN2 = 0;

    /* Configure ADCCSSx */
    ADCCSS1 = 0;                // No scanning is used
    ADCCSS2 = 0;

    /* Configure ADCCMPCONx */
    ADCCMPCON1 = 0;             // No digital comparators are used. Setting the ADCCMPCONx
    ADCCMPCON2 = 0;             // register to '0' ensures that the comparator is disabled.
    ADCCMPCON3 = 0;             // Other registers are "don't care".
    ADCCMPCON4 = 0;
    ADCCMPCON5 = 0;             // ADCCMPCON6 = 0;

    /* Configure ADCFLTRx */
    ADCFLTR1 = 0;               // No oversampling filters are used. ADCFLTR2 = 0;
    ADCFLTR3 = 0; ADCFLTR4 = 0; ADCFLTR5 = 0; ADCFLTR6 = 0;
    /* Set up the trigger sources */
    ADCTRGNSbits.LVL7 = 0;      // Edge trigger ADCTRGNSbits.LVL8 = 0; // Edge trigger
    ADCTRGNSbits.LVL9 = 0;      // Edge trigger
    ADC1TRG2bits.TRGSRC7 = 1; // Set AN7 to trigger from software
    ADC2TRG3bits.TRGSRC8 = 1; // Set AN8 to trigger from software
    ADC2TRG3bits.TRGSRC9 = 1; // Set AN9 to trigger from software
    /* Early interrupt */
    ADCEIEN1 = 0;                // No early interrupt
    ADCEIEN2 = 0;

    /* Turn the ADC on */ ADCCON1bits.ON = 1;

    /* Wait for voltage reference to be stable */
    while(!ADCCON2bits.BGVRRDY); // Wait until the reference voltage is ready
    while(ADCCON2bits.REFFLT);   // Wait if there is a fault with the reference voltage

    /* Enable clock to analog circuit */
    ADCANCONbits.ANEN7 = 1;      // Enable the clock to analog bias

```

```

/* Wait for ADC to be ready */
while(!ADCANCONbits.WKRDY7); // Wait until ADC7 is ready

/* Enable the ADC module */ ADCCON3bits.DIGEN7 = 1;           // Enable ADC7

while (1) {
/* Trigger a conversion */ ADCCON3bits.GSWTRG = 1;

/* Wait the conversions to complete */
while (ADCDSTAT1bits.ARDY7 == 0);
/* fetch the result */
result[0] = ADCDATA7;

while (ADCDSTAT1bits.ARDY8 == 0);
/* fetch the result */
result[1] = ADCDATA8;

while (ADCDSTAT1bits.ARDY9 == 0);
/* fetch the result */
result[2] = ADCDATA9;

/*
 * Process results here
 *
 * Note 1: Loop time determines the sampling time since all inputs are Class 2.
 * If the loop time happens is small and the next trigger happens before the
 * completion of set sample time, the conversion will happen only after the
 * sample time has elapsed.
 *
 * Note 2: Results are in fractional format
 *
 */
}

return (1);
}

```

36.2.4 Selecting the Conversion Trigger Source

Class 2 inputs to the ADC module can be triggered for conversion either individually, or as part of a scan sequence. Class 3 inputs can only be triggered as part of a scan sequence. Individual or scan triggers can originate from an on-board timer or output compare peripheral event, from external digital circuits connected to INT0, from external analog circuits connected to an analog comparator, or through software by setting a trigger bit in a SFR.

Note: When conversion triggers for multiple Class 2 analog inputs occur simultaneously, they are prioritized according to a natural order priority scheme based on the analog input used. AN6 has the highest priority, AN7 has the next highest priority, and so on.

36.2.4.1 Trigger Selection Class 2 Inputs

For each one of the Class 2 inputs, the user application can independently specify a conversion trigger source. The individual trigger source for an analog input 'x' is specified by the TRGSRC[4:0] bits located in registers ADCTRG1 through ADCTRG3. For example, these trigger sources may include:

- **General Purpose (GP) Timers:** When a period match occurs for the 32-bit timer, Timer3/2 or Timer5/4, or the 16-bit Timer1, Timer3 or Timer5, a special ADC trigger event signal is generated by the timer. This feature does not exist for other timers. For more information, see *Timer/Counter (TC)* from Related Links.
- **Output Compare:** The Output Compare peripherals, OC1, OC3, and OC5, can be used to generate an ADC trigger when the output transitions from a low to high state. For more information, see *Timer/Counter (TC)* from Related Links.
- **Comparators:** The analog Comparators can be used to generate an ADC trigger when the output transitions from a low state to a high state. For more information, see *Digital Comparator* from Related Links.
- **External INT0 Pin Trigger:** In this mode, the ADC module starts a conversion on an active transition on the INT0 pin. The INT0 pin may be programmed for either a rising edge input or a falling edge input to trigger the conversion process.
- **Global Software Trigger:** The ADC module can be configured for manually triggering a conversion for all inputs that have selected this trigger option. The user can manually trigger a conversion by setting the Global Software Trigger bit, GSWTRG (ADCCON3[6]).

Related Links

- [36.3.1. Digital Comparator](#)
- [38. Timer/Counter \(TC\)](#)

36.2.4.2 Conversion Trigger Sources and Control

The following are the possible sources for each trigger signal:

- External trigger selection through the TRGSRCx[4:0]bits in the ADCTRGx registers. This capability is supported only for Class 2 analog inputs. Typically, the user specifies a particular trigger source to initiate a conversion for specific input. All of the analog inputs may select the same trigger source if desired. In such an event, the result resembles a “scanned conversion”, which have its order of completion enforced by the priority of the inputs associated with the same trigger source. The first trigger selection is 00000 (no trigger), which amounts to temporarily disabling that particular trigger and consequently, temporarily disabling that analog input from being converted. The next two selections for trigger source (GSWTRG and GLSWTRG) are software generated trigger sources. The second software generated trigger selection is the Global Software Trigger (GSWTRG). This trigger links to the GSWTRG bit in the ADCCON3 register, which may be used to enable the user application to initiate a single conversion. Since GSWTRG is a self-clearing bit, it clears itself on the next ADC clock cycle after being set by the user application. The third software generated trigger selection is the Global Level Software Trigger (GLSWTRG), which is linked to the GLSWTRG bit in the ADCCON3 register. This trigger may be used by the user application to initiate a burst of consecutive samples, as the GLSWTRG bit is not self-clearing. The fourth trigger selection is a special selection, the Scan Trigger selection, which allows the Class 2 analog inputs to be included as members of a global scan of all inputs.
- Scanned trigger selection via the STRGSRC[4:0]bits in the ADCCON1 register and select bits in the ADCCSS1 registers. This mode is typically used to initiate the conversion of a group of analog inputs. This capability works for 2, and 3 analog inputs, but is typically used for Class 3 inputs because they do not have individual associated TRGSRC bits. One of the trigger selections is the GSWTRG bit in the ADCCON3 register, which may be used to enable the user software to initiate a conversion.
- User initiated trigger via the ADINSEL[5:0]bits and the RQCNVRT bit in the ADCCON3 register. This mode enables the user application to create an individual conversion trigger request for a specified analog input. Using this mode enables the user application to trigger the conversion of an input without changing the trigger source configuration of the ADC. This is useful in handling error situations where another software module wants ADC information without disrupting the normal operation of the ADC. This is also the preferred method to generate the initial trigger to start an digital filter sequence.
- User controlled sampling of Class 2 and Class 3 inputs via the ADINSEL[5:0]bits and the SAMP bit in the ADCCON3 register. Setting the SAMP bit causes the Class 2 and Class 3 inputs to be in Sampling mode, while ignoring the selection of the SAMC[9:0]bits. This mode is also useful in software conversion of ADC with software selectable sample time.
- External module (such as PTG) may specify an analog input for conversion via the setting of ECRIEN bit in the ADCCON2 register. This method operates independently of the normal TRGSRC and STRGSRC methods. External modules may still use individual trigger signals and initiate conversions via the normal TRGSRC and STRGSRC methods.

36.2.4.3 User-Requested Individual Conversion Trigger (Software ADC Conversion) (Only for Class 2 and Class 3 Inputs)

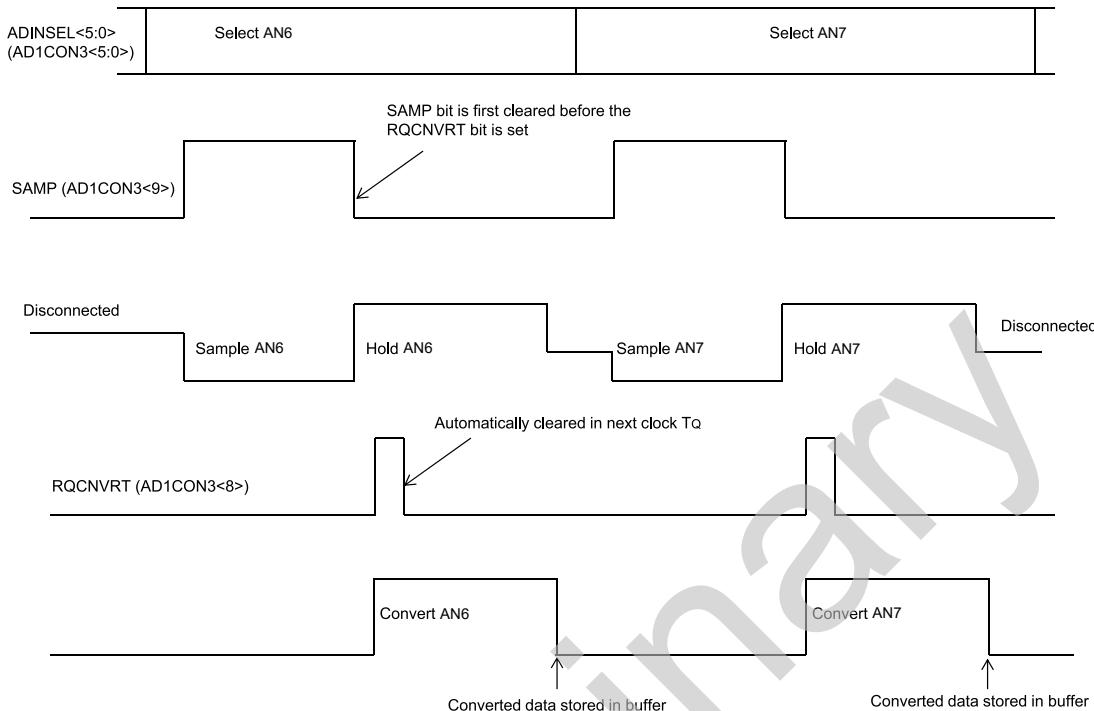
The user can explicitly request a single conversion (by software) of any selected analog input at any time during program execution, without changing the trigger source configuration of the ADC.

The steps to be followed for conversion are as follows:

1. The analog input ID to be converted is specified by the ADC Input Select bits, ADINSEL[5:0](ADCCON3[5:0]).
2. The sampling of analog input is started by setting the SAMP bit (ADCCON3[9]).
3. After the required sampling time (time delay), the SAMP bit is cleared.
4. The conversion of sampled signal is started by setting RQCNVRT bit (ADCCON3[8]).
5. Once the conversion is complete, the ARDYx bit of the ADCSTATx register is set. The data can be read from ADCDATAx register.

The following figure illustrates the conversion process in graphical form.

Figure 36-6. Individual Conversion Trigger Process



36.2.5 Selecting the Voltage Reference Source

The user application can select the voltage reference for the ADC module, which can be internal or external. The Voltage Reference Input Selection bits, VREFSEL[2:0] (ADCCON3[15:13]), select the voltage reference for analog-to-digital conversions. The upper voltage reference (V_{REFH}) and the lower voltage reference (V_{REFL}) may be the internal AV_{DD} and AV_{SS} voltage rails or the band gap reference generator or the external V_{REFH+} and V_{REFL} input pins. When the voltage reference and band gap reference are ready, the BGVRDY (ADCCON2[31]) bit is set. If a Fault occurs in the voltage reference (such as a brown-out), the REFFLT bit (ADCCON2[30]) is set. The BGVRDY and REFFLT bits can also generate interrupts if the BGVIEN bit (ADCCON2[15]) and REFFLTIEN bit (ADCCON2[14]) are set, respectively.

The voltages applied to the external reference pins must comply with certain specifications. Refer to the Electrical Specifications in the specific device data sheet for the electrical specifications.

The Analog Input Charge Pump Enable bit, AICMPEN (ADCCON1[12]), should be set when the difference between the selected reference voltages ($V_{REFH} - V_{REFL}$) is less than $0.65 * (AV_{DD} - AV_{SS})$. Setting this bit does not increase the magnitude of reference voltage; however, setting this bit reduces the series source resistance to the sampling capacitors. This maximizes the SNR for analog-to-digital conversions using small reference voltage rails.

36.2.6 Selecting the Scanned Inputs

All available analog inputs can be configured for scanning. Class 2 and Class 3 inputs are sampled using the shared ADC module. A single conversion trigger source is selected for all of the inputs selected for scanning using the STRGSRC[4:0] bits (ADCCON1[20:16]). On each conversion trigger, the ADC module starts converting in the natural priority all inputs specified in the user-specified scan list (ADCCSS1 or ADCCSS2). For Class 2 and Class 3 inputs, the trigger initiates a sequential sample/conversion process in the natural priority order.

An analog input belongs to the scan if it is:

- A Class 3 input. For Class 3 inputs, scan is the only mechanism for conversion.

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- A Class 2 input, which has the scan trigger selected as the trigger source, by selecting the STRIG option in the TRGSRCx[4:0] bits located in the ADCTRG1 through ADCTRG8 registers.

The trigger options available for scan are identical to those available for independent triggering of Class 2 inputs. Any Class 2 inputs that are part of the scan must have the STRIG option selected as their trigger source in the TRGSRCx[4:0] bits.

Note: The end-of-scan (EOS) is generated only if the last shared input conversion has completed. Until this condition is met, the scan sequence is still in effect. Therefore, the EOS Interrupt can be used for any scan sequence, with any combination of input types.

The following code is an example for ADC scanning multiple inputs.

```
int main(int argc, char** argv) {
    int result[3];

    /* Configure ADCCON1 */
    ADCCON1 = 0;           // No ADCCON1 features are enabled including: Stop-in-Idle, turbo,
    // CVD mode, Fractional mode and scan trigger source. ADCCON1bits.SELRES = 3; // ADC7
    resolution is 12 bits
    ADCCON1bits.TRGSRC = 1; // Select scan trigger.

    /* Configure ADCCON2 */
    ADCCON2bits.SAMC = 5;   // ADC7 sampling time = 5 * TAD7
    ADCCON2bits.ADCDIV = 1; // ADC7 clock freq is half of control clock = TAD7

    /* Initialize warm up time register */ ADCANCON = 0;
    ADCANCONbits.WKUPCLKCNT = 5; // Wakeup exponent = 32 * TADX

    /* Clock setting */
    ADCCON3bits.ADCSEL = 0;     // Select input clock source
    ADCCON3bits.CONCLKDIV = 1;  // Control clock frequency is half of input clock
    ADCCON3bits.VREFSEL = 0;    // Select AVDD and AVSS as reference source

    ADC0TIMEbits.ADCDIV = 1;    // ADC0 clock frequency is half of control clock = TAD0
    ADC0TIMEbits.SAMC = 5;      // ADC0 sampling time = 5 * TAD0
    ADC0TIMEbits SELRES = 3;    // ADC0 resolution is 12 bits

    /* Select analog input for ADC modules, no presync trigger, not sync sampling */
    ADCTRGMODEbits.SH0ALT = 0; // ADC0 = AN0

    /* Select ADC input mode */
    ADCIMCON1bits.SIGN0 = 0;    // unsigned data format ADCIMCON1bits.DIFF0 = 0;      //
    Single ended mode ADCIMCON1bits.SIGN8 = 0;    // unsigned data format ADCIMCON1bits.DIFF8
    = 0;          // Single ended mode ADCIMCON1bits.SIGN40 = 0;    // unsigned data format
    ADCIMCON1bits.DIFF40 = 0;    // Single ended mode

    /* Configure ADCGIRQENx */
    ADCGIRQEN1 = 0;           // No interrupts are used. ADCGIRQEN2 = 0;

    /* Configure ADCCSSx */
    ADCCSS1 = 0;               // Clear all bits
    ADCCSS2 = 0;
    ADCCSS1bits.CSS0 = 1;      // AN0 (Class 1) set for scan ADCCSS1bits.CSS8 = 1;      //
    AN8 (Class 2) set for scan ADCCSS2bits.CSS40 = 1;    // AN40 (Class 3) set for scan

    /* Configure ADCCMPCONx */
    ADCCMPCON1 = 0;            // No digital comparators are used. Setting the ADCCMPCONx
    ADCCMPCON2 = 0;            // register to '0' ensures that the comparator is disabled.
    ADCCMPCON3 = 0;            // Other registers are 'don't care'.
    ADCCMPCON4 = 0;
    ADCCMPCON5 = 0; ADCCMPCON6 = 0;

    /* Configure ADCFLTRx */
    ADCFLTR1 = 0;              // No oversampling filters are used. ADCFLTR2 = 0;
    ADCFLTR3 = 0; ADCFLTR4 = 0; ADCFLTR5 = 0; ADCFLTR6 = 0;
    /* Set up the trigger sources */
    ADCTRG1bits.TRGSRC0 = 3;   // Set AN0 (Class 1) to trigger from scan source
    ADCTRG3bits.TRGSRC8 = 3;   // Set AN8 (Class 2) to trigger from scan source
    // AN40 (Class 3) always uses scan trigger source

    /* Early interrupt */
    ADCEIEN1 = 0;               // No early interrupt
    ADCEIEN2 = 0;
```

```

/* Turn the ADC on */ ADCCON1bits.ON = 1;

/* Wait for voltage reference to be stable */
while(!ADCCON2bits.BGVRDY); // Wait until the reference voltage is ready
while(ADCCON2bits.REFFLT); // Wait if there is a fault with the reference voltage

/* Enable clock to analog circuit */
ADCANCONbits.ANEN0 = 1; // Enable the clock to analog bias ADC0
ADCANCONbits.ANEN7 = 1; // Enable, ADC7

/* Wait for ADC to be ready */
while(!ADCANCONbits.WKRDY0); // Wait until ADC0 is ready while(!
ADCANCONbits.WKRDY7); // Wait until ADC7 is ready

/* Enable the ADC module */
ADCCON3bits.DIGEN0 = 1; // Enable ADC0
ADCCON3bits.DIGEN7 = 1; // Enable ADC7

while (1) {
/* Trigger a conversion */ ADCCON3bits.GSWTRG = 1;

/* Wait the conversions to complete */
while (ADCDSTAT1bits.ARDY0 == 0);
/* fetch the result */
result[0] = ADCDATA0;

while (ADCDSTAT1bits.ARDY8 == 0);
/* fetch the result */
result[1] = ADCDATA8;

while (ADCDSTAT2bits.ARDY40 == 0);
/* fetch the result */
result[2] = ADCDATA40;

/*
 * Process results here
 *
 */
}
return (1);
}

```

36.2.7 Selecting the Analog-to-Digital Conversion Clock Source and Prescaler

The ADC module can use the internal Fast RC (FRC) oscillator output, system clock (SYSCLK), reference clock (REFCLK3) or peripheral bus clock (PBCLK) as the conversion clock source (T_Q). See *ADCCON3* register from Related Links.

When the ADCSEL[1:0] bits (ADCCON2[31:30]) = '01', the internal FRC oscillator is used as the ADC clock source. When using the internal FRC oscillator, the ADC module can continue to function in Sleep and Idle modes.

Note: It is recommended that applications that require precise timing of ADC acquisitions use SYSCLK as the clock source for the ADC.

For correct analog-to-digital conversions, the conversion clock limits must not be exceeded. Clock frequencies from 1 MHz to 28 MHz are supported by the ADC module.

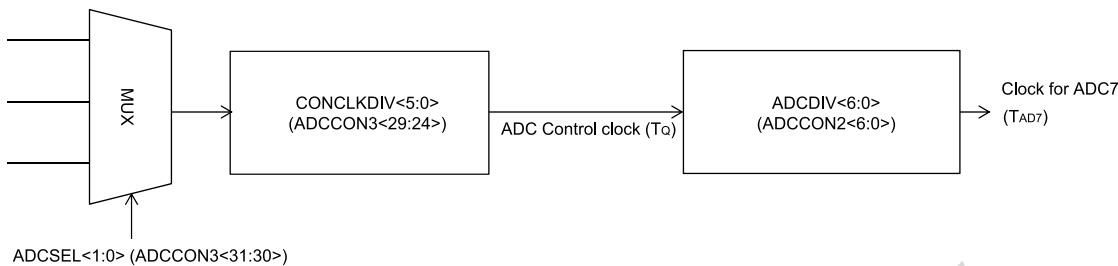
The maximum rate at which analog-to-digital conversions may be completed by the ADC module (effective conversion throughput) is 2 Msps. However, the maximum rate at which a single input can be converted is dependent on the sampling time requirements. In addition, the sampling time depends on the output impedance of the analog signal source. For more information on sampling time, see *ADC Sampling Requirements* from Related Links.

The input clock source for the ADC is selected using the ADCSEL[1:0] bits (ADCCON3[31:30]). The input clock is further divided by the control clock divider CONCLKDIV[5:0] bits (ADCCON3[29:24]). The output clock is called the "ADC control clock" with a time period of T_Q .

The ADC control clock is divided by the ADCDIV[6:0] bits (ADCxTIME[22:16]). This acts as the clock source for the respective dedicated ADC modules with a time period of T_{ADX} .

The ADC control clock is divided before it is used for the shared ADC by the ADCCDIV[6:0] bits(ADCCON2[6:0]). The time period for this clock is denoted as T_{AD7} .

Figure 36-7. Clock Derivation for Shared ADC Modules



Equation 36-2. Sample Time for the Shared ADC Module

$$t_{SAMC} = ADCCON2 < 25:16 > T_{AD}$$

$$t_{conversion} = 2 + ADCCON2 < 22:21 > T_{AD}$$

Related Links

[36.10.4. ADCCON3](#)

[36.8. ADC Sampling Requirements](#)

36.2.8 Turning ON the ADC

Turning ON the ADC module involves the following procedure.

When the ADC module enable bit, ON (ADCCON1[15]), is set to '1', the module is in Active mode and is fully powered and functional. When the ON bit is '0', the ADC module is disabled. Once disabled, the digital and analog portions of the ADC are turned off for maximum current savings. In addition to setting the ON bit, the analog and digital circuits of ADC should be turned ON. See [ADC Low-power Mode](#) from Related Links.

Note: Writing to the ADC control bits that control the ADC clock, input assignments, scanning, voltage reference selection, S&H circuit operating modes, and interrupt configuration is not recommended while the ADC module is enabled.

Related Links

[36.5.3. ADC Low-power Mode](#)

36.2.9 ADC Status Bits

The ADC module includes the WKRDYx/WKRDY7 status bit in the ADCANCON register, which indicates the current state of ADC Analog and bias circuit. The user application should not perform any ADC operations until this bit is set.

36.3 Additional ADC Functions

This section describes some additional features of the ADC module, which includes:

- Digital comparator
- Oversampling filter

36.3.1 Digital Comparator

The ADC module features digital comparators that can be used to monitor selected analog input conversion results and generate interrupts when a conversion result is within the user-specified limits. Conversion triggers are still required to initiate conversions. The comparison occurs automatically once the conversion is complete. This feature is enabled by setting the Digital Comparator Module Enable bit, ENDCMP (ADCCMPCONx[7]).

The user application makes use of an interrupt that is generated when the analog-to-digital conversion result is higher or lower than the specified high and low limit values in the ADCCMPx register. The high and low limit values are specified in the DCMPHI[15:0] bits (ADCCMPx[31:16]) and the DCMPLO[15:0] bits (ADCCMPx[15:0]).

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The CMPE_x bits ('x' = 0 through 31) in the ADCCMPEN_x registers are used to specify which analog inputs are monitored by the digital comparator (for the first 8 analog inputs, AN_x, where 'x' = 0 through 31). The ADCCMPCON_x register specifies the comparison conditions that generates an interrupt, as follows:

- When IEBTWN = 1, interrupt is generated when DCMPL0 ≤ ADCDATA < DCMPHI
- When IEHIHI = 1, interrupt is generated when DCMPHI ≤ ADCDATA
- When IEHILO = 1, interrupt is generated when ADCDATA < DCMPHI
- When IELOHI = 1, interrupt is generated when DCMPL0 ≤ ADCDATA
- When IELOLO = 1, interrupt is generated when ADCDATA < DCMPL0

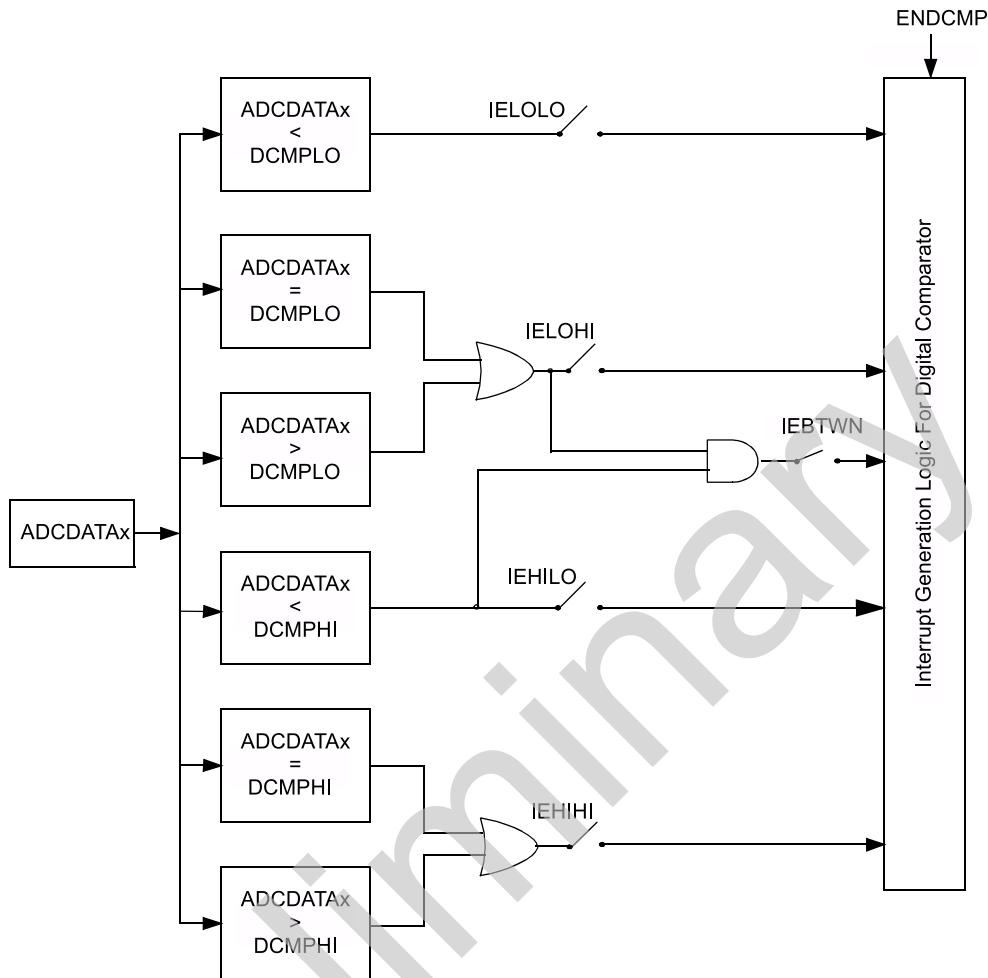
The comparator event generation is illustrated in the following figure. When the ADC module generates a conversion result, the conversion result is provided to the comparator. The comparator uses the DIFF_x and SIGN_x bits of the ADCIMCON_x register (depending on the analog input used) to determine the data format used and appropriately select whether the comparison should be signed or unsigned. The global ADC setting, which is specified by the FRACT bit (ADCCON1[23]), is also used to set the fractional or integer format. The digital comparator compares the ADC result with the high and low limit values (depending on the selected comparison criteria) in the ADCCMP_x register.

Depending on the comparator results, a digital comparator interrupt event may be generated. If a comparator event occurs, the Digital Comparator Interrupt Event Detected status bit, DCMPED (ADCCMPCON_x[5]), is set, and the Analog Input Identification (ID) bits, AINID[4:0] (ADCCMPCON_x[12:8]), are automatically updated so that the user application knows which analog input generated the interrupt event.

Note: The user software must format the values contained in the ADCCMP_x registers to match converted data format as either signed or unsigned, and fractional or integer.

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Figure 36-8. Digital Comparator



The following code is an example for ADC digital comparator.

```

int main(int argc, char** argv) {
    int result = 0, eventFlag = 0;

    /* Configure ADCCON1 */
    ADCCON1 = 0;                                // No ADCCON1 features are enabled including: Stop-in-Idle,
    // turbo, CVD mode, Fractional mode and scan trigger source. ADCCON1bits.SELRES = 3;           //
    ADC resolution is 12 bits
    ADCCON1bits.STRGSRC = 0;                      // No scan trigger.

    /* Configure ADCCON2 */
    ADCCON2bits.SAMC = 5;                         // ADC7 sampling time = 5 * TAD7
    ADCCON2bits.ADCDIV = 1;                        // ADC7 clock freq = TAD7

    /* Initialize warm up time register */ ADCANCON = 0;

    /* No selection for dedicated ADC modules, no presync trigger, not sync sampling */
    ADCTRGMODEbits = 0;

    /* Select ADC input mode */
    ADCIMCON1bits.SIGN8 = 0;                      // unsigned data format

```

```

ADCIMCON1bits.DIFF8 = 0;           // Single ended mode

/* Configure ADCGIRQENx */
ADCGIRQEN1 = 0;                  // No interrupts are used
ADCGIRQEN2 = 0;

/* Configure ADCCSSx */
ADCCSS1 = 0;                     // No scanning is used
ADCCSS2 = 0;

/* Configure ADCCMPCONx */
ADCCMP1 = 0;                     // Clear the register ADCCMP1bits.DCMPHI = 0xC00; // High
limit is a 3072 result. ADCCMP1bits.DCMPL0 = 0x500; // Low limit is a 1280 result.
ADCCMPCON1bits.IEBTWN = 1;        // Create an event when the measured result is
// >= low limits and < high limit. ADCCMPEN1 = 0; // Clear all enable bits
ADCCMPEN1bits.CMPE8 = 1;          // set the bit corresponding to AN8
ADCCMPCON1bits.ENABLE = 1;         // enable comparator
ADCCMPCON2 = 0; ADCCMPCON3 = 0; ADCCMPCON4 = 0; ADCCMPCON5 = 0; ADCCMPCON6 = 0;

/* Configure ADCFLTRx */
ADCFLTR1 = 0;                   // No oversampling filters are used. ADCFLTR2 = 0;
ADCFLTR3 = 0; ADCFLTR4 = 0; ADCFLTR5 = 0; ADCFLTR6 = 0;
/* Set up the trigger sources */
ADCTRG3bits.TRGSRC8 = 3;        // Set AN8 (Class 2) to trigger from scan source

/* Early interrupt */
ADCEIEN1 = 0;                   // No early interrupt
ADCEIEN2 = 0;

/* Turn the ADC on */ ADCCON1bits.ON = 1;

/* Wait for voltage reference to be stable */
while(!ADCCON2bits.BGVRDY);      // Wait until the reference voltage is ready
while(ADCCON2bits.REFFLT);       // Wait if there is a fault with the reference voltage

/* Enable clock to analog circuit */
ADCANCONbits.ANEN7 = 1;          // Enable the clock to analog bias

/* Wait for ADC to be ready */
while(!ADCANCONbits.WKRDY7);     // Wait until ADC7 is ready

/* Enable the ADC module */
ADCCON3bits.DIGEN7 = 1;          // Enable ADC7

while (1) {
/* Trigger a conversion */ ADCCON3bits.GSWTRG = 1;

while (ADCDSTAT1bits.ARDY8 == 0);
/* fetch the result */
result = ADCDATA8;

/* Note: It is not necessary to fetch the result for the digital
 * comparator to work. In this example we are triggering from
 * software so we are using the ARDY8 to gate our loop. Reading the
 * data clears the ARDY bit.
*/
/* See if we have a comparator event*/
if (ADCCMPCON1bits.DCMPED == 1) {
eventFlag = 1;
/*
* Process results here
*/
}
}
return (1);
}

```

36.3.2 Oversampling Digital Filter

The ADC module supports two oversampling digital filters. The oversampling digital filter consists of an accumulator and a decimator (down-sampler), which function together as a low-pass filter. By sampling an analog input at a higher than required sample rate, and then processing the data through the oversampling digital filter, the effective resolution of the ADC module can be increased at the expense of decreased conversion throughput.

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To obtain 'x' bits of extra resolution, number of samples required (over and above the Nyquist rate) = $(2^x)^2$:

- 4x oversampling yields one extra bit of resolution (total 13 bits resolution)
- 16x oversampling yields two extra bits of resolution (total 14 bits resolution)
- 64x oversampling provides three extra bits of resolution (total 15 bits resolution)
- 256x oversampling provides four extra bits of resolution (total 16 bits resolution)

The digital filter also has an averaging mode, where it accumulates the samples and divides it by the number of samples.

Note:

1. Only Class 2 analog inputs can engage the digital filter. Therefore, the CHNLID[2:0] bits are 3 bits wide (0 to 7).
2. During the burst conversion process (repeated trigger until all required data for oversampling is obtained) in the case of filtering Class 2 input using the shared ADC module, higher priority ADC inputs may still process conversions; lower priority ADC conversion requests are held waiting until the filter burst sequence has been completed.
3. If higher priority requests occur during the digital filter sequence, they delay the completion of the filtering process. This delay may affect the accuracy of the result because the multiple samples cannot be contiguous. The user should arrange the initiation trigger for the oversampling filters to occur while there are no expected interruptions from higher priority ADC conversion requests.

The user application should configure the following bits to perform an oversampling conversion:

- Select the amount of oversampling through the Oversampling Filter Oversampling Ratio (OVRSAM[2:0]) bits in the ADC Filter register (ADCFLTRx[28:26])
- Set the filter mode to either Oversampling mode or Averaging mode using the DFMODE bit(ADCFLTRx[29])
- If the filter is set to Averaging mode and the data format is set to fractional (FRACT bit), set or clear the DATA16EN bit (ADCFLTRx[30]) to set the output resolution
- Set the sample time for subsequent samples:
 - If using Class 2 inputs, select the sample time using the SAMC[9:0] bits (ADC-CON2[25:16])
- Select the specific analog input to be oversampled by configuring the Analog Input ID Selection bits, CHNLID[4:0] (ADCFLTRx[20:16])
- If needed, include the oversampling filter interrupt event in the global ADC interrupt, by setting the Accumulator Filter Global Interrupt Enable bit, AFGIEN (ADCFLTRx[25])
- Enable the oversampling filter by setting the Oversampling Filter Accumulator Enable bit, AFEN (ADCFLTRx[31])

Once the digital filter module is configured, the filter's control logic waits for an external trigger to initiate the process. The trigger signal for the analog input to be oversampled causes the accumulator to be cleared and initiates the first conversion. The trigger also forces the trigger sensitivity into level mode and forces the trigger itself to 1 as long as the filter needs to acquire the user specified number of samples via the OVRSAM[2:0] bits (ADCFLTRx[28:26]). The time delay between each acquired sample is decided by the set sample time in the SAMC[9:0] bits in the ADCCON2 register for Class 2) and the time for conversion. When the required number set by OVRSAM[2:0] have been received and processed, the data stored in the FLTRDATA[15:0] bit (ADCFLTRx[15:0]) and the AFRDY bit (ADCFLTRx[24]) is set, and the interrupt is generated (if enabled).

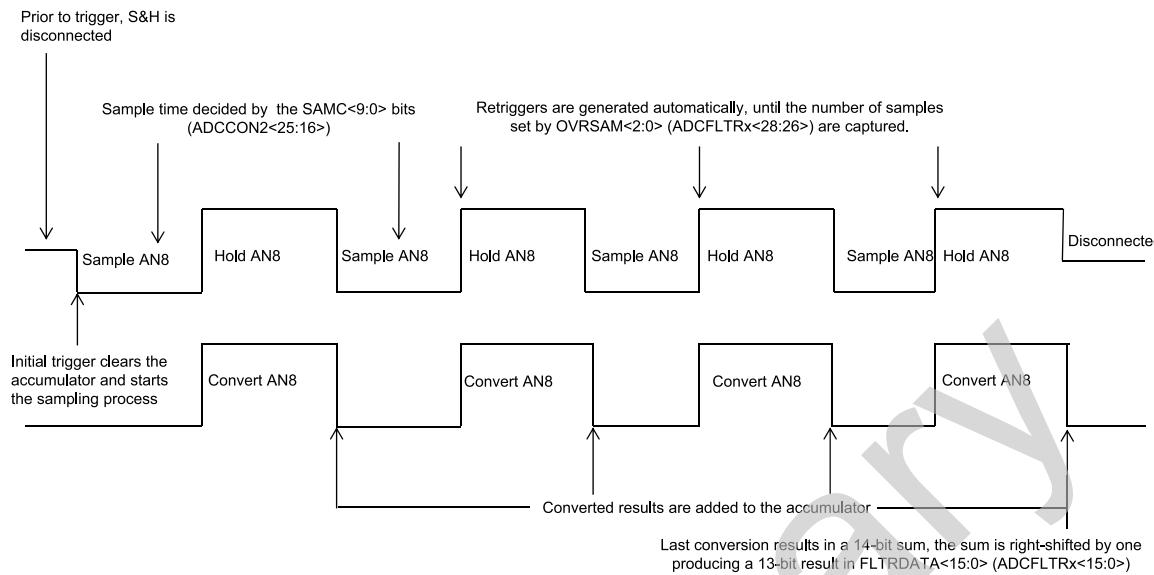
The following figure illustrates 4x oversampling using a Class 2 input. Triggering a Class 2 input initiates sampling for the length of time defined by the SAMC[9:0] bits. Retriggers generated by the oversampling logic use the SAMC[9:0] bits, to set the sample time.

Since Class 2 inputs use the shared S&H, oversampling blocks lower priority Class 2 and Class 3 triggers. Higher priority Class 2 triggers completely disrupt the oversampling process, and therefore, should be avoided completely. The same priority rule applies to two Class 2 inputs that use two digital filters. In such a case, the higher priority input is also use the shared ADC module in Burst mode and prevents the lower priority input to use the shared ADC. Only after all required samples are obtained by the higher priority input, the lower priority input can use the shared ADC to acquire samples for its own digital filtering.

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Figure 36-9. 4x Oversampling of a Class 2 Input



The following code is an example for ADC digital oversampling filter.

```

int main(int argc, char** argv) {
    int result;

    /* Configure ADCCON1 */
    ADCCON1 = 0;           // No ADCCON1 features are enabled including: Stop-in-Idle, turbo,
    // CVD mode, Fractional mode and scan trigger source.

    /* Configure ADCCON2 */
    ADCCON2 = 0;           // Since, we are using only the Class 1 inputs, no setting is
    // required for ADCDIV

    /* Initialize warm up time register */ ADCANCON = 0;
    ADCANCONbits.WKUPCLKCNT = 5; // Wake-up exponent = 32 * TADx

    /* Clock setting */ ADCCON3 = 0;
    ADCCON3bits.ADCSEL = 0;      // Select input clock source
    ADCCON3bits.CONCLKDIV = 1;   // Control clock frequency is half of input clock
    ADCCON3bits.VREFSEL = 0;     // Select AVDD and AVSS as reference source

    ADC0TIMEbits.ADCDIV = 1;    // ADC0 clock frequency is half of control clock = TAD0
    ADC0TIMEbits.SAMC = 5;      // ADC0 sampling time = 5 * TAD0
    ADC0TIMEbits.SELRES = 3;    // ADC0 resolution is 12 bits

    /* Select analog input for ADC modules, no presync trigger, not sync sampling */
    ADCTRGMODEbits.SH0ALT = 0;  // ADC0 = AN0

    /* Select ADC input mode */
    ADCIMCON1bits.SIGN0 = 0;    // unsigned data format
    ADCIMCON1bits.DIFF0 = 0;    // Single ended mode

    /* Configure ADCGIRQENx */
    ADCGIRQEN1 = 0;            // No interrupts are used
    ADCGIRQEN2 = 0;

    /* Configure ADCCSSx */
    ADCCSS1 = 0;                // No scanning is used
    ADCCSS2 = 0;
    /* Configure ADCCMPCONx */
    ADCCMPCON1 = 0;             // No digital comparators are used. Setting the ADCCMPCONx
    ADCCMPCON2 = 0;             // register to '0' ensures that the comparator is disabled.
    ADCCMPCON3 = 0;             // Other registers are 'don't care'.
    ADCCMPCON4 = 0; ADCCMPCON5 = 0; ADCCMPCON6 = 0;

```

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```
/* Configure ADCFLTRx */
ADCFLTR1 = 0; // Clear all bits ADCFLTR1bits.CHNLID = 0; // Use AN0 as
the source ADCFLTR1bits.OVRSAM = 3; // 16x oversampling ADCFLTR1bits.DFMODE = 0; // 
Oversampling mode ADCFLTR1bits.AFEN = 1; // Enable filter 1
ADCFLTR2 = 0; // Clear all bits
ADCFLTR3 = 0; ADCFLTR4 = 0; ADCFLTR5 = 0; ADCFLTR6 = 0;

/* Set up the trigger sources */ ADCTGSNSbits.LVL0 = 0; // Edge trigger
ADCTRGLbits.TRGSRC0 = 1; // Set AN0 to trigger from software.

/* Turn the ADC on */ ADCCON1bits.ON = 1;

/* Wait for voltage reference to be stable */
while(!ADCCON2bits.BGVRRDY); // Wait until the reference voltage is ready
while(ADCCON2bits.REFFLT); // Wait if there is a fault with the reference voltage

/* Enable clock to analog circuit */
ADCANCONbits.ANENO = 1; // Enable the clock to analog bias and digital control

/* Wait for ADC to be ready */
while(!ADCANCONbits.WKRDY0); // Wait until ADC0 is ready

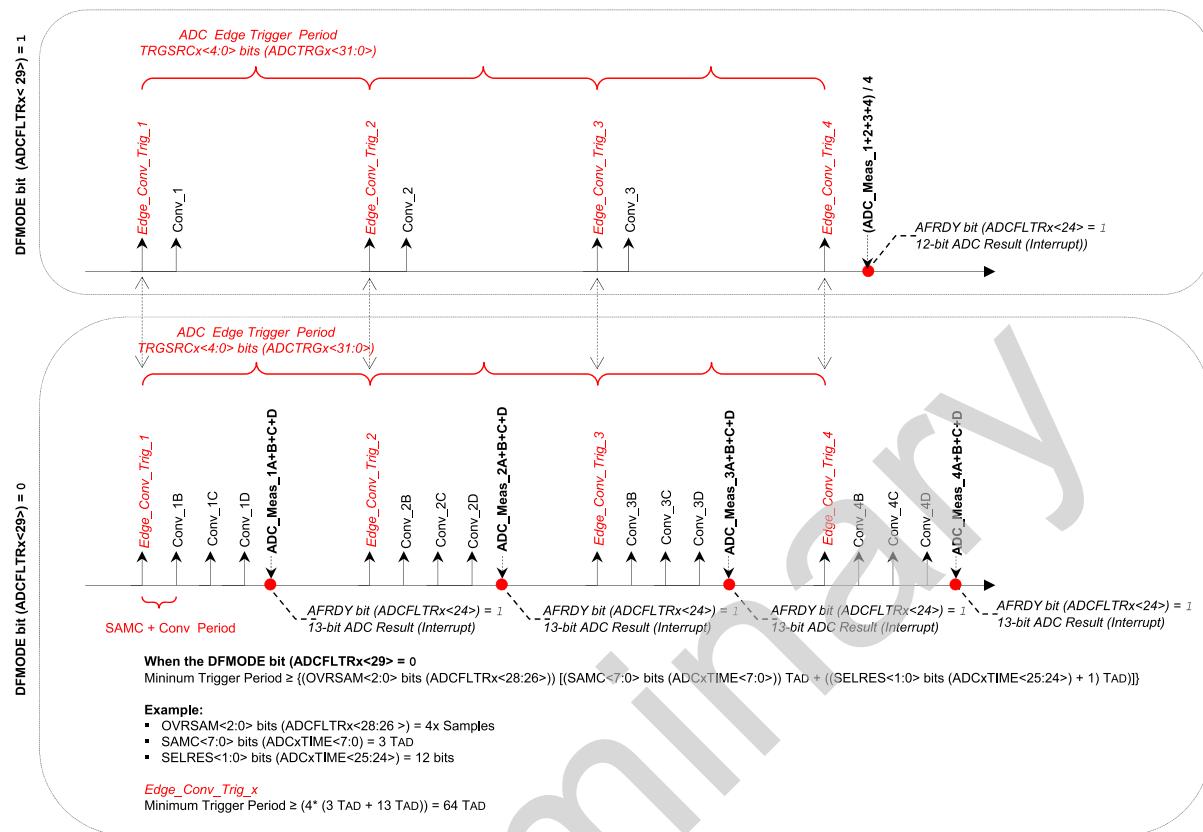
/* Enable the ADC module */ ADCCON3bits.DIGENO = 1; // Enable ADC0

while (1) {
/* Trigger a conversion */ ADCCON3bits.GSWTRG = 1;

/* Wait for the oversampling process to complete */
while (ADCFLTR1bits.AFRDY == 0);
/* fetch the result */
result = ADCFLTR1bits.FLTRDATA;

/*
 * Process result Here
 *
 * Note 1: Loop time determines the sampling time for the first sample.
 * remaining samples sample time is determined by set sampling + conversion time.
 *
 * Note 2: The first 5 samples may have reduced accuracy.
 *
 */
}
return (1);
}
```

Figure 36-10. ADC Filter Comparisons Example



36.4 Interrupts

The ADC module supports interrupts triggered from a variety of sources, which can be processed individually or globally. An early interrupt feature is also available to compensate for interrupt servicing latency.

After an enabled interrupt is generated, the CPU jumps to the vector assigned to that interrupt. The CPU begins executing code at the vector address. The user software at this vector address should perform the required operations, such as processing the data results, clearing the interrupt flag, and then exit. See *Nested Vector Interrupt Controller* from Related Links for more information on interrupts and the vector address table details.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

36.4.1 Interrupt Sources

The ADC is capable of generating interrupts from the events listed in the following table.

Table 36-4. ADC Interrupt Sources

Interrupt Event	Description	Interrupt Enable Bit	Interrupt Status Bit
ANx Data Ready Event	Interrupt is generated upon a completion of a conversion from an analog input source (ANx). Each of the ARDYx bits is capable of generating a unique interrupt when set, using the ADCBASE register.	AGIENx of ADCGIRQEN1	ARDYx of ADCDSTAT1 register

.....continued

Interrupt Event	Description	Interrupt Enable Bit	Interrupt Status Bit
Digital Comparator Event	When an conversion's comparison criteria are met by a configured and enabled digital comparator. Each of the digital comparators is capable of generating a unique interrupt when its DCMPED bit is set	DCMPGIEN of ADCCMPCONx register	DCMPED of ADCCMPCONx register
Oversampling Filter Data Ready Event	When an oversampling filter has completed the accumulation/decimation process and has stored the result.	AFGIEN of ADCFLTRx register	AFRDY of ADCFLTRx register
Both Band Gap Voltage and ADC Reference Voltage Ready Event	Interrupt is generated when both band gap voltage and ADC reference voltage are ready.	BGVRIEN of ADCCON2 register	BGVRDY of ADCCON2 register
Band Gap Fault/Reference Voltage Fault/AV _{DD} Brown-out Fault Event	Interrupt is generated when Band Gap Fault/Reference Voltage Fault/AV _{DD} Brown-out occurs.	REFFLTIEN of ADCCON2 register	REFFLT of ADCCON2 register
ADC Module Wake-up Event	Interrupt is generated when ADC wakes-up after being enabled.	WKIEN0 of ADCANCON register	WKRDY0 of ADCANCON register
Update Ready Event	Interrupt is generated when ADC SFRs are ready to be (and can be safely) updated with new values.	UPDIEN of ADCCON3 register	UPDRDY of ADCCON3 register

36.4.2 ADC Base Register (ADCBASE) Usage

After conversion of ADC is complete, if the interrupt is vectored to a function which is common to all analog inputs, it takes some significant time to find the ADC input by evaluating the ARDYx bits in the ADCDSTATx. To avoid this time spent, ADCBASE register is provided, which contains the base address of the user's ADC ISR jump table. When read, the ADCBASE register provides a sum of the contents of the ADCBASE register plus an encoding of the ARDYx bits set in the ADCDSTATx registers. This use of the ADCBASE register supports the creation of an interrupt vector address that can be used to improve the performance of an ISR.

The ARDYx bits are binary priority encoded with ARDY1 being the highest priority, and ARDY8 being the lowest priority. The encoded priority result is then shifted left the amount specified by the number of bit positions specified by the IRQVS[2:0] bits in the ADCCON1 register, and then added to the contents of the ADCBASE register. If there are no ARDYx bits set, then reading the ADCBASE register equals the value written into the ADCBASE register.

The ADCBASE register is typically be loaded with the base address of a jump table that contains the address of appropriate ISR. The kth interrupt request is enabled via the AGIENx bit (1-8) in one of ADCGIRQENx SFRs ('x' = 1 or 2).

The following codes are example for ADCBASE register usage.

Case 1:

```
ADCBASE = 0x1234; // Set the address
ADCCON1bits.IRQVS = 2; // left shift by 2
ADCGIRQEN1bits.AGIENO = 1; // enable interrupt when AN0 completion is done.
```

Once the ADC conversion for AN0 is complete, bit 0 of ADCDSTAT1 = ARDY0 is set.

Read value of ADCBASE = 0x1234 + (0 << 2) = 0x1234.

Therefore, the ISR should be placed at address 0x1234 for AN0.

Case 2:

```
ADCBASE = 0x1234; // Set the address  
ADCCON1bits.IRQVS = 2; // left shift by 2  
ADCGIRQEN1bits.AGIENO = 2; // enable interrupt when AN2 completion is done.
```

Once the ADC conversion for AN2 is complete, bit 2 of ADCDSTAT1 = ARDY2 is set.

Read value of ADCBASE = $0x1234 + (2 \ll 2) = 0x123C$.

Therefore, the ISR should be placed at address $0x123C$ for AN2.

Note: The contents of the ADCBASE register are not altered. Summation is performed when ADCBASE register is read and the summation result is the returned read value from the ADCBASE SFR.

36.4.3 Interrupt Enabling, Priority and Vectoring

Each of the ADC events previously mentioned generates an interrupt when its associate Interrupt Enable bit, IE, is set. Each of the ADC events previously listed also has an associated interrupt vector. See [Nested Vector Interrupt Controller](#) from Related Links for more information on the vector location and control/status bits associated with each individual interrupt.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

36.4.4 Individual and Global Interrupts

The use of the individual interrupts previously listed can significantly optimize the servicing of multiple ADC events, by keeping each ISR focused on efficiently handling a specific event. In addition, different ISRs can be easily segregated according to the tasks performed, thereby making user software easier to implement and maintain. There may be cases where it is desirable to have a single ISR service multiple interrupt events. To facilitate this, each ADC event can be logically "ORed" to create a single global ADC interrupt. When an ADC event is enabled for a global interrupt, it vectors to a single interrupt routine. It is the responsibility of this single global ISR to determine the source of the interrupt through polling and process it accordingly.

Use of the Global Interrupt requires configuration of its own unique IE, IF, IP and IS bits as well as configuration of its interrupt vector as described in [Interrupt Enabling, Priority and Vectoring](#), see [Interrupt Enabling, Priority and Vectoring](#) from Related Links.

Interrupts for the ADC can be configured as individual or global, or utilize both where some are processed individually and others in the global ISR.

Related Links

[36.4.3. Interrupt Enabling, Priority and Vectoring](#)

36.5 Power-Saving Modes of Operation

The Power-Saving, Sleep and Idle modes, are useful for reducing the conversion noise by minimizing the digital activity of the CPU, buses and other peripherals.

36.5.1 Sleep Mode

When device enters Sleep mode, the system clock (SYCCLK) is halted. If an ADC module selects SYSCLK as its clock source or selects REFCLK3 as its clock source (REFCLK3 is generated from SYSCLK), the ADC enters the Sleep mode.

When the SYSCLK is the source, (directly or indirectly) and Sleep mode occurs during a conversion, the conversion is aborted. The converter cannot resume a partially completed conversion on exiting from Sleep mode. The ADC register contents are not affected by the device entering or leaving Sleep mode. The ADC module can operate during Sleep mode if the ADC clock source is derived from a source other than SYSCLK that is active during Sleep mode. The FRC clock source is a logical choice for operation during Sleep; however, the REFCLK3 clock source can also be used, provided it has an input clock that is operational during Sleep mode.

ADC operation during Sleep mode reduces the digital switching noise from the conversion. When the conversion is completed, the ARDYx status bit for that analog input is set and the result is loaded into the corresponding ADC Result register (ADCDATAx).

If any of the ADC interrupts is enabled, the device is wake-up from Sleep mode when the ADC interrupt occurs. The program execution resumes at the ADC ISR, if the ADC interrupt is greater than the current CPU priority. Otherwise, execution continues from the instruction after the WAIT instruction that placed the device in Sleep mode.

To minimize the effects of digital noise on the ADC module operation, the user must select a conversion trigger source that ensures that the analog-to-digital conversion take places in Sleep mode. For example, the external interrupt pin (INT0) conversion trigger option (TRGSRC[4:0] = 00100) can be used for performing sampling and conversion while the device is in Sleep mode.

Note: For the ADC module to operate in Sleep mode, the ADC clock source must be set to Internal FRC (ADCSEL[1:0] bits (ADCCON2[31:30]) = 01). Alternately, the REFCLK3 source can be used; however, the clock source used for REFCLK3 must operate during Sleep. Any changes to the ADC clock configuration require that the ADC be disabled.

36.5.2 ADC Operation During Idle Mode

For the ADC, the stop in Idle Mode bit, SIDL (ADCCON1[13]), specifies whether the ADC module stops on Idle or continue on Idle. If SIDL = 0, the ADC module continues normal operation when the device enters Idle mode. If any of the ADC interrupts are enabled, the device wake-up from Idle mode when the ADC interrupt occurs. The program execution resumes at the ADC ISR if the ADC interrupt is greater than the current CPU priority. Otherwise, execution continues from the instruction after the WAIT instruction that placed the device in Idle mode.

If SIDL = 1, the ADC module stops in Idle mode. If the device enters Idle mode during a conversion, the conversion is aborted. The converter cannot resume a partially completed conversion on exiting from Idle mode.

36.5.3 ADC Low-power Mode

The ADC module can be placed in a low-power state by disabling the digital circuit for individual ADC modules, which are not running. This is possible by clearing the DIGENx bits and the DIGEN7 bit in the ADCCON3 register (see ADCCON3 register from Related Links).

An even lower power state is possible by disabling the analog and bias circuit for individual ADC modules, which are not running. This is possible by clearing the ANENx bits and the ANEN7 bit in the ADCANCON register (see ADCANCON register from Related Links). Disabling the digital circuit to achieve Low-power mode provides a significantly faster module restart compared to disabling and re-enabling the analog and bias circuit of the ADC module. This is because disabling and re-enabling the analog and bias circuit using the ANENx bits and the ANEN7 bit requires a wake-up time (typical minimum wake-up time of 20 μ s) for the ADC module, before it can be used. Refer to the Electrical Specifications in the specific device data sheet for more information on the stabilization time.

Once the analog and bias circuit for an ADC module is enabled, the wake-up should be polled (or through an interrupt) using the wake-up ready bits, WKRDY6:WKRDY0 and WKRDY7, which should be equal to '1'.

Related Links

[36.10.4. ADCCON3](#)

[36.10.24. ADCANCON](#)

36.6 Effects of Reset

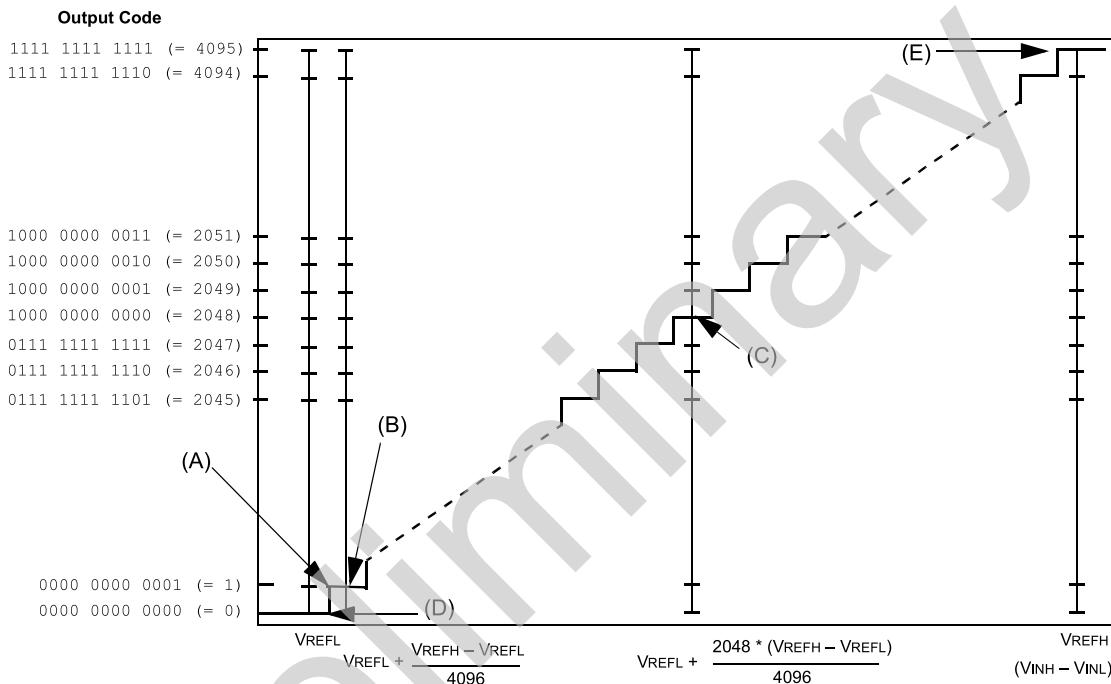
Following any Reset event, all the ADC control and status registers are reset to their default values with control bits in a non-active state. This disables the ADC module and sets the analog input pins to Analog Input mode. Any conversion that was in progress terminates and the result cannot be written to the result buffer. The values in the ADCDATAx registers are initialized to 0x00000000 during a device Reset. The bias circuits are also turned off, so the ADC resuming operations are wait for the bias circuits to stabilize by polling (or requesting to be interrupted by) the BGVRDY bit (ADCCON2 register).

36.7 Transfer Function

A typical transfer function of the 12-bit ADC is illustrated in the following figure. The difference of the input voltages ($V_{INH} - V_{INL}$) is compared with the reference ($V_{REFH} - V_{REFL}$).

- The first code transition (A) occurs when the input voltage is $(V_{REFH} - V_{REFL})/8192$ or 0.5 Lsb
- The 0000 0000 0001 code is centered at $(V_{REFH} - V_{REFL})/4096$ or 1.0 Lsb (B)
- The 1000 0000 0000 code is centered at $(2048 * (V_{REFH} - V_{REFL})/4096)$ (C)
- An input voltage less than $(1 * (V_{REFH} - V_{REFL})/8192)$ converts as 0000 0000 0000 (D)
- An input greater than $(8192 * (V_{REFH} - V_{REFL})/8192)$ converts as 1111 1111 1111 (E)

Figure 36-11. Analog-to-Digital Transfer Function



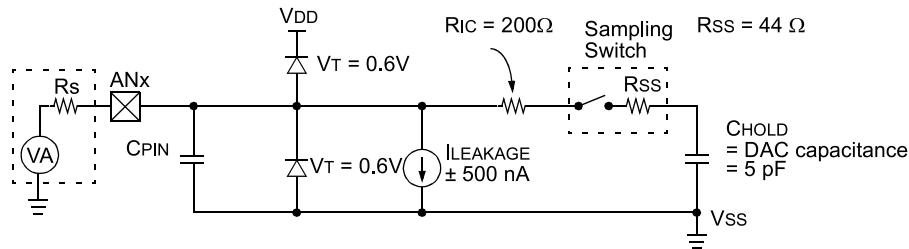
36.8 ADC Sampling Requirements

The analog input model of the 12-bit ADC is illustrated in the following figure. The total acquisition time for the analog-to-digital conversion is a function of the internal circuit settling time and the holding capacitor charge time.

For the ADC module to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the voltage level on the analog input pin. The analog output source impedance (R_S), the interconnect impedance (R_{IC}), and the internal sampling switch (R_{SS}) impedance combine to directly affect the time required to charge the C_{HOLD} . The combined impedance of the analog sources must therefore be small enough to fully charge (to within one-fourth LSB of the desired voltage) the holding capacitor within the selected sample time. The internal holding capacitor is in the discharged state prior to each sample operation.

At least 1 T_{AD} time period should be allowed between conversions for the acquisition time. Refer to the Electrical Specifications in the specific device data sheet for more information.

Figure 36-12. 12-bit ADC Analog Input Model



Note: The C_{PIN} value depends on the device package and is not tested. The effect of the C_{PIN} is negligible if $R_s \leq 5\text{ k}\Omega$.

Legend:

- C_{PIN} = Input capacitance
- R_{SS} = Sampling switch resistance
- R_s = Source resistance
- $I_{LEAKAGE}$ = Leakage current at the pin due to various junctions
- V_T = Threshold voltage
- R_{IC} = Interconnect resistance
- C_{HOLD} = Sample/hold capacitance

36.9 Connection Considerations

Because the analog inputs employ Electrostatic Discharge (ESD) protection, they have diodes to V_{DD} and V_{SS} ; therefore, the analog input must be between V_{DD} and V_{SS} . The presence of diodes is the reason why the analog pins cannot be 5V tolerant. If the input voltage exceeds this range by greater than 0.3V (either direction), one of the diodes becomes forward biased and it may damage the device if the input current specification exceeds.

An external RC filter is sometimes added for antialiasing of the input signal. The R (resistive) component should be selected to ensure that the acquisition time is met. Any external components connected (through high-impedance) to an analog input pin (capacitor, Zener diode, and so on) should have very little leakage current at the pin.

36.10 Control Registers

Notes: Following conventions are used in the following registers:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
- -n = Value at POR
- HS = Hardware Set
- HC = Hardware Cleared

Note: Register offsets shown below are with respect to Base Address = 0x4400_0000. CLR/SET/INV registers for each register are located at offset <register offset> + 0x04, 0x08, 0x0C, respectively.

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36.10.1 Register Summary

The PIC32CX-BZ2 12-bit High Speed SAR ADC module has the following Special Function Registers (SFRs):

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x13FF	Reserved									
0x1400	ADCCON1	7:0		IRQVS[2:0]			STRGLVL	DMABL[2:0]		
		15:8	ON	FRZ	SIDL			FSYDMA	FSYUPB	SCANEN
		23:16	FRACT	SELRES[1:0]		STRGSRC[4:0]				
		31:24								
0x1404 ... 0x140F	Reserved									
0x1410	ADCCON2	7:0		ADCDIV[6:0]						
		15:8	BGVRIEN	REFFLTIEN	EOSIEN		ENXCNVRT			
		23:16		SAMC[7:0]						
		31:24	BGVRRDY	REFFLT	EOSRDY				SAMC[9:8]	
0x1414 ... 0x141F	Reserved									
0x1420	ADCCON3	7:0	GLSWTRG	GSWTRG	ADINSEL[5:0]					
		15:8	VREFSEL[2:0]			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT
		23:16	CHN_EN_SH R							
		31:24	ADCSEL[1:0]			CONCLKDIV[5:0]				
0x1424 ... 0x143F	Reserved									
0x1440	ADCIMCON1	7:0	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0
		15:8	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
		23:16	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
		31:24								
0x1444 ... 0x147F	Reserved									
0x1480	ADCGIRQEN1	7:0	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0
		15:8					AGIEN11	AGIEN10	AGIEN9	AGIEN8
		23:16								
		31:24								
0x1484 ... 0x149F	Reserved									
0x14A0	ADCCSS1	7:0	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
		15:8					CSS11	CSS10	CSS9	CSS8
		23:16								
		31:24								
0x14A4 ... 0x14BF	Reserved									
0x14C0	ADCDSTAT1	7:0	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0
		15:8					ARDY11	ARDY10	ARDY9	ARDY8
		23:16								
		31:24								
0x14C4 ... 0x14DF	Reserved									
0x14E0	ADCCMPEN1	7:0	CMPEX[7:0]							
		15:8								
		23:16								
		31:24								

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x14E4 ...	Reserved									
0x14EF										
0x14F0	ADCCMP1	7:0								
		15:8								
		23:16								
		31:24								
0x14F4 ...	Reserved									
0x14FF										
0x1500	ADCCMPEN2	7:0					CMPEX[7:0]			
		15:8								
		23:16								
		31:24								
0x1504 ...	Reserved									
0x150F										
0x1510	ADCCMP2	7:0					DCMPLO[7:0]			
		15:8					DCMPLO[15:8]			
		23:16					DCMPHI[7:0]			
		31:24					DCMPHI[15:8]			
0x1514 ...	Reserved									
0x159F										
0x15A0	ADCFLTR1	7:0					FLTRDATA[7:0]			
		15:8					FLTRDATA[15:8]			
		23:16						CHNLID[4:0]		
		31:24	AFEN	DATA16EN	DFMODE		OVRSAM[2:0]		AFGIEN	AFRDY
0x15A4 ...	Reserved									
0x15AF										
0x15B0	ADCFLTR2	7:0					FLTRDATA[7:0]			
		15:8					FLTRDATA[15:8]			
		23:16						CHNLID[4:0]		
		31:24	AFEN	DATA16EN	DFMODE		OVRSAM[2:0]		AFGIEN	AFRDY
0x15B4 ...	Reserved									
0x15FF										
0x1600	ADCTRG1	7:0						TRGSRC0[4:0]		
		15:8						TRGSRC1[4:0]		
		23:16						TRGSRC2[4:0]		
		31:24						TRGSRC3[4:0]		
0x1604 ...	Reserved									
0x160F										
0x1610	ADCTRG2	7:0						TRGSRC4[4:0]		
		15:8						TRGSRC5[4:0]		
		23:16						TRGSRC6[4:0]		
		31:24						TRGSRC7[4:0]		
0x1614 ...	Reserved									
0x167F										
0x1680	ADCCMPCON1	7:0	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHIL0	IELOHI	IELOLO
		15:8						AINID[5:0]		
		23:16								
		31:24								
0x1684 ...	Reserved									
0x168F										

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1690	ADCCMPCON2	7:0	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHIL0	IELOHI	IELOLO
		15:8								AINID[4:0]
		23:16								
		31:24								
0x1694 ... 0x16FF	Reserved									
0x1700	ADCBASE	7:0								ADCBASE[7:0]
		15:8								ADCBASE[15:8]
		23:16								
		31:24								
0x1704 ... 0x170F	Reserved									
0x1710	ADCDMASTAT	7:0								RAF0
		15:8	DMACNTEN							RAF0IEN
		23:16	WROVRERR							RBF0
		31:24	DMAEN							RBF0IEN
0x1714 ... 0x171F	Reserved									
0x1720	ADCCNTB	7:0								ADCCNTB[7:0]
		15:8								ADCCNTB[15:8]
		23:16								ADCCNTB[23:16]
		31:24								ADCCNTB[31:24]
0x1724 ... 0x172F	Reserved									
0x1730	ADCDMAB	7:0								ADDMAB[7:0]
		15:8								ADDMAB[15:8]
		23:16								ADDMAB[23:16]
		31:24								ADDMAB[31:24]
0x1734 ... 0x173F	Reserved									
0x1740	ADCTRGSNS	7:0	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0
		15:8								
		23:16								
		31:24								
0x1744 ... 0x17FF	Reserved									
0x1800	ADCANCON	7:0	ANEN7							ANENO
		15:8	WKRDY7							WKRDY0
		23:16	WKIEN7							WKIENO
		31:24								WKUPCLKCNT[3:0]
0x1804 ... 0x1AFF	Reserved									
0x1B00	ADCSYSCFG0	7:0								AN[7:0]
		15:8								AN[15:8]
		23:16								AN[19:16]
		31:24								
0x1B04 ... 0x1DFF	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1E00	ADCDATAx	7:0					DATA[7:0]			
		15:8					DATA[15:8]			
		23:16					DATA[23:16]			
		31:24					DATA[31:24]			

Preliminary

36.10.2 ADCCON1 - ADC Control Register 1

Name: ADCCON1
Offset: 0x1400
Reset: 0x00601000
Property: -

This register controls the basic operation of the ADC module, including behavior in Sleep and Idle modes, and data formatting. This register also specifies the vector shift amounts for the Interrupt Controller. Additional ADCCON1 functions include the RAM buffer length in DMA mode.

Bit	31	30	29	28	27	26	25	24
Access								
Reset	0	0	1	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	STRGSRC[4:0]		
Reset	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W			FSYDMA	FSYUPB	SCANEN
Reset	0	0	0			0	0	0
Bit	7	6	5	4	3	2	1	0
Access		R/W	R/W	R/W	STRGLVL		DMABL[2:0]	
Reset		0	0	0	0	0	0	0

Bit 23 – FRACT Fractional Data Output Format bit

Value	Description
0	Integer
1	Fractional

Bits 22:21 – SELRES[1:0] Shared ADC (ADC2) Resolution bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result occupies 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits results in ADCDATAx[5:0] being set to '0', and ADCDATAx[11:6] holding the result.

Value	Description
11	12 bits (default)
10	10 bits
01	8 bits
00	6 bits

Bits 20:16 – STRGSRC[4:0] ScanTrigger Source Select bits

Value	Description
10001 – 11111	Reserved
10000	EVSYS_47
01111	EVSYS_46
01110	EVSYS_45
01101	EVSYS_44
01100	EVSYS_43
01011	EVSYS_42
01010	EVSYS_41

Value	Description
01001	EVSYS_40
01000	EVSYS_39
00111	EVSYS_38
00110	EVSYS_37
00101	EVSYS_36
00100	INT0 External interrupt
00011	Reserved
00010	Global level software trigger (GLSWTRG)
00001	Global software edge trigger (GSWTRG)
00000	No Trigger

Bit 15 – ON ADC Module Enable bit

Note: The ON bit should be set only after the ADC module has been configured.

Value	Description
0	ADC module is disabled
1	ADC module is enabled

Bit 14 – FRZ Freeze in Debug Mode

Value	Description
0	Do not freeze in Debug mode
1	Freeze in Debug mode

Bit 13 – SIDL Stop in Idle Mode bit

Value	Description
0	Continue module operation in Idle mode
1	Discontinue module operation when device enters Idle mode

Bit 10 – FSYDMA Fast Synchronous DMA System Clock bit

Value	Description
0	Fast synchronous DMA system clock is disabled
1	Fast synchronous DMA system clock is enabled

Bit 9 – FSYUPB Fast Synchronous UPB Clock bit

Value	Description
0	Fast synchronous UPB clock is disabled
1	Fast synchronous UPB clock is enabled

Bit 8 – SCANEN SCAN Enable bit**Bits 6:4 – IRQVS[2:0]** Interrupt Vector Shift bits

To determine interrupt vector address, this bit specifies the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + $x \ll \text{IRQVS}[2:0]$, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

Value	Description
111	Shift x left 7 bit position
110	Shift x left 6 bit position
101	Shift x left 5 bit position
100	Shift x left 4 bit position
011	Shift x left 3 bit position
010	Shift x left 2 bit position
001	Shift x left 1 bit position
000	Shift x left 0 bit position

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Bit 3 – STRGLVL ScanTrigger High Level/Positive Edge Sensitivity bit

Value	Description
0	Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx[4:0] in the ADCTRGx register), only a single scan trigger is generated, which completes the scan of all selected analog inputs.
1	Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx[4:0] in the ADCTRGx register), the scan trigger continues for all selected analog inputs, until the STRIG option is removed.

Bits 2:0 – DMABL[2:0] DMA to System RAM Buffer Length Size

Defines the number of locations in system memory allocated per analog input for DMA interface use. As each output data is 16-bit wide, one location consists of 2 bytes. Therefore the actual size reserved in the system RAM follows the formula: RAM Buffer Length in bytes = $2^{(DMABL+1)}$.

36.10.3 ADCCON2 - ADC Control Register 2

Name: ADCCON2
Offset: 0x1410
Reset: 0x00000000
Property: -

This register controls the reference selection for the ADC module, the sample time for the shared ADC module, interrupt enable for reference, early interrupt selection, and clock division selection for the shared ADC.

Bit	31	30	29	28	27	26	25	24
	BGVRRDY	REFFLT	EOSRDY				SAMC[9:8]	
Access	R/HS/HC	R/HS/HC	R/HS/HC				R/W	R/W
Reset	0	0	0				0	0
Bit	23	22	21	20	19	18	17	16
				SAMC[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	BGVRIEN	REFFLTIEN	EOSIEN		ENXCNVRT			
Access	R/W	R/W	R/W		R/W			
Reset	0	0	0		0			
Bit	7	6	5	4	3	2	1	0
				ADCDIV[6:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 31 – BGVRRDY Band Gap Voltage/ADC Reference Voltage Status bit

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1[15]) = 0.

Value	Description
0	Either or both band gap voltage and ADC reference voltages (V_{REF}) are not ready
1	Both band gap and ADC reference voltages (V_{REF}) are ready

Bit 30 – REFFLT Band Gap/ V_{REF} / V_{DD} BOR Fault Status bit

This bit is cleared when the ON bit (ADCCON1[15]) = 0 and the BGVRRDY bit = 1.

Value	Description
0	Band gap and V_{REF} voltage are working properly
1	Fault in band gap or the V_{REF} voltage while the ON bit (ADCCON1[15]) was set. Most likely a band gap or V_{REF} fault is caused by a BOR of the analog V_{DD} supply.

Bit 29 – EOSRDY End of Scan Interrupt Status bit

This bit is cleared when ADCCON2[31:24] are read in software.

Value	Description
0	Scanning has not completed
1	All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning

Bits 25:16 – SAMC[9:0] SampleTime for the Shared ADC (ADC2) bits

Where T_{AD7} = Period of the ADC conversion clock for the Shared ADC (ADC2) controlled by the ADCDIV[6:0] bits.

Value	Description
11111111	$1025 T_{AD7}$
11	
...	

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Value	Description
00000000 01	$3 T_{AD7}$
00000000 00	$2 T_{AD7}$

Bit 15 – BGVRIEN Band Gap/V_{REF} Voltage Ready Interrupt Enable bit

Value	Description
0	No interrupt is generated when the BGVRRDY bit is set
1	Interrupt is generated when the BGVRDDY bit is set

Bit 14 – REFFLTIEN Band Gap/V_{REF} Voltage Fault Interrupt Enable bit

Value	Description
0	No interrupt is generated when the REFFLT bit is set
1	Interrupt is generated when the REFFLT bit is set

Bit 13 – EOSIEN End of Scan Interrupt Enable bit

Value	Description
0	No interrupt is generated when the EOSRDY bit is set
1	Interrupt is generated when the EOSRDY bit is set

Bit 11 – ENXCNVRT Enable External Conversion Request Interface

Setting this bit enables another module (such as the PTG) to specify and request conversion of an ADC input.

Note: The external module (such as the PTG) is responsible for asserted **only** the proper trigger signals. This ADC module has no method to block specific trigger requests from the external module.

Bits 6:0 – ADCDIV[6:0] Division Ratio for the Shared SAR ADC Core Clock bits

The ADCDIV[6:0] bits divide the ADC control clock (T_Q) to generate the clock for the shared SAR ADC.

Value	Description
1111111	$254 * T_Q = T_{AD2}$
...	
0000011	$6 * T_Q = T_{AD2}$
0000010	$4 * T_Q = T_{AD2}$
0000001	$2 * T_Q = T_{AD2}$
0000000	Reserved

36.10.4 ADCCON3 - ADC Control Register 3

Name: ADCCON3
Offset: 0x1420
Reset: 0x00000000
Property: -

This register enables ADC clock selection, enables/disables the digital feature for the shared ADC module and controls the manual (software) sampling and conversion.

Bit	31	30	29	28	27	26	25	24		
	ADCSEL[1:0]		CONCLKDIV[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0		
Bit	23	22	21	20	19	18	17	16		
	CHN_EN_SHR									
Access	R/W									
Reset	0									
Bit	15	14	13	12	11	10	9	8		
	VREFSEL[2:0]			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT		
Access	R/W	R/W	R/W	R/W	R/W	R/HS/HC	R/W	R/HS/HC		
Reset	0	0	0	0	0	0	0	0		
Bit	7	6	5	4	3	2	1	0		
	GLSWTRG	GSWTRG	ADINSEL[5:0]							
Access	R/W	R/W, HC	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0		

Bits 31:30 – ADCSEL[1:0] Analog-to-Digital Clock Source (T_{CLK}) bits

Value	Description
00	Peripheral Bus Clock
01	FRC Clock
10	REFO3 Clock Output
11	System Clock (SYS_CLK)

Bits 29:24 – CONCLKDIV[5:0] Analog-to-Digital Control Clock (T_Q) Divider bits

Value	Description
111111	$64 * T_{CLK} = T_Q$
...	
000011	$4 * T_{CLK} = T_Q$
000010	$3 * T_{CLK} = T_Q$
000001	$2 * T_{CLK} = T_Q$
000000	$T_{CLK} = T_Q$

Bit 23 – CHN_EN_SHR Shared ADC Digital Enable bit

Value	Description
1	ADC is digital enabled
0	ADC is digital disabled

Bits 15:13 – VREFSEL[2:0] Voltage Reference (V_{REF}) Input Selection bits

Table 36-5.

VREFSEL[2:0]	AD _{REF+}	AD _{REF-}
000	AV _{DD}	AV _{SS}
001-111	RESERVED FOR FUTURE USE	

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Bit 12 – TRGSUSP Trigger Suspend bit

Value	Description
1	Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0	Triggers are not blocked

Bit 11 – UPDIEN Update Ready Interrupt Enable bit

Value	Description
1	Interrupt is generated when the UPDRDY bit is set by hardware
0	No interrupt is generated

Bit 10 – UPDRDY ADC Update Ready Status bit

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

Value	Description
1	ADC SFRs can be updated
0	ADC SFRs cannot be updated

Bit 9 – SAMP Class 2 and Class 3 Analog Input Sampling Enable bit^(1,2,3,4)

Value	Description
1	The ADC S&H amplifier is sampling
0	The ADC S&H amplifier is holding

Bit 8 – RQCNVRT Individual ADC Input Conversion Request bit

This bit and its associated ADINSEL[5:0] bits enable the user to individually request an analog-to-digital conversion of an analog input through software.

Note: This bit is automatically cleared in the next ADC clock cycle.

Value	Description
1	Trigger the conversion of the selected ADC input as specified by the ADINSEL[5:0] bits
0	Do not trigger the conversion

Bit 7 – GLSWTRG Global Level Software Trigger bit

Value	Description
1	Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC[4:0] bits in the ADCTRGx registers or through the STRGSRC[4:0] bits in the ADCCON1 register
0	Do not trigger an analog-to-digital conversion

Bit 6 – GSWTRG Global Software Trigger bit

This bit is automatically cleared in the next ADC clock cycle.

Value	Description
0	Trigger conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC[4:0] bits in the ADCTRGx registers or through the STRGSRC[4:0] bits in the ADCCON1 register
1	Do not trigger an analog-to-digital conversion

Bits 5:0 – ADINSEL[5:0] Analog Input Select bits

These bits select the analog input to be converted when the RQCNVRT bit is set.

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Note:

1. The SAMP bit has the highest priority and setting this bit keeps the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit causes settings of SAMC[9:0] bits (ADCCON2[25:16]) to be ignored.
2. The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC.
3. The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.
4. Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx[4:0] bits and STRGSRC[4:0] bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

Value	Description
111111	Reserved
...	
001011	PMU Test Output
001010	VddCore (Internal)
001001	CP_Test_1.2V (Internal)
001000	BandGap Reference (Internal)
000111	AN7 is being monitored
...	
000001	AN1 is being monitored
000000	AN0 is being monitored

36.10.5 ADCIMCON1 - ADC Input Mode Control Register 1

Name: ADCIMCON1
Offset: 0x1440
Reset: 0x00000000
Property: -

This register enables the user to select between single-ended and differential operation as well as select between signed and unsigned data format.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 23 – DIFF11 AN11 Mode bit

Value	Description
1	AN11 is using Differential mode
0	AN11 is using Single-ended mode

Bit 22 – SIGN11 AN11 Signed Data Mode bit

Value	Description
1	AN11 is using Signed Data mode
0	AN11 is using Unsigned Data mode

Bit 21 – DIFF10 AN10 Mode bit

Value	Description
1	AN10 is using Differential mode
0	AN10 is using Single-ended mode

Bit 20 – SIGN10 AN10 Signed Data Mode bit

Value	Description
1	AN10 is using Signed Data mode
0	AN10 is using Unsigned Data mode

Bit 19 – DIFF9 AN9 Mode bit

Value	Description
1	AN9 is using Differential mode
0	AN9 is using Single-ended mode

Bit 18 – SIGN9 AN9 Signed Data Mode bit

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Value	Description
1	AN9 is using Signed Data mode
0	AN9 is using Unsigned Data mode

Bit 17 – DIFF8 AN8 Mode bit

Value	Description
1	AN8 is using Differential mode
0	AN8 is using Single-ended mode

Bit 16 – SIGN8 AN8 Signed Data Mode bit

Value	Description
1	AN8 is using Signed Data mode
0	AN8 is using Unsigned Data mode

Bit 15 – DIFF7 AN7 Mode bit

Value	Description
1	AN7 is using Differential mode
0	AN7 is using Single-ended mode

Bit 14 – SIGN7 AN7 Signed Data Mode bit

Value	Description
1	AN7 is using Signed Data mode
0	AN7 is using Unsigned Data mode

Bit 13 – DIFF6 AN6 Mode bit

Value	Description
1	AN6 is using Differential mode
0	AN6 is using Single-ended mode

Bit 12 – SIGN6 AN6 Signed Data Mode bit

Value	Description
1	AN6 is using Signed Data mode
0	AN6 is using Unsigned Data mode

Bit 11 – DIFF5 AN5 Mode bit

Value	Description
1	AN5 is using Differential mode
0	AN5 is using Single-ended mode

Bit 10 – SIGN5 AN5 Signed Data Mode bit

Value	Description
1	AN5 is using Signed Data mode
0	AN5 is using Unsigned Data mode

Bit 9 – DIFF4 AN4 Mode bit

Value	Description
1	AN4 is using Differential mode
0	AN4 is using Single-ended mode

Bit 8 – SIGN4 AN4 Signed Data Mode bit

Value	Description
1	AN4 is using Signed Data mode
0	AN4 is using Unsigned Data mode

Bit 7 – DIFF3 AN3 Mode bit

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Value	Description
1	AN3 is using Differential mode
0	AN3 is using Single-ended mode

Bit 6 – SIGN3 AN3 Signed Data Mode bit

Value	Description
1	AN3 is using Signed Data mode
0	AN3 is using Unsigned Data mode

Bit 5 – DIFF2 AN2 Mode bit

Value	Description
1	AN2 is using Differential mode
0	AN2 is using Single-ended mode

Bit 4 – SIGN2 AN2 Signed Data Mode bit

Value	Description
1	AN2 is using Signed Data mode
0	AN2 is using Unsigned Data mode

Bit 3 – DIFF1 AN1 Mode bit

Value	Description
1	AN1 is using Differential mode
0	AN1 is using Single-ended mode

Bit 2 – SIGN1 AN1 Signed Data Mode bit

Value	Description
1	AN1 is using Signed Data mode
0	AN1 is using Unsigned Data mode

Bit 1 – DIFF0 AN0 Mode bit

Value	Description
1	AN0 is using Differential mode
0	AN0 is using Single-ended mode

Bit 0 – SIGN0 AN0 Signed Data Mode bit

Value	Description
1	AN0 is using Signed Data mode
0	AN0 is using Unsigned Data mode

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36.10.6 ADCGIRQEN1 - ADC Global Interrupt Enable Register 1

Name: ADCGIRQEN1
Offset: 0x1480
Reset: 0x00000000
Property: -

This register specifies which of the individual input conversion interrupts can generate the global ADC interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – AGIEN ADC Global Interrupt Enable bits

Value	Description
1	Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the ARDY x bit (' x ' = 8-1) of the ADCSTAT1 register)
0	Interrupts are disabled

36.10.7 ADCCSS1 - ADC Common Scan Select Register 1

Name: ADCCSS1
Offset: 0x14A0
Reset: 0x00000000
Property: -

This register specifies the analog inputs to be scanned by the common scan trigger.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – CSS Analog Common Scan Select bits

Notes:

1. In addition to setting the appropriate bits in this register Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSSx bits. Refer to the bit descriptions in the ADCTR_G registers for selecting the STRIG option.
2. If a Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRC_x[4:0] bits to STRIG mode (0b11), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

Value	Description
1	Select AN _x for input scan
0	Skip AN _x for input scan

36.10.8 ADCDSTAT1 - ADC Data Ready Status Register 1

Name: ADCDSTAT1
Offset: 0x14C0
Reset: 0x00000000
Property: -

This register contains the interrupt status of the individual analog input conversions. Each bit represents the data-ready status for its associated conversion result.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access				ARDY11	ARDY10	ARDY9	ARDY8	
Reset				R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	
Bit	7	6	5	4	3	2	1	0
Access	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0
Reset	R/HS/HC							

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – ARDY Conversion Data Ready for Corresponding Analog Input Ready bits

Value	Description
1	This bit is set when converted data is ready in the data register
0	This bit is cleared when the associated data register is read

36.10.9 ADCCMPEN1 - ADC Digital Comparator 1 Enable Register

Name: ADCCMPEN1
Offset: 0x14E0
Reset: 0x00000000
Property: -

These registers select which analog input conversion results is processed by the digital comparator.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	CMPE _x [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CMPE_x[7:0] ADC Digital Comparator 'x' Enable bits

Note: CMPE_x = where "x" stands for bit value from 0 to 7.

These bits enable conversion results corresponding to the analog input to be processed by the digital comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Notes:

1. CMPE_x = AN_x, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).
2. Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

36.10.10 ADCCMPEN2 - ADC Digital Comparator 2 Enable Register

Name: ADCCMPEN2
Offset: 0x1500
Reset: 0x00000000
Property: -

These registers select which analog input conversion results is processed by the digital comparator.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	CMPE _x [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CMPE_x[7:0] ADC Digital Comparator ‘x’ Enable bits

Note: CMPE_x = where “x” stands for bit value from 0 to 7.

These bits enable conversion results corresponding to the analog input to be processed by the digital comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Notes:

1. CMPE_x = AN_x, where ‘x’ = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).
2. Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

36.10.11 ADCCMP1 - ADC Digital Comparator 1 Limit Value Register

Name: ADCCMP1
Offset: 0x14F0
Reset: 0x00000000
Property: -

These registers contain the high and low digital comparison values for use by the digital comparator.

Notes:

1. Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.
2. The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.
3. For Digital Comparator 0 used in CVD mode, the DCMPIH[15:0] and DCMPL0[15:0] bits must always be specified in signed format, as the CVD output data is differential and is always signed.

Bit	31	30	29	28	27	26	25	24
DCMPIH[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPIH[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPL0[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPL0[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – DCMPIH[15:0] Digital Comparator ‘x’ High Limit Value bits^(1,2,3)

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

Bits 15:0 – DCMPL0[15:0] Digital Comparator ‘x’ Low Limit Value bits^(1,2,3)

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

36.10.12 ADCCMP2 - ADC Digital Comparator 2 Limit Value Register

Name: ADCCMP2
Offset: 0x1510
Reset: 0x00000000
Property: -

These registers contain the high and low digital comparison values for use by the digital comparator.

Notes:

1. Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.
2. The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.
3. For Digital Comparator 0 used in CVD mode, the DCMPIH[15:0] and DCMPL0[15:0] bits must always be specified in signed format, as the CVD output data is differential and is always signed.

Bit	31	30	29	28	27	26	25	24
DCMPIH[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPL0[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPL0[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DCMPL0[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – DCMPIH[15:0] Digital Comparator ‘x’ High Limit Value bits^(1,2,3)

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

Bits 15:0 – DCMPL0[15:0] Digital Comparator ‘x’ Low Limit Value bits^(1,2,3)

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

36.10.13 ADCFLTR1 - ADC Digital Filter 1 Register

Name: ADCFLTR1
Offset: 0x15A0
Reset: 0x00000000
Property: -

These registers provide control and status bits for the oversampling filter accumulator, and also includes the 16-bit filter output data.

Bit	31	30	29	28	27	26	25	24
Access					OVRSAM[2:0]			
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access					CHNLID[4:0]			
Reset					R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access				FLTRDATA[15:8]				
Reset	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
0	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access				FLTRDATA[7:0]				
Reset	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
0	0	0	0	0	0	0	0	0

Bit 31 – AFEN Digital Filter 'x' Enable bit

Value	Description
1	Digital filter is enabled
0	Digital filter is disabled and the AFRDY status bit is cleared

Bit 30 – DATA16EN Filter Significant Data Length bit

Note: This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1[23]) = 1 (Fractional Output Mode).

Value	Description
1	All 16 bits of the filter output data are significant
0	Only the first 12 bits are significant, followed by four zeros

Bit 29 – DFMODE ADC Filter Mode bit

Value	Description
1	Filter 'x' works in Averaging mode
0	Filter 'x' works in Oversampling Filter mode (default)

Bits 28:26 – OVRSAM[2:0] Oversampling Filter Ratio bits

Value	Description
	If DFMODE is '0'
111	128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110	32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101	8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100	2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011	256 samples (shift sum 4 bits to right, output data is 16 bits)
010	64 samples (shift sum 3 bits to right, output data is 15 bits)

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Value	Description
001	16 samples (shift sum 2 bits to right, output data is 14 bits)
000	4 samples (shift sum 1 bit to right, output data is 13 bits)
If DFMODE is '1'	
111	256 samples (256 samples to be averaged)
110	128 samples (128 samples to be averaged)
101	64 samples (64 samples to be averaged)
100	32 samples (32 samples to be averaged)
011	16 samples (16 samples to be averaged)
010	8 samples (8 samples to be averaged)
001	4 samples (4 samples to be averaged)
000	2 samples (2 samples to be averaged)

Bit 25 – AFGIEN Digital Filter 'x' Interrupt Enable bit

Value	Description
1	Digital filter interrupt is enabled and is generated by the AFRDY status bit
0	Digital filter is disabled

Bit 24 – AFRDY Digital Filter 'x' Data Ready Status bit

Note: This bit is cleared by reading the FLTRDATA[15:0] bits or by disabling the Digital Filter module (by setting AFEN to '0').

Value	Description
1	Data is ready in the FLTRDATA[15:0] bits
0	Data is not ready

Bits 20:16 – CHNLID[4:0] Digital Filter Analog Input Selection bits

Note: Only the first 12 analog inputs, Class 2 (AN0-AN11), can use a digital filter.

These bits specify the analog input to be used as the oversampling filter data source.

Value	Description
11111	Reserved
...	
...	
...	
01100	Reserved
01011	AN11
...	
...	
...	
00010	AN2
00001	AN1
00000	AN0

Bits 15:0 – FLTRDATA[15:0] Digital Filter 'x' Data Output Value bits

The filter output data is as per the fractional format set in the FRACT bit (ADCCON1[23]). The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended should not update the value of the FLTRDATA[15:0] bits to reflect the new format.

36.10.14 ADCFLTR2 - ADC Digital Filter 2 Register

Name: ADCFLTR2
Offset: 0x15B0
Reset: 0x00000000
Property: -

These registers provide control and status bits for the oversampling filter accumulator, and also includes the 16-bit filter output data.

Bit	31	30	29	28	27	26	25	24
Access	AFEN	DATA16EN	DFMODE		OVRSAM[2:0]		AFGIEN	AFRDY
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access					CHNLID[4:0]			
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
Reset	0	0	0	0	0	0	0	0

Bit 31 – AFEN Digital Filter 'x' Enable bit

Value	Description
1	Digital filter is enabled
0	Digital filter is disabled and the AFRDY status bit is cleared

Bit 30 – DATA16EN Filter Significant Data Length bit

Note: This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1[23]) = 1 (Fractional Output Mode).

Value	Description
1	All 16 bits of the filter output data are significant
0	Only the first 12 bits are significant, followed by four zeros

Bit 29 – DFMODE ADC Filter Mode bit

Value	Description
1	Filter 'x' works in Averaging mode
0	Filter 'x' works in Oversampling Filter mode (default)

Bits 28:26 – OVRSAM[2:0] Oversampling Filter Ratio bits

Value	Description
	If DFMODE is '0'
111	128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110	32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101	8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100	2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011	256 samples (shift sum 4 bits to right, output data is 16 bits)
010	64 samples (shift sum 3 bits to right, output data is 15 bits)

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Value	Description
001	16 samples (shift sum 2 bits to right, output data is 14 bits)
000	4 samples (shift sum 1 bit to right, output data is 13 bits)
If DFMODE is '1'	
111	256 samples (256 samples to be averaged)
110	128 samples (128 samples to be averaged)
101	64 samples (64 samples to be averaged)
100	32 samples (32 samples to be averaged)
011	16 samples (16 samples to be averaged)
010	8 samples (8 samples to be averaged)
001	4 samples (4 samples to be averaged)
000	2 samples (2 samples to be averaged)

Bit 25 – AFGIEN Digital Filter 'x' Interrupt Enable bit

Value	Description
1	Digital filter interrupt is enabled and is generated by the AFRDY status bit
0	Digital filter is disabled

Bit 24 – AFRDY Digital Filter 'x' Data Ready Status bit

Note: This bit is cleared by reading the FLTRDATA[15:0] bits or by disabling the Digital Filter module (by setting AFEN to '0').

Value	Description
1	Data is ready in the FLTRDATA[15:0] bits
0	Data is not ready

Bits 20:16 – CHNLID[4:0] Digital Filter Analog Input Selection bits

Note: Only the first 12 analog inputs, Class 2 (AN0-AN11), can use a digital filter.

These bits specify the analog input to be used as the oversampling filter data source.

Value	Description
11111	Reserved
...	
...	
...	
01100	Reserved
01011	AN11
...	
...	
...	
00010	AN2
00001	AN1
00000	AN0

Bits 15:0 – FLTRDATA[15:0] Digital Filter 'x' Data Output Value bits

The filter output data is as per the fractional format set in the FRACT bit (ADCCON1[23]). The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended should not update the value of the FLTRDATA[15:0] bits to reflect the new format.

36.10.15 ADCTRG1 - ADC Trigger Source 1 Register

Name: ADCTRG1
Offset: 0x1600
Reset: 0x00000000
Property: -

This register controls the trigger source selection for AN0 through AN3 analog inputs.

Bit	31	30	29	28	27	26	25	24
TRGSRC3[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC2[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC1[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC0[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24 – TRGSRC3[4:0] Trigger Source for Conversion of Analog Input AN3 Select bits

Note: For STRIG, in addition to setting the trigger, it also requires programming of the TRGSRC[4:0] bits (ADCCON1[20:16]) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

Value	Description
10001	- Reserved
11111	
10000	EVSYS_47
01111	EVSYS_46
01110	EVSYS_45
01101	EVSYS_44
01100	EVSYS_43
01011	EVSYS_42
01010	EVSYS_41
01001	EVSYS_40
01000	EVSYS_39
00111	EVSYS_38
00110	EVSYS_37
00101	EVSYS_36
00100	INT0 External interrupt
00011	STRIG
00010	Global level software trigger (GLSWTRG)
00001	Global software edge trigger (GSWTRG)
00000	No Trigger

Bits 20:16 – TRGSRC2[4:0] Trigger Source for Conversion of Analog Input AN2 Select bits

Note: See bits 28-24 for bit value definitions.

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Bits 12:8 – TRGSRC1[4:0] Trigger Source for Conversion of Analog Input AN1 Select bits

Note: See bits 28-24 for bit value definitions.

Bits 4:0 – TRGSRC0[4:0] Trigger Source for Conversion of Analog Input AN0 Select bits

Note: See bits 28-24 for bit value definitions.

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36.10.16 ADCTRG2 - ADC Trigger Source 2 Register

Name: ADCTRG2
Offset: 0x1610
Reset: 0x00000000
Property: -

This register controls the trigger source selection for AN4 through AN7 analog inputs.

Bit	31	30	29	28	27	26	25	24
TRGSRC7[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC6[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC5[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
TRGSRC4[4:0]								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24 – TRGSRC7[4:0] Trigger Source for Conversion of Analog Input AN7 Select bits

Note: For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC[4:0] bits (ADCCON1[20:16]) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

Value	Description
10001	- Reserved
11111	
10000	EVSYS_47
01111	EVSYS_46
01110	EVSYS_45
01101	EVSYS_44
01100	EVSYS_43
01011	EVSYS_42
01010	EVSYS_41
01001	EVSYS_40
01000	EVSYS_39
00111	EVSYS_38
00110	EVSYS_37
00101	EVSYS_36
00100	INT0 External interrupt
00011	STRIG
00010	Global level software trigger (GLSWTRG)
00001	Global software edge trigger (GSWTRG)
00000	No Trigger

Bits 20:16 – TRGSRC6[4:0] Trigger Source for Conversion of Analog Input AN6 Select bits

Note: See bits 28-24 for bit value definitions.

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Bits 12:8 – TRGSRC5[4:0] Trigger Source for Conversion of Analog Input AN5 Select bits

Note: See bits 28-24 for bit value definitions.

Bits 4:0 – TRGSRC4[4:0] Trigger Source for Conversion of Analog Input AN4 Select bits

Note: See bits 28-24 for bit value definitions.

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36.10.17 ADCCMPCON1 - ADC Digital Comparator 1 Control Register

Name: ADCCMPCON1
Offset: 0x1680
Reset: 0x00000000
Property: -

This register controls the operation of Digital Comparator 1, including the generation of interrupts, comparison criteria to be used, and provides status when a comparator event occurs.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset			R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/HS/HC	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 13:8 – AINID[5:0] Digital Comparator 1 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by digital comparator 1.

Note: In normal ADC mode, only analog inputs [8:1] can be processed by the digital comparator 1.

Value	Description
111111	Reserved
...	
...	
...	
101101	Reserved
101100	Reserved
101011	Reserved
000111	AN7 is being monitored
...	
000001	AN1 is being monitored
000000	AN0 is being monitored

Bit 7 – ENDCMP Digital Comparator 1 Enable bit

Value	Description
1	Digital comparator 1 is enabled
0	Digital comparator 1 is not enabled, and the DCMPED status bit (ADCCMP0CON[5]) is cleared

Bit 6 – DCMPGIEN Digital Comparator 1 Global Interrupt Enable bit

Value	Description
1	A Digital comparator 1 interrupt is generated when the DCMPED status bit (ADCCMP0CON[5]) is set
0	A Digital comparator 1 interrupt is disabled

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Bit 5 – DCMPED Digital Comparator 1 “Output True” Event Status bit

The logical conditions under which the digital comparator becomes “True” are defined by the IEBTWN, IEHIHI, IEHILo, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID[5:0] bits or by disabling the Digital Comparator module (by setting ENDCMP to ‘0’).

Value	Description
1	Digital comparator 1 output true event has occurred (output of comparator is ‘1’)
0	Digital comparator 1 output is false (output of comparator is ‘0’)

Bit 4 – IEBTWN Between Low/High Digital Comparator 1 Event bit

Value	Description
1	Generate a digital comparator event when DATA[31:0] is less than DCMPHI[15:0] AND greater than DCMPLO[15:0]
0	Do not generate a digital comparator event

Bit 3 – IEHIHI High/High Digital Comparator 1 Event bit

Value	Description
1	Generate a digital comparator 1 event when DCMPHI[15:0] bits are less than or equal to DATA[31:0] bits
0	Do not generate an event

Bit 2 – IEHILo High/Low Digital Comparator 1 Event bit

Value	Description
1	Generate a digital comparator 1 event when DATA[31:0] bits are less than DCMPHI[15:0] bits
0	Do not generate an event

Bit 1 – IELOHI Low/High Digital Comparator 1 Event bit

Value	Description
1	Generate a digital comparator 1 event when DCMPLO[15:0] bits are less than or equal to DATA[31:0] bits
0	Do not generate an event

Bit 0 – IELOLO Low/Low Digital Comparator 1 Event bit

Value	Description
1	Generate a digital comparator 1 event when DATA[31:0] bits are less than DCMPLO[15:0] bits
0	Do not generate an event

36.10.18 ADCCMPCON2 - ADC Digital Comparator 2 Control Register

Name: ADCCMPCON2
Offset: 0x1690
Reset: 0x00000000
Property: -

These registers control the operation of Digital Comparator 2, including the generation of interrupts and the comparison criteria to be used. This register also provides status when a comparator event occurs.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access				R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC	R/HS/HC
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	
Access	R/W	R/W	R/HS/HC	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – AINID[4:0] Digital Comparator 2 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by the digital comparator.

Note: Only analog inputs [8:1] can be processed by the Digital Comparator module 'x' ('x' = 1-2).

Value	Description
11111	Reserved
11110	Reserved
...	
...	
...	
00011	Reserved
000111	AN7 is being monitored
...	
00001	AN1 is being monitored
00000	AN0 is being monitored

Bit 7 – ENDCMP Digital Comparator 2 Enable bit

Value	Description
1	Digital comparator 2 is enabled
0	Digital comparator 2 is not enabled, and the DCMPED status bit (ADCCMP0CON[5]) is cleared

Bit 6 – DCMPGIEN Digital Comparator 2 Global Interrupt Enable bit

Value	Description
1	Digital comparator 2 interrupt is generated when the DCMPED status bit (ADCCMP0CON[5]) is set
0	Digital comparator 2 interrupt is disabled

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Bit 5 – DCMPED Digital Comparator 2 “Output True” Event Status bit

The logical conditions under which the digital comparator gets “True” are defined by the IEBTWN, IEHIHI, IEHILo, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID[5:0] bits (ADCCMP0CON[13:8]) or by disabling the Digital Comparator module (by setting ENDCMP to ‘0’).

Value	Description
1	Digital comparator 2 output true event has occurred (output of comparator is ‘1’)
0	Digital comparator 2 output is false (output of comparator is ‘0’)

Bit 4 – IEBTWN Between Low/High Digital Comparator 2 Event bit

Value	Description
1	Generate a digital comparator event when DCMPLO[15:0] bits DATA[31:0] bits [DCMPHI[15:0] bits
0	Do not generate a digital comparator event

Bit 3 – IEHIHI High/High Digital Comparator 2 Event bit

Value	Description
1	Generate a digital comparator 2 event when DCMPHI[15:0] bits are less than or equal to DATA[31:0] bits
0	Do not generate an event

Bit 2 – IEHILo High/Low Digital Comparator 2 Event bit

Value	Description
1	Generate a digital comparator 2 event when DATA[31:0] bits are less than DCMPHI[15:0] bits
0	Do not generate an event

Bit 1 – IELOHI Low/High Digital Comparator 2 Event bit

Value	Description
1	Generate a digital comparator 2 event when DCMPLO[15:0] bits are less than or equal to DATA[31:0] bits
0	Do not generate an event

Bit 0 – IELOLO Low/Low Digital Comparator 2 Event bit

Value	Description
1	Generate a digital comparator 2 event when DATA[31:0] bits are less than DCMPLO[15:0] bits
0	Do not generate an event

36.10.19 ADCBASE - ADC Base Register

Name: ADCBASE
Offset: 0x1700
Reset: 0x00000000
Property: -

This register specifies the base address of the user ADC Interrupt Service Routine (ISR) jump table.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADCBASE[15:0] ADCISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS[2:0] bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 register, prior to adding with ADCBASE register.

Interrupt vector address = Read value of ADCBASE

Read value of ADCBASE = Value written to ADCBASE + x << IRQVS[2:0], where 'x' is the smallest active analog input ID from the ADCDSTAT1 register (which has highest priority).

36.10.20 ADCDMASTAT - ADC DMA Status Register

Name: ADCDMASTAT
Offset: 0x1710
Reset: 0x00000000
Property: -

This register contains the DMA status bits.

Bit	31	30	29	28	27	26	25	24
	DMAEN							RBF0IEN
Access	R/W							R/W
Reset	0							0
Bit	23	22	21	20	19	18	17	16
	WROVRERR							RBF0
Access	R/HS/HC							R/HS/HC
Reset	0							0
Bit	15	14	13	12	11	10	9	8
	DMACNTEN							RAF0IEN
Access	R/W							R/W
Reset	0							0
Bit	7	6	5	4	3	2	1	0
								RAF0
Access								R/HS/HC
Reset								0

Bit 31 – DMAEN DMA Interface Enable bit

When DMAEN = 0, no data is being saved into the DMA FIFO, no SRAM writes occur and the DMA interface logic is being kept in Reset state.

Value	Description
1	DMA interface is enabled
0	DMA interface is disabled

Bit 24 – RBF0IEN RAM Buffer B Full Interrupt Enable for channel 0

Value	Description
1	Interrupts are enabled and generated when the RBFx Status bit is set
0	Interrupts are disabled

Bit 23 – WROVRERR Write Overflow Error in the DMA FIFO

Set by hardware, cleared by hardware after a software read of the ADDMAST register.

Note: The write always occurs and the old data is being replaced with new data because the software missed reading the old data on time.

Bit 16 – RBF0 RAM Buffer B FULL status bit for channel 0

This bit is self-clearing upon being read by software.

Bit 15 – DMACNTEN DMA Buffer Sample Count Enable bit

The DMA interface saves the current sample count for each buffer in the table starting at the ADCCNTB address after each sample write into the corresponding buffer in the SRAM.

Bit 8 – RAF0IEN RAM Buffer A FULL Interrupt Enable for channel 0

Value	Description
1	Interrupts are enabled and generated when the RAFx Status bit is set
0	Interrupts are disabled

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Bit 0 – RAF0 RAM Buffer A FULL status bit for channel 0
This bit is self-clearing upon being read by software.

Preliminary

36.10.21 ADCCNTB - ADC Channel Sample Count Base Address Register

Name: ADCCNTB
Offset: 0x1720
Reset: 0x00000000
Property: -

This register contains the base address of the sample count in RAM. In addition to storing the converted data of the ADC module in RAM, DMA also stores the converted sample count.

Bit	31	30	29	28	27	26	25	24
ADCCNTB[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADCCNTB[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADCCNTB[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADCCNTB[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADCCNTB[31:0] ADC Channel Count Base Address

ADC Channel Count Base Address: SRAM address for the DMA interface at which to save the first class channel buffer A sample count values into the System RAM. If first class channel x , $x=0\ldots6$, is ready with a new available sample data, and the DMA interface is currently saving data for channel x to RAM Buffer z (where $z==0$ means BufferA and $z==1$ means Buffer B, z depending on x), then the DMA interface will increment (+1) the 1 byte count value stored at System RAM address (ADCCNTB + $2^*x + z$).

ADCCNTB works in conjunction with ADDMAB. The DMA interface uses ADCCNTB to save the buffer sample counts only if ADDMAST.DMA_CNT_EN is set to 1.

36.10.22 ADCDMAB - ADC DMA Base Address Register

Name: ADCDMAB
Offset: 0x1730
Reset: 0x00000000
Property: -

This register contains the base address of RAM for the DMA engine.

Bit	31	30	29	28	27	26	25	24
ADDMAB[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADDMAB[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADDMAB[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
ADDMAB[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDMAB[31:0] Base Address for the DMA Interface

BASE ADDRESS for the DMA interface at which to save first class channels data into the System RAM. If first class channel x , $x == 0..6$, is ready with a new available sample data, and the DMA interface is currently saving data for channel x to RAM Buffer z (where $z == 0$ means Buffer A and $z == 1$ means Buffer B, z depending on x), and the current DMA x -counter value is y (y depending on x), then the DMA interface stores the 2-byte output data value at System RAM address $(ADDMAB + (2*x + z)*2(DMABL+1) + 2*y)$. Also, if ADDMAST.DMA_CNT_EN is set to 1, the DMA interface stores without delay the value y itself at the System RAM address $(ADCCNTB + 2*x + z)$.

36.10.23 ADCTRGsns - ADC Trigger Level/Edge Sensitivity Register

Name: ADCTRGsns
Offset: 0x1740
Reset: 0x00000000
Property: -

This register contains the setting for trigger level for each ADC analog input.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
LVL7	R/W							
Access	0	0	0	0	0	0	0	0
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7 – LVL Trigger Level and Edge Sensitivity bits

Notes:

1. This register specifies the trigger level for analog inputs 0 to 7.
2. The higher analog input ID belongs to Class 3, and therefore, is only scan triggered. All Class 3 analog inputs use the scan trigger, for which the level/edge is defined by the STRGLVL bit (ADCCON1[3]).

Value	Description
1	Analog input is sensitive to the high level of its trigger (level sensitivity implies retriggering as long as the trigger signal remains high)
0	Analog input is sensitive to the positive edge of its trigger (this is the value after a reset)

36.10.24 ADCANCON - ADC Analog Warm-up Control Register

Name: ADCANCON
Offset: 0x1800
Reset: 0x00000000
Property: -

This register contains the warm-up control settings for the analog and bias circuit of the ADC module.

Bit	31	30	29	28	27	26	25	24
WKUPCLKCNT[3:0]								
Access				R/W	R/W	R/W	R/W	
Reset				0	0	0	0	
WKIEN7								
Access	R/W							R/W
Reset	0							0
WKRDY7								
Access	R/HS/HC							R/HS/HC
Reset	0							0
ANEN7								
Access	R/W							R/W
Reset	0							0
ANENO								

Bits 27:24 – WKUPCLKCNT[3:0] Wake-up Clock Count bits

These bits represent the number of ADC clocks required to warm-up the ADC module before it can perform conversion. Although the clocks are specific to each ADC, the WKUPCLKCNT bit is common to all ADC modules.

Value	Description
1111	$2^{15} = 32,768$ clocks
...	
...	
...	
0110	$2^6 = 64$ clocks
0101	$2^5 = 32$ clocks
0100	$2^4 = 16$ clocks
0011	$2^4 = 16$ clocks
0010	$2^4 = 16$ clocks
0001	$2^4 = 16$ clocks
0000	$2^4 = 16$ clocks

Bit 23 – WKIEN7 Shared ADC (ADC2) Wake-up Interrupt Enable bit

Value	Description
1	Enable interrupt and generate interrupt when the WKRDY2 status bit is set
0	Disable interrupt

Bit 16 – WKIEN0 ADC1Wake-up Interrupt Enable bit

Value	Description
1	Enable interrupt and generate interrupt when the WKRDYx status bit is set
0	Disable interrupt

Bit 15 – WKRDY7 Shared ADC (ADC2) Wake-up Status bit

Note: This bit is cleared by hardware when the ANEN2 bit is cleared.

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Value	Description
1	ADC2 Analog and bias circuitry ready after the wake-up count number 2^{WKUPEXP} clocks after setting ANEN2 to '1'
0	ADC2 Analog and bias circuitry is not ready

Bit 8 – WKRDY0 ADC1 Wake-up Status bit

Note: These bit are cleared by hardware when the ANENx bit is cleared.

Value	Description
1	ADC1 Analog and bias circuitry ready after the wake-up count number 2^{WKUPEXP} clocks after setting ANEN1 to '1'
0	ADC1 Analog and bias circuitry is not ready

Bit 7 – ANEN7 Shared ADC (ADC2) Analog and Bias Circuitry Enable bit

Value	Description
1	Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT[3:0] bits.
0	Analog and bias circuitry disabled

Bit 0 – ANEN0 ADC1 Analog and Bias Circuitry Enable bits

Value	Description
1	Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT[3:0] bits.
0	Analog and bias circuitry disabled

36.10.25 ADCSYSCFG0 - ADC System Configuration Register 0

Name: ADCSYSCFG0
Offset: 0x1B00
Reset: 0x00000000
Property: -

This register contains read-only bits corresponding to the analog input.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					R	R	R	R
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bits 19:0 – AN[19:0] ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

36.10.26 ADCDATAx - ADC Output Data Register ('x' = 0 to 11)

Name: ADCDATAx
Offset: 0x1Exx
Reset: 0x00000000
Property: -

These registers are the analog-to-digital conversion output data registers. The ADCDATAx register is associated with each external analog input, 0-7, plus internal analog inputs 8-11.

Bit	31	30	29	28	27	26	25	24
DATA[31:24]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
DATA[23:16]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
DATA[15:8]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
DATA[7:0]								
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] ADC Converted Data Output bits

Notes:

1. When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output register.
2. Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

37. AC – Analog Comparators

37.1 Overview

The Analog Comparator (AC) supports two individual comparators; one shared (with built-in supply voltage monitor (MVREF)) AC_CMP1, and one dedicated AC_CMP0.

Continuous mode of operation on shared comparator is supported only if MVREF is disabled; PMU.CLKCTRL.MVREFFSMEN bit = 0 (Disabled). Each comparator (COMP) compares the voltage levels on two inputs, and provides a digital output based on the comparison. Each comparator may be configured to generate interrupt requests and/or peripheral events upon several different combinations of input change.

The input selection includes up to four shared analog port pins and several internal signals. Each Comparator Output state can also be output on a pin for use by external devices.

The comparators are grouped in pairs on each port. The AC peripheral implements pair of comparators . These are called Comparator 0 (COMP0) and Comparator 1 (COMP1) . They have identical behaviors, but separate Control registers. The pair can be set in Window mode to compare a signal to a voltage range instead of a single voltage level.

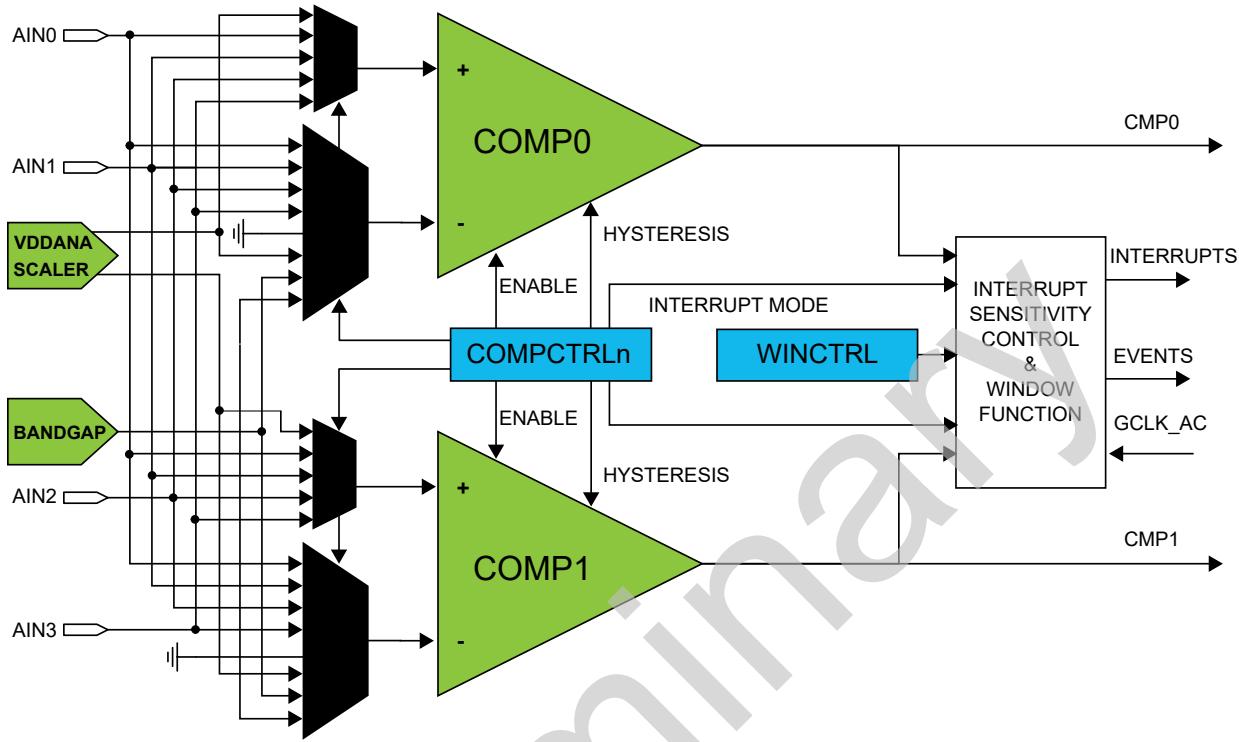
Note: MVREF will not be able to monitor supply voltage for 275 μ s from the time MCLR is released.

37.2 Features

- Two individual comparators (Single pair configuration)
- Analog comparator outputs available on pins
 - Asynchronous or synchronous
- Flexible input selection:
 - Up to four pins selectable for positive or negative inputs
 - Ground (for zero crossing)
 - Bandgap reference voltage
 - Programmable VDD scaler for AC_CMP1 (shared with Programmable Low Voltage Detector (PLVD)) and fixed VDD/2 for AC_CMP0
- Interrupt generation on:
 - Rising or falling edge
 - Toggle
 - End of comparison
- Window function interrupt generation on:
 - Signal above window
 - Signal inside window
 - Signal below window
 - Signal outside window
- Event generation on:
 - Comparator output
 - Window function inside/outside window
- Optional digital filter on comparator output

37.3 Block Diagram

Figure 37-1. Analog Comparator Block Diagram



37.4 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

37.4.1 I/O Lines

Using the AC's I/O lines requires the I/O pins to be configured as analog pins for AC_AINx inputs. See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.

Table 37-1. I/O LINES

Signal	Peripheral Function
AC_AIN0	—
AC_AIN1	—
AC_AIN2	—
AC_AIN3	—
AC_CMP0	CFGCON1.CMP0_OE
AC_CMP1	CFGCON1.CMP1_OE

Related Links

- 5. [I/O Ports and Peripheral Pin Select \(PPS\)](#)

37.4.2 Power Management

The AC will continue to operate in any Sleep mode where the selected source clock is running. The AC's interrupts can be used to wake up the device from Sleep modes. Events connected to the Event System can trigger other operations in the system without exiting Sleep modes.

37.4.3 Clocks

The AC bus clock (PB2_CLK) can be enabled and disabled in the Main Clock module, CRU (see *Clock and Reset (CRU)* from Related Links), and the Analog Comparator module can be enabled or disabled via the PMD1 register, see *Peripheral Module Disable Register (PMD)* from Related Links.

A generic clock (GCLK_AC) is required to clock the AC. This clock must be configured and enabled in the generic clock controller before using the AC.

This generic clock is asynchronous to the bus clock (PB2_CLK). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. See *Synchronization* from Related Links.

Related Links

- [12. Clock and Reset Unit \(CRU\)](#)
- [19. Peripheral Module Disable Register \(PMD\)](#)
- [37.5.13. Synchronization](#)

37.4.4 DMA

Not applicable.

37.4.5 Interrupts

The interrupt request lines are connected to the interrupt controller. Using the AC interrupts requires the interrupt controller to be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

- [9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

37.4.6 Events

The events are connected to the Event System. See *Event System (EVSYS)* from Related Links, for details on how to configure the Event System.

Related Links

- [27. Event System \(EVSYS\)](#)

37.4.7 Debug Operation

When the CPU is halted in debug mode, the AC will halt normal operation after any on-going comparison is completed. The AC can be forced to continue normal operation during debugging. See *DBGCTRL* register from Related Links. If the AC is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

Related Links

- [37.7.9. DBGCTRL](#)

37.4.8 Register Access Protection

All registers with write access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Control B register (CTRLB)
- Interrupt Flag register (INTFLAG)

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

PAC write protection does not apply to accesses through an external debugger.

37.4.9 Analog Connections

Each comparator has up to four I/O pins that can be used as analog inputs. Each pair of comparators shares the same four pins. These pins must be configured for analog operation before using them as comparator inputs.

Any internal reference source, such as a bandgap voltage reference, must be configured and enabled prior to its use as a comparator input.

37.5 Functional Description

37.5.1 Principle of Operation

Each comparator has one positive input and one negative input. Each positive input may be chosen from a selection of analog input pins. Each negative input may be chosen from a selection of both analog input pins and internal inputs, such as INTREF voltage reference.

The digital output from the comparator is '1' when the difference between the positive and the negative input voltage is positive, and '0' otherwise.

The individual comparators can be used independently (Normal mode) or paired to form a window comparison (Window mode).

37.5.2 Basic Operation

37.5.2.1 Initialization

Some registers are enable-protected, meaning they can only be written when the module is disabled.

The following register is enable-protected:

- Event Control register (EVCTRL)

Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

37.5.2.2 Enabling, Disabling and Resetting

The AC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The AC is disabled writing a '0' to CTRLA.ENABLE.

The AC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the AC will be reset to their initial state, and the AC will be disabled. See *CTRLA* register from Related Links.

Related Links

37.7.1. *CTRLA*

37.5.2.3 Comparator Configuration

Each individual comparator must be configured by its respective Comparator Control register (COMPCTRLx) before that comparator is enabled. These settings cannot be changed while the comparator is enabled.

- Select the desired measurement mode with COMPCTRLx.SINGLE. See *Starting a Comparison* from Related Links.
- Fixed hysteresis, does not support programmable Hysteresis.
- Fixed speed of operation.
- Select the interrupt source with COMPCTRLx.INTSEL.
- Select the positive and negative input sources with the COMPCTRLx.MUXPOS and COMPCTRLx.MUXNEG bits. See *Selecting Comparator Inputs* from Related Links.
- Select the filtering option with COMPCTRLx.FLEN.
- Select standby operation with Run in Standby bit (COMPCTRLx.RUNSTDBY).

The individual comparators are enabled by writing a '1' to the Enable bit in the Comparator x Control registers (COMPCTRLx.ENABLE). The individual comparators are disabled by writing a '0' to COMPCTRLx.ENABLE. Writing a '0' to CTRLA.ENABLE will also disable all the comparators, but will not clear their COMPCTRLx.ENABLE bits.

Related Links

- [37.5.2.4. Starting a Comparison](#)
- [37.5.3. Selecting Comparator Inputs](#)

37.5.2.4 Starting a Comparison

Each comparator channel can be in one of two different measurement modes, determined by the COMPCTRLx.SINGLE bit:

- Continuous measurement
- Single-shot

After being enabled, a start-up delay is required before the result of the comparison is ready. This start-up time is measured automatically to account for environmental changes, such as temperature or voltage supply level, and is specified in the Electrical Specifications. During the start-up time, the COMP output is not available.

The comparator can be configured to generate interrupts when the output toggles, when the output changes from '0' to '1' (rising edge), when the output changes from '1' to '0' (falling edge) or at the end of the comparison.

An end-of-comparison interrupt can be used with the Single-Shot mode to chain further events in the system, regardless of the state of the comparator outputs. The Interrupt mode is set by the Interrupt Selection bit group in the Comparator Control register (COMPCTRLx.INTSEL). Events are generated using the comparator output state, regardless of whether the interrupt is enabled or not.

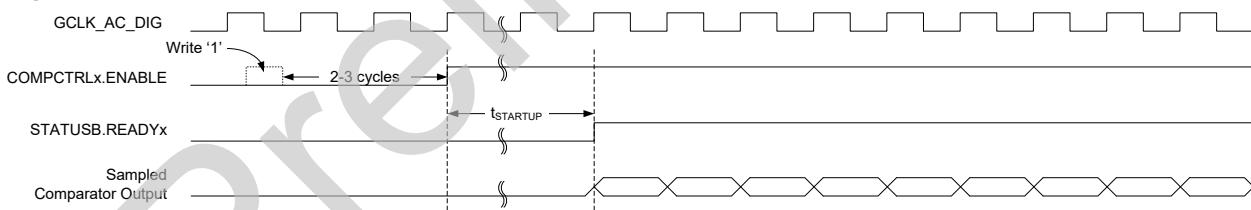
37.5.2.4.1 Continuous Measurement

Continuous measurement is selected by writing COMPCTRLx.SINGLE to zero. In continuous mode, the comparator is continuously enabled and performing comparisons. This ensures that the result of the latest comparison is always available in the Current State bit in the Status A register (STATUSA.STATEx).

After the start-up time has passed, a comparison is done and STATUSA is updated. The Comparator x Ready bit in the Status B register (STATUSB.READYx) is set, and the appropriate peripheral events and interrupts are also generated. New comparisons are performed continuously until the COMPCTRLx.ENABLE bit is written to zero. The start-up time applies only to the first comparison.

In continuous operation, edge detection of the comparator output for interrupts is done by comparing the current and previous sample. The sampling rate is the GCLK_AC frequency. An example of continuous measurement is shown in the following figure.

Figure 37-2. Continuous Measurement Example



For low-power operation, comparisons can be performed during sleep mode without a clock. The comparator is enabled continuously, and changes of the comparator state are detected asynchronously. When a toggle occurs, the CRU will start GCLK_AC to register the appropriate peripheral events and interrupts. The GCLK_AC clock is then disabled again automatically, unless configured to wake up the system from sleep.

37.5.2.4.2 Single-Shot

Single-shot operation is selected by writing COMPCTRLx.SINGLE to '1'. During single-shot operation, the comparator is normally idle. The user starts a single comparison by writing '1' to the respective Start Comparison bit in the write-only Control B register (CTRLB.STARTx). The comparator is enabled, and after the start-up time has passed, a single comparison is done and STATUSA is updated. Appropriate peripheral events and interrupts are also generated. No new comparisons will be performed.

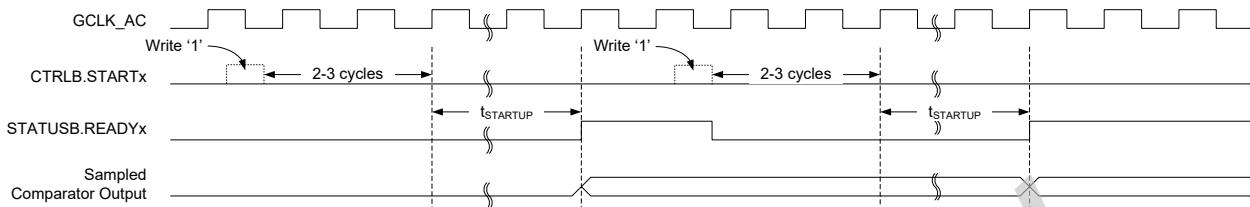
Writing '1' to CTRLB.STARTx also clears the Comparator x Ready bit in the Status B register (STATUSB.READYx). STATUSB.READYx is set automatically by hardware when the single comparison has completed.

A single-shot measurement can also be triggered by the Event System. Setting the Comparator x Event Input bit in the Event Control Register (EVCTRL.COMPEIx) enables triggering on incoming peripheral events. Each comparator can be triggered independently by separate events. Event-triggered operation is similar to user-triggered operation;

the difference is that a peripheral event from another hardware module causes the hardware to automatically start the comparison and will not clear STATUSUSB.READYx.

To detect an edge of the comparator output in single-shot operation for the purpose of interrupts, the result of the current measurement is compared with the result of the previous measurement (one sampling period earlier). An example of single-shot operation is shown in the following figure.

Figure 37-3. Single-Shot Example



For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the CRU will start GCLK_AC. The comparator is enabled, and after the startup time has passed, a comparison is done and appropriate peripheral events and interrupts are also generated. The comparator and GCLK_AC are then disabled again automatically, unless configured to wake up the system from sleep.

37.5.3 Selecting Comparator Inputs

Each comparator has one positive and one negative input. The positive input is one of the external input pins (AINx). The negative input can be fed either from an external input pin (AINx) or from one of the internal reference voltage sources common to all comparators. The user selects the input source as follows:

- The positive input is selected by the Positive Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXPOS)
- The negative input is selected by the Negative Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXNEG)

In the case of using an external I/O pin, the selected pin must be configured for analog use in the GPIO by disabling the digital input and output. The switching of the analog input multiplexers is controlled to minimize crosstalk between the channels. The input selection must be changed only while the individual comparator is disabled.

Note: For internal use of the comparison results by the CCL module (see *Configurable Custom Logic (CCL)* from Related Links), COMPCTRLx.OUT must be 0x1 or 0x2.

37.5.4 Window Operation

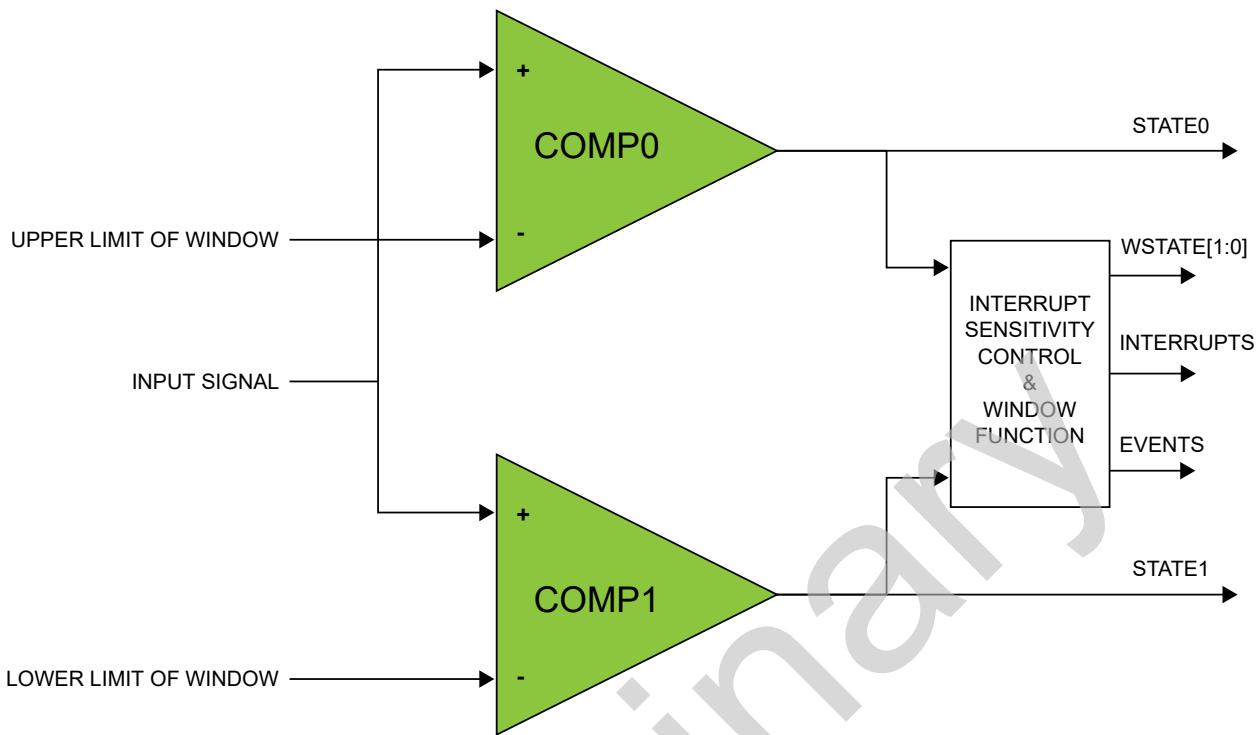
Each comparator pair can be configured to work together in Window mode. In this mode, a voltage range is defined, and the comparators give information about whether an input signal is within this range or not. Window mode is enabled by the Window Enable x bit in the Window Control register (WINCTRL.WENx). Both comparators in a pair must have the same measurement mode setting in their respective Comparator Control Registers (COMPCTRLx.SINGLE).

To physically configure the pair of comparators for Window mode, the same I/O pin must be chosen as positive input for each comparator, providing a shared input signal. The negative inputs define the range for the window. In [Figure 37-4](#), COMP0 defines the upper limit and COMP1 defines the lower limit of the window, as shown but the window will also work in the opposite configuration with COMP0 lower and COMP1 higher. The current state of the window function is available in the Window x State bit group of the Status register (STATUSA.WSTATEx).

Window mode can be configured to generate interrupts when the input voltage reaches values below the window, above the window, inside the window or outside of the window. The interrupt selections are set by the Window Interrupt Selection bit field in the Window Control register (WINCTRL.WINTSEL). Events are generated using the inside/outside state of the window, regardless of whether the interrupt is enabled or not. Note that the individual comparator outputs, interrupts and events continue to function normally during Window mode.

When the comparators are configured for Window mode and Single-shot mode, measurements are performed simultaneously on both comparators. Writing '1' to either Start Comparison bit in the Control B register (CTRLB.STARTx) will start a measurement. Likewise either peripheral event can start a measurement.

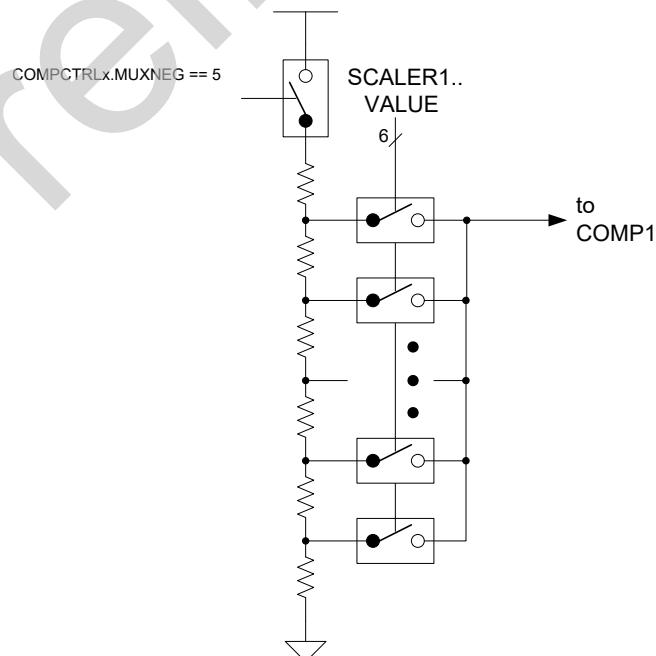
Figure 37-4. Comparators in Window Mode



37.5.5 VDD Scaler

The VDD scaler generates a reference voltage that is a fraction of the device's supply voltage, with 64 levels. The programmable VDD scaler is available for AC_CMP1 only. AC_CMP0 uses fixed VDD/2 reference. The scaler of a comparator is enabled when the Negative Input Mux bit field or the Positive Input Mux in the respective Comparator Control register (COMPCTRLx.MUXNEG) is set to 0x5 and the comparator is enabled. The voltage of each channel is selected by the Value bit field in the SCALER1 registers (SCALER1.VALUE) using VDD resistor ladder.

Figure 37-5. VDD Scaler



37.5.6 Filtering

The output of the comparators can be filtered digitally to reduce noise. The filtering is determined by the Filter Length bits in the Comparator Control x register (COMPCTRLx.FLEN), and is independent for each comparator. Filtering is selectable from none, 3-bit majority (N=3) or 5-bit majority (N=5) functions. Any change in the comparator output is considered valid only if $N/2+1$ out of the last N samples agree. The filter sampling rate is the GCLK_AC frequency.

Note that filtering creates an additional delay of $N-1$ sampling cycles from when a comparison is started until the comparator output is validated. For Continuous mode, the first valid output will occur when the required number of filter samples is taken. Subsequent outputs will be generated every cycle based on the current sample plus the previous $N-1$ samples, as shown in [Figure 37-6](#). For Single-shot mode, the comparison completes after the Nth filter sample, as shown in [Figure 37-7](#).

Figure 37-6. Continuous Mode Filtering

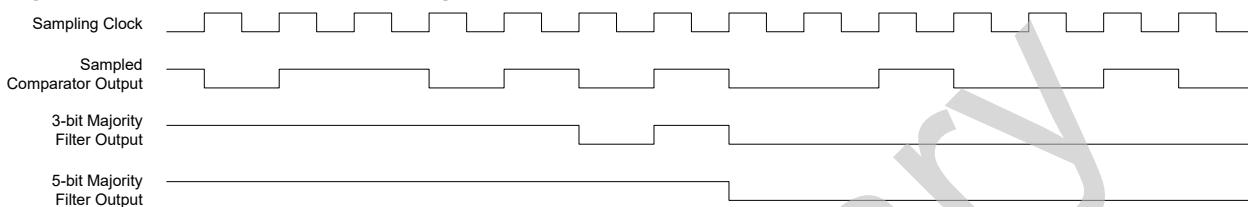
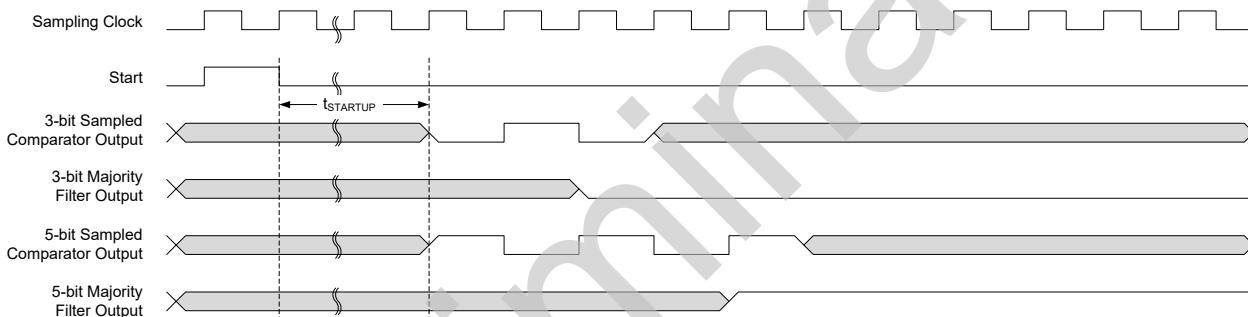


Figure 37-7. Single-Shot Filtering



During Sleep modes, filtering is supported only for single-shot measurements. Filtering must be disabled if continuous measurements will be done during Sleep modes, or the resulting interrupt/event may be generated incorrectly.

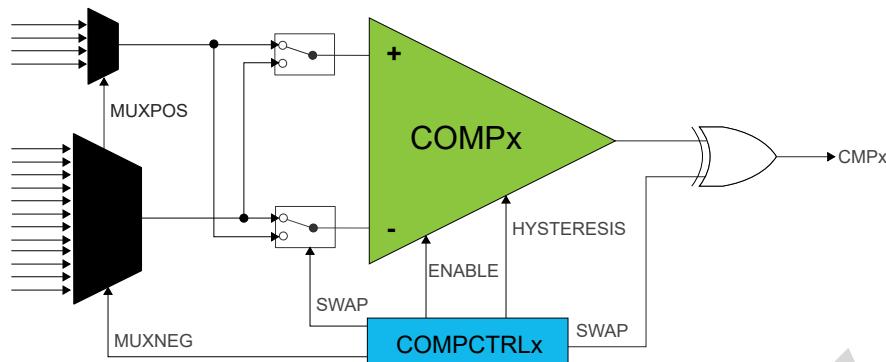
37.5.7 Comparator Output

The output of each comparator can be routed to an I/O pin by setting the Output bit group in the Comparator Control x register (COMPCTRLx.OUT). To get the analog comparator output on I/O line, CFGCON1.CMP0_OE/CFGCON1.CMP1_OE also needs to be set or enabled. This allows the comparator to be used by external circuitry. Either the raw, non-synchronized output of the comparator or the GCLK_AC-synchronized version, including filtering, can be used as the I/O signal source. The output appears on the corresponding AC_CMPx pin. The AC_CMP1 can be output on alternate pin by configuring CFGCON0.AC_CMP1_ALTN configuration.

37.5.8 Offset Compensation

The Swap bit in the Comparator Control registers (COMPCTRLx.SWAP) controls switching of the input signals to a comparator's positive and negative terminals. When the comparator terminals are swapped, the output signal from the comparator is also inverted, as shown in [Figure 37-8](#). This allows the user to measure or compensate for the comparator input offset voltage. As part of the input selection, COMPCTRLx.SWAP can be changed only while the comparator is disabled.

Figure 37-8. Input Swapping for Offset Compensation



37.5.9 DMA Operation

Not applicable.

37.5.10 Interrupts

The AC has the following interrupt sources:

- Comparator (COMP0, COMP1): Indicates a change in comparator status.
- Window (WIN0): Indicates a change in the window status.

Comparator interrupts are generated based on the conditions selected by the Interrupt Selection bit group in the Comparator Control registers (COMPCTRLx.INTSEL). Window interrupts are generated based on the conditions selected by the Window Interrupt Selection bit group in the Window Control register (WINCTRL.WINTSEL[1:0]).

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the AC is Reset. See *INTFLAG* register from Related Links, for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Note that interrupts must be globally enabled for interrupt requests to be generated.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

[37.7.6. INTFLAG](#)

37.5.11 Events

The AC can generate the following output events:

- Comparator (COMP0, COMP1): Generated as a copy of the comparator status
- Window (WIN0): Generated as a copy of the window inside/outside status

Writing a one to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. See *Event System (EVSYS)* from Related Links, for details on how to configure the Event System.

The AC can take the following action on an input event:

- Start comparison (START0, START1): Start a comparison.

Writing a one to an Event Input bit into the Event Control register (EVCTRL.COMPEIx) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event. Note that if several

events are connected to the AC, the enabled action will be taken on any of the incoming events. See *Event System (EVSYS)* from Related Links, for details on how to configure the Event System.

When EVCTRL.COMPEIx is one, the event will start a comparison on COMPx after the start-up time delay. In normal mode, each comparator responds to its corresponding input event independently. For a pair of comparators in window mode, either comparator event will trigger a comparison on both comparators simultaneously.

Related Links

[27. Event System \(EVSYS\)](#)

37.5.12 Sleep Mode Operation

The Run in Standby bits in the Comparator x Control registers (COMPCTRLx.RUNSTDBY) control the behavior of the AC during standby sleep mode. Each RUNSTDBY bit controls one comparator. When the bit is zero, the comparator is disabled during sleep, but maintains its current configuration. When the bit is one, the comparator continues to operate during sleep. Note that when RUNSTDBY is zero, the analog blocks are powered off for the lowest power consumption. This necessitates a start-up time delay when the system returns from sleep.

For Window Mode operation, both comparators in a pair must have the same RUNSTDBY configuration.

When RUNSTDBY is one, any enabled AC interrupt source can wake up the CPU. The AC can also be used during sleep modes where the clock used by the AC is disabled, provided that the AC is still powered (not in shutdown). In this case, the behavior is slightly different and depends on the measurement mode, as listed in [Table 37-2](#).

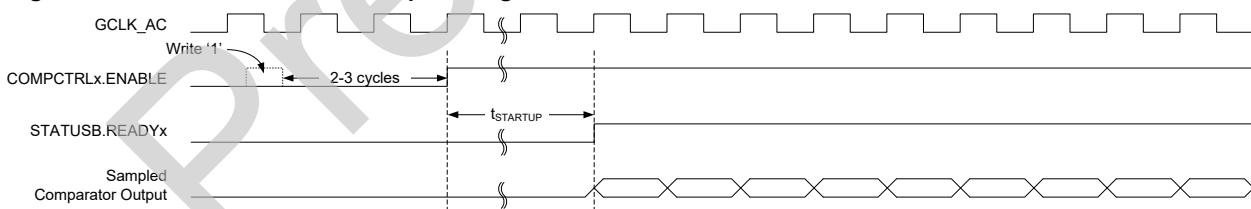
Table 37-2. Sleep Mode Operation

COMPCTRLx.MODE	RUNSTDBY=0	RUNSTDBY=1
0 (Continuous)	COMPx disabled	GCLK_AC stopped, COMPx enabled
1 (Single-shot)	COMPx disabled	GCLK_AC stopped, COMPx enabled only when triggered by an input event

37.5.12.1 Continuous Measurement during Sleep

When a comparator is enabled in continuous measurement mode and GCLK_AC is disabled during sleep, the comparator will remain continuously enabled and will function asynchronously. The current state of the comparator is asynchronously monitored for changes. If an edge matching the interrupt condition is found, GCLK_AC is started to register the interrupt condition and generate events. If the interrupt is enabled in the Interrupt Enable registers (INTENCLR/SET), the AC can wake up the device; otherwise GCLK_AC is disabled until the next edge detection. Filtering is not possible with this configuration.

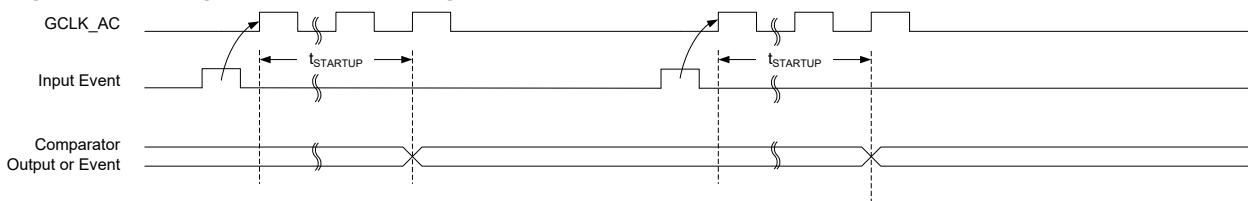
Figure 37-9. Continuous Mode SleepWalking



37.5.12.2 Single-Shot Measurement during Sleep

For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the CRU will start GCLK_AC. The comparator is enabled, and after the start-up time has passed, a comparison is done, with filtering if desired, and the appropriate peripheral events and interrupts are also generated, as shown in the following figure. The comparator and GCLK_AC are then disabled again automatically, unless configured to wake the system from sleep. Filtering is allowed with this configuration.

Figure 37-10. Single-Shot SleepWalking



37.5.13 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in Control register (CTRLA.SWRST)
- Enable bit in Control register (CTRLA.ENABLE)
- Enable bit in Comparator Control register (COMPCTRLn.ENABLE)

The following registers are synchronized when written:

- Window Control register (WINCTRL)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

37.6 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0							ENABLE	SWRST
0x01	CTRLB	7:0							START1	START0
0x02	EVCTRL	7:0			WINEO0				COMPEO1	COMPEO0
		15:8			INVEI1	INVEI0			COMPEI1	COMPEI0
0x04	INTENCLR	7:0			WIN0				COMP1	COMP0
0x05	INTENSET	7:0			WIN0				COMP1	COMP0
0x06	INTFLAG	7:0			WIN0				COMP1	COMP0
0x07	STATUSA	7:0			WSTATE0[1:0]				STATE1	STATE0
0x08	STATUSB	7:0							READY1	READY0
0x09	DBGCTRL	7:0								DBGRUN
0x0A	WINCTRL	7:0					WINTSEL0[1:0]			WEN0
0x0B	...									
0x0C	Reserved									
0x0D	SCALER1	7:0					VALUE[3:0]			
0x0E	...									
0x0F	Reserved									
0x10	COMPCTRL0	7:0		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
		15:8	SWAP		MUXPOS[2:0]					MUXNEG[2:0]
		23:16								
		31:24			OUT[1:0]					FLEN[2:0]
0x14	COMPCTRL1	7:0		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
		15:8	SWAP		MUXPOS[2:0]					MUXNEG[2:0]
		23:16								
		31:24			OUT[1:0]					FLEN[2:0]
0x18	...									
0x1F	Reserved									
0x20	SYNCBUSY	7:0			COMPCTRL1	COMPCTRL0	WINCTRL	ENABLE	SWRST	
		15:8								
		23:16								
		31:24								

37.7 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. See *Synchronization* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

[37.4.8. Register Access Protection](#)

[37.5.13. Synchronization](#)

37.7.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
Access							ENABLE	SWRST
Reset							R/W	W
							0	0

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from updating the register until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the corresponding bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the peripheral is enabled/disabled.

Value	Description
0	The AC is disabled.
1	The AC is enabled. Each comparator must also be enabled individually by the Enable bit in the Comparator Control register (COMPCTRLn.ENABLE).

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the AC to their initial state, and the AC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

37.7.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
Access							START1	START0
Reset							R/W	R/W
							0	0

Bits 0, 1 – STARTx Comparator x Start Comparison

Writing a '0' to this field has no effect.

Writing a '1' to STARTx starts a single-shot comparison on COMPx if both the Single-Shot and Enable bits in the Comparator x Control Register are '1' (COMPCTRLx.SINGLE and COMPCTRLx.ENABLE). If comparator x is not implemented, or if it is not enabled in single-shot mode, Writing a '1' has no effect.

This bit always reads as zero.

37.7.3 Event Control

Name: EVCTRL
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
Access			INVEI1	INVEI0			COMPEI1	COMPEI0
Reset				R/W	R/W		R/W	R/W
				0	0		0	0
Bit	7	6	5	4	3	2	1	0
Access				WINEO0			COMPEO1	COMPEO0
Reset				R/W			R/W	R/W
				0			0	0

Bits 12, 13 – INVEIx Inverted Event Input Enable x

Value	Description
0	Incoming event is not inverted for comparator x.
1	Incoming event is inverted for comparator x.

Bits 8, 9 – COMPEIx Comparator x Event Input

Note that several actions can be enabled for incoming events. If several events are connected to the peripheral, the enabled action will be taken for any of the incoming events. There is no way to tell which of the incoming events caused the action.

These bits indicate whether a comparison will start or not on any incoming event.

Value	Description
0	Comparison will not start on any incoming event.
1	Comparison will start on any incoming event.

Bit 4 – WINEO0 Window 0 Event Output Enable

These bits indicate whether the window 0 function can generate a peripheral event or not.

Value	Description
0	Window 0 Event is disabled.
1	Window 0 Event is enabled.

Bits 0, 1 – COMPEOx Comparator x Event Output Enable

These bits indicate whether the comparator x output can generate a peripheral event or not.

Value	Description
0	COMPx event generation is disabled.
1	COMPx event generation is enabled.

37.7.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
Access				WIN0			COMP1	COMP0
Reset				R/W			R/W	R/W

Bit 4 – WIN0 Window 0 Interrupt Enable

Reading this bit returns the state of the Window 0 interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit disables the Window 0 interrupt.

Value	Description
0	The Window 0 interrupt is disabled.
1	The Window 0 interrupt is enabled.

Bits 0, 1 – COMPx Comparator x Interrupt Enable

Reading this bit returns the state of the Comparator x interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit disables the Comparator x interrupt.

Value	Description
0	The Comparator x interrupt is disabled.
1	The Comparator x interrupt is enabled.

37.7.5 Interrupt Enable Set

Name: INTENSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
Access				WIN0			COMP1	COMP0
Reset				R/W			R/W	R/W

Bit 4 – WIN0 Window 0 Interrupt Enable

Reading this bit returns the state of the Window 0 interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit enables the Window 0 interrupt.

Value	Description
0	The Window 0 interrupt is disabled.
1	The Window 0 interrupt is enabled.

Bits 0, 1 – COMPx Comparator x Interrupt Enable

Reading this bit returns the state of the Comparator x interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Ready interrupt bit and enable the Ready interrupt.

Value	Description
0	The Comparator x interrupt is disabled.
1	The Comparator x interrupt is enabled.

37.7.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
				WIN0			COMP1	COMP0
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0

This flag is set according to the Window 0 Interrupt Selection bit group in the [WINCTRL](#) register (WINCTRL.WINTSELx) and will generate an interrupt if INTENCLR/SET.WINx is also one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Window 0 interrupt flag.

Bits 0, 1 – COMPx Comparator x

Reading this bit returns the status of the Comparator x interrupt flag. If comparator x is not implemented, COMPx always reads as zero.

This flag is set according to the Interrupt Selection bit group in the Comparator x Control register (COMPCTRLx.INTSEL) and will generate an interrupt if INTENCLR/SET.COMPx is also one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Comparator x interrupt flag.

37.7.7 Status A

Name: STATUSA
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
				WSTATE0[1:0]			STATE1	STATE0
Access			R	R			R	R
Reset			0	0			0	0

Bits 5:4 – WSTATE0[1:0] Window 0 Current State

These bits show the current state of the signal if the window 0 mode is enabled.

Value	Name	Description
0x0	ABOVE	Signal is above window
0x1	INSIDE	Signal is inside window
0x2	BELOW	Signal is below window
0x3		Reserved

Bits 0, 1 – STATEx Comparator x Current State

This bit shows the current state of the output signal from COMPx. STATEx is valid only when STATUSB.READYx is one.

37.7.8 Status B

Name: STATUSB
Offset: 0x08
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
Access							READY1	READY0
Reset							R	R

Bits 0, 1 – READYx Comparator x Ready

This bit is cleared when the comparator x output is not ready.

This bit is set when the comparator x output is ready.

37.7.9 Debug Control

Name: DBGCTRL
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	R/W
								DBGRUN		0

Bit 0 – DBGRUN Debug Run

This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The AC is halted when the CPU is halted by an external debugger. Any on-going comparison will complete.
1	The AC continues normal operation when the CPU is halted by an external debugger.

37.7.10 Window Control

Name: WINCTRL
Offset: 0x0A
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							WINTSEL0[1:0]	WEN0
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:1 – WINTSEL0[1:0] Window 0 Interrupt Selection

These bits configure the interrupt mode for the comparator window 0 mode.

Value	Name	Description
0x0	ABOVE	Interrupt on signal above window
0x1	INSIDE	Interrupt on signal inside window
0x2	BELOW	Interrupt on signal below window
0x3	OUTSIDE	Interrupt on signal outside window

Bit 0 – WEN0 Window 0 Mode Enable

Value	Description
0	Window mode is disabled for comparators 0 and 1.
1	Window mode is enabled for comparators 0 and 1.

37.7.11 Scaler 1

Name: SCALER1
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	VALUE[3:0]							
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – VALUE[3:0] Scaler Value

These bits define the scaling factor for channel 1 of the VDD voltage scaler. The output voltage, V_{SCALE} , is:

$$V_{SCALE} = \frac{V_{DD} \cdot (\text{VALUE}+1)}{16}$$

37.7.12 Comparator Control n

Name: COMPCTRL
Offset: 0x10 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
			OUT[1:0]				FLEN[2:0]	
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	SWAP		MUXPOS[2:0]				MUXNEG[2:0]	
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
Access		R/W		R/W	R/W	R/W	R/W	
Reset		0		0	0	0	0	

Bits 29:28 – OUT[1:0] Output

These bits configure the output selection for comparator n. COMPCTRLn.OUT can be written only while COMPCTRLn.ENABLE is zero.

Note: For internal use of the comparison results by the CCL, this must be 0x1 or 0x2.

These bits are not synchronized.

Value	Name	Description
0x0	OFF	The output of COMPn is not routed to the COMPn I/O port
0x1	ASYNC	The asynchronous output of COMPn is routed to the COMPn I/O port
0x2	SYNC	The synchronous output (including filtering) of COMPn is routed to the COMPn I/O port
0x3	N/A	Reserved

Bits 26:24 – FLEN[2:0] Filter Length

These bits configure the filtering for comparator n. COMPCTRLn.FLEN can only be written while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	OFF	No filtering
0x1	MAJ3	3-bit majority function (2 of 3)
0x2	MAJ5	5-bit majority function (3 of 5)
0x3–0x7	N/A	Reserved

Bit 15 – SWAP Swap Inputs and Invert

This bit swaps the positive and negative inputs to COMPn and inverts the output. This function can be used for offset cancellation. COMPCTRLn.SWAP can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Description
0	The output of MUXPOS connects to the positive input, and the output of MUXNEG connects to the negative input.

Value	Description
1	The output of MUXNEG connects to the positive input, and the output of MUXPOS connects to the negative input.

Bits 14:12 – MUXPOS[2:0] Positive Input Mux Selection

These bits select which input will be connected to the positive input of comparator n. COMPCTRLn.MUXPOS can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	VSCALE	VDD scaler
0x5–0x7	-	Reserved

Bits 10:8 – MUXNEG[2:0] Negative Input Mux Selection

These bits select which input will be connected to the negative input of comparator n. COMPCTRLn.MUXNEG can only be written while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	GND	Ground
0x5	VSCALE	VDD scaler
0x6	BANDGAP	Internal bandgap voltage

Bit 6 – RUNSTDBY Run in Standby

This bit controls the behavior of the comparator during standby sleep mode.

This bit is not synchronized

Value	Description
0	The comparator is disabled during sleep.
1	The comparator continues to operate during sleep.

Bits 4:3 – INTSEL[1:0] Interrupt Selection

These bits select the condition for comparator n to generate an interrupt or event. COMPCTRLn.INTSEL can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	TOGGLE	Interrupt on comparator output toggle
0x1	RISING	Interrupt on comparator output rising
0x2	FALLING	Interrupt on comparator output falling
0x3	EOC	Interrupt on end of comparison (single-shot mode only)

Bit 2 – SINGLE Single-Shot Mode

This bit determines the operation of comparator n. COMPCTRLn.SINGLE can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Description
0	Comparator n operates in continuous measurement mode.
1	Comparator n operates in single-shot mode.

Bit 1 – ENABLE Enable

Writing a zero to this bit disables comparator n.

Writing a one to this bit enables comparator n.

PIC32CX-BZ2 and WBZ45 Family

AC – Analog Comparators

Due to synchronization, there is delay from updating the register until the comparator is enabled/disabled. The value written to COMPCTRLn.ENABLE will read back immediately after being written. SYNCBUSY.COMPCTRLn is set. SYNCBUSY.COMPCTRLn is cleared when the peripheral is enabled/disabled.

Writing a one to COMPCTRLn.ENABLE will prevent further changes to the other bits in COMPCTRLn. These bits remain protected until COMPCTRLn.ENABLE is written to zero and the write is synchronized.

Preliminary

37.7.13 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access				COMPCTRL1	COMPCTRL0	WINCTRL	ENABLE	SWRST
Reset				R	R	R	R	R
				0	0	0	0	0

Bits 3, 4 – COMPCTRLx COMPCTRLx Synchronization Busy

This bit is cleared when the synchronization of the COMPCTRLx register between the clock domains is complete.
This bit is set when the synchronization of the COMPCTRLx register between clock domains is started.

Bit 2 – WINCTRL WINCTRL Synchronization Busy

This bit is cleared when the synchronization of the WINCTRL register between the clock domains is complete.
This bit is set when the synchronization of the WINCTRL register between clock domains is started.

Bit 1 – ENABLE Enable Synchronization Busy

This bit is cleared when the synchronization of the CTRLA.ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the CTRLA.ENABLE bit between clock domains is started.

Bit 0 – SWRST Software Reset Synchronization Busy

This bit is cleared when the synchronization of the CTRLA.SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the CTRLA.SWRST bit between clock domains is started.

38. Timer/Counter (TC)

38.1 Overview

There are up to four TC peripheral instances. Up to four TCs (TC[3:0]) are in PD1, whereas TC4, present in all device configurations, is always located in power domain PD0.

Each TC consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events, or clock pulses. The counter, together with the compare/capture channels, can be configured to timestamp input events or IO pin edges, allowing for capturing of frequency and/or pulse width.

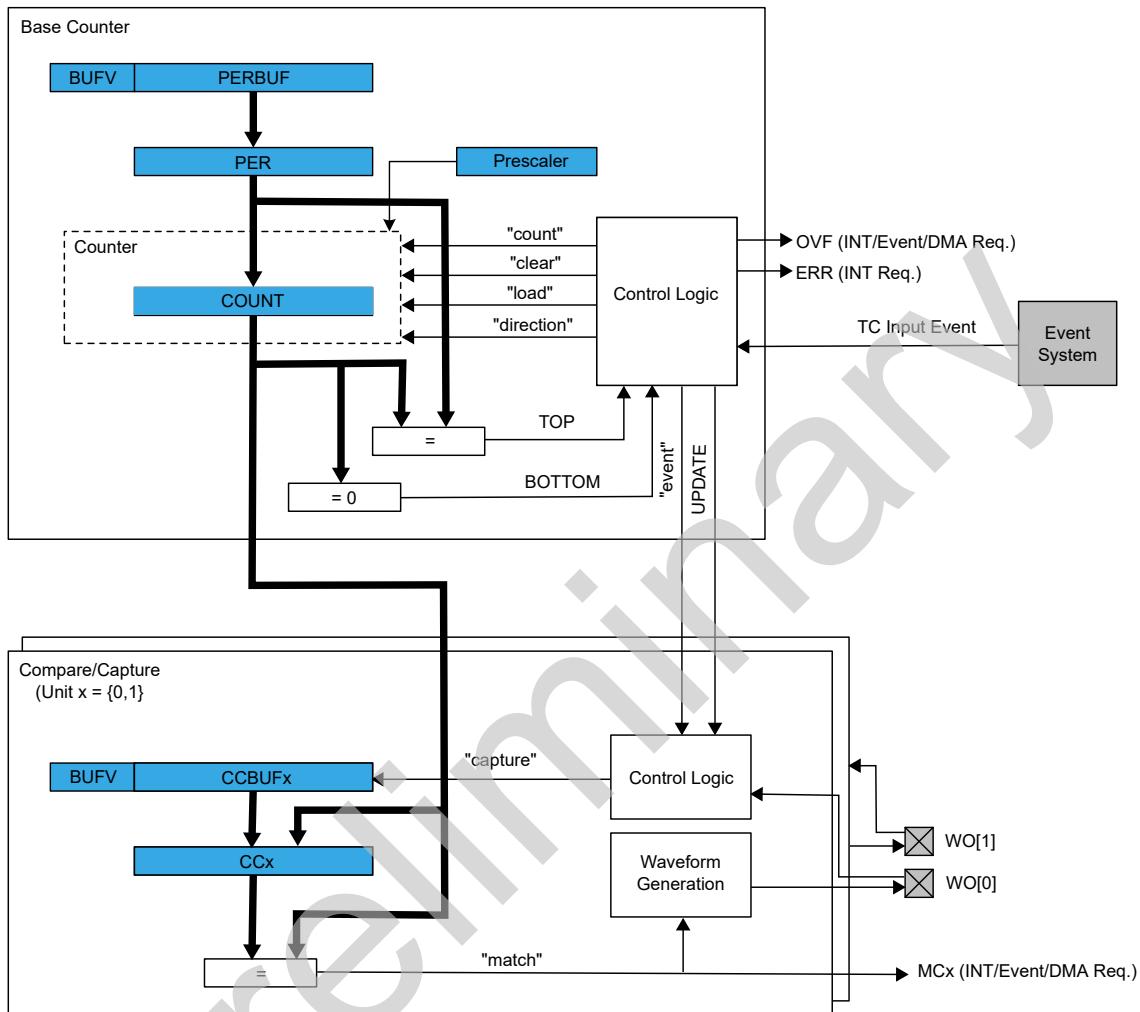
A TC can also perform waveform generation, such as frequency generation and pulse-width modulation.

38.2 Features

- Selectable Configuration
 - 8-, 16- or 32-bit TC operation, with compare/capture channels
- 2 Compare/Capture Channels (CC) with:
 - Double buffered timer period setting (in 8-bit mode only)
 - Double buffered compare channel
- Waveform Generation
 - Frequency generation
 - Single-slope pulse-width modulation
- Input Capture
 - Event / IO pin edge capture
 - Frequency capture
 - Pulse-width capture
 - Time-stamp capture
 - Minimum and maximum capture
- One Input Event
- Interrupts/Output Events ON:
 - Counter overflow/underflow
 - Compare match or capture
- Internal Prescaler
- DMA Support

38.3 Block Diagram

Figure 38-1. Timer/Counter Block Diagram



38.4 Signal Description

Table 38-1. Signal Description for TC

Signal Name	Type	Description
WO[1:0]	Digital output	Waveform output
	Digital input	Capture input

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links, for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

[5. I/O Ports and Peripheral Pin Select \(PPS\)](#)

38.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

38.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Peripheral Pin Select (PPS).

38.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake up the device from Sleep modes. Events connected to the event system can trigger other operations in the system without exiting Sleep modes.

38.5.3 Clocks

The TC bus clocks (PB1_CLK) can be enabled and disabled in the PMD Registers. For more details and default status of this clock, see *Peripheral Module Disable Register (PMD)* from Related Links.

The generic clocks (GCLK_TCx) are asynchronous to the user interface clock (PB1_CLK). Due to this asynchronicity, accessing certain registers will require synchronization between the clock domains.

Note: Two instances of the TC may share a peripheral clock channel. In this case, they cannot be set to different clock frequencies. See *System and Peripheral Clock Generation (CLKGEN)* from Related Links to identify shared peripheral clocks.

Related Links

[12.4. System and Peripheral Clock Generation \(CLKGEN\)](#)

[19. Peripheral Module Disable Register \(PMD\)](#)

38.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

[21. Direct Memory Access Controller \(DMAC\)](#)

38.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

38.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links

[27. Event System \(EVSYS\)](#)

38.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will halt normal operation. This peripheral can be forced to continue operation during debugging. For more details, refer to the Debug Control ([38.7.1.11. DBGCTRL](#)) register.

38.5.8 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)
- Period and Period Buffer registers (PER, PERBUF)
- Compare/Capture Value registers and Compare/Capture Value Buffer registers (CCx, CCBUFx)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

38.5.9 Analog Connections

Not applicable.

38.6 Functional Description

38.6.1 Principle of Operation

The following definitions are used throughout the documentation:

Table 38-2. Timer/Counter Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the waveform generator mode in Waveform Output Operations. See <i>Waveform Output Operations</i> from Related Links.
ZERO	The counter is ZERO when it contains all zeroes
MAX	The counter reaches MAX when it contains all ones
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source
Counter	The clock control is handled externally (e.g. counting external events)
CC	For compare operations, the CC are referred to as "compare channels" For capture operations, the CC are referred to as "capture channels."

Each TC instance has up to two compare/capture channels (CC0 and CC1).

The counter in the TC can either count events from the Event System, or clock ticks of the GCLK_TCx clock, which may be divided by the prescaler.

The counter value is passed to the CCx where it can be either compared to user-defined values or captured.

For optimized timing the CCx and CCBUFx registers share a common resource. When writing into CCBUFx, lock the access to the corresponding CCx register (SYNCBUSY.CCX = 1) till the CCBUFx register value is not loaded into the CCx register (BUFVx == 1). Each buffer register has a buffer valid (BUFV) flag that indicates when the buffer contains a new value.

The Counter register (COUNT) and the Compare and Capture registers with buffers (CCx and CCBUFx) can be configured as 8-, 16- or 32-bit registers, with according MAX values. Mode settings (CTRLA.MODE) determine the maximum range of the Counter register.

In 8-bit mode, a Period Value (PER) register and its Period Buffer Value (PERBUF) register are also available. The counter range and the operating frequency determine the maximum time resolution achievable with the TC peripheral.

The TC can be set to count up or down. Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached that value. On a comparison match the TC can request DMA transactions, or generate interrupts or events for the Event System.

In compare operation, the counter value is continuously compared to the values in the CCx registers. In case of a match the TC can request DMA transactions, or generate interrupts or events for the Event System. In waveform generator mode, these comparisons are used to set the waveform period or pulse width.

Capture operation can be enabled to perform input signal period and pulse width measurements, or to capture selectable edges from an IO pin or internal event from Event System.

Related Links

[38.6.2.6.1. Waveform Output Operations](#)

38.6.2 Basic Operation

38.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TC is disabled (CTRLA.ENABLE =0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits
- Drive Control register (DRVCTRL)
- Wave register (WAVE)
- Event Control register (EVCTRL)

Writing to Enable-Protected bits and setting the CTRLA.ENABLE bit can be performed in a single 32-bit access of the CTRLA register. Writing to Enable-Protected bits and clearing the CTRLA.ENABLE bit cannot be performed in a single 32-bit access.

Before enabling the TC, the peripheral must be configured by the following steps:

1. Enable the TC bus clock if not already enabled by default (PB1_CLK).
2. Select 8-, 16- or 32-bit counter mode via the TC Mode bit group in the Control A register (CTRLA.MODE). The default mode is 16-bit.
3. Select one wave generation operation in the Waveform Generation Operation bit group in the WAVE register (WAVE.WAVEGEN).
4. If desired, the GCLK_TCx clock can be prescaled via the Prescaler bit group in the Control A register (CTRLA.PRESCALER).
 - If the prescaler is used, select a prescaler synchronization operation via the Prescaler and Counter Synchronization bit group in the Control A register (CTRLA.PRESYNC).
5. If desired, select one-shot operation by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT).
6. If desired, configure the counting direction 'down' (starting from the TOP value) by writing a '1' to the Counter Direction bit in the Control B register (CTRLBSET.DIR).
7. For capture operation, enable the individual channels to capture in the Capture Channel x Enable bit group in the Control A register (CTRLA.CAPEN).
8. If desired, enable inversion of the waveform output or IO pin input signal for individual channels via the Invert Enable bit group in the Drive Control register (DRVCTRL.INVEN).

38.6.2.2 Enabling, Disabling, and Resetting

The TC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TC is disabled by writing a zero to CTRLA.ENABLE.

The TC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TC, except DBGCTRL, will be reset to their initial state. Refer to the [CTRLA](#) register for details.

The TC should be disabled before the TC is reset in order to avoid undefined behavior.

38.6.2.3 Prescaler Selection

The GCLK_TCx is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

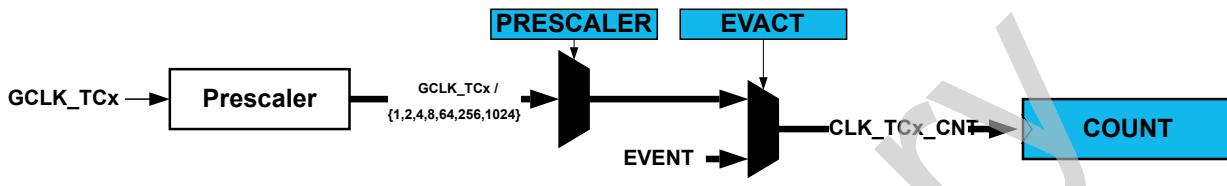
If the prescaler value is higher than one, the Counter Update condition can be optionally executed on the next GCLK_TCx clock pulse or the next prescaled clock pulse. For further details, refer to Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) description.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCx_CNT.

Figure 38-2. Prescaler



38.6.2.4 Counter Mode

The counter mode is selected by the Mode bit group in the Control A register (CTRLA.MODE). By default, the counter is enabled in the 16-bit counter resolution. Three counter resolutions are available:

- COUNT8: The 8-bit TC has its own Period Value and Period Buffer Value registers (PER and PERBUF).
- COUNT16: 16-bit is the default counter mode. There is no dedicated period register in this mode.
- COUNT32: 32-bit mode is achieved by pairing two 16-bit TC peripherals. TC(2n) is paired with TC(n+1). When paired, the TC peripherals are configured using the registers of the even-numbered TC (TC0 or TC2 respectively).

The TC bus clocks (PB1_CLK) for both master and slave TCs need to be enabled.

The odd-numbered partner (TC1 or TC3 respectively) will act as a slave, and the Slave bit in the Status register (STATUS.SLAVE) will be set. The register values of a slave will not reflect the registers of the 32-bit counter.

Writing to any of the slave registers will not affect the 32-bit counter. Normal access to the slave COUNT and CCx registers is not allowed.

38.6.2.5 Counter Operations

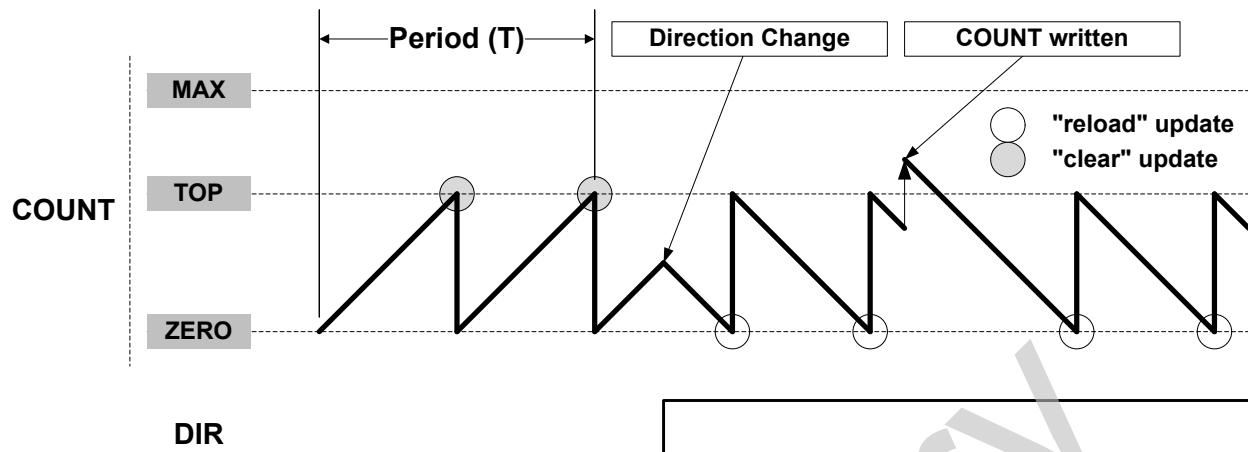
Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TC clock input (CLK_TCx_CNT). A counter clear or reload marks the end of the current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If this bit is zero the counter is counting up, and counting down if CTRLB.DIR=1. The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it is counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When it is counting down, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

INTFLAG.OVF can be used to trigger an interrupt, a DMA request, or an event. An overflow/underflow occurrence (i.e., a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT).

It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. When starting the TC, the COUNT value will be either ZERO or TOP (depending on the counting direction set by CTRLBSET.DIR or CTRLBCLR.DIR), unless a different value has been written to it, or the TC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed when the counter is running. See also the following figure.

Figure 38-3. Counter Operation



Due to asynchronous clock domains, the internal counter settings are written when the synchronization is complete. Normal operation must be used when using the counter as timer base for the capture channels.

38.6.2.5.1 Stop Command and Event Action

A Stop command can be issued from software by using Command bits in the Control B Set register (CTRLBSET.CMD = 0x2, STOP). When a Stop is detected while the counter is running, the counter will not retain its current value. All waveforms are cleared and the Stop bit in the Status register is set (STATUS.STOP).

38.6.2.5.2 Re-Trigger Command and Event Action

A re-trigger command can be issued from software by writing the Command bits in the Control B Set register (CTRLBSET.CMD = 0x1, RETRIGGER), or from event when a re-trigger event action is configured in the Event Control register (EVCTRL.EVACT = 0x1, RETRIGGER).

When the command is detected during counting operation, the counter will be reloaded or cleared, depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). When the re-trigger command is detected while the counter is stopped, the counter will resume counting from the current value in the COUNT register.

Note: When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACT=0x1, RETRIGGER), enabling the counter will not start the counter. The counter will start on the next incoming event and restart on corresponding following event.

38.6.2.5.3 Count Event Action

The TC can count events. When an event is received, the counter increases or decreases the value, depending on direction settings (CTRLBSET.DIR or CTRLBCLR.DIR). The count event action can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT=0x2, COUNT).

Note: If this operation mode is selected, PWM generation is not supported.

38.6.2.5.4 Start Event Action

The TC can start counting operation on an event when previously stopped. In this configuration, the event has no effect if the counter is already counting. When the peripheral is enabled, the counter operation starts when the event is received or when a re-trigger software command is applied.

The Start TC on Event action can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT=0x3, START).

38.6.2.6 Compare Operations

By default, the Compare/Capture channel is configured for compare operations.

When using the TC and the Compare/Capture Value registers (CCx) for compare operations, the counter value is continuously compared to the values in the CCx registers. This can be used for timer or for waveform operation.

The Channel x Compare Buffer (CCBUFx) registers provide double buffer capability. The double buffering synchronizes the update of the CCx register with the buffer value at the UPDATE condition or a forced update command (CTRLBSET.CMD=UPDATE). See *Double Buffering* from Related Links. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses and ensures glitch-free output.

Related Links

38.6.2.7. Double Buffering

38.6.2.6.1 Waveform Output Operations

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a Waveform Generation mode in the Waveform Generation Operation bit in Waveform register (WAVE.WAVEGEN).
2. Optionally invert the waveform output $WO[x]$ by writing the corresponding Output Waveform x Invert Enable bit in the Driver Control register (DRVCTRL.INVENx).
3. Configure the pins with the I/O Peripheral Pin Select (PPS). See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.

Note: Event must not be used when the compare channel is set in waveform output operating mode.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TC_CNT (see Normal Frequency Operation). An interrupt/and or event can be generated on comparison match if enabled. The same condition generates a DMA request.

There are four waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

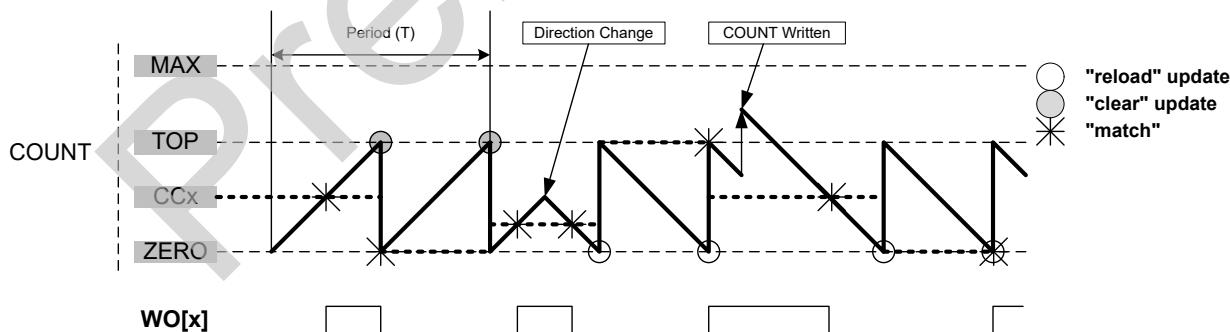
- Normal frequency (NFRQ)
- Match frequency (MFRQ)
- Normal pulse-width modulation (NPWM)
- Match pulse-width modulation (MPWM)

When using NPWM or NFRQ configuration, the TOP will be determined by the counter resolution. In 8-bit Counter mode, the Period register (PER) is used as TOP, and the TOP can be changed by writing to the PER register. In 16- and 32-bit Counter mode, TOP is fixed to the maximum (MAX) value of the counter.

Normal Frequency Generation (NFRQ)

For Normal Frequency Generation, the period time (T) is controlled by the period register (PER) for 8-bit Counter mode and MAX for 16- and 32-bit mode. The waveform generation output ($WO[x]$) is toggled on each compare match between COUNT and CCx , and the corresponding Match or Capture Channel x Interrupt Flag (INTFLAG.MCx) will be set.

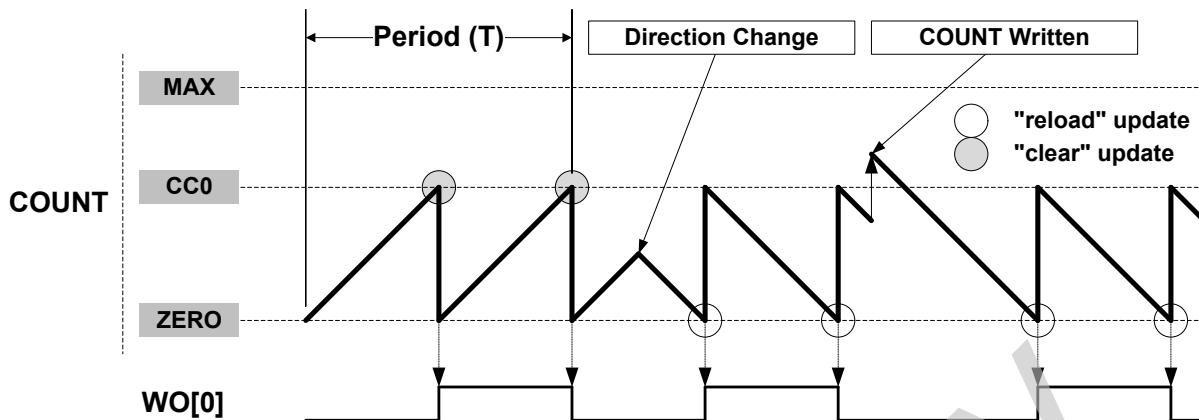
Figure 38-4. Normal Frequency Operation



Match Frequency Generation (MFRQ)

For Match Frequency Generation, the period time (T) is controlled by the $CC0$ register instead of PER or MAX. $WO[0]$ toggles on each Update condition.

Figure 38-5. Match Frequency Operation



Normal Pulse-Width Modulation Operation (NPWM)

NPWM uses single-slope PWM generation.

For single-slope PWM generation, the period time (T) is controlled by the TOP value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

The following equation calculates the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{PWM_SS} = \frac{\log(TOP+1)}{\log(2)}$$

The PWM frequency (f_{PWM_SS}) depends on TOP value and the peripheral clock frequency (f_{GCLK_TC}), and can be calculated by the following equation:

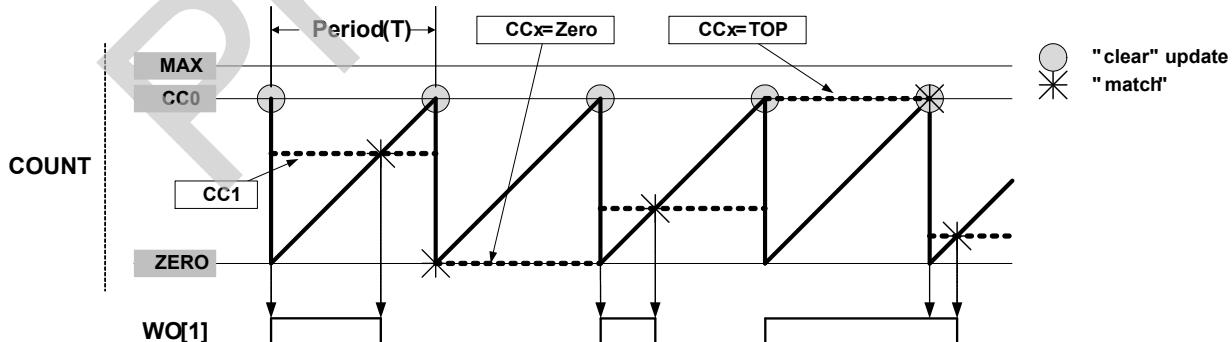
$$f_{PWM_SS} = \frac{f_{GCLK_TC}}{N(TOP+1)}$$

Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

Match Pulse-Width Modulation Operation (MPWM)

In MPWM, the output of WO[1] is depending on CC1 as shown in the figure below. On every overflow/underflow, a one-TC-clock-cycle negative pulse is put out on WO[0] (not shown in the figure).

Figure 38-6. Match PWM Operation



The following table shows the Update Counter and Overflow Event/Interrupt Generation conditions in different operation modes.

Table 38-3. Counter Update and Overflow Event/interrupt Conditions in TC

Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See description above.		TOP	ZERO
MPWM	Single-slope PWM	CC0	TOP/ ZERO	Toggle	Toggle	TOP	ZERO

Related Links

[5. I/O Ports and Peripheral Pin Select \(PPS\)](#)

38.6.2.7 Double Buffering

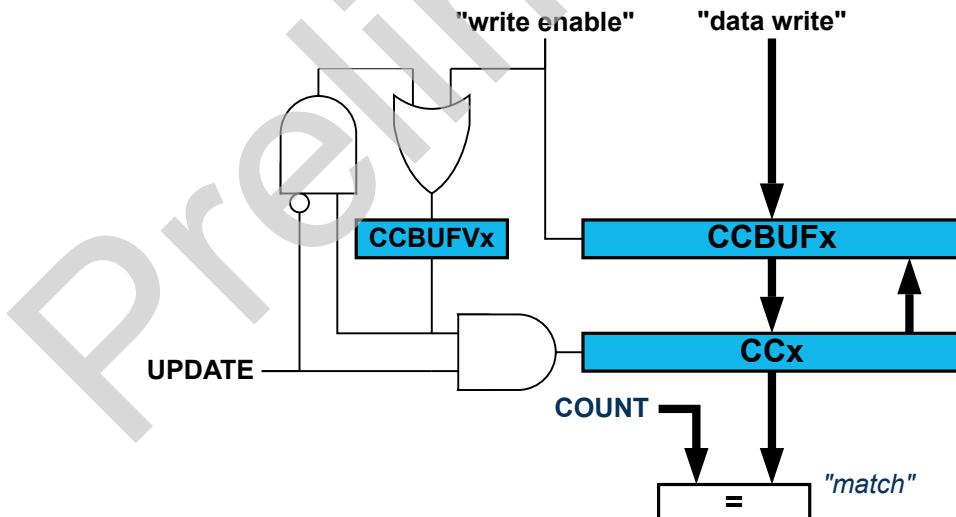
The Compare Channels (CCx) registers, and the Period (PER) register in 8-bit mode are double buffered. Each buffer register has a buffer valid bit (CCBUFVx or PERBUFV) in the STATUS register, which indicates that the buffer register contains a new valid value that can be copied into the corresponding register. As long as the respective buffer valid status flag (PERBUFV or CCBUFVx) are set to '1', related syncbusy bits are set (SYNCBUSY.PER or SYNCBUSY.CCx), a write to the respective PER/PERBUF or CCx/CCBUFx registers will generate a PAC error, and access to the respective PER or CCx register is invalid.

When the buffer valid flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0', (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from buffer registers will be copied into the corresponding register under hardware UPDATE conditions, then the buffer valid flags bit in the STATUS register are automatically cleared by hardware.

Note: The software update command (CTRLBSET.CMD=0x3) is acting independently of the LUPD value.

A compare register is double buffered as in the following figure.

Figure 38-7. Compare Channel Double Buffering



Both the registers (PER/CCx) and corresponding buffer registers (PERBUF/CCBUFx) are available in the I/O register map, and the double buffering feature is not mandatory. The double buffering is disabled by writing a '1' to CTRLBSET.LUPD.

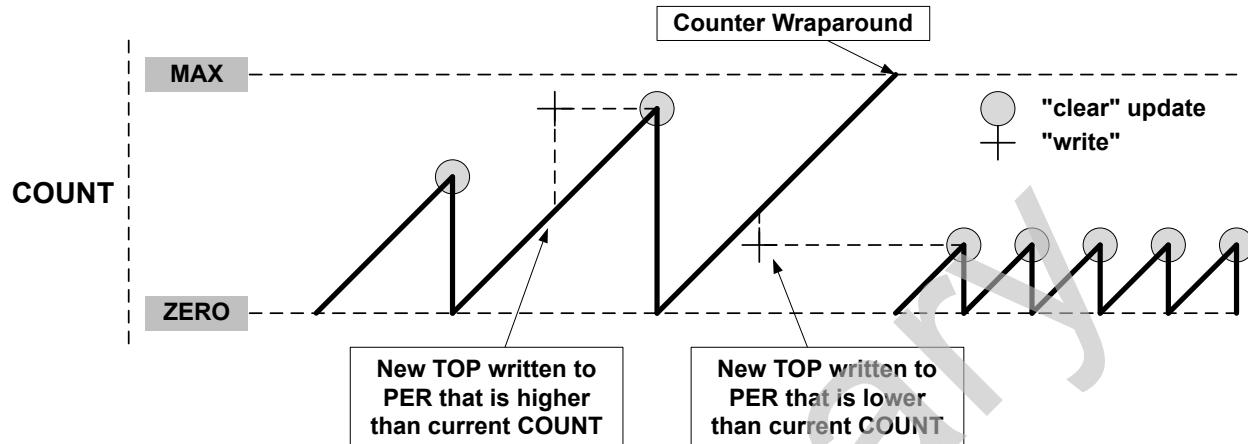
Note: In NFRQ, MFRQ or PWM down-counting counter mode (CTRLBSET.DIR=1), when double buffering is enabled (CTRLBCLR.LUPD=1), PERBUF register is continuously copied into the PER independently of update conditions.

Changing the Period

The counter period can be changed by writing a new TOP value to the Period register (PER or CC0, depending on the waveform generation mode), which is available in 8-bit mode. Any period update on registers (PER or CCx) is effective after the synchronization delay.

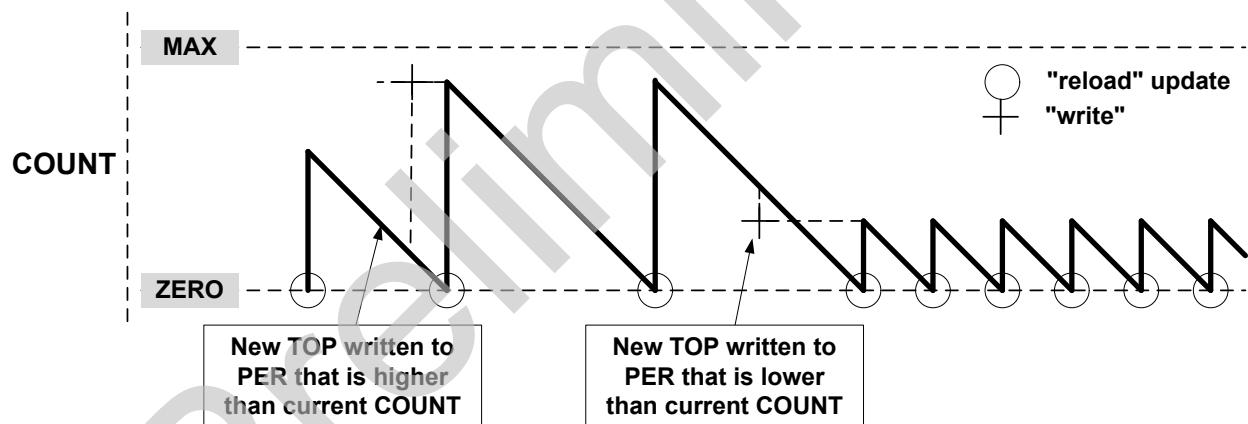
A counter wraparound can occur in any operation mode when up-counting without buffering, see the following figure.

Figure 38-8. Unbuffered Single-Slope Up-Counting Operation



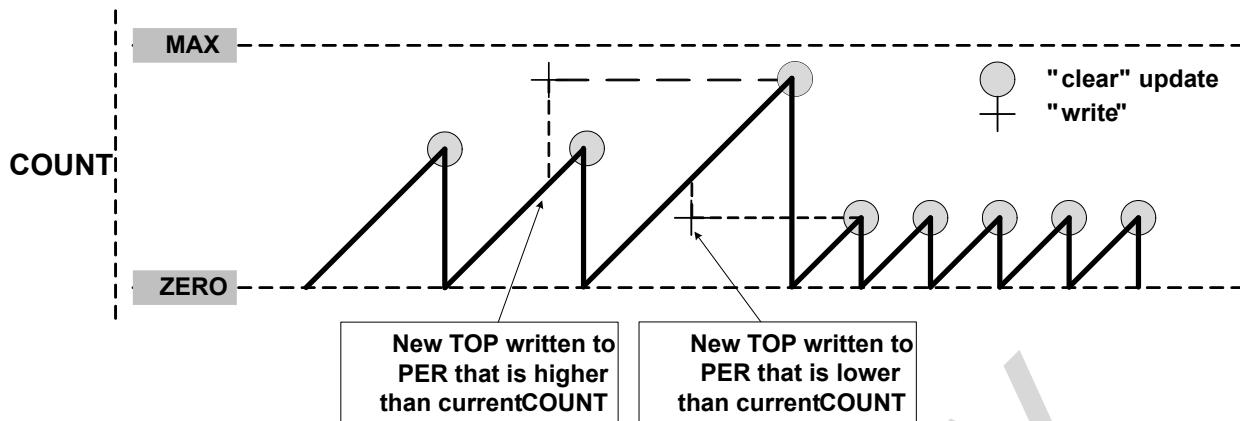
COUNT and TOP are continuously compared, so when a new TOP value that is lower than current COUNT is written to TOP, COUNT will wrap before a compare match.

Figure 38-9. Unbuffered Single-Slope Down-Counting Operation



When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as shown in the following figure. This prevents wraparound and the generation of odd waveforms.

Figure 38-10. Changing the Period Using Buffering



38.6.2.8 Capture Operations

To enable and use capture operations, the corresponding Capture Channel x Enable bit in the Control A register (CTRLA.CAPENx) must be written to '1'.

A capture trigger can be provided by input event line TC_EV or by asynchronous IO pin WO[x] for each capture channel or by a TC event. To enable the capture from input event line, Event Input Enable bit in the Event Control register (EVCTRL.TCEI) must be written to '1'. To enable the capture from the IO pin, the Capture On Pin x Enable bit in CTRLA register (CTRLA.COPENx) must be written to '1'.

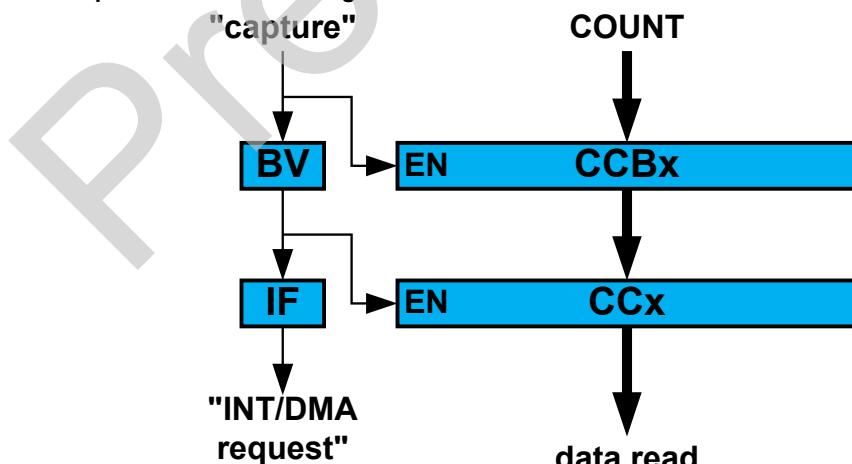
Notes:

1. The RETRIGGER, COUNT and START event actions are available only on an event from the Event System.
2. Event system channels must be configured to operate in asynchronous mode of operation when used for capture operations.

By default, a capture operation is done when a rising edge is detected on the input signal. Capture on falling edge is available, its activation is depending on the input source:

- When the channel is used with a IO pin, write a '1' to the corresponding Invert Enable bit in the Drive Control register (DRVCTRL.INVENx).
- When the channel is counting events from the Event System, write a '1' to the TC Event Input Invert Enable bit in Event Control register (EVCTRL.TCINV).

Figure 38-11. Capture Double Buffering



For input capture, the buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBUFx is transferred to CCx. The buffer valid flag is passed to set the CCx interrupt flag (IF) and generate the optional interrupt, event or DMA request. The CCBUFx register value can't be read, all captured data must be read from CCx register.

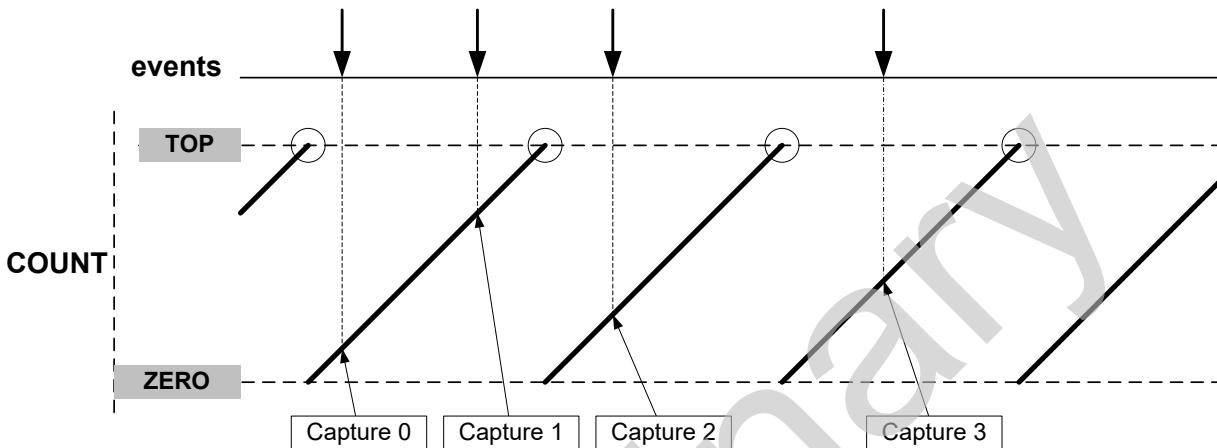
Note:

When up-counting (CTRLBSET.DIR=0), counter values lower than 1 cannot be captured. To capture the full range including value 0, the TC must be in down-counting mode (CTRLBSET.DIR=0).

38.6.2.8.1 Event Capture Action

The compare/capture channels can be used as input capture channels to capture events from the Event System and give them a timestamp. The following figure shows four capture events for one capture channel.

Figure 38-12. Input Capture Timing



The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

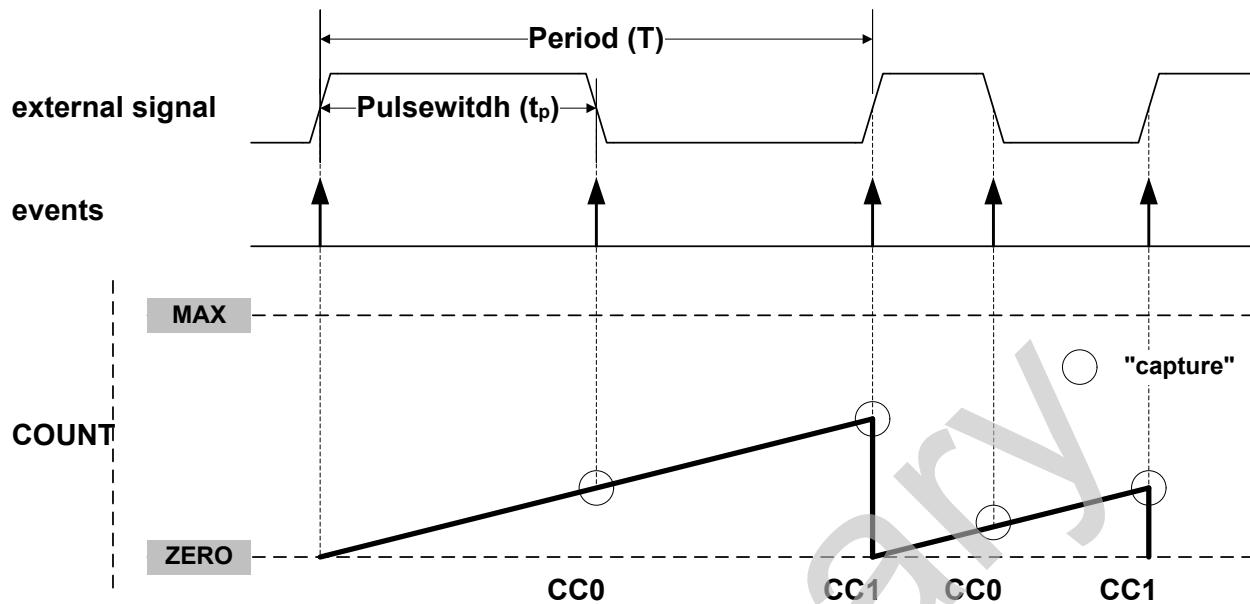
38.6.2.8.2 Period and Pulse-Width (PPW) Capture Action

The TC can perform two input captures and restart the counter on one of the edges. This enables the TC to measure the pulse width and period and to characterize the frequency f and duty cycle of an input signal:

$$f = \frac{1}{T}$$

$$\text{dutyCycle} = \frac{t_p}{T}$$

Figure 38-13. PWP Capture



Selecting PWP in the Event Action bit group in the Event Control register (EVCTRL.EVACT) enables the TC to perform one capture action on the rising edge and the other one on the falling edge. The period T will be captured into CC1 and the pulse width t_p in CC0. EVCTRL.EVACT=PPW (period and pulse-width) offers identical functionality, but will capture T into CC0 and t_p into CC1.

The TC Event Input Invert Enable bit in the Event Control register (EVCTRL.TCINV) is used to select whether the wraparound should occur on the rising edge or the falling edge. If EVCTRL.TCINV=1, the wraparound will happen on the falling edge. In case pin capture is enabled, this can also be achieved by modifying the value of the DRVCTRL.INVENx bit.

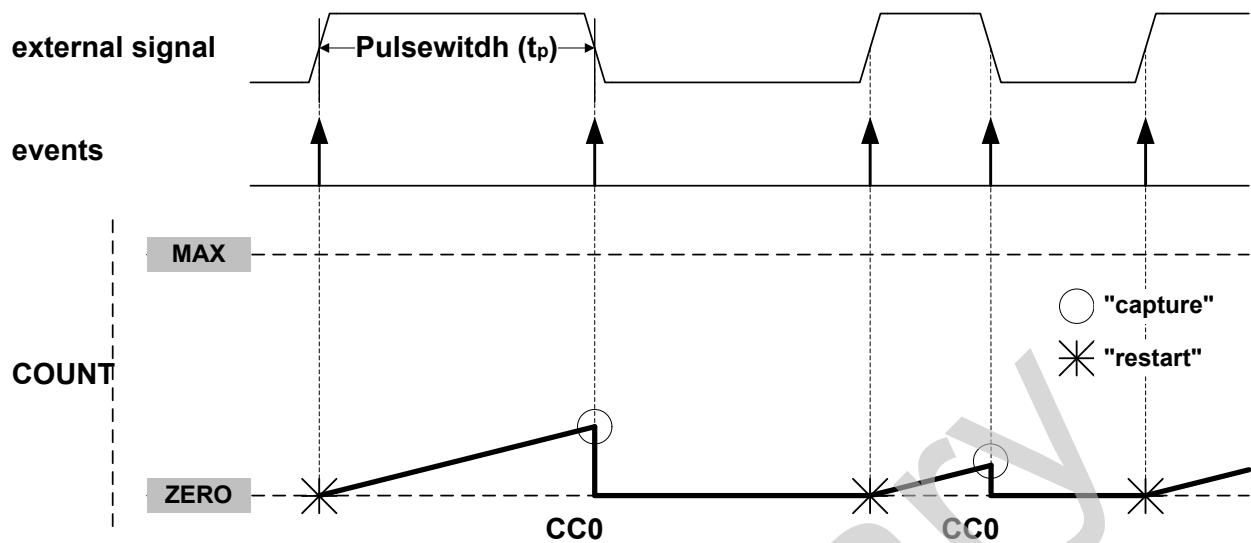
The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Note: The corresponding capture is working only if the channel is enabled in capture mode (CTRLA.CAPTENx=1). If not, the capture action is ignored and the channel is enabled in compare mode of operation. Consequently, both channels must be enabled in order to fully characterize the input.

38.6.2.8.3 Pulse-Width Capture Action

The TC performs the input capture on the falling edge of the input signal. When the edge is detected, the counter value is cleared and the TC stops counting. When a rising edge is detected on the input signal, the counter restarts the counting operation. To enable the operation on opposite edges, the input signal to capture must be inverted (refer to DRVCTRL.INVEN or EVCTRL.TCEINV).

Figure 38-14. Pulse-Width Capture on Channel 0



The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

38.6.3 Additional Features

38.6.3.1 One-Shot Operation

When one-shot is enabled, the counter automatically stops on the next Counter Overflow or Underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is automatically set and the waveform outputs are set to zero.

One-shot operation is enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT), and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TC will count until an overflow or underflow occurs and stops counting operation. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event, or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

38.6.3.2 Time-Stamp Capture

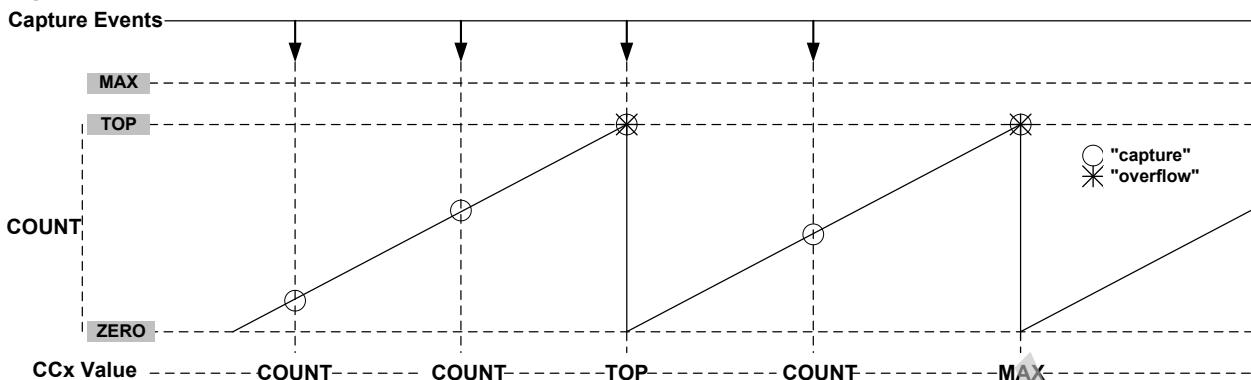
This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. In case of an overflow, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new time-stamp will not be stored and INTFLAG.ERR will be set.

Figure 38-15. Time-Stamp



38.6.3.3 Minimum Capture

The minimum capture is enabled by writing the CAPTMIN mode in the Channel n Capture Mode bits in the Control A register (CTRLA.CAPTMODEn = CAPTMIN).

CCx Content:

In CAPTMIN operations, CCx keeps the Minimum captured values. Before enabling this mode of capture, the user must initialize the corresponding CCx register value to a value different from zero. If the CCx register initial value is zero, no captures will be performed using the corresponding channel.

MCx Behaviour:

In CAPTMIN operation, capture is performed only when on capture event time, the counter value is lower than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is upper or equal to the value captured on the previous event. So interrupt flag is set when a new absolute local Minimum value has been detected.

38.6.3.4 Maximum Capture

The maximum capture is enabled by writing the CAPTMAX mode in the Channel n Capture Mode bits in the Control A register (CTRLA.CAPTMODEn = CAPTMAX).

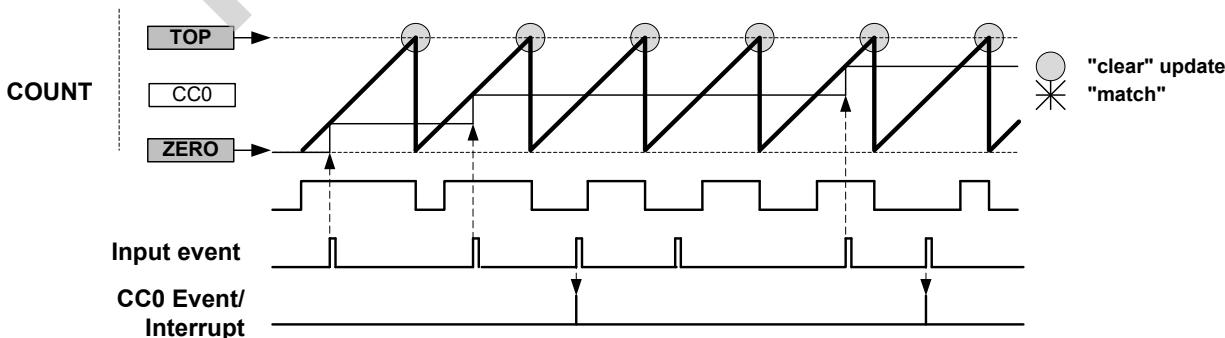
CCx Content:

In CAPTMAX operations, CCx keeps the Maximum captured values. Before enabling this mode of capture, the user must initialize the corresponding CCx register value to a value different from TOP. If the CCx register initial value is TOP, no captures will be performed using the corresponding channel.

MCx Behaviour:

In CAPTMAX operation, capture is performed only when on capture event time, the counter value is upper than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is lower or equal to the value captured on the previous event. So interrupt flag is set when a new absolute local Maximum value has been detected.

Figure 38-16. Maximum Capture Operation with CC0 Initialized with ZERO Value



38.6.4 DMA Operation

The TC can generate the following DMA requests:

- Overflow (OVF): the request is set when an update condition (overflow, underflow or re-trigger) is detected, the request is cleared by hardware on DMA acknowledge.
- Match or Capture Channel x (MCx): for a compare channel, the request is set on each compare match detection, the request is cleared by hardware on DMA acknowledge. For a capture channel, the request is set when valid data is present in the CC_x register, and cleared when CC_x register is read.

38.6.5 Interrupts

The TC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCx)
- Capture Overflow Error (ERR)

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition occurs.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the TC is reset. See *INTFLAG* from Related Links for more details on how to clear the interrupt flags.

The TC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

[38.7.1.7. INTFLAG](#)

38.6.6 Events

The TC can generate the following output events:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCX0-1)

Writing a '1' to an Event Output bit in the Event Control register (EVCTRL.MCEO_x) enables the corresponding output event. The output event is disabled by writing EVCTRL.MCEO_x=0.

One of the following event actions can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT):

- Disable event action (OFF)
- Start TC (START)
- Re-trigger TC (RETRIGGER)
- Count on event (COUNT)
- Capture time stamp (STAMP)
- Capture Period (PPW and PWP)
- Capture Pulse Width (PW)

Writing a '1' to the TC Event Input bit in the Event Control register (EVCTRL.TCEI) enables input events (EVU0-2) to the TC. Writing a '0' to this bit disables input events to the TC. The TC requires only asynchronous event inputs. See *Event System (EVSYS)* from Related Links for additional information on configuring the asynchronous events.

Related Links

[27. Event System \(EVSYS\)](#)

38.6.7 Sleep Mode Operation

The TC can be configured to operate in any sleep mode. To be able to run in standby, the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. This peripheral can wake up the device from any sleep mode using interrupts or perform actions through the Event System.

If the On Demand bit in the Control A register (CTRLA.ONDEMAND) is written to '1', the module stops requesting its peripheral clock when the STOP bit in STATUS register (STATUS.STOP) is set to '1'. When a re-trigger or start condition is detected, the TC requests the clock before the operation starts.

38.6.8 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)
- Capture Channel Buffer Valid bit in STATUS register (STATUS.CCBUFVx)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Channel x Compare/Capture Value and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

The following registers are synchronized when read:

- Count Value register (COUNT): synchronization is done on demand through READSYNC command (CTRLBSET.CMD)
- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Channel x Compare/Capture Value (CCx)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

38.7 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

PIC32CX-BZ2 and WBZ45 Family

Timer/Counter (TC)

38.7.1 Register Summary - 8-bit Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK		PRESCALER[2:0]	
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV			EVACT[2:0]	
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0								WAVEGEN[1:0]
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x14	COUNT	7:0				COUNT[7:0]				
0x15	Reserved									
0x1A										
0x1B	PER	7:0				PER[7:0]				
0x1C	CC0	7:0				CC[7:0]				
0x1D	CC1	7:0				CC[7:0]				
0x1E	Reserved									
0x2E										
0x2F	PERBUF	7:0				PERBUF[7:0]				
0x30	CCBUF0	7:0				CCBUF[7:0]				
0x31	CCBUF1	7:0				CCBUF[7:0]				

38.7.1.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	CAPTMODE1[1:0]	26	25	24
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0
Bit	23	22	21	20	COPEN1	COPEN0	CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0
Bit	15	14	13	12	ALOCK	PRESCALER[2:0]		
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0
Bit	7	6	5	4	PRESCSYNC[1:0]	MODE[1:0]	ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1

These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0

These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable

Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable

Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.

Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command. Writing a '0' to this bit will generate DMA triggers on each TC cycle.

This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.

This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.

In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.

This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter should wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.

These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.

These bits are not synchronized.

PIC32CX-BZ2 and WBZ45 Family

Timer/Counter (TC)

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

This bit is not enable-protected.

38.7.1.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TCx clock cycle. When a command has been executed, the CMD bit group will be read back as zero. Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUF _x and PERBUF buffer registers value are copied into CC _x and PER registers on hardware update condition.
1	The CCBUF _x and PERBUF buffer registers value are not copied into CC _x and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.1.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero. Writing 0x0 to these bits has no effect.

Writing a value different from 0x0 from the following table will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the LUPD bit.

This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.1.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0
Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV			EVACT[2:0]	
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEO_x Match or Capture Channel x Event Output Enable [x = 1..0]

These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable

This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable

This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity

This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action

These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

38.7.1.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.1.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.1.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MC_x Match or Capture Channel x

This flag is set on a comparison match, or when the corresponding CC_x register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MC_x) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag.

In capture operation, this flag is automatically cleared when CC_x register is read.

Bit 1 – ERR Error Interrupt Flag

This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag

This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

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38.7.1.8 Status

Name:	STATUS
Offset:	0x0B
Reset:	0x01
Property:	Read-Synchronized, Write-Synchronized

Bits 4, 5 – CCBUFV_x Channel x Compare or Capture Buffer Valid

For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register. The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.

For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag

This bit is only available in 32-bit mode on the client TC (i.e., TC1 and/or TC3). The bit is set when the associated host TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag

This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

38.7.1.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	WAVEGEN[1:0]							
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode

These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER ¹ / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER ¹ / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

Related Links

[38.6.2.6.1. Waveform Output Operations](#)

38.7.1.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
Access							INVEN1	INVEN0
Reset							R/W	R/W

Bits 0, 1 – INVENx Output Waveform x Invert Enable

INVENx bit selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

38.7.1.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	R/W
								DBGRUN	Reset	0

Bit 0 – DBGRUN Run in Debug Mode

This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

38.7.1.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]

For details on CC channels number, refer to each TC feature list.

This bit is set when the synchronization of CCx between clock domains is started.

This bit is also set when the CCBUF_x is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUF_x bit is cleared.

Bit 5 – PER PER Synchronization Busy

This bit is cleared when the synchronization of PER between the clock domains is complete.

This bit is set when the synchronization of PER between clock domains is started.

This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy

This bit is cleared when the synchronization of COUNT between the clock domains is complete.

This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy

This bit is cleared when the synchronization of STATUS between the clock domains is complete.

This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUF_{Vx}) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy

This bit is cleared when the synchronization of CTRLB between the clock domains is complete.

This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy

This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

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Bit 0 – SWRST SWRST Synchronization Busy

This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Preliminary

38.7.1.13 Counter Value, 8-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	7	6	5	4	3	2	1	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – COUNT[7:0] Counter Value
These bits contain the current counter value.

38.7.1.14 Period Value, 8-bit Mode

Name: PER
Offset: 0x1B
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
PER[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PER[7:0] Period Value

These bits hold the value of the Period Buffer register PERBUF. The value is copied to PER register on UPDATE condition.

38.7.1.15 Channel x Compare/Capture Value, 8-bit Mode

Name: CCx
Offset: 0x1C + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
CC[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CC[7:0] Channel x Compare/Capture Value

These bits contain the compare/capture value in 8-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

38.7.1.16 Period Buffer Value, 8-bit Mode

Name: PERBUF
Offset: 0x2F
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
PERBUF[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PERBUF[7:0] Period Buffer Value

These bits hold the value of the period buffer register. The value is copied to PER register on UPDATE condition.

38.7.1.17 Channel x Compare Buffer Value, 8-bit Mode

Name: CCBUF_x
Offset: 0x30 + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
CCBUF[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CCBUF[7:0] Channel x Compare Buffer Value

These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CC_x register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

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38.7.2 Register Summary - 16-bit Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK		PRESCALER[2:0]	
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV			EVACT[2:0]	
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0								WAVEGEN[1:0]
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x14	COUNT	7:0				COUNT[7:0]				
		15:8				COUNT[15:8]				
0x16 ... 0x1B	Reserved									
0x1C	CC0	7:0				CC[7:0]				
		15:8				CC[15:8]				
0x1E	CC1	7:0				CC[7:0]				
		15:8				CC[15:8]				
0x20 ... 0x2F	Reserved									
0x30	CCBUFO	7:0				CCBUF[7:0]				
		15:8				CCBUF[15:8]				
0x32	CCBUFI	7:0				CCBUF[7:0]				
		15:8				CCBUF[15:8]				

38.7.2.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	CAPTMODE1[1:0]	26	25	24
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0
Bit	23	22	21	20	COPEN1	COPEN0	CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0
Bit	15	14	13	12	ALOCK	PRESCALER[2:0]		
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0
Bit	7	6	5	4	PRESCSYNC[1:0]	MODE[1:0]	ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1

These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0

These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable

Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable

Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.

Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command. Writing a '0' to this bit will generate DMA triggers on each TC cycle.

This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.

This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.

In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.

This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter should wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.

These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.

These bits are not synchronized.

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Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

This bit is not enable-protected.

38.7.2.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TCx clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUF _x and PERBUF buffer registers value are copied into CC _x and PER registers on hardware update condition.
1	The CCBUF _x and PERBUF buffer registers value are not copied into CC _x and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.2.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero. Writing 0x0 to these bits has no effect.

Writing a value different from 0x0 from the following table will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the LUPD bit.

This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.2.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0
Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV			EVACT[2:0]	
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEO_x Match or Capture Channel x Event Output Enable [x = 1..0]

These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable

This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable

This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity

This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action

These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

38.7.2.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.2.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.2.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MC_x Match or Capture Channel x

This flag is set on a comparison match, or when the corresponding CC_x register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MC_x) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag.

In capture operation, this flag is automatically cleared when CC_x register is read.

Bit 1 – ERR Error Interrupt Flag

This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag

This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

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38.7.2.8 Status

Name:	STATUS
Offset:	0x0B
Reset:	0x01
Property:	Read-Synchronized, Write-Synchronized

Bits 4, 5 – CCBUFV_x Channel x Compare or Capture Buffer Valid

For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register. The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.

For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag

This bit is only available in 32-bit mode on the client TC (i.e., TC1 and/or TC3). The bit is set when the associated host TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag

This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

38.7.2.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	WAVEGEN[1:0]							
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode

These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER ¹ / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER ¹ / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

Related Links

[38.6.2.6.1. Waveform Output Operations](#)

38.7.2.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
Access							INVEN1	INVEN0
Reset							R/W	R/W

Bits 0, 1 – INVENx Output Waveform x Invert Enable

INVENx bit selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

38.7.2.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	R/W
								DBGRUN	Reset	0

Bit 0 – DBGRUN Run in Debug Mode

This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

38.7.2.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]

For details on CC channels number, refer to each TC feature list.

This bit is set when the synchronization of CCx between clock domains is started.

This bit is also set when the CCBUF_x is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUF_x bit is cleared.

Bit 5 – PER PER Synchronization Busy

This bit is cleared when the synchronization of PER between the clock domains is complete.

This bit is set when the synchronization of PER between clock domains is started.

This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy

This bit is cleared when the synchronization of COUNT between the clock domains is complete.

This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy

This bit is cleared when the synchronization of STATUS between the clock domains is complete.

This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUF_{Vx}) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy

This bit is cleared when the synchronization of CTRLB between the clock domains is complete.

This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy

This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

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Bit 0 – SWRST SWRST Synchronization Busy

This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Preliminary

38.7.2.13 Counter Value, 16-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	15	14	13	12	11	10	9	8
COUNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Counter Value

These bits contain the current counter value.

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38.7.2.14 Channel x Compare/Capture Value, 16-bit Mode

Name: CCx
Offset: 0x1C + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
CC[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
CC[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CC[15:0] Channel x Compare/Capture Value

These bits contain the compare/capture value in 16-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

38.7.2.15 Channel x Compare Buffer Value, 16-bit Mode

Name: CCBUF_x
Offset: 0x30 + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
CCBUF[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CCBUF[7:0]								
Bit	7	6	5	4	3	2	1	0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CCBUF[15:0] Channel x Compare Buffer Value

These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CC_x register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

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38.7.3 Register Summary - 32-bit Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]	ENABLE	SWRST	
		15:8	DMAOS				ALOCK		PRESCALER[2:0]	
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV			EVACT[2:0]	
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0								WAVEGEN[1:0]
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x14	COUNT	7:0				COUNT[7:0]				
		15:8				COUNT[15:8]				
		23:16				COUNT[23:16]				
		31:24				COUNT[31:24]				
0x18	...									
0x1B	Reserved									
0x1C	CC0	7:0				CC[7:0]				
		15:8				CC[15:8]				
		23:16				CC[23:16]				
		31:24				CC[31:24]				
0x20	CC1	7:0				CC[7:0]				
		15:8				CC[15:8]				
		23:16				CC[23:16]				
		31:24				CC[31:24]				
0x24	...									
0x2F	Reserved									
0x30	CCBUFO	7:0				CCBUF[7:0]				
		15:8				CCBUF[15:8]				
		23:16				CCBUF[23:16]				
		31:24				CCBUF[31:24]				
0x34	CCBUFI	7:0				CCBUF[7:0]				
		15:8				CCBUF[15:8]				
		23:16				CCBUF[23:16]				
		31:24				CCBUF[31:24]				

38.7.4 Register Description - 32-bit Mode

This Register Description section is valid if the TC is in 32-bit mode (CTRLA.MODE=2).

38.7.4.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	CAPTMODE1[1:0]	26	25	24
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0
Bit	23	22	21	20	COPEN1	COPEN0	CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0
Bit	15	14	13	12	ALOCK	PRESCALER[2:0]		
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0
Bit	7	6	5	4	PRESCSYNC[1:0]	MODE[1:0]	ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1

These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0

These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable

Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable

Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.

Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command. Writing a '0' to this bit will generate DMA triggers on each TC cycle.

This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.

This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.

In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.

This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter should wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.

These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.

These bits are not synchronized.

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Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

This bit is not enable-protected.

38.7.4.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TCx clock cycle. When a command has been executed, the CMD bit group will be read back as zero. Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUF _x and PERBUF buffer registers value are copied into CC _x and PER registers on hardware update condition.
1	The CCBUF _x and PERBUF buffer registers value are not copied into CC _x and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.4.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
CMD[2:0]								
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero. Writing 0x0 to these bits has no effect.

Writing a value different from 0x0 from the following table will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the LUPD bit.

This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

38.7.4.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0
Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV			EVACT[2:0]	
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEO_x Match or Capture Channel x Event Output Enable [x = 1..0]

These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable

This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable

This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity

This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action

These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

38.7.4.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.4.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
Access			MC1	MC0			ERR	OVF
Reset			R/W	R/W			R/W	R/W

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.4.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x

This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag.

In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag

This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag

This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

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38.7.4.8 Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized, Write-Synchronized

Bits 4, 5 – CCBUFV_x Channel x Compare or Capture Buffer Valid

For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register. The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.

For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag

This bit is only available in 32-bit mode on the client TC (i.e., TC1 and/or TC3). The bit is set when the associated host TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag

This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

38.7.4.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	WAVEGEN[1:0]							
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode

These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation should be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER ¹ / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER ¹ / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode it is the respective MAX value.

Related Links

[38.6.2.6.1. Waveform Output Operations](#)

38.7.4.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
Access							INVEN1	INVEN0
Reset							R/W	R/W

Bits 0, 1 – INVENx Output Waveform x Invert Enable

INVENx bit selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

38.7.4.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0	Access	R/W
								DBGRUN	Reset	0

Bit 0 – DBGRUN Run in Debug Mode

This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

38.7.4.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]

For details on CC channels number, refer to each TC feature list.

This bit is set when the synchronization of CCx between clock domains is started.

This bit is also set when the CCBUF_x is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUF_x bit is cleared.

Bit 5 – PER PER Synchronization Busy

This bit is cleared when the synchronization of PER between the clock domains is complete.

This bit is set when the synchronization of PER between clock domains is started.

This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy

This bit is cleared when the synchronization of COUNT between the clock domains is complete.

This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy

This bit is cleared when the synchronization of STATUS between the clock domains is complete.

This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUF_{Vx}) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy

This bit is cleared when the synchronization of CTRLB between the clock domains is complete.

This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy

This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

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Bit 0 – SWRST SWRST Synchronization Busy

This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

Preliminary

38.7.4.13 Counter Value, 32-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	31	30	29	28	27	26	25	24
COUNT[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0] Counter Value
These bits contain the current counter value.

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38.7.4.14 Channel x Compare/Capture Value, 32-bit Mode

Name: CC_x
Offset: 0x1C + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
CC[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CC[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CC[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CC[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CC[31:0] Channel x Compare/Capture Value

These bits contain the compare/capture value in 32-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

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38.7.4.15 Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUF_x
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
CCBUF[31:24]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CCBUF[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CCBUF[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
CCBUF[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CCBUF[31:0] Channel x Compare Buffer Value

These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CC_x register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

39. TCC – Timer/Counter for Control Applications

39.1 Overview

The device provides three instances of the Timer/Counter for Control Applications (TCC).

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation, such as frequency generation and pulse-width modulation.

Waveform extensions are featured for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. They allow for low-side and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

Note: The TCC configurations, such as channel numbers and features, may be reduced for some of the TCC instances.

Table 39-1. TCC Specific Configuration

TCC No.	Counter Size (SIZE)	Master Link (MASTER_SLAVE_MODE) (0 = NA, 1 = Master, 2 = Slave)	Channels (CC_NUM)	Pins WO_NUM (OW_NUM)	Extensions						
					Fault 1=YES	Dithering 1=YES	OutMatrix 1=YES (OTMX)	Dead Time Insertion 1=YES (DTI)	Swap 1=YES (SWAP)	Pattern Generation 1=YES (PG)	
0	24	1	6	6	1	1	1	1	1	1	
1	24	2	6	6	1	1	1	1	1	1	
2	16	0	2	2	1	0	1	0	0	0	

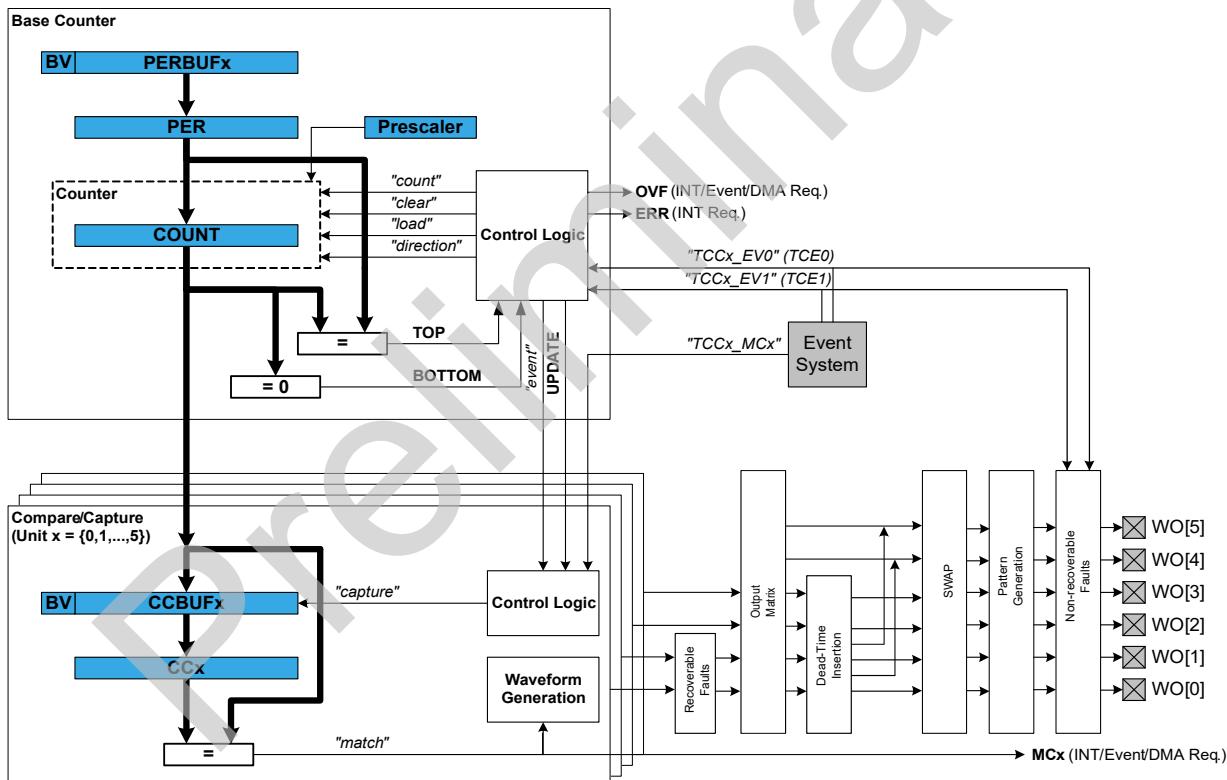
39.2 Features

- Up to six Compare/Capture Channels (CC) with:
 - Double buffered period setting
 - Double buffered compare or capture channel
 - Circular buffer on period and compare channel registers
- Waveform Generation:
 - Frequency generation
 - Single-slope pulse-width modulation (PWM)
 - Dual-slope PWM with half-cycle reload capability
- Input Capture:
 - Event capture
 - Frequency capture
 - Pulse-width capture
- Waveform Extensions:
 - Configurable distribution of compare channels outputs across port pins
 - Low-side and high-side output with programmable dead-time insertion
 - Waveform swap option with double buffer support
 - Pattern generation with double buffer support
 - Dithering support
- Fault Protection for Safe Disabling of Drivers:

- Two recoverable fault sources
- Two non-recoverable fault sources
- Debugger can be a source of non-recoverable fault
- Input Events:
 - Two input events (EVx) for counter
 - One input event (MCx) for each channel
- Output Events:
 - Three output events (Count, re-trigger and overflow) are available for counter
 - One compare match/input capture event output for each channel
- Interrupts:
 - Overflow and re-trigger interrupt
 - Compare match/input capture interrupt
 - Interrupt on fault detection

39.3 Block Diagram

Figure 39-1. Timer/Counter for Control Applications - Block Diagram



39.4 Signal Description

Table 39-2. Signal Description

Pin Name	Type	Description
TCCx/WO[0]	Digital output	Compare channel 0 waveform output
TCCx/WO[1]	Digital output	Compare channel 1 waveform output

.....continued

Pin Name	Type	Description
...
TCCx/WO[WO_NUM-1]	Digital output	Compare channel n waveform output

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links, for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

- 5. [I/O Ports and Peripheral Pin Select \(PPS\)](#)

39.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

39.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Peripheral Pin Select (PPS).

39.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake up the device from Sleep modes. Events connected to the event system can trigger other operations in the system without exiting Sleep modes.

39.5.3 Clocks

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC. Note that TCC1 and TCC2 share a single peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (PB1_CLK). Due to this asynchronicity, writing certain registers will require synchronization between the clock domains.

39.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first, see *Direct Memory Access Controller* from Related Links.

Related Links

- 21. [Direct Memory Access Controller \(DMAC\)](#)

39.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

- 9.2. [Nested Vector Interrupt Controller \(NVIC\)](#)

39.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links

- 27. [Event System \(EVSYS\)](#)

39.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will halt normal operation. This peripheral can be forced to continue operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

Refer to [39.8.8. DBGCTRL](#) register for details.

39.5.8 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Interrupt Flag register (INTFLAG)
- Status register (STATUS)
- Period and Period Buffer registers (PER, PERBUF)
- Compare/Capture and Compare/Capture Buffer registers (CCx, CCBUFx)
- Control Waveform register (WAVE)
- Pattern Generation Value and Pattern Generation Value Buffer registers (PATT, PATTBUF)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

39.5.9 Analog Connections

Not applicable.

39.6 Functional Description

39.6.1 Principle of Operation

The following definitions are used throughout the documentation:

Table 39-3. Timer/Counter for Control Applications - Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the Waveform Generator mode in Waveform Output Operations. See <i>Waveform Output Operations</i> from Related Links.
ZERO	The counter reaches ZERO when it contains all zeroes.
MAX	The counter reaches maximum when it contains all ones.
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source.
Counter	The clock control is handled externally (e.g., counting external events).
CC	For compare operations, the CC are referred to as "compare channels." For capture operations, the CC are referred to as "capture channels."

Each TCC instance has up to six compare/capture channels (CCx).

The Counter register (COUNT), Period registers with Buffer (PER and PERBUF), and Compare and Capture registers with buffers (CCx and CCBUFx) are 16- or 24-bit registers, depending on each TCC instance. Each Buffer register has a Buffer Valid (BUFV) flag that indicates when the buffer contains a new value.

Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached TOP or ZERO. In either case, the TCC can generate interrupt requests or generate events for the Event System. In Waveform Generator mode, these comparisons are used to set the waveform period or pulse width.

A prescaled generic clock (GCLK_TCCx) and events from the event system can be used to control the counter. The event system is also used as a source to the input capture.

The Recoverable Fault Unit enables event controlled waveforms by acting directly on the generated waveforms of the TCC compare channels output. These events can restart, halt the timer/counter period, shorten the output pulse active time, or disable waveform output as long as the fault condition is present. This can typically be used for current sensing regulation, and zero-crossing and demagnetization re-triggering.

The MCE0 and MCE1 asynchronous event sources are shared with the recoverable fault unit. Only asynchronous events are used internally when fault unit extension is enabled. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Recoverable fault sources can be filtered and/or windowed to avoid false triggering, for example from I/O pin glitches, by using digital filtering, input blanking, and qualification options. See *Recoverable Faults* from Related Links.

In order to support applications with different types of motor control, ballast, LED, H-bridge, power converter, and other types of power switching applications, the following independent units are implemented in some of the TCC instances as optional and successive units:

- Recoverable faults and non-recoverable faults
- Output matrix
- Dead-time insertion
- Swap
- Pattern generation

See *Timer/Counter for Control Applications - Block Diagram* in the *Block Diagram* from Related Links.

The output matrix (OTMX) can distribute and route out the TCC waveform outputs across the port pins in different configurations, each optimized for different application types. The Dead-Time Insertion (DTI) unit splits the four lower OTMX outputs into two non-overlapping signals: the non-inverted Low Side (LS) and inverted High Side (HS) of the waveform output with optional dead-time insertion between LS and HS switching. The SWAP unit can swap the LS and HS pin outputs, and can be used for fast decay motor control.

The pattern generation unit can be used to generate synchronized waveforms with constant logic level on TCC UPDATE conditions. This is useful for easy stepper motor and full bridge control.

The non-recoverable fault module enables event controlled fault protection by acting directly on the generated waveforms of the timer/counter compare channel outputs. When a non-recoverable fault condition is detected, the output waveforms are forced to a preconfigured value that is safe for the application. This is typically used for instant and predictable shut down and disabling high current or voltage drives.

The count event sources (TCE0 and TCE1) are shared with the non-recoverable fault extension. The events can be optionally filtered. If the filter options are not used, the non-recoverable faults provide an immediate asynchronous action on waveform output, even for cases where the clock is not present. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Related Links

- 27. Event System (EVSYS)
- 38.6.2.6.1. Waveform Output Operations
- 39.3. Block Diagram
- 39.6.3.5. Recoverable Faults

39.6.2 Basic Operation

39.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TCC is disabled(CTRLA.ENABLE=0):

- Control A (CTRLA) register, except Run Standby (RUNSTDBY), Enable (ENABLE) and Software Reset (SWRST) bits
- Recoverable Fault n Control registers (FCTRLA and FCTRLB)
- Waveform Extension Control register (WEXCTRL)
- Drive Control register (DRVCTRL)
- Event Control register (EVCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'. Enable-protection is denoted by the "Enable-Protected" property in the register description.

Before the TCC is enabled, it must be configured as outlined by the following steps:

1. Enable the TCC bus clock if not already enabled by default (PB1_CLK).
2. If Capture mode is required, enable the channel in Capture mode by writing a '1' to the Capture Enable bit in the Control A register (CTRLA.CPTEN).

Optionally, the following configurations can be set before enabling TCC:

1. Select PRESCALER setting in the Control A register (CTRLA.PRESCALER).
2. Select Prescaler Synchronization setting in Control A register (CTRLA.PRESCSYNC).
3. If down-counting operation is desired, write the Counter Direction bit in the Control B Set register (CTRLBSET.DIR) to '1'.
4. Select the Waveform Generation operation in the WAVE register (WAVE.WAVEGEN).
5. Select the Waveform Output Polarity in the WAVE register (WAVE.POL).
6. The waveform output can be inverted for the individual channels using the Waveform Output Invert Enable bit group in the Driver register (DRVCTRL.INVEN).

39.6.2.2 Enabling, Disabling, and Resetting

The TCC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TCC is disabled by writing a zero to CTRLA.ENABLE.

The TCC is reset by writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TCC, except DBGCTRL, will be reset to their initial state, and the TCC will be disabled. Refer to Control A (39.8.1. [CTRLA](#)) register for details.

The TCC should be disabled before the TCC is reset to avoid undefined behavior.

39.6.2.3 Prescaler Selection

The GCLK_TCCx clock is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

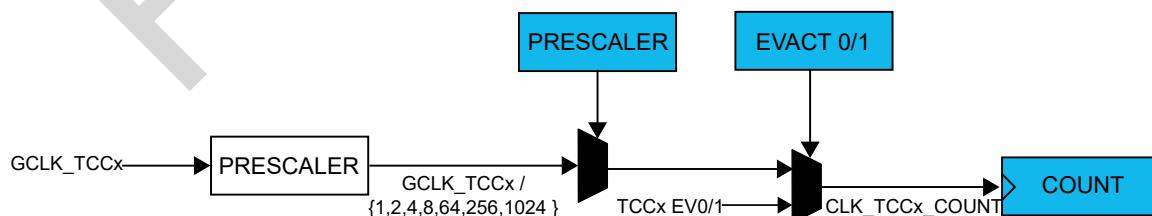
If the prescaler value is higher than one, the Counter Update condition can be optionally executed on the next GCLK_TCCx clock pulse or the next prescaled clock pulse. For further details, refer to the Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) descriptions.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCCx_COUNT.

Figure 39-2. Prescaler



39.6.2.4 Counter Operation

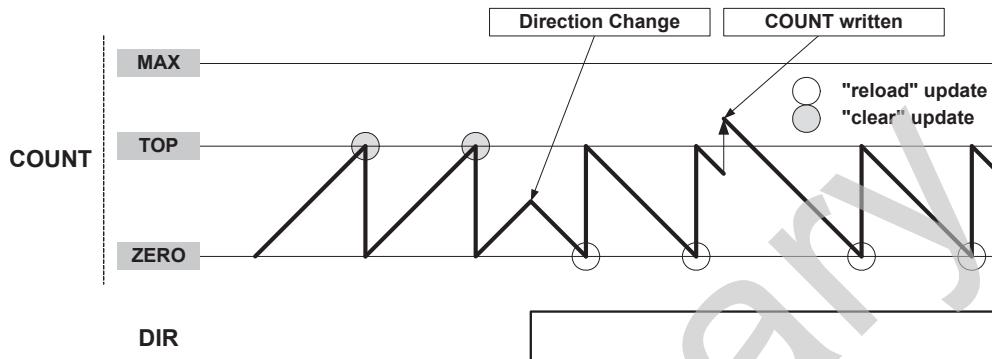
Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TCC clock input (CLK_TCCx_COUNT). A counter clear or reload mark the end of current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If the bit is zero, it's counting up and one if counting down.

The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it's counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When down-counting, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

INTFLAG.OVF can be used to trigger an interrupt, or an event. An overflow/underflow occurrence (i.e. a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT). The One-Shot feature is explained in the [Additional Features](#) section.

Figure 39-3. Counter Operation



It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. The COUNT value will always be ZERO or TOP, depending on direction set by CTRLBSET.DIR or CTRLBCLR.DIR, when starting the TCC, unless a different value has been written to it, or the TCC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed during normal operation. See also [Figure 39-3](#).

Stop Command

A stop command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x2, STOP).

When a stop is detected while the counter is running, the counter will maintain its current value. If the waveform generation (WG) is used, all waveforms are set to a state defined in Non-Recoverable State x Output Enable bit and Non-Recoverable State x Output Value bit in the Driver Control register (DRVCTRL.NRE_x and DRVCTRL.NRV_x), and the Stop bit in the Status register is set (STATUS.STOP).

Pause Event Action

A pause command can be issued when the stop event action is configured in the Input Event Action 1 bits in Event Control register (EVCTRL.EVACT1=0x3, STOP).

When a pause is detected, the counter can stop immediately maintaining its current value and all waveforms keep their current state, as long as a start event action is detected: Input Event Action 0 bits in Event Control register (EVCTRL.EVACT0=0x3, START).

Re-Trigger Command and Event Action

A re-trigger command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x1, RETRIGGER), or from event when the re-trigger event action is configured in the Input Event 0/1 Action bits in Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER).

When the command is detected during counting operation, the counter will be reloaded or cleared, depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). The Re-Trigger bit in the Interrupt Flag Status and Clear register will be set (INTFLAG.TRG). It is also possible to generate an event by writing a '1' to the Re-Trigger Event Output Enable bit in the Event Control register (EVCTRL.TRGEO). If the re-trigger command is detected when the counter is stopped, the counter will resume counting operation from the value in COUNT.

Note:

When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER), enabling the counter will not start the counter. The counter will start on the next incoming event and restart on corresponding following event.

Start Event Action

The start action can be selected in the Event Control register (EVCTRL.EVACT0=0x3, START) and can start the counting operation when previously stopped. The event has no effect if the counter is already counting. When the module is enabled, the counter operation starts when the event is received or when a re-trigger software command is applied.

Note:

When a start event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACT0=0x3, START), enabling the counter will not start the counter. The counter will start on the next incoming event, but it will not restart on subsequent events.

Count Event Action

The TCC can count events. When an event is received, the counter increases or decreases the value, depending on direction settings (CTRLBSET.DIR or CTRLBCLR.DIR).

The count event action is selected by the Event Action 0 bit group in the Event Control register (EVCTRL.EVACT0=0x5, COUNT).

Direction Event Action

The direction event action can be selected in the Event Control register (EVCTRL.EVACT1=0x2, DIR). When this event is used, the asynchronous event path specified in the event system must be configured or selected. The direction event action can be used to control the direction of the counter operation, depending on external events level. When received, the event level overrides the Direction settings (CTRLBSET.DIR or CTRLBCLR.DIR) and the direction bit value is updated accordingly.

Increment Event Action

The increment event action can be selected in the Event Control register (EVCTRL.EVACT0=0x4, INC) and can change the Counter state when an event is received. When the TCE0 event (TCCx_EV0) is received, the counter increments, whatever the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR) is.

Decrement Event Action

The decrement event action can be selected in the Event Control register (EVCTRL.EVACT1=0x4, DEC) and can change the Counter state when an event is received. When the TCE1 (TCCx_EV1) event is received, the counter decrements, whatever the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR) is.

Non-recoverable Fault Event Action

Non-recoverable fault actions can be selected in the Event Control register (EVCTRL.EVACTn=0x7, FAULT). When received, the counter will be stopped and the output of the compare channels is overridden according to the Driver Control register settings (DRVCTRL.NREx and DRVCTRL.NRVx). TCE0 and TCE1 must be configured as asynchronous events.

Event Action Off

If the event action is disabled (EVCTRL.EVACTn=0x0, OFF), enabling the counter will also start the counter.

Related Links

[39.6.3.1. One-Shot Operation](#)

39.6.2.5 Compare Operations

By default, the Compare/Capture channel is configured for compare operations. To perform capture operations, it must be re-configured.

When using the TCC with the Compare/Capture Value registers (CCx) for compare operations, the counter value is continuously compared to the values in the CCx registers. This can be used for timer or for waveform operation.

The Channel x Compare/Capture Buffer Value (CCBUFx) registers provide double buffer capability. The double buffering synchronizes the update of the CCx register with the buffer value at the UPDATE condition or a force update command (CTRLBSET.CMD=0x3, UPDATE). See *Double Buffering* from Related Links. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses and ensures glitch-free output.

Related Links

[39.6.2.6. Double Buffering](#)

39.6.2.5.1 Waveform Output Generation Operations

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a Waveform Generation mode in the Waveform Generation Operation bit in Waveform register (WAVE.WAVEGEN).
2. Optionally invert the waveform output WO[x] by writing the corresponding Waveform Output x Inversion bit in the Driver Control register (DRVCTRL.INVENx).
3. Configure the pins with the I/O Pin Controller. See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.

Note: Event must not be used when the compare channel is set in waveform output operating mode.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TCC_COUNT (see Normal Frequency Operation). An interrupt and/or event can be generated on the same condition if Match/Capture occurs, i.e. INTENSET.MCx and/or EVCTRL.MCEOx is '1'. Both interrupt and event can be generated simultaneously.

There are seven waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

- Normal Frequency (NFRQ)
- Match Frequency (MFRQ)
- Normal Pulse-Width Modulation (NPWM)
- Dual-slope, interrupt/event at TOP (DSTOP)
- Dual-slope, interrupt/event at ZERO (DSBOTTOM)
- Dual-slope, interrupt/event at Top and ZERO (DSBOTH)
- Dual-slope, critical interrupt/event at ZERO (DSCRITICAL)

When using MFRQ configuration, the TOP value is defined by the CC0 register value. For the other waveform operations, the TOP value is defined by the Period (PER) register value.

For dual-slope waveform operations, the update time occurs when the counter reaches ZERO. For the other Waveforms Generation modes, the update time occurs on counter wraparound, on overflow, underflow, or re-trigger.

The table below shows the update counter and overflow event/interrupt generation conditions in different operation modes.

Table 39-4. Counter Update and Overflow Event/interrupt Conditions

Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See section 'Output Polarity' below		TOP	ZERO
DSCRITICAL	Dual-slope PWM	PER	ZERO			-	ZERO
DSBOTTOM	Dual-slope PWM	PER	ZERO			-	ZERO
DSBOTH	Dual-slope PWM	PER	TOP ⁽¹⁾ & ZERO			TOP	ZERO
DSTOP	Dual-slope PWM	PER	ZERO			TOP	-

1. The UPDATE condition on TOP only will occur when circular buffer is enabled for the channel.

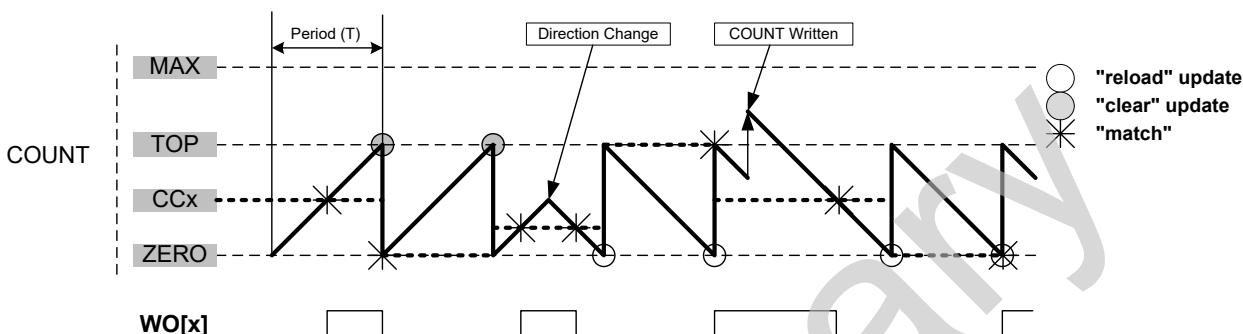
Related Links

5. I/O Ports and Peripheral Pin Select (PPS)

39.6.2.5.2 Normal Frequency (NFRQ)

For Normal Frequency generation, the period time (T) is controlled by the period register (PER). The waveform generation output (WO[x]) is toggled on each compare match between COUNT and CCx, and the corresponding Match or Capture Channel x Interrupt Flag (EVCTRL.MCEOx) will be set.

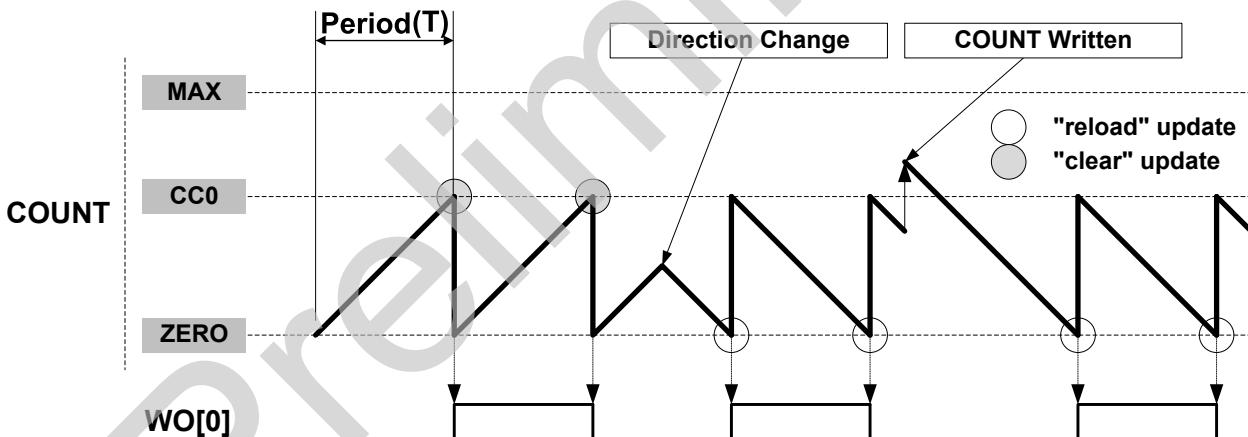
Figure 39-4. Normal Frequency Operation



39.6.2.5.3 Match Frequency (MFRQ)

For Match Frequency generation, the period time (T) is controlled by CC0 register instead of PER. WO[0] toggles on each update condition.

Figure 39-5. Match Frequency Operation



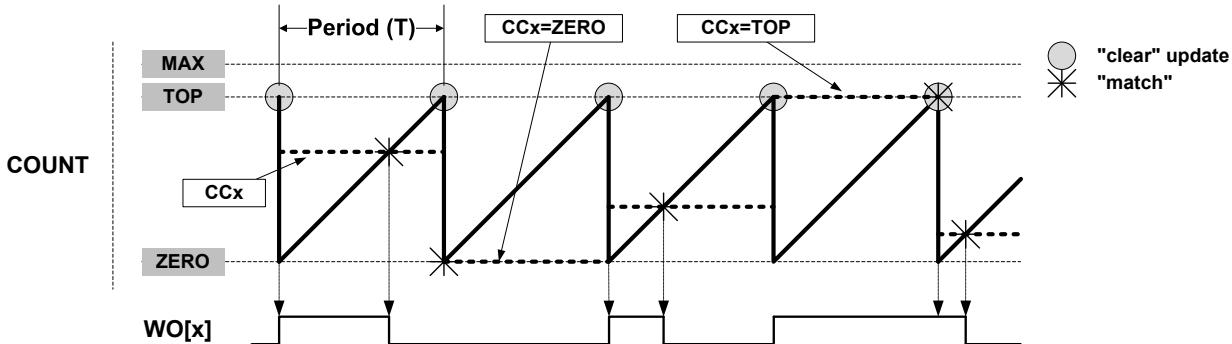
39.6.2.5.4 Normal Pulse-Width Modulation (NPWM)

NPWM uses single-slope PWM generation.

39.6.2.5.5 Single-Slope PWM Operation

For single-slope PWM generation, the period time (T) is controlled by Top value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

Figure 39-6. Single-Slope PWM Operation



The following equation calculates the exact resolution for a single-slope PWM ($R_{\text{PWM_SS}}$) waveform:

$$R_{\text{PWM_SS}} = \frac{\log(\text{TOP}+1)}{\log(2)}$$

The PWM frequency depends on the Period register value (PER) and the peripheral clock frequency ($f_{\text{GCLK_TCCx}}$), and can be calculated by the following equation:

$$f_{\text{PWM_SS}} = \frac{f_{\text{GCLK_TCCx}}}{N(\text{TOP}+1)}$$

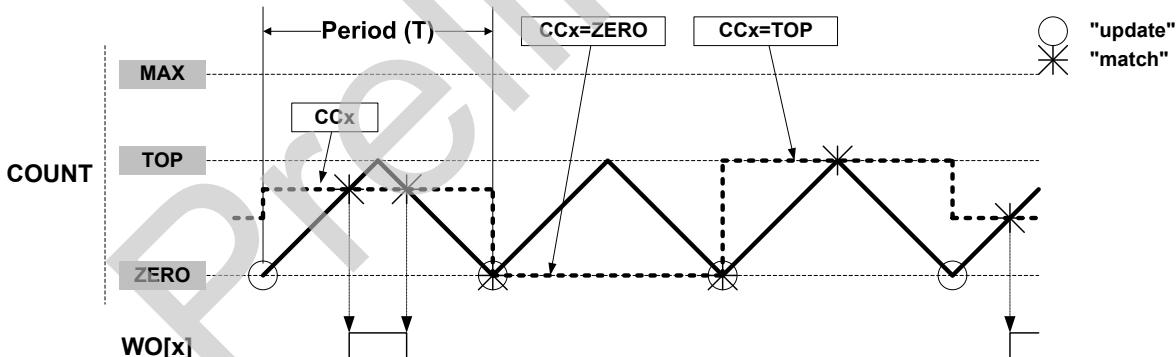
Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

39.6.2.5.6 Dual-Slope PWM Generation

For dual-slope PWM generation, the period setting (TOP) is controlled by PER, while CCx control the duty cycle of the generated waveform output. The figure below shows how the counter repeatedly counts from ZERO to PER and then from PER to ZERO. The waveform generator output is set on compare match when up-counting, and cleared on compare match when down-counting. An interrupt and/or event is generated on TOP (when counting upwards) and/or ZERO (when counting up or down).

In DS BOTH operation, the circular buffer must be enabled to enable the update condition on TOP.

Figure 39-7. Dual-Slope Pulse Width Modulation



Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM ($R_{\text{PWM_DS}}$):

$$R_{\text{PWM_DS}} = \frac{\log(\text{PER}+1)}{\log(2)}$$

The PWM frequency $f_{\text{PWM_DS}}$ depends on the period setting (TOP) and the peripheral clock frequency $f_{\text{GCLK_TCCx}}$, and can be calculated by the following equation:

$$f_{\text{PWM_DS}} = \frac{f_{\text{GCLK_TCCx}}}{2N \cdot \text{PER}}$$

N represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency (f_{GCLK_TCCx}) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width (P_{PWM_DS}) depends on the compare channel (CCx) register value and the peripheral clock frequency (f_{GCLK_TCCx}), and can be calculated by the following equation:

$$P_{PWM_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK_TCCx}}$$

N represents the prescaler divider used.

Note: In DSTOP, DSBOTTOM and DSBOTM operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB] = 0, falling if CCx[MSB] = 1.)

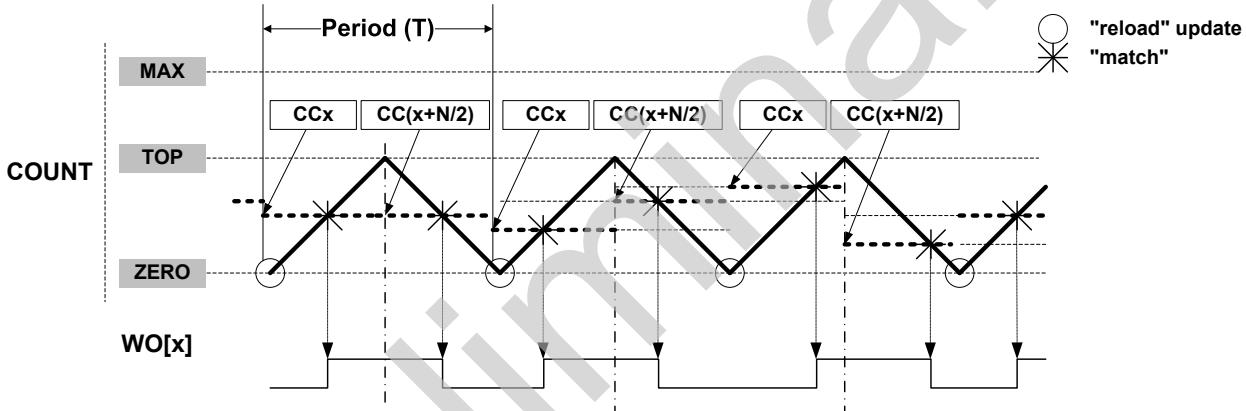
Related Links

[39.6.3.2. Circular Buffer](#)

39.6.2.5.7 Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC_NUM/2) control the generated waveform output edge during down-counting.

Figure 39-8. Dual-Slope Critical Pulse Width Modulation (N=CC_NUM)



39.6.2.5.8 Output Polarity

The polarity (WAVE.POLx) is available in all waveform output generation. In single-slope and dual-slope PWM operation, it is possible to invert the pulse edge alignment individually on start or end of a PWM cycle for each compare channels. The table below shows the waveform output set/clear conditions, depending on the settings of timer/counter, direction, and polarity.

Table 39-5. Waveform Generation Set/Clear Conditions

Waveform Generation Operation	DIR	POLx	Waveform Generation Output Update	
			Set	Clear
Single-Slope PWM	0	0	Timer/counter matches TOP	Timer/counter matches CCx
		1	Timer/counter matches CC	Timer/counter matches TOP
	1	0	Timer/counter matches CC	Timer/counter matches ZERO
		1	Timer/counter matches ZERO	Timer/counter matches CC
Dual-Slope PWM	x	0	Timer/counter matches CC when counting up	Timer/counter matches CC when counting down
		1	Timer/counter matches CC when counting down	Timer/counter matches CC when counting up

In Normal and Match Frequency, the WAVE.POLx value represents the initial state of the waveform output.

39.6.2.6 Double Buffering

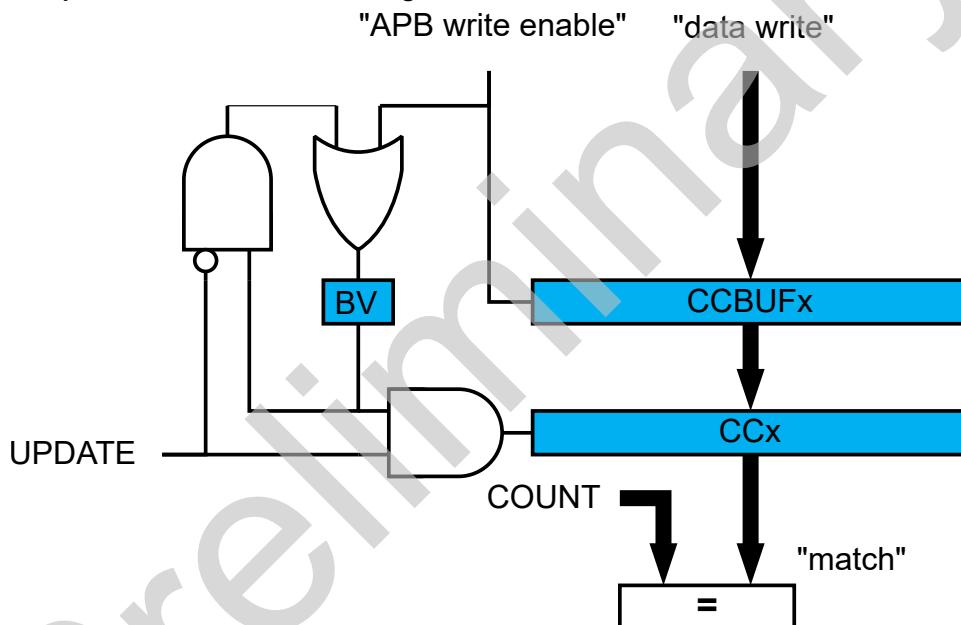
The Pattern (PATT), Period (PER) and Compare Channels (CCx) registers are all double buffered. Each buffer register has a buffer valid (PATTBUFV, PERBUFV and CCBUFVx) bit in the STATUS register, which indicates that the Buffer register contains a valid value that can be copied into the corresponding register. As long as the respective Buffer Valid Status flag (PATTBUFV, PERBUFV or CCBUFVx) are set to '1', the related SYNCBUSY bits are set (SYNCBUSY.PATT, SYNCBUSY.PER or SYNCBUSY.CCx), a write to the respective PATT/PATBUF, PER/PERBUF or CCx/CCBUF registers will generate a PAC error, and read access to the respective PATT, PER or CCx register is invalid.

When the Buffer Valid Flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0', (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from buffer registers will be copied into the corresponding register under hardware UPDATE conditions, then the Buffer Valid flags bit in the STATUS register are automatically cleared by hardware.

Note: Software update command (CTRLBSET.CMD=0x3) act independently of LUPD value.

A compare register is double buffered as in the following figure.

Figure 39-9. Compare Channel Double Buffering



Both the registers (PATT/PER/CCx) and corresponding Buffer registers (PATTBUF/PERBUF/CCBUFx) are available in the I/O register map, and the double buffering feature is not mandatory. The double buffering is disabled by writing a '1' to CTRLSET.LUPD.

Note: In NFRQ, MFRQ or PWM Down-Counting Counter mode (CTRLBSET.DIR=1), when double buffering is enabled (CTRLBCLR.LUPD=1), PERBUF register is continuously copied into the PER independently of update conditions.

Changing the Period

The counter period can be changed by writing a new Top value to the Period register (PER or CC0, depending on the Waveform Generation mode), any period update on registers (PER or CCx) is effective after the synchronization delay, whatever double buffering enabling is.

Figure 39-10. Unbuffered Single-Slope Up-Counting Operation

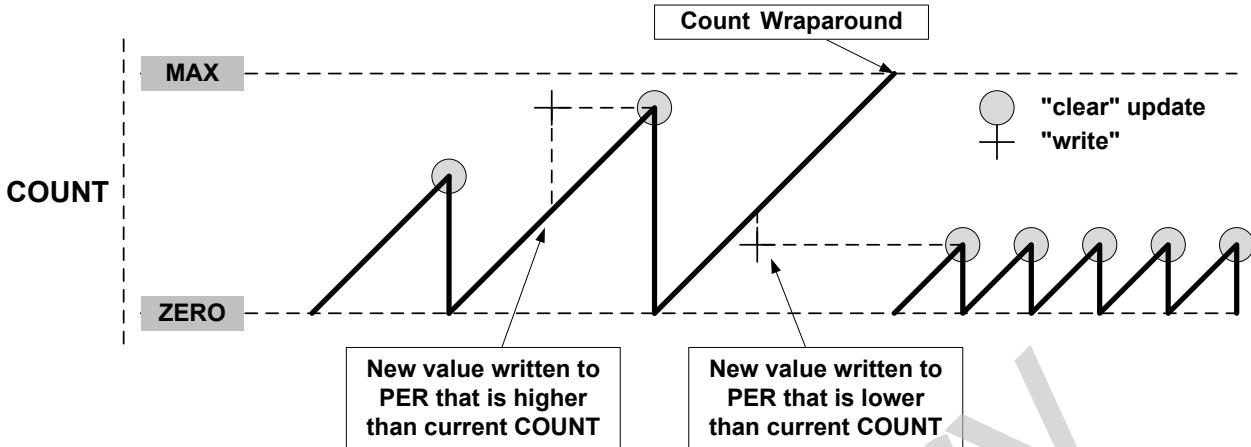
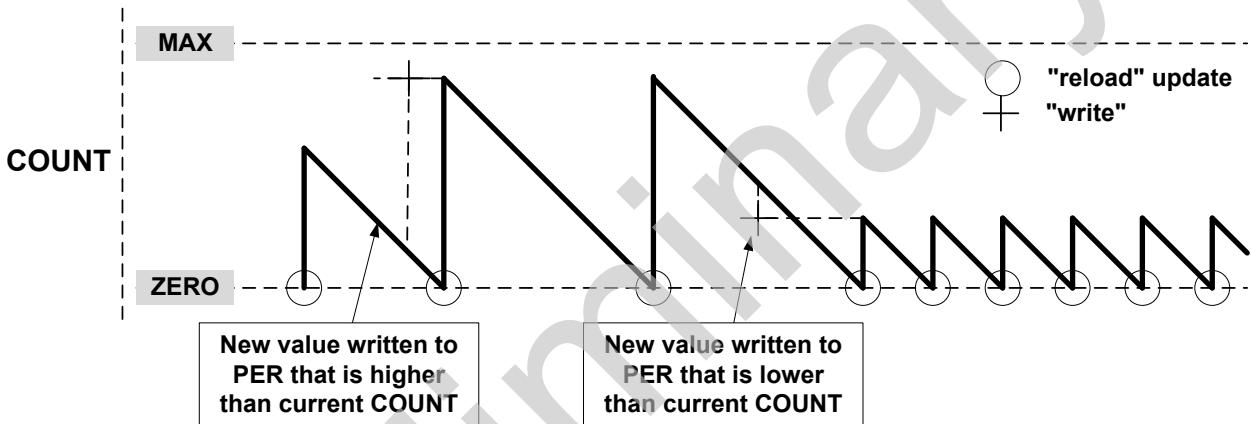
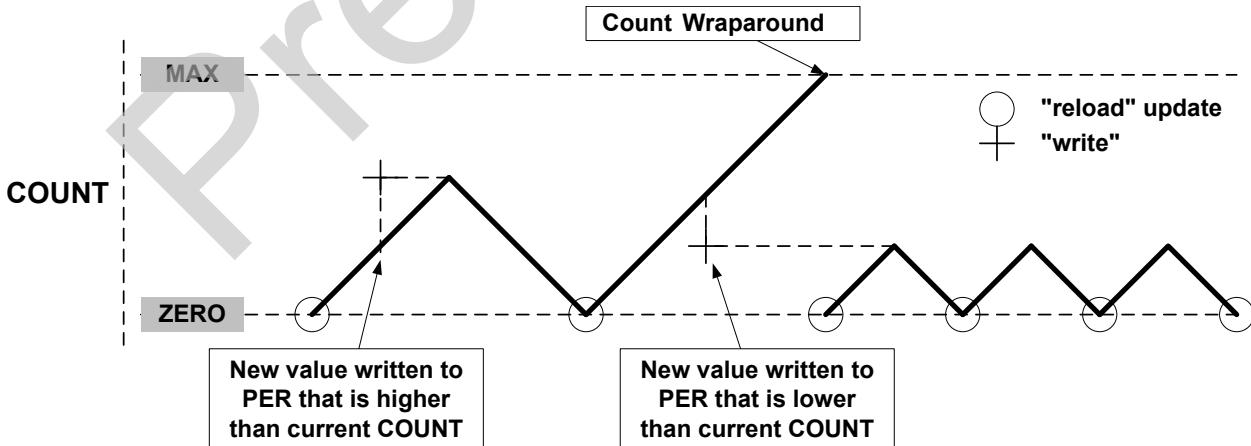


Figure 39-11. Unbuffered Single-Slope Down-Counting Operation



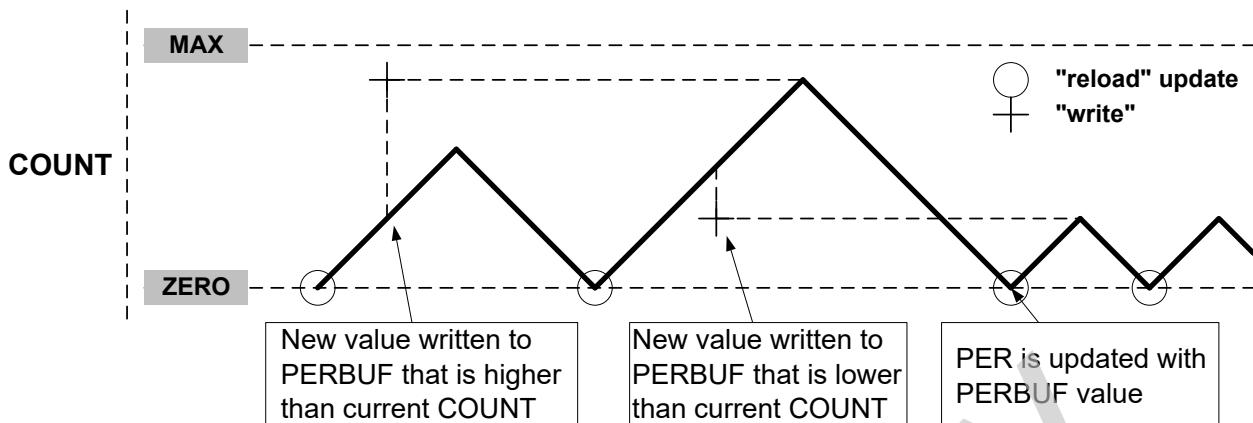
A counter wraparound can occur in any operation mode when up-counting without buffering, see [Figure 39-10](#). COUNT and TOP are continuously compared, so when a new value that is lower than the current COUNT is written to TOP, COUNT will wrap before a compare match.

Figure 39-12. Unbuffered Dual-Slope Operation



When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as shown in [Figure 39-13](#). This prevents wraparound and the generation of odd waveforms.

Figure 39-13. Changing the Period Using Buffering



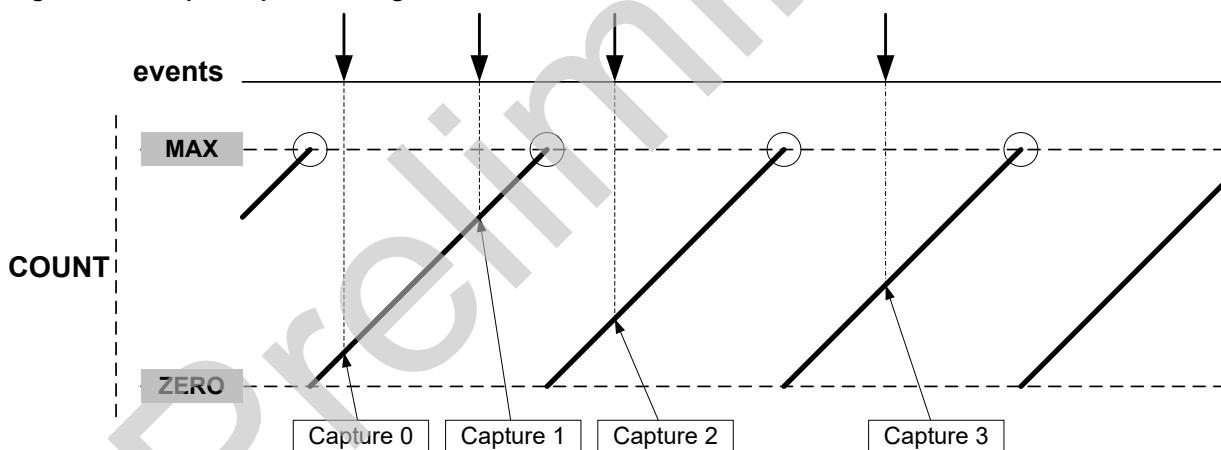
39.6.2.7 Capture Operations

To enable and use capture operations, the Match or Capture Channel x Event Input Enable bit in the Event Control register (EVCTRL.MCEIx) must be written to '1'. The capture channels to be used must also be enabled in the Capture Channel x Enable bit in the Control A register (CTRLA.CPTENx) before capturing can be performed.

Event Capture Action

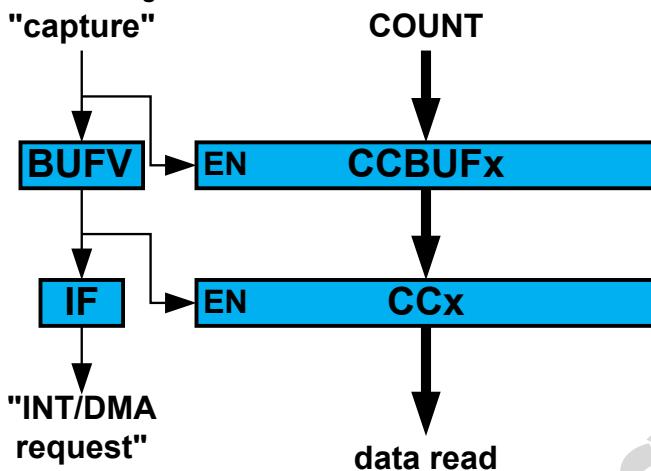
The compare/capture channels can be used as input capture channels to capture events from the Event System, and give them a timestamp. The following figure shows four capture events for one capture channel. Event system channels must be configured to operate in asynchronous mode when used for capture operations.

Figure 39-14. Input Capture Timing



For input capture, the Buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBUFx is transferred to CCx. The Buffer Valid flag is passed to set the CCx Interrupt flag (IF) and generate the optional interrupt, event, or DMA request. The CCBUFx register value cannot be read, all captured data must be read from the CCx register.

Figure 39-15. Capture Double Buffering



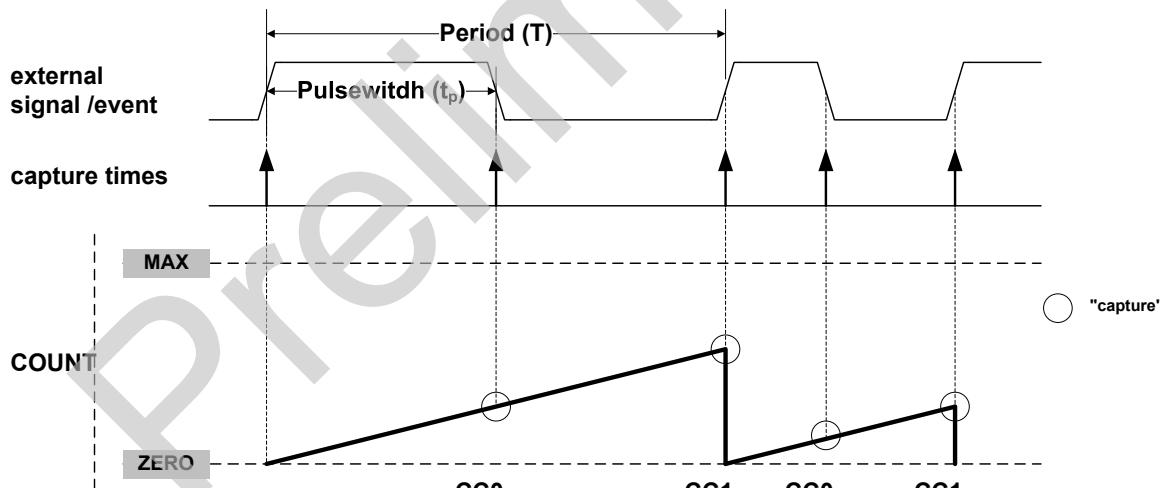
The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Buffer Valid flag (STATUS.CCBUFV) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Period and Pulse-Width (PPW) Capture Action

The TCC can perform two input captures and restart the counter on one of the edges. This enables the TCC to measure the pulse-width and period and to characterize the frequency f and *dutyCycle* of an input signal, as shown below:

$$f = \frac{1}{T} \quad , \quad \text{dutyCycle} = \frac{t_p}{T}$$

Figure 39-16. PWP Capture



Selecting PWP or PPW in the Timer/Counter Event Input 1 Action bit group in the Event Control register (EVCTRL.EVACT1) enables the TCC to perform one capture action on the rising edge and the other one on the falling edge. When using PPW event action, period T will be captured into CC0 and the pulse-width t_p into CC1. The PWP (Pulse-width and Period) event action offers the same functionality, but T will be captured into CC1 and t_p into CC0.

The Timer/Counter Event x Invert Enable bit in Event Control register (EVCTRL.TCEINVx) is used for event source x to select whether the wraparound should occur on the rising edge or the falling edge. If EVCTRL.TCEINVx=1, the wraparound will happen on the falling edge.

The corresponding capture is done only if the channel is enabled in Capture mode (CTRLA.CPTENx=1). If not, the capture action will be ignored and the channel will be enabled in compare mode of operation. When only one of these channel is required, the other channel can be used for other purposes.

The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the INTFLAG.MCx is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Note: When up-counting (CTRLBSET.DIR=0), counter values lower than 1 cannot be captured in Capture Minimum mode (FCTRLn.CAPTURE=CAPTMIN). To capture the full range including value 0, the TCC must be configured in Down-counting mode (CTRLBSET.DIR=0).

Note: In dual-slope PWM operation, and when TOP is lower than MAX/2, the CCx MSB captures the CTRLB.DIR state to identify the ramp on which the capture has been done. For rising ramps CCx[MSB] is zero, for falling ramps CCx[MSB]=1.

39.6.3 Additional Features

39.6.3.1 One-Shot Operation

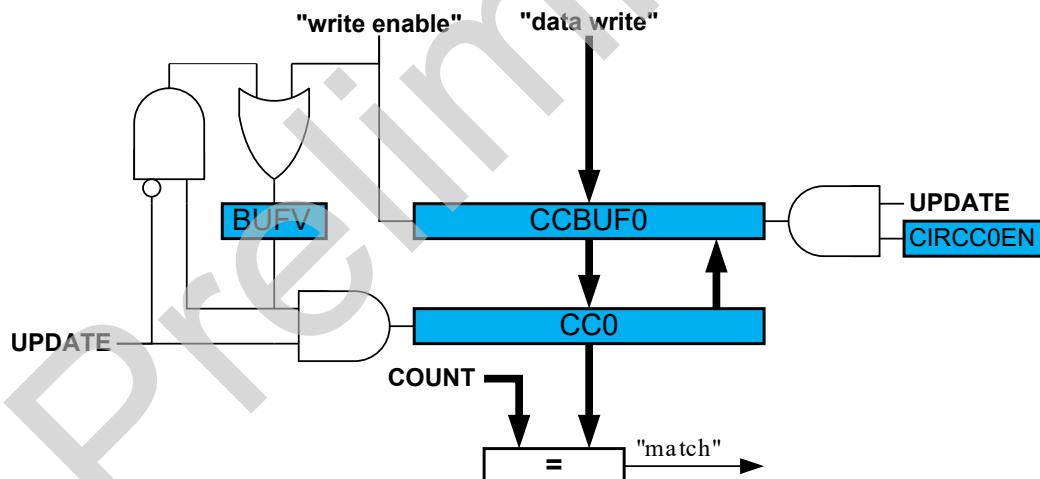
When one-shot is enabled, the counter automatically stops on the next Counter Overflow or Underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is set and the waveform outputs are set to the value defined by DRVCTRL.NREx and DRVCTRL.NRVx.

One-shot operation can be enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TCC will count until an overflow or underflow occurs and stop counting. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

39.6.3.2 Circular Buffer

The Period register (PER) and the Compare Channels register (CC0 to CC5) support circular buffer operation. When circular buffer operation is enabled, the PER or CCx values are copied into the corresponding buffer registers at each update condition. Circular buffering is dedicated to RAMP2, RAMP2A, and DS BOTH operations.

Figure 39-17. Circular Buffer on Channel 0



39.6.3.3 Dithering Operation

The TCC supports dithering on Pulse-width or Period on a 16, 32 or 64 PWM cycles frame.

Dithering consists in adding some extra clock cycles in a frame of several PWM cycles, and can improve the accuracy of the average output pulse width and period. The extra clock cycles are added on some of the compare match signals, one at a time, through a "blue noise" process that minimizes the flickering on the resulting dither patterns.

Dithering is enabled by writing the corresponding configuration in the Enhanced Resolution bits in CTRLA register (CTRLA.RESOLUTION):

- DITH4 enable dithering every 16 PWM frames
- DITH5 enable dithering every 32 PWM frames
- DITH6 enable dithering every 64 PWM frames

The DITHERCY bits of COUNT, PER and CCx define the number of extra cycles to add into the frame (DITHERCY bits from the respective COUNT, PER or CCx registers). The remaining bits of COUNT, PER, CCx define the compare value itself.

The pseudo code, giving the extra cycles insertion regarding the cycle is:

```
int extra_cycle(resolution, dithercy, cycle) {
    int MASK;
    int value;
    switch (resolution) {
        DITH4: MASK = 0x0f;
        DITH5: MASK = 0x1f;
        DITH6: MASK = 0x3f;
    }
    value = cycle * dithercy;
    if (((MASK & value) + dithercy) > MASK)
        return 1;
    return 0;
}
```

Dithering on Period

Writing DITHERCY in PER will lead to an average PWM period configured by the following formulas.

DITH4 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{16} + PER \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

Note: If DITH4 mode is enabled, the last 4 significant bits from PER/CCx or COUNT register correspond to the DITHERCY value, rest of the bits corresponds to PER/CCx or COUNT value.

DITH5 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{32} + PER \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

DITH6 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{64} + PER \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

Dithering on Pulse-Width

Writing DITHERCY in CCx will lead to an average PWM pulse width configured by the following formula.

DITH4 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{16} + CCx \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

DITH5 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{32} + CCx \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

DITH6 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{64} + CCx \right) \left(\frac{1}{f_{GCLK_TCCx}} \right)$$

Note: The PWM period will remain static in this case.

39.6.3.4 Ramp Operations

Three ramp operation modes are supported. All of them require the timer/counter running in single-slope PWM generation. The Ramp mode is selected by writing to the Ramp Mode bits in the Waveform Control register (WAVE.RAMP).

RAMP1 Operation

This is the default PWM operation, described in [Single-Slope PWM Generation](#).

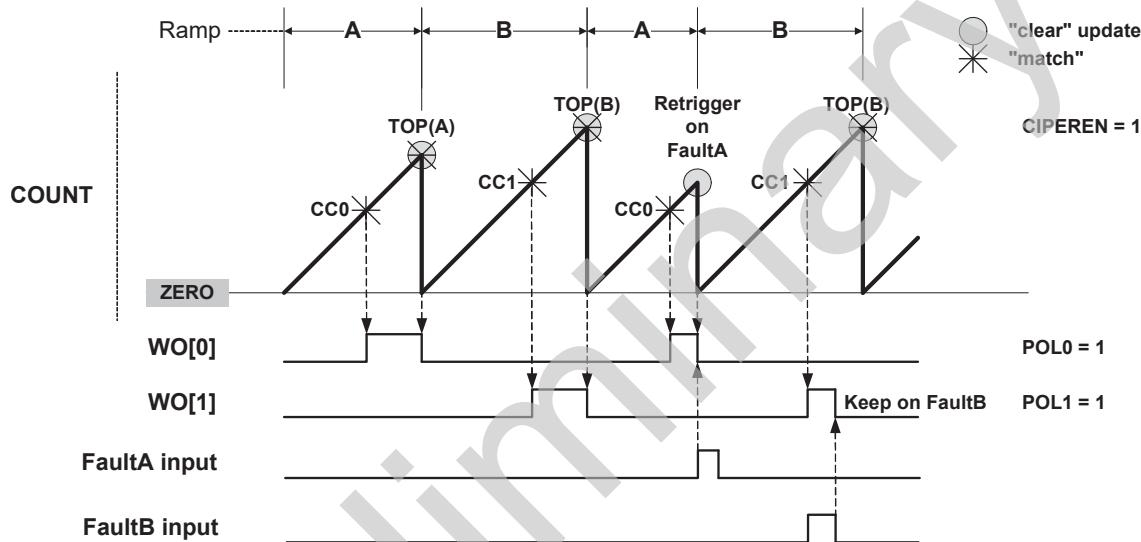
RAMP2 Operation

These operation modes are dedicated for power factor correction (PFC), Half-Bridge and Push-Pull SMPS topologies, where two consecutive timer/counter cycles are interleaved, see [Figure 39-18](#). In cycle A, odd channel output is disabled, and in cycle B, even channel output is disabled. The ramp index changes after each update, but can be software modified using the Ramp index command bits in Control B Set register (CTRLBSET.IDXCMD).

Standard RAMP2 (RAMP2) Operation

Ramp A and B periods are controlled by the PER register value. The PER value can be different on each ramp by the Circular Period buffer option in the Wave register (WAVE.CIPEREN=1). This mode uses a two-channel TCC to generate two output signals, or one output signal with another CC channel enabled in Capture mode.

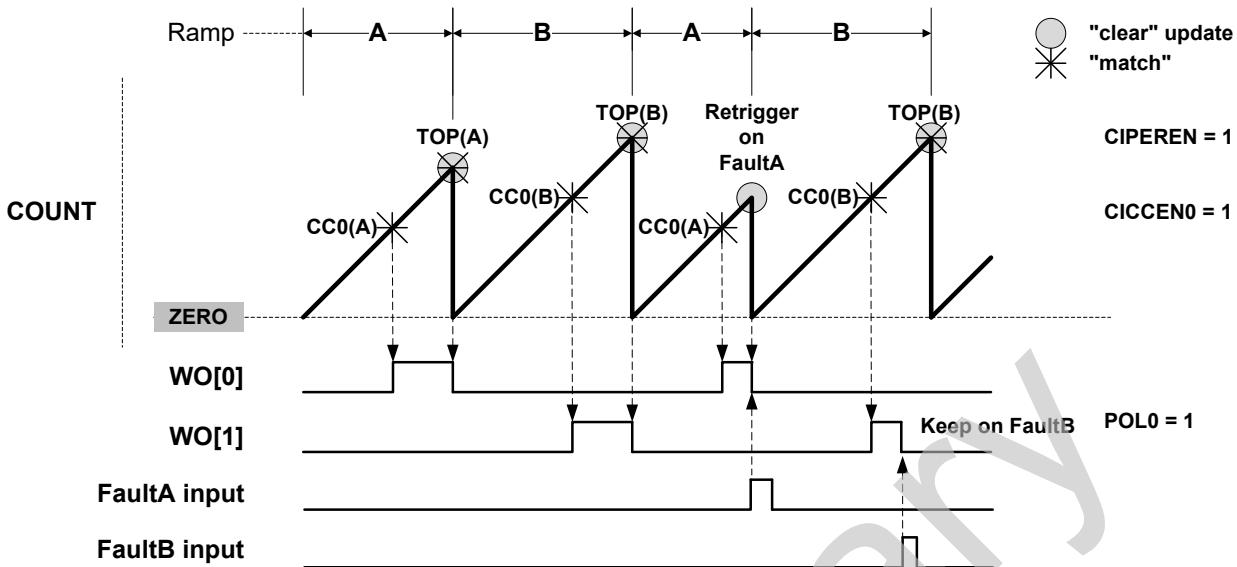
Figure 39-18. RAMP2 Standard Operation



Alternate RAMP2 (RAMP2A) Operation

Alternate RAMP2 operation is similar to RAMP2, but CC0 controls both WO[0] and WO[1] waveforms when the corresponding circular buffer option is enabled (CIPEREN=1). The waveform polarity is the same on both outputs. Channel 1 can be used in capture mode.

Figure 39-19. RAMP2 Alternate Operation



Critical RAMP2 (RAMP2C) Operation

Critical RAMP2 operation provides a way to cover RAMP2 operation requirements without the update constraint associated with the use of circular buffers. In this mode, CC0 is controlling the period of ramp A and PER is controlling the period of ramp B. When using more than two channels, WO[0] output is controlled by CC2 (HIGH) and CC0 (LOW). On TCC with 2 channels, a pulse on WO[0] will last the entire period of ramp A, if WAVE.POL0=0.

Figure 39-20. RAMP2 Critical Operation With More Than 2 Channels

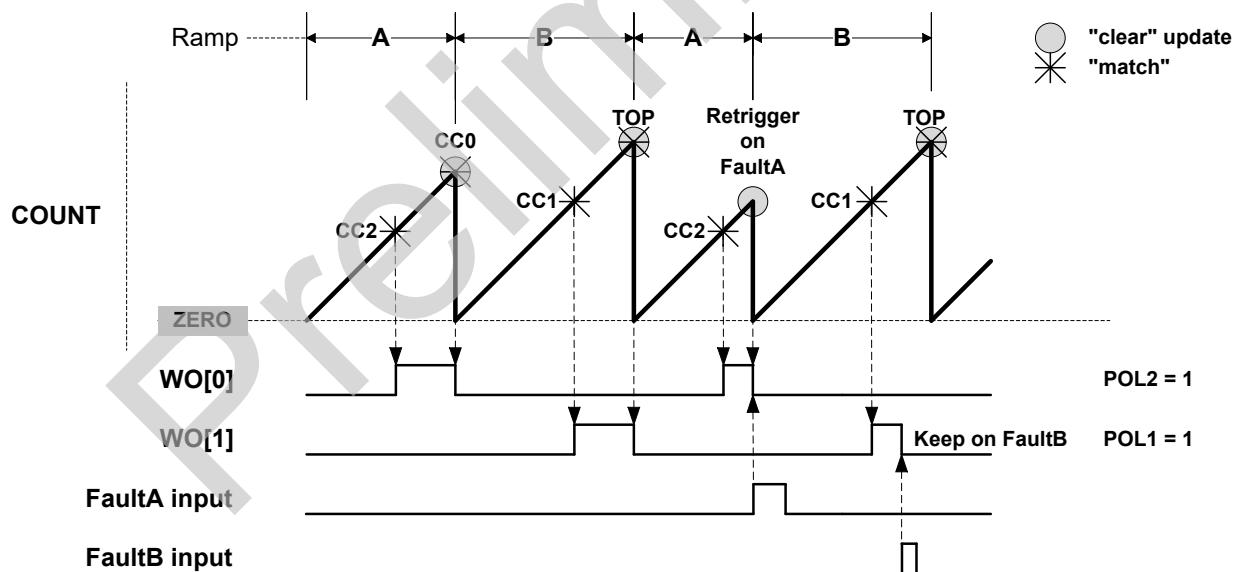
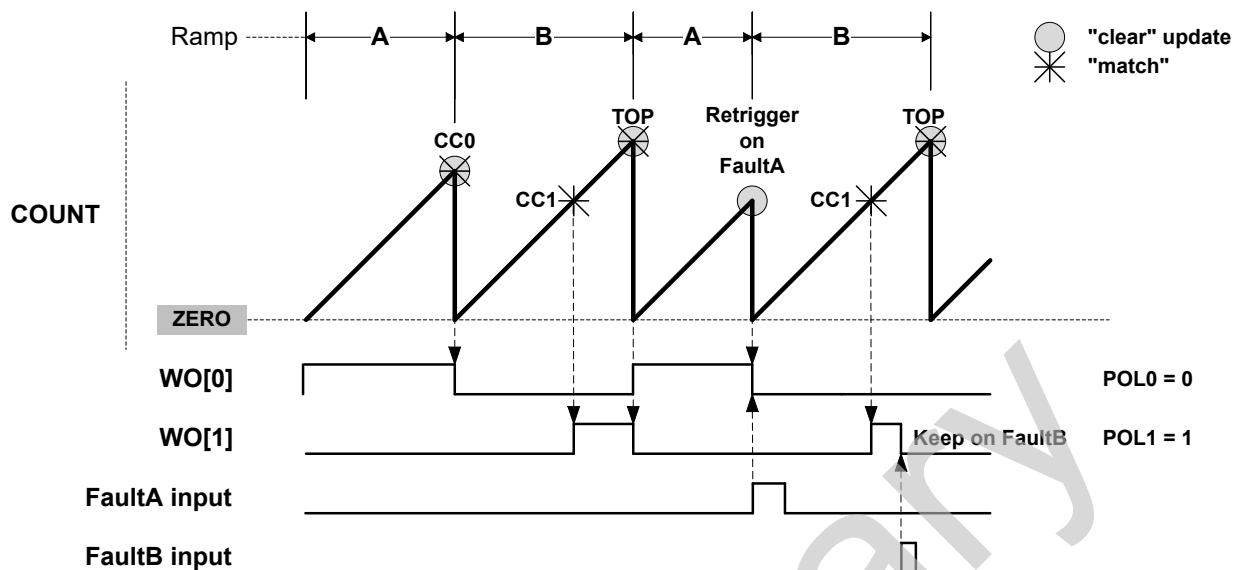


Figure 39-21. RAMP2 Critical Operation With 2 Channels



39.6.3.5 Recoverable Faults

Recoverable faults can restart or halt the timer/counter. Two faults, called Fault A and Fault B, can trigger recoverable fault actions on the compare channels CC0 and CC1 of the TCC. The compare channels' outputs can be clamped to inactive state either as long as the fault condition is present, or from the first valid fault condition detection on until the end of the timer/counter cycle.

Fault Inputs

The first two channel input events (TCCxMC0 and TCCxMC1) can be used as Fault A and Fault B inputs, respectively. Event system channels connected to these fault inputs must be configured as asynchronous. The TCC must work in a PWM mode.

Fault Filtering

There are three filters available for each input Fault A and Fault B. They are configured by the corresponding Recoverable Fault n Configuration registers (FCTRLA and FCTRLB). The three filters can either be used independently or in any combination.

Input Filtering By default, the event detection is asynchronous. When the event occurs, the fault system will immediately and asynchronously perform the selected fault action on the compare channel output, also in device power modes where the clock is not available. To avoid false fault detection on external events (e.g. due to a glitch on an I/O port) a digital filter can be enabled and configured by the Fault B Filter Value bits in the Fault n Configuration registers (FCTRLn.FILTERVAL). If the event width is less than FILTERVAL (in clock cycles), the event will be discarded. A valid event will be delayed by FILTERVAL clock cycles.

Fault Blanking This ignores any fault input for a certain time just after a selected waveform output edge. This can be used to prevent false fault triggering due to signal bouncing, as shown in the figure below. Blanking can be enabled by writing an edge triggering configuration to the Fault n Blanking Mode bits in the Recoverable Fault n Configuration register (FCTRLn.BLANK). The desired duration of the blanking must be written to the Fault n Blanking Time bits (FCTRLn.BLANKVAL). The blanking time t_b is calculated by

$$t_b = \frac{1 + \text{BLANKVAL}}{f_{\text{GCLK_TCCx_PRESC}}}$$

Here, $f_{\text{GCLK_TCCx_PRESC}}$ is the frequency of the prescaled peripheral clock frequency $f_{\text{GCLK_TCCx}}$.

The prescaler is enabled by writing '1' to the Fault n Blanking Prescaler bit (FCTRLn.BLANKPRES). When disabled, $f_{\text{GCLK_TCCx_PRESC}} = f_{\text{GCLK_TCCx}}$. When enabled, $f_{\text{GCLK_TCCx_PRESC}} = f_{\text{GCLK_TCCx}}/64$.

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The maximum blanking time (FCTRLn.BLANKVAL=255) at $f_{GCLK_TCCx}=96MHz$ is $2.67\mu s$ (no prescaler) or $170\mu s$ (prescaling). For $f_{GCLK_TCCx}=1MHz$, the maximum blanking time is either $170\mu s$ (no prescaling) or $10.9ms$ (prescaling enabled).

Figure 39-22. Fault Blanking in RAMP1 Operation with Inverted Polarity

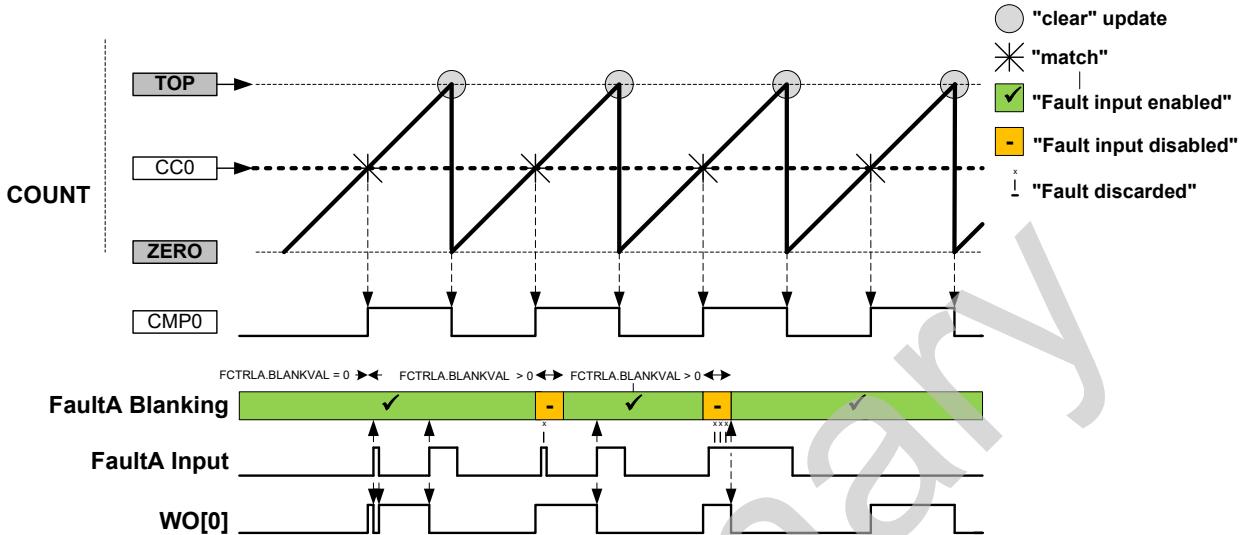


Figure 39-23. Fault Qualification in RAMP1 Operation

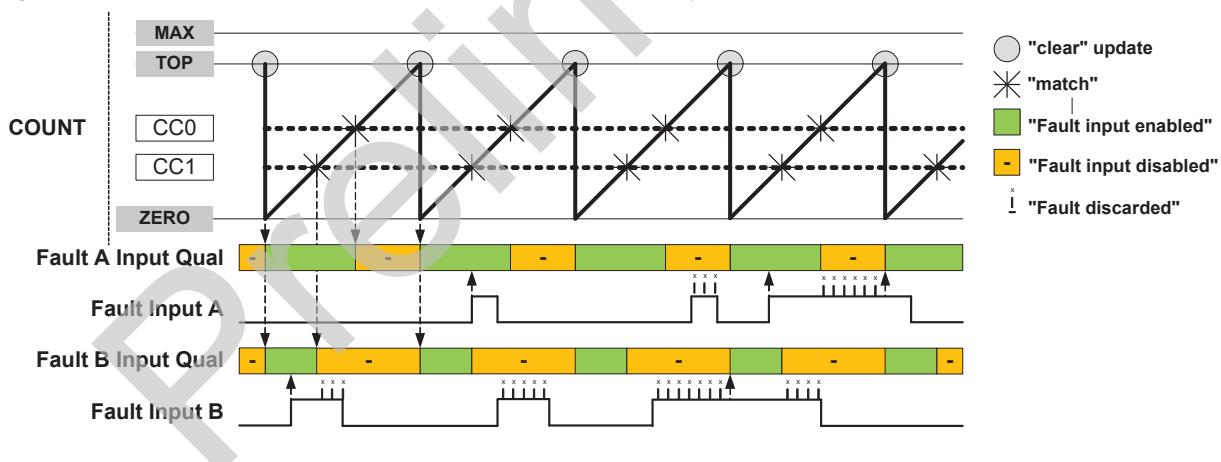
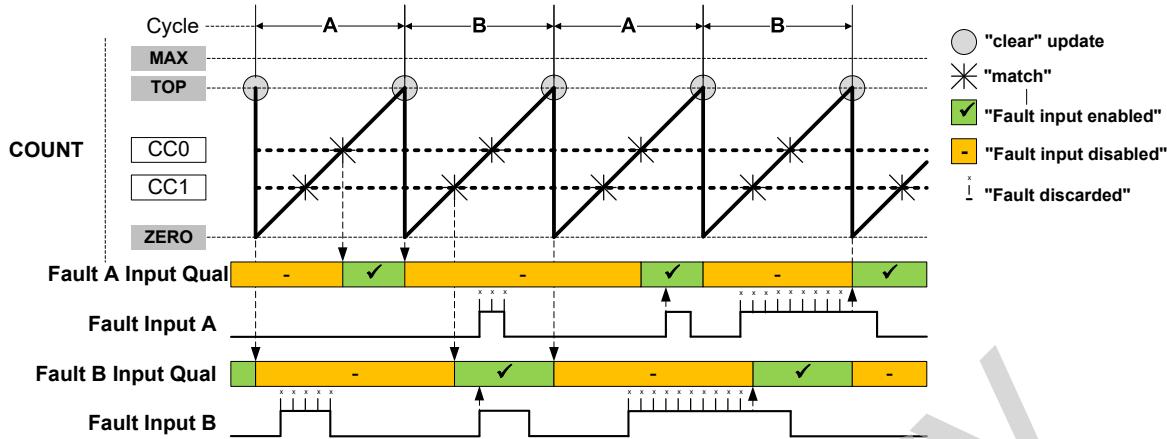


Figure 39-24. Fault Qualification in RAMP2 Operation with Inverted Polarity

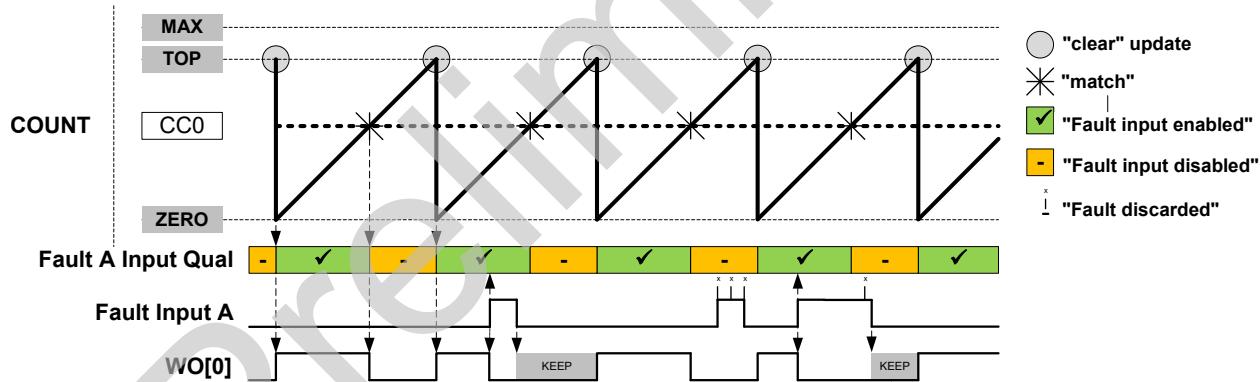


Fault Actions

Different fault actions can be configured individually for Fault A and Fault B. Most fault actions are not mutually exclusive; hence two or more actions can be enabled at the same time to achieve a result that is a combination of fault actions.

- | | |
|--------------------|---|
| Keep Action | This is enabled by writing the Fault n Keeper bit in the Recoverable Fault n Configuration register (FCTRLn.KEEP) to '1'. When enabled, the corresponding channel output will be clamped to zero as long as the fault condition is present. The clamp will be released on the start of the first cycle after the fault condition is no longer present, see next Figure. |
|--------------------|---|

Figure 39-25. Waveform Generation with Fault Qualification and Keep Action



- | | |
|-----------------------|--|
| Restart Action | This is enabled by writing the Fault n Restart bit in Recoverable Fault n Configuration register (FCTRLn.RESTART) to '1'. When enabled, the timer/counter will be restarted as soon as the corresponding fault condition is present. The ongoing cycle is stopped and the timer/counter starts a new cycle, see Figure 39-26 . In Ramp 1 mode, when the new cycle starts, the compare outputs will be clamped to inactive level as long as the fault condition is present. |
|-----------------------|--|

Note: For RAMP2 operation, when a new timer/counter cycle starts the cycle index will change automatically, see [Figure 39-27](#). Fault A and Fault B are qualified only during the cycle A and cycle B respectively: Fault A is disabled during cycle B, and Fault B is disabled during cycle A.

Figure 39-26. Waveform Generation in RAMP1 mode with Restart Action

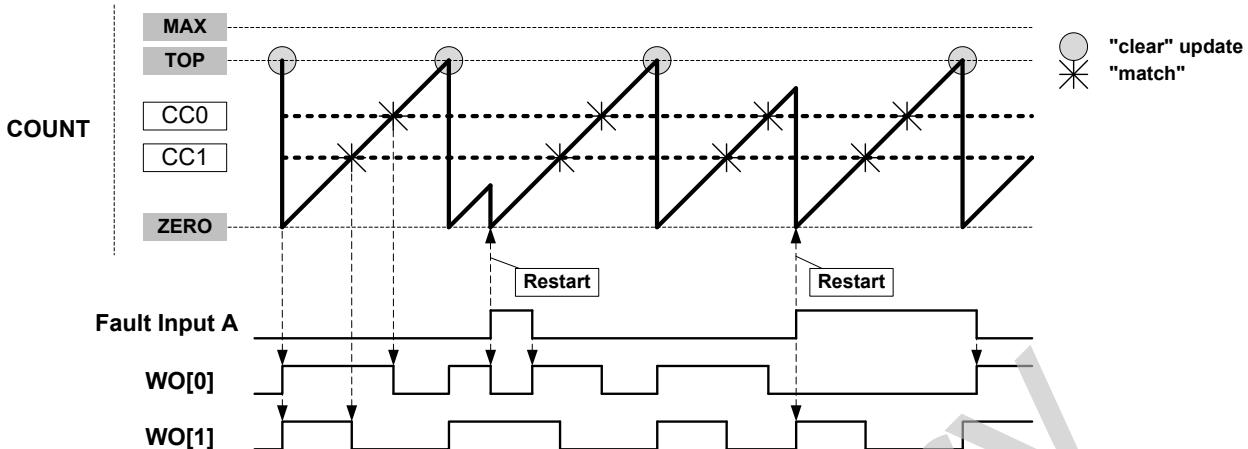
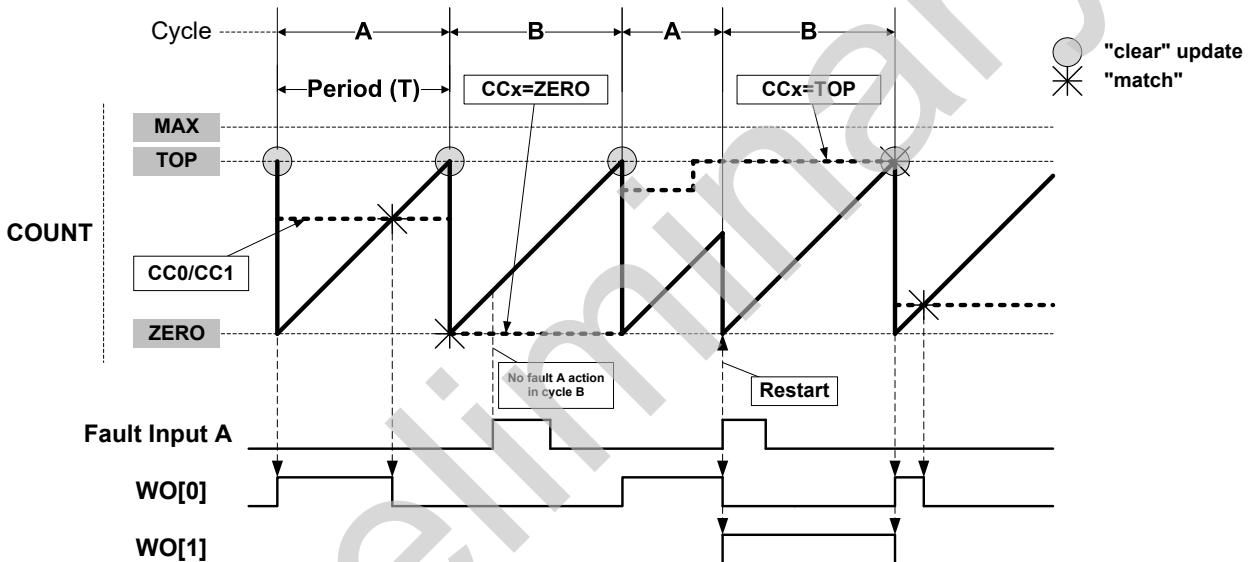


Figure 39-27. Waveform Generation in RAMP2 mode with Restart Action



Capture Action Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT - the equivalent to a standard capture operation, for further details refer to [39.6.2.7. Capture Operations](#)
- CAPTMIN - gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued.
- CAPTMAX - gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued, see [Figure 39-28](#).
- LOCMIN - notifies by event or interrupt when a local minimum captured value is detected.
- LOCMAX - notifies by event or interrupt when a local maximum captured value is detected.
- DERIV0 - notifies by event or interrupt when a local extreme captured value is detected, see [Figure 39-29](#).

CCx Content:

In CAPTMIN and CAPTMAX operations, CCx keeps the respective extremum captured values, see [Figure 39-28](#). In LOCMIN, LOCMAX or DERIV0 operation, CCx follows the counter value at fault time, see [Figure 39-29](#).

Before enabling CAPTMIN or CAPTMAX mode of capture, the user must initialize the corresponding CCx register value to a value different from zero (for CAPTMIN) top (for CAPTMAX). If the CCx register initial value is zero (for CAPTMIN) top (for CAPTMAX), no captures will be performed using the corresponding channel.

MCx Behaviour:

In LOCMIN and LOCMAX operation, capture is performed on each capture event. The MCx interrupt flag is set only when the captured value is above or equal (for LOCMIN) or below or equal (for LOCMAX) to the previous captured value. So interrupt flag is set when a new relative local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected. DERIV0 is equivalent to an OR function of (LOCMIN, LOCMAX).

In CAPT operation, capture is performed on each capture event. The MCx interrupt flag is set on each new capture.

In CAPTMIN and CAPTMAX operation, capture is performed only when on capture event time, the counter value is lower (for CAPTMIN) or higher (for CAPTMAX) than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is higher or equal (for CAPTMIN) or lower or equal (for CAPTMAX) to the value captured on the previous event. So interrupt flag is set when a new absolute local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected.

Interrupt Generation

In CAPT mode, an interrupt is generated on each filtered Fault n and each dedicated CCx channel capture counter value. In other modes, an interrupt is only generated on an extreme captured value.

Figure 39-28. Capture Action “CAPTMAX”

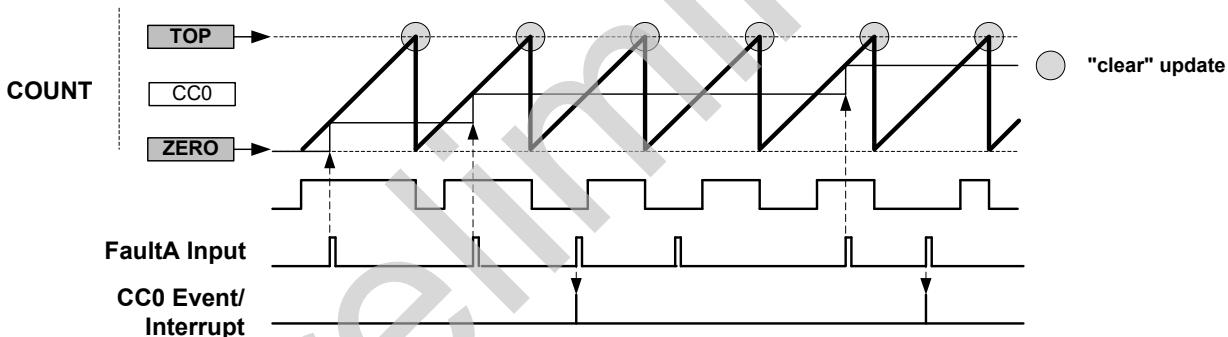
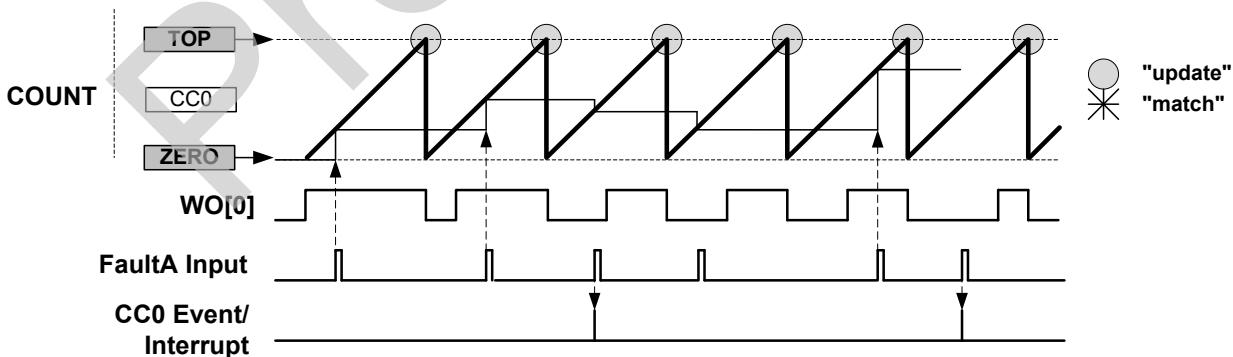


Figure 39-29. Capture Action “DERIV0”



- Hardware Halt Action** This is configured by writing 0x1 to the Fault n Halt mode bits in the Recoverable Fault n Configuration register (FCTRLn.HALT). When enabled, the timer/counter is halted and the cycle is extended as long as the corresponding fault is present.

The next figure ('Waveform Generation with Halt and Restart Actions') shows an example where both restart action and hardware halt action are enabled for Fault A. The compare channel 0 output

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is clamped to inactive level as long as the timer/counter is halted. The timer/counter resumes the counting operation as soon as the fault condition is no longer present. As the restart action is enabled in this example, the timer/counter is restarted after the fault condition is no longer present.

The figure after that ('Waveform Generation with Fault Qualification, Halt, and Restart Actions') shows a similar example, but with additionally enabled fault qualification. Here, counting is resumed after the fault condition is no longer present.

Note that in RAMP2 and RAMP2A operations, when a new timer/counter cycle starts, the cycle index will automatically change.

Figure 39-30. Waveform Generation with Halt and Restart Actions

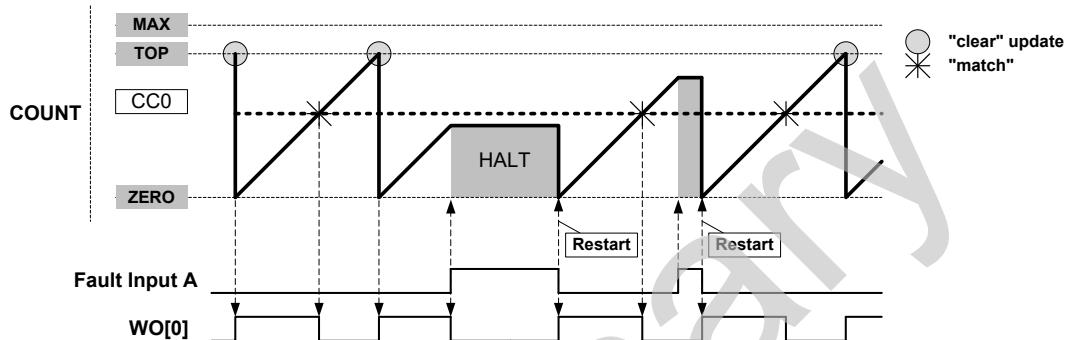
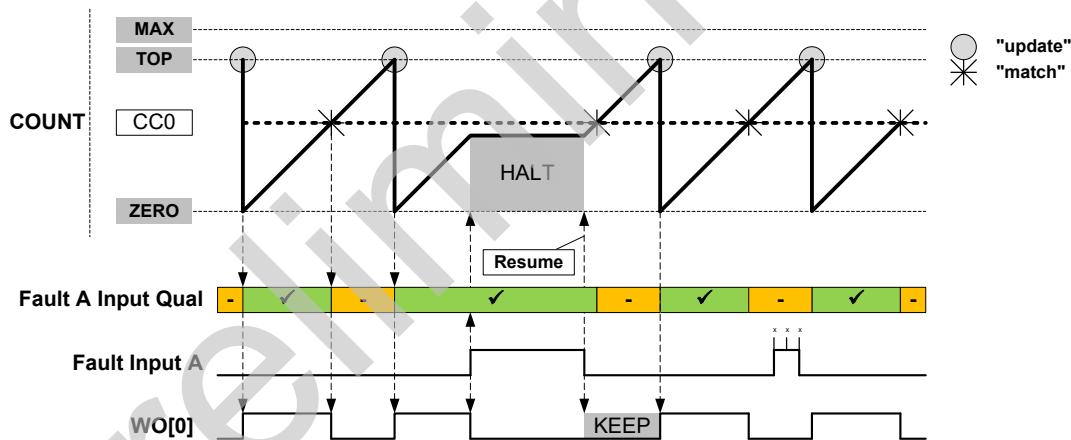


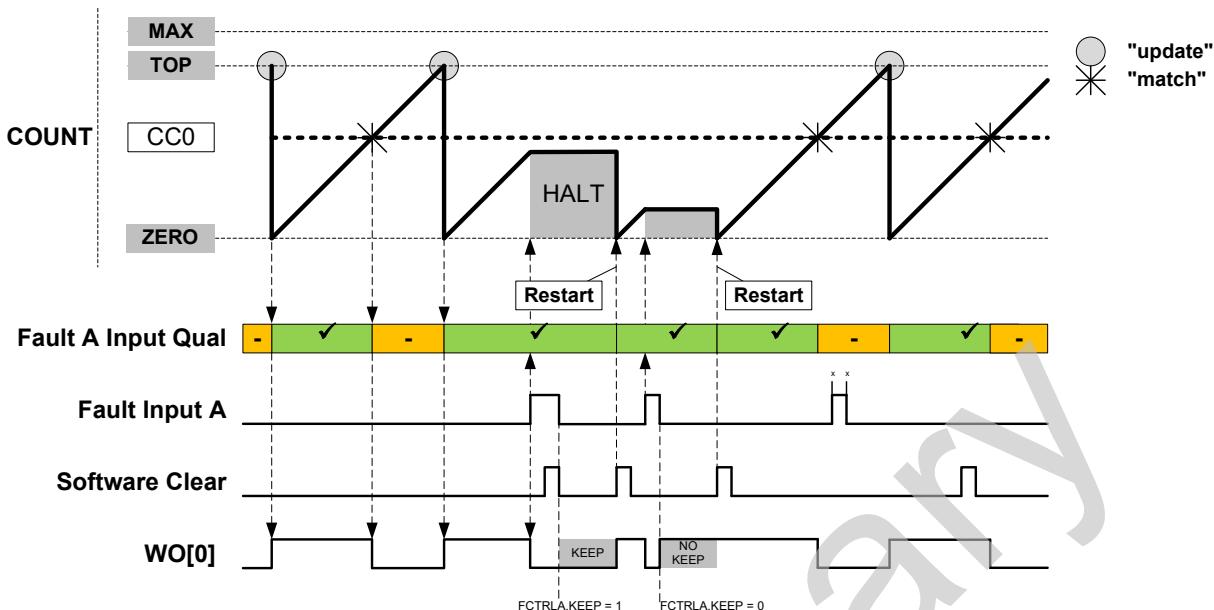
Figure 39-31. Waveform Generation with Fault Qualification, Halt, and Restart Actions



Software Halt Action

This is configured by writing 0x2 to the Fault n Halt mode bits in the Recoverable Fault n configuration register (FCTRLn.HALT). Software halt action is similar to hardware halt action, but in order to restart the timer/counter, the corresponding fault condition must not be present anymore, and the corresponding FAULT n bit in the STATUS register must be cleared by software.

Figure 39-32. Waveform Generation with Software Halt, Fault Qualification, Keep and Restart Actions



39.6.3.6 Non-Recoverable Faults

The non-recoverable fault action will force all the compare outputs to a pre-defined level programmed into the Driver Control register (DRVCTRL.NRE and DRVCTRL.NRV). The non-recoverable fault input (EV0 and EV1) actions are enabled in Event Control register (EVCTRL.EVACT0 and EVCTRL.EVACT1).

To avoid false fault detection on external events (e.g. a glitch on an I/O port) a digital filter can be enabled using Non-Recoverable Fault Input x Filter Value bits in the Driver Control register (DRVCTRL.FILTERVALn). Therefore, the event detection is synchronous, and event action is delayed by the selected digital filter value clock cycles.

When the Fault Detection on Debug Break Detection bit in Debug Control register (DGBCTRL.FDDBD) is written to '1', a non-recoverable Debug Faults State and an interrupt (DFS) is generated when the system goes in debug operation.

In RAMP2, RAMP2A, or DS BOTH operation, when the Lock Update bit in the Control B register is set by writing CTRLBSET.LUPD=1 and the ramp index or counter direction changes, a non-recoverable Update Fault State and the respective interrupt (UFS) are generated.

39.6.3.7 Time-Stamp Capture

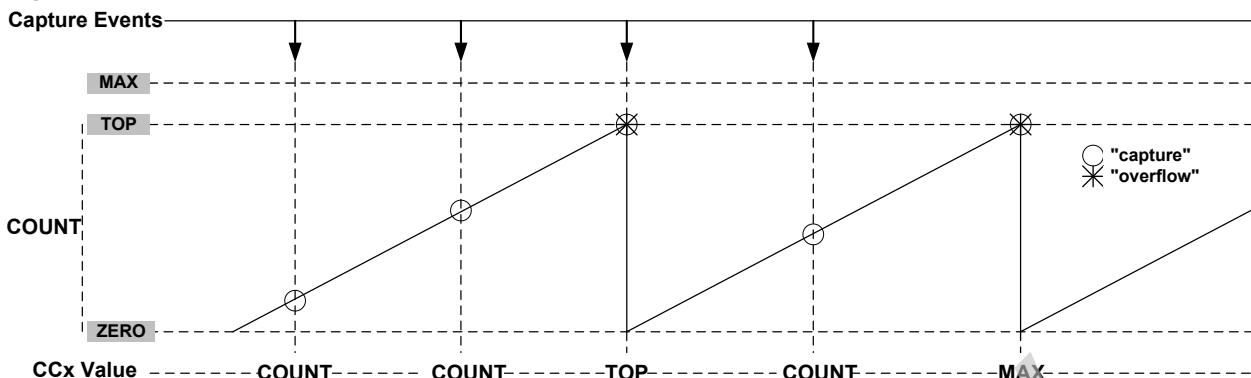
This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. In case of an overflow, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new time-stamp will not be stored and INTFLAG.ERR will be set.

Figure 39-33. Time-Stamp



39.6.3.8 Waveform Extension

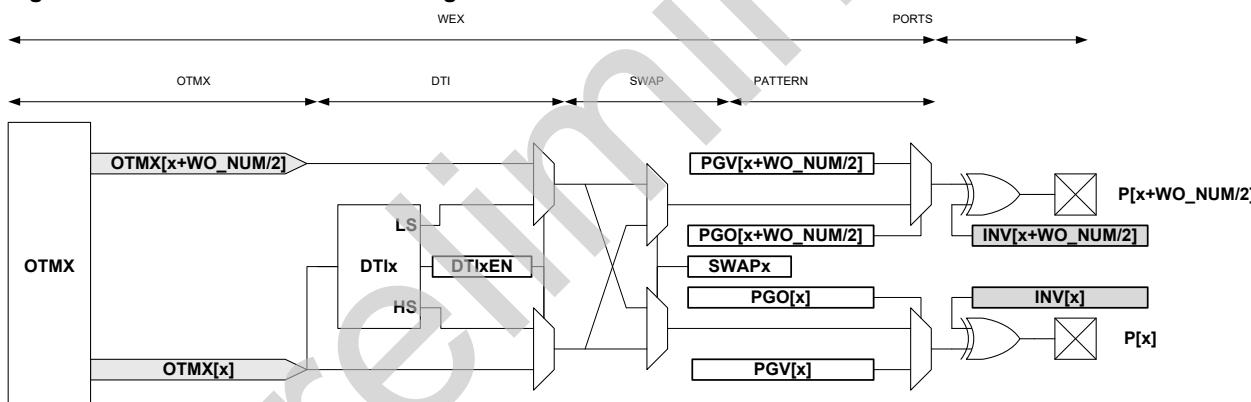
Figure 39-34 shows a schematic diagram of actions of the four optional units that follow the recoverable fault stage on a port pin pair: Output Matrix (OTMX), Dead-Time Insertion (DTI), SWAP and Pattern Generation. The DTI and SWAP units can be seen as a four port pair slices:

- Slice 0 DTI0 / SWAP0 acting on port pins ($WO[0]$, $WO[WO_NUM/2 + 0]$)
- Slice 1 DTI1 / SWAP1 acting on port pins ($WO[1]$, $WO[WO_NUM/2 + 1]$)

And generally:

- Slice n DTIx / SWAPx acting on port pins ($WO[x]$, $WO[WO_NUM/2 + x]$)

Figure 39-34. Waveform Extension Stage Details



The **output matrix (OTMX)** unit distributes compare channels, according to the selectable configurations in the following table.

Table 39-6. Output Matrix Channel Pin Routing Configuration

Value	OTMX[7]	OTMX[6]	OTMX[5]	OTMX[4]	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC1	CC0	CC5	CC4	CC3	CC2	CC1	CC0
0x1	CC1	CC0	CC2	CC1	CC0	CC2	CC1	CC0
0x2	CC0							
0x3	CC1	CC0						

- Configuration 0x0 is the default configuration. The channel location is the default one and channels are distributed on outputs modulo the number of channels. Channel 0 is routed to the Output matrix output OTMX[0], and Channel 1 to OTMX[1]. If there are more outputs than channels, then channel 0 is duplicated to the Output matrix output OTMX[CC_NUM], channel 1 to OTMX[CC_NUM+1] and so on.

- Configuration 0x1 distributes the channels on output modulo half the number of channels. This assigns twice the number of output locations to the lower channels than the default configuration. This can be used, for example, to control the four transistors of a full bridge using only two compare channels.
- Using pattern generation, some of these four outputs can be overwritten by a constant level, enabling flexible drive of a full bridge in all quadrant configurations.
- Configuration 0x2 distributes compare channel 0 (CC0) to all port pins. With pattern generation, this configuration can control a stepper motor.
- Configuration 0x3 distributes the compare channel CC0 to the first output, and the channel CC1 to all other outputs. Together with pattern generation and the fault extension, this configuration can control up to seven LED strings, with a boost stage.

The table below is an example showing four compare channels on four outputs.

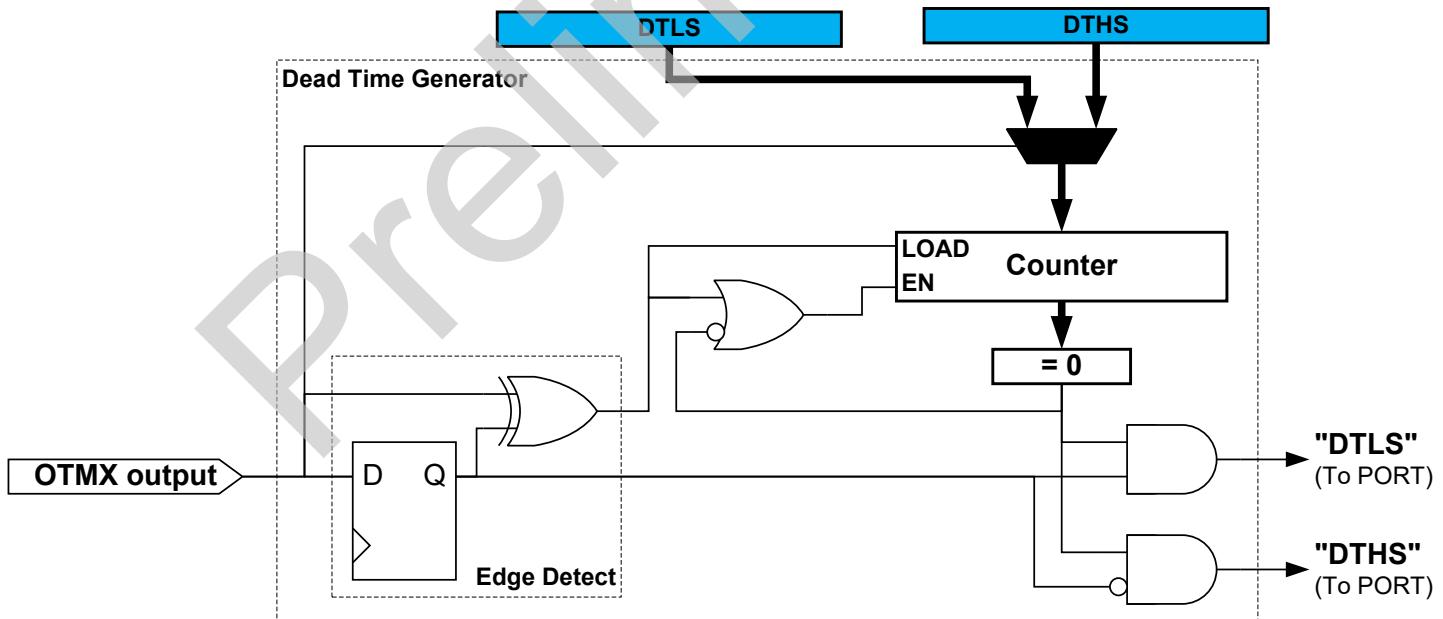
Table 39-7. Four Compare Channels on Four Outputs

Value	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC3	CC2	CC1	CC0
0x1	CC1	CC0	CC1	CC0
0x2	CC0	CC0	CC0	CC0
0x3	CC1	CC1	CC1	CC0

The dead-time insertion (DTI) unit generates OFF time with the non-inverted low side (LS) and inverted high side (HS) of the wave generator output forced at low level. This OFF time is called dead time. Dead-time insertion ensures that the LS and HS will never switch simultaneously.

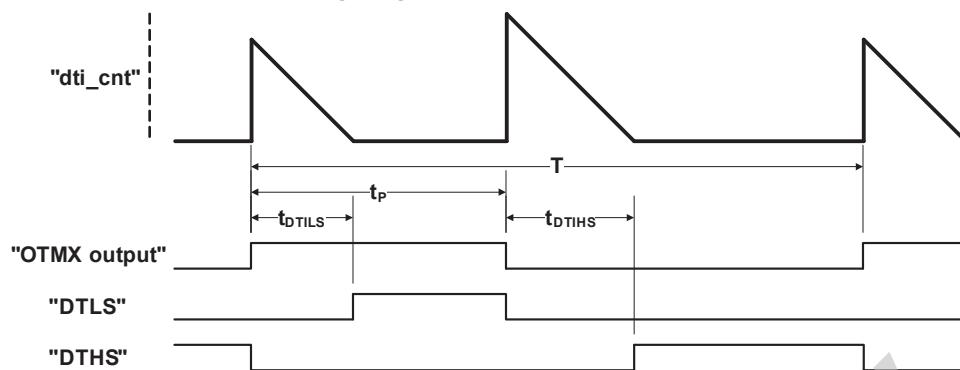
The DTI stage consists of four equal dead-time insertion generators; one for each of the first four compare channels. [Figure 39-35](#) shows the block diagram of one DTI generator. The four channels have a common register which controls the dead time, which is independent of high side and low side setting.

Figure 39-35. Dead-Time Generator Block Diagram



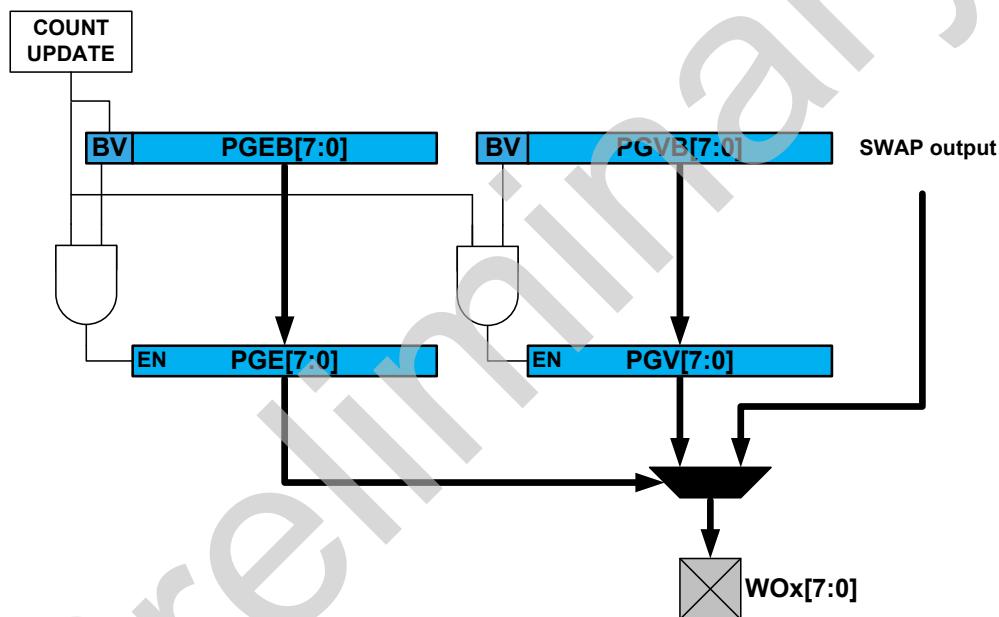
As shown in [Figure 39-36](#), the 8-bit dead-time counter is decremented by one for each peripheral clock cycle until it reaches zero. A non-zero counter value will force both the low side and high side outputs into their OFF state. When the output matrix (OTMX) output changes, the dead-time counter is reloaded according to the edge of the input. When the output changes from low to high (positive edge) it initiates a counter reload of the DTLS register. When the output changes from high to low (negative edge) it reloads the DTHS register.

Figure 39-36. Dead-Time Generator Timing Diagram



The pattern generator unit produces a synchronized bit pattern across the port pins it is connected to. The pattern generation features are primarily intended for handling the commutation sequence in brushless DC motors (BLDC), stepper motors, and full bridge control. See also [Figure 39-37](#).

Figure 39-37. Pattern Generator Block Diagram



As with other double-buffered timer/counter registers, the register update is synchronized to the UPDATE condition set by the timer/counter waveform generation operation. If synchronization is not required by the application, the software can simply access directly the PATT.PGE, PATT.PGV bits registers.

39.6.4 Master/Slave Operation

Two or more TCC instances sharing the same GCLK_TCCx clock, can be linked to provide more synchronized CC channels. The operation is enabled by setting the Master Synchronization bit in Control A register (CTRLA.MSYNC) in the Slave instance. When the bit is set, the slave TCC instance will synchronize the CC channels to the Master counter.

Related Links

[39.8.1. CTRLA](#)

39.6.5 DMA, Interrupts, and Events

Table 39-8. Module Requests for TCC

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Overflow / Underflow	Yes	Yes		Yes ⁽¹⁾	On DMA acknowledge
Channel Compare Match or Capture	Yes	Yes	Yes ⁽²⁾	Yes ⁽³⁾	For circular buffering: on DMA acknowledge For capture channel: when CCx register is read
Retrigger	Yes	Yes			
Count	Yes	Yes			
Capture Overflow Error	Yes				
Debug Fault State	Yes				
Recoverable Faults	Yes				
Non-Recoverable Faults	Yes				
TCCx Event 0 input				Yes ⁽⁴⁾	
TCCx Event 1 input				Yes ⁽⁵⁾	

Notes:

1. DMA request set on Overflow, Underflow or Re-trigger conditions.
2. Can perform capture or generate recoverable fault on an event input.
3. In Capture or Circular modes.
4. On event input, either action can be executed:
 - re-trigger counter
 - control counter direction
 - stop the counter
 - decrement the counter
 - perform period and pulse width capture
 - generate non-recoverable fault
5. On event input, either action can be executed:
 - re-trigger counter
 - increment or decrement counter depending on direction
 - start the counter
 - increment or decrement counter based on direction
 - increment counter regardless of direction
 - generate non-recoverable fault

39.6.5.1 DMA Operation

The TCC can generate the following DMA requests:

Counter overflow (OVF)	If the One-shot Trigger mode in the control A register (CTRLA.DMAOS) is written to '0', the TCC generates a DMA request on each cycle when an update condition (Overflow, Underflow or Re-trigger) is detected. When an update condition (Overflow, Underflow or Re-trigger) is detected while CTRLA.DMAOS=1, the TCC generates a DMA trigger on the cycle following the DMA One-Shot Command written to the Control B register (CTRLBSET.CMD=DMAOS).
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In both cases, the request is cleared by hardware on DMA acknowledge.

Channel Match (MCx)	A DMA request is set only on a compare match if CTRLA.DMAOS=0. The request is cleared by hardware on DMA acknowledge. When CTRLA.DMAOS=1, the DMA requests are not generated.
Channel Capture (MCx)	For a capture channel, the request is set when valid data is present in the CCx register, and cleared once the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.

DMA Operation with Circular Buffer

When circular buffer operation is enabled, the Buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.

Note: Circular buffer are intended to be used with RAMP2, RAMP2A and DS BOTH operation only.

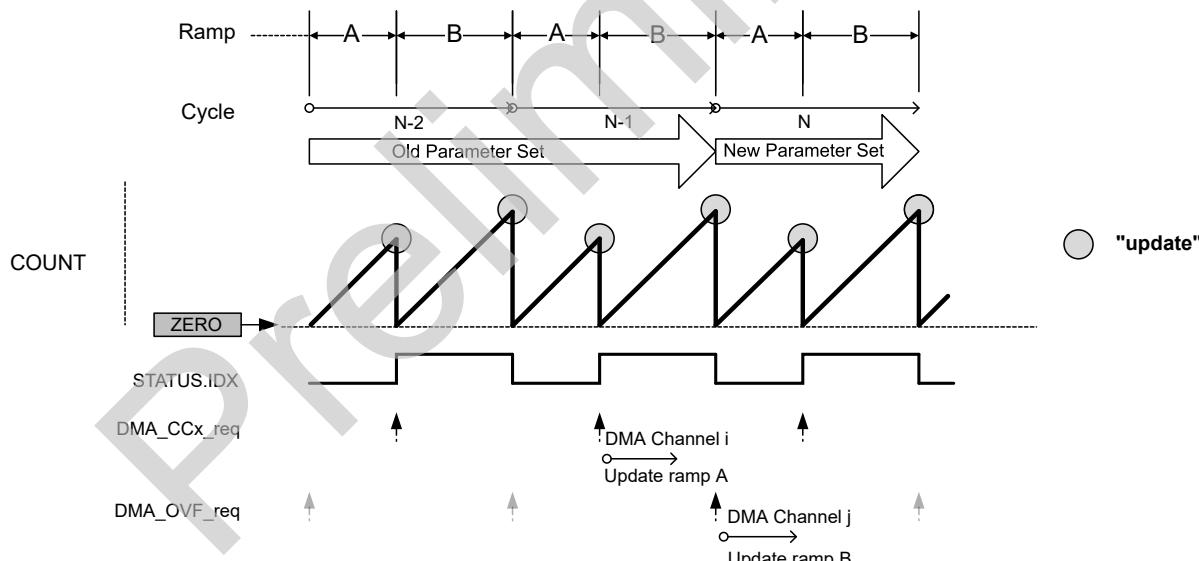
DMA Operation with Circular Buffer in RAMP2 and RAMP2A Mode

When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on a MC trigger. The update of all circular buffer values for ramp B, can be done through a second DMA channel triggered by the overflow DMA request.

Figure 39-38. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled



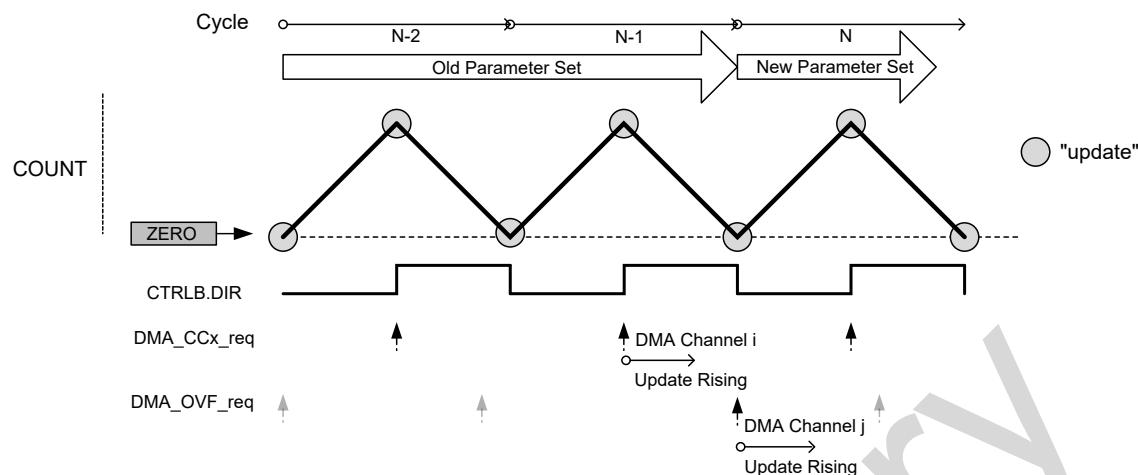
DMA Operation with Circular Buffer in DS BOTH Mode

When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of up-counting phase with an effective DMA transfer on previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

Figure 39-39. DMA Triggers in DSBOTH Operation Mode and Circular Buffer Enabled



39.6.5.2 Interrupts

The TCC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Retrigger (TRG)
- Count (CNT) - refer also to description of EVCTRL.CNTSEL.
- Capture Overflow Error (ERR)
- Non-Recoverable Update Fault (UFS)
- Debug Fault State (DFS)
- Recoverable Faults (FAULTn)
- Non-recoverable Faults (FAULTx)
- Compare Match or Capture Channels (MCx)

These interrupts are asynchronous wake-up sources.

Each interrupt source has an Interrupt flag associated with it. The Interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the Interrupt flag is cleared, the interrupt is disabled, or the TCC is reset. See *INTFLAG* from Related Links for details on how to clear Interrupt flags. The TCC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which Interrupt condition is present.

Interrupts must be globally enabled for interrupt requests to be generated. See *Nested Vector Interrupt Controller* from Related Links.

Related Links

[9.2. Nested Vector Interrupt Controller \(NVIC\)](#)

[39.8.12. INTFLAG](#)

39.6.5.3 Events

The TCC can generate the following output events:

- Overflow/Underflow (OVF)
- Trigger (TRG)
- Counter (CNT) For further details, refer to EVCTRL.CNTSEL description.

- Compare Match or Capture on compare/capture channels: MCx

Writing a '1' ('0') to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables (disables) the corresponding output event. See *Event System (EVSYS)* from Related Links.

The TCC can take the following actions on a channel input event (MCx):

- Capture event
- Generate a recoverable or non-recoverable fault

The TCC can take the following actions on counter Event 1 (TCCx EV1):

- Counter re-trigger
- Counter direction control
- Stop the counter
- Decrement the counter on event
- Period and pulse width capture
- Non-recoverable fault

The TCC can take the following actions on counter Event 0 (TCCx EV0):

- Counter re-trigger
- Count on event (increment or decrement, depending on counter direction)
- Counter start - start counting on the event rising edge. Further events will not restart the counter; the counter will keep on counting using prescaled GCLK_TCCx, until it reaches TOP or ZERO, depending on the direction.
- Counter increment on event. This will increment the counter, irrespective of the counter direction.
- Count during active state of an asynchronous event (increment or decrement, depending on counter direction). In this case, the counter will be incremented or decremented on each cycle of the prescaled clock, as long as the event is active.
- Non-recoverable fault

The counter Event Actions are available in the Event Control registers (EVCTRL.EVACT0 and EVCTRL.EVACT1). See *EVCTRL* from related links.

Writing a '1' ('0') to an Event Input bit in the Event Control register (EVCTRL.MCEIx or EVCTRL.TCEIx) enables (disables) the corresponding action on input event.

Note: When several events are connected to the TCC, the enabled action will apply for each of the incoming events. See *Event System (EVSYS)* from Related Links, for details on how to configure the Event System.

Related Links

[27. Event System \(EVSYS\)](#)

[39.8.9. EVCTRL](#)

39.6.6 Sleep Mode Operation

The TCC can be configured to operate in any Sleep mode. To be able to run in standby the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. The MODULE can in any Sleep mode wake-up the device using interrupts or perform actions through the Event System.

39.6.7 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Pattern and Pattern Buffer registers (PATT and PATTBUF)
- Waveform register (WAVE)

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- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

The following registers are synchronized when read:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Count Value register (COUNT): synchronization is done on demand through READSYNC command (CTRLBSET.CMD)
- Pattern and Pattern Buffer registers (PATT and PATTBUF)
- Waveform register (WAVE)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

39.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0		
0x00	CTRLA	7:0		RESOLUTION[1:0]					ENABLE	SWRST		
		15:8	MSYNC	ALOCK	PRESCSYNC[1:0]		RUNSTDBY	PRESCALER[2:0]				
		23:16	DMAOS									
		31:24				CPTEN3	CPTEN2	CPTEN1	CPTEN0			
0x04	CTRLBCLR	7:0	CMD[2:0]			IDXCMD[1:0]	ONESHOT	LUPD	DIR			
0x05	CTRLBSET	7:0	CMD[2:0]			IDXCMD[1:0]	ONESHOT	LUPD	DIR			
0x06 ... 0x07	Reserved											
0x08	SYNCBUSY	7:0	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST		
		15:8			CC5	CC4	CC3	CC2	CC1	CC0		
		23:16										
		31:24										
0x0C	FCTRLA	7:0	RESTART	BLANK[1:0]		QUAL	KEEP	SRC[1:0]				
		15:8	BLANKPRES C	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]			
		23:16		BLANKVAL[7:0]				FILTERVAL[3:0]				
		31:24						FILTERVAL[3:0]				
0x10	FCTRLB	7:0	RESTART	BLANK[1:0]		QUAL	KEEP	SRC[1:0]				
		15:8	BLANKPRES C	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]			
		23:16		BLANKVAL[7:0]				FILTERVAL[3:0]				
		31:24						FILTERVAL[3:0]				
0x14	WEXCTRL	7:0						OTMX[1:0]				
		15:8					DTIEN3	DTIEN2	DTIEN1	DTIEN0		
		23:16		DTLS[7:0]								
		31:24		DTHS[7:0]								
0x18	DRVCTRL	7:0	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0		
		15:8	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0		
		23:16	INVEN7	INVEN6	INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0		
		31:24	FILTERVAL1[3:0]			FILTERVAL0[3:0]						
0x1C ... 0x1D	Reserved											
0x1E	DBGCTRL	7:0						FDDBD		DBGRUN		
0x1F	Reserved											
0x20	EVCTRL	7:0	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]				
		15:8	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO		
		23:16					MCEI3	MCEI2	MCEI1	MCEI0		
		31:24					MCEO3	MCEO2	MCEO1	MCEO0		
0x24	INTENCLR	7:0				ERR	CNT	TRG	OVF			
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS				
		23:16					MCx3	MCx2	MCx1	MCx0		
		31:24										
0x28	INTENSET	7:0				ERR	CNT	TRG	OVF			
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS				
		23:16					MC3	MC2	MC1	MC0		
		31:24										
0x2C	INTFLAG	7:0				ERR	CNT	TRG	OVF			
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS				
		23:16					MC3	MC2	MC1	MC0		
		31:24										
0x30	STATUS	7:0	PERBUFV		PATBUFV	SLAVE	DFS	UFS	IDX	STOP		
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN		
		23:16					CCBUFV3	CCBUFV2	CCBUFV1	CCBUFV0		
		31:24					CMP3	CMP2	CMP1	CMP0		

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x34	COUNT	7:0				COUNT[7:0]				
		15:8				COUNT[15:8]				
		23:16				COUNT[23:16]				
		31:24								
0x38	PATT	7:0	PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
0x3A ... 0x3B	Reserved	15:8	PGV7	PGV6	PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
0x3C	WAVE	7:0	CIPEREN		RAMP[1:0]				WAVEGEN[2:0]	
		15:8					CICCEN3	CICCEN2	CICCEN1	CICCEN0
		23:16			POL5	POL4	POL3	POL2	POL1	POL0
		31:24				SWAP3	SWAP2	SWAP1	SWAP0	
0x40	PER	7:0		PER[1:0]			DITHER[5:0]			
		15:8				PER[9:2]				
		23:16				PER[17:10]				
		31:24								
0x44	CC0	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x48	CC1	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x4C	CC2	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x50	CC3	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x54	CC4	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x58	CC5	7:0		CC[1:0]			DITHER[5:0]			
		15:8				CC[9:2]				
		23:16				CC[17:10]				
		31:24								
0x5C ... 0x63	Reserved									
0x64	PATTBUF	7:0	PGEB7	PGEB6	PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
		15:8	PGV7	PGVB6	PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
0x66 ... 0x6B	Reserved									
0x6C	PERBUF	7:0		PERBUF[1:0]			DITHERBUF[5:0]			
		15:8				PERBUF[9:2]				
		23:16				PERBUF[17:10]				
		31:24								
0x70	CCBUFO	7:0		CCBUF[1:0]			DITHERBUF[5:0]			
		15:8				CCBUF[9:2]				
		23:16				CCBUF[17:10]				
		31:24								

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x74	CCBUF1	7:0	CCBUF[1:0]				DITHERBUF[5:0]			
		15:8				CCBUF[9:2]				
		23:16				CCBUF[17:10]				
		31:24								
0x78	CCBUF2	7:0	CCBUF[1:0]			DITHERBUF[5:0]				
		15:8			CCBUF[9:2]					
		23:16			CCBUF[17:10]					
		31:24								
0x7C	CCBUF3	7:0	CCBUF[1:0]			DITHERBUF[5:0]				
		15:8			CCBUF[9:2]					
		23:16			CCBUF[17:10]					
		31:24								
0x80	CCBUF4	7:0	CCBUF[1:0]			DITHERBUF[5:0]				
		15:8			CCBUF[9:2]					
		23:16			CCBUF[17:10]					
		31:24								
0x84	CCBUF5	7:0	CCBUF[1:0]			DITHERBUF[5:0]				
		15:8			CCBUF[9:2]					
		23:16			CCBUF[17:10]					
		31:24								

39.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

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TCC – Timer/Counter for Control Applications

39.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized (ENABLE, SWRST)

Bit	31	30	29	28	27	26	25	24
Access					CPTEN3	CPTEN2	CPTEN1	CPTEN0
Reset					R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access	DMAOS							
Reset	R/W							
	0							
Bit	15	14	13	12	11	10	9	8
Access	MSYNC	ALOCK	PRESCSYNC[1:0]	RUNSTDBY		PRESCALER[2:0]		
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access		RESOLUTION[1:0]					ENABLE	SWRST
Reset	R/W	R/W					R/W	R/W
	0	0					0	0

Bits 24, 25, 26, 27 – CPTENx Capture Channel x Enable

These bits are used to select the capture or compare operation on channel x.

Writing a '1' to CPTENx enables capture on channel x.

Writing a '0' to CPTENx disables capture on channel x.

Bit 23 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.

Writing a '1' to this bit will generate a DMA trigger on TCC cycle following a TCC_CTRLBSET_CMD_DMAOS command.

Writing a '0' to this bit will generate DMA triggers on each TCC cycle.

This bit is not synchronized.

Bit 15 – MSYNC Master Synchronization (only for TCC slave instance)

This bit must be set if the TCC counting operation must be synchronized on its Master TCC.

This bit is not synchronized.

Value	Description
0	The TCC controls its own counter.
1	The counter is controlled by its Master TCC.

Bit 14 – ALOCK Auto Lock

This bit is not synchronized.

Value	Description
0	The Lock Update bit in the Control B register (CTRLB.LUPD) is not affected by overflow/underflow, and re-trigger events
1	CTRLB.LUPD is set to '1' on each overflow/underflow or re-trigger event.

Bits 13:12 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select if on re-trigger event, the Counter is cleared or reloaded on either the next GCLK_TCCx clock, or on the next prescaled GCLK_TCCx clock. It is also possible to reset the prescaler on re-trigger event.

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These bits are not synchronized.

Value	Name	Description	
Counter Reloaded			Prescaler
0x0	GCLK	Reload or reset Counter on next GCLK	-
0x1	PRESC	Reload or reset Counter on next prescaler clock	-
0x2	RESYNC	Reload or reset Counter on next GCLK	Reset prescaler counter
0x3	Reserved		

Bit 11 – RUNSTDBY Run in Standby

This bit is used to keep the TCC running in Standby mode.

These bits are not synchronized.

Value	Description
0	The TCC is halted in standby.
1	The TCC continues to run in standby.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the Counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TCCx
0x1	DIV2	Prescaler: GCLK_TCCx/2
0x2	DIV4	Prescaler: GCLK_TCCx/4
0x3	DIV8	Prescaler: GCLK_TCCx/8
0x4	DIV16	Prescaler: GCLK_TCCx/16
0x5	DIV64	Prescaler: GCLK_TCCx/64
0x6	DIV256	Prescaler: GCLK_TCCx/256
0x7	DIV1024	Prescaler: GCLK_TCCx/1024

Bits 6:5 – RESOLUTION[1:0] Dithering Resolution

These bits increase the TCC resolution by enabling the dithering options.

These bits are not synchronized.

Table 39-9. Dithering

Value	Name	Description
0x0	NONE	The dithering is disabled.
0x1	DITH4	Dithering is done every 16 PWM frames. PER[3:0] and CCx[3:0] contain dithering pattern selection.
0x2	DITH5	Dithering is done every 32 PWM frames. PER[4:0] and CCx[4:0] contain dithering pattern selection.
0x3	DITH6	Dithering is done every 64 PWM frames. PER[5:0] and CCx[5:0] contain dithering pattern selection.

Bit 1 – ENABLE Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TCC (except DBGCTRL) to their initial state, and the TCC will be disabled.

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Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no Reset operation ongoing.
1	The Reset operation is ongoing.

Preliminary

39.8.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

This register allows the user to change this register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set (CTRLBSET) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:5 – CMD[2:0] TCC Command

Writing zero to this bit group has no effect.

Writing a '1' to any of these bits will clear the pending command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Clear start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force COUNT read synchronization
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command

These bits can be used to force cycle A and cycle B changes in RAMP2 and RAMP2A operation. On timer/counter update condition, the command is executed, the IDX flag in STATUS register is updated and the IDXCMD command is cleared.

Writing zero to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Value	Name	Description
0x0	DISABLE	DISABLE Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot

This bit controls one-shot operation of the TCC. When one-shot operation is enabled, the TCC will stop counting on the next overflow/underflow condition or on a stop command.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable the one-shot operation.

Value	Description
0	The TCC will update the counter value on overflow/underflow condition and continue operation.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TCC buffered registers.

When CTRLB.LUPD is cleared, the hardware UPDATE registers with value from their buffered registers is enabled. This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable the registers updates on hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB, and PGEB buffer registers values are copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.

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Value	Description
1	The CCBx, PERB, PGVB, and PGEB buffer registers values are <i>not</i> copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

39.8.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

This register allows the user to change this register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set (CTRLBCLR) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:5 – CMD[2:0] TCC Command

These bits can be used for software control of re-triggering and stop commands of the TCC. When a command has been executed, the CMD bit field will be read back as zero. The commands are executed on the next prescaled GCLK_TCCx clock cycle.

Writing zero to this bit group has no effect

Writing a valid value to this bit group, as shown in the following table, will set the associated command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command

These bits can be used to force cycle A and cycle B changes in RAMP2 and RAMP2A operation. On timer/counter update condition, the command is executed, the IDX flag in STATUS register is updated and the IDXCMD command is cleared.

Writing a zero to these bits has no effect.

Writing a valid value to these bits will set a command.

Value	Name	Description
0x0	DISABLE	Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot

This bit controls one-shot operation of the TCC. When in one-shot operation, the TCC will stop counting on the next overflow/underflow condition or a stop command.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable the one-shot operation.

Value	Description
0	The TCC will count continuously.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TCC buffered registers.

When CTRLB.LUPD is set, the hardware UPDATE registers with value from their buffered registers is disabled.

Disabling the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

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Writing a '1' to this bit will disable the registers updates on hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB, and PGEB buffer registers values are copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.
1	The CCBx, PERB, PGVB, and PGEB buffer registers values are <i>not</i> copied into CCx, PER, PGV, and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

39.8.4 Synchronization Busy

Name: SYNCBUSY
Offset: 0x08
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access			CC5	CC4	CC3	CC2	CC1	CC0
Reset			R 0	R 0	R 0	R 0	R 0	R 0
Bit	7	6	5	4	3	2	1	0
Access	PER R 0	WAVE R 0	PATT R 0	COUNT R 0	STATUS R 0	CTRLB R 0	ENABLE R 0	SWRST R 0
Reset								

Bits 8, 9, 10, 11, 12, 13 – CC Compare/Capture Channel x Synchronization Busy

This bit is cleared when the synchronization of Compare/Capture Channel x register between the clock domains is complete.

This bit is set when the synchronization of Compare/Capture Channel x register between clock domains is started. CCx bit is available only for existing Compare/Capture Channels. For details on CC channels number, refer to each TCC feature list.

This bit is set when the synchronization of CCx register between clock domains is started.

Bit 7 – PER PER Synchronization Busy

This bit is cleared when the synchronization of PER register between the clock domains is complete.

This bit is set when the synchronization of PER register between clock domains is started.

Bit 6 – WAVE WAVE Synchronization Busy

This bit is cleared when the synchronization of WAVE register between the clock domains is complete.

This bit is set when the synchronization of WAVE register between clock domains is started.

Bit 5 – PATT PATT Synchronization Busy

This bit is cleared when the synchronization of PATTERN register between the clock domains is complete.

This bit is set when the synchronization of PATTERN register between clock domains is started.

Bit 4 – COUNT COUNT Synchronization Busy

This bit is cleared when the synchronization of COUNT register between the clock domains is complete.

This bit is set when the synchronization of COUNT register between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy

This bit is cleared when the synchronization of STATUS register between the clock domains is complete.

This bit is set when the synchronization of STATUS register between clock domains is started.

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Bit 2 – CTRLB CTRLB Synchronization Busy

This bit is cleared when the synchronization of CTRLB register between the clock domains is complete.

This bit is set when the synchronization of CTRLB register between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy

This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy

This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

39.8.5 Fault Control A and B

Name: FCTRLn
Offset: 0x0C + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
FILTERVAL[3:0]								
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	23	22	21	20	19	18	17	16
BLANKVAL[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
BLANKPRESC CAPTURE[2:0] CHSEL[1:0] HALT[1:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
RESTART BLANK[1:0] QUAL KEEP SRC[1:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 27:24 – FILTERVAL[3:0] Recoverable Fault n Filter Value

These bits define the filter value applied on MCE_x (x=0,1) event input line. The value must be set to zero when MCE_x event is used as synchronous event.

Bits 23:16 – BLANKVAL[7:0] Recoverable Fault n Blanking Value

These bits determine the duration of the blanking of the fault input source. Activation and edge selection of the blank filtering are done by the BLANK bits (FCTRLn.BLANK).

When enabled, the fault input source is internally disabled for BLANKVAL* prescaled GCLK_TCCx periods after the detection of the waveform edge.

Bit 15 – BLANKPRESC Recoverable Fault n Blanking Value Prescaler

This bit enables a factor 64 prescaler factor on used as base frequency of the BLANKVAL value.

Value	Description
0	Blank time is BLANKVAL* prescaled GCLK_TCCx.
1	Blank time is BLANKVAL* 64 * prescaled GCLK_TCCx.

Bits 14:12 – CAPTURE[2:0] Recoverable Fault n Capture Action

These bits select the capture and Fault n interrupt/event conditions.

Table 39-10. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.

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Value	Name	Description
0x3	CAPTMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is higher than the last stored capture value (CC). INTFLAGFAULTn flag rises on each local maximum detection.
0x4	LOCMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAGFAULTn flag rises on each local minimum value detection.
0x5	LOCMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAGFAULTn flag rises on each local maximum detection.
0x6	DERIV0	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAGFAULTn flag rises on each local maximum or minimum detection.
0x7	CAPTMARK	Capture with ramp index as MSB value.

Bits 11:10 – CHSEL[1:0] Recoverable Fault n Capture Channel

These bits select the channel for capture operation triggered by recoverable Fault n.

Value	Name	Description
0x0	CC0	Capture value stored into CC0
0x1	CC1	Capture value stored into CC1
0x2	CC2	Capture value stored into CC2
0x3	CC3	Capture value stored into CC3

Bits 9:8 – HALT[1:0] Recoverable Fault n Halt Operation

These bits select the halt action for recoverable Fault n.

Value	Name	Description
0x0	DISABLE	Halt action disabled
0x1	HW	Hardware halt action
0x2	SW	Software halt action
0x3	NR	Non-recoverable fault

Bit 7 – RESTART Recoverable Fault n Restart

Setting this bit enables restart action for Fault n.

Value	Description
0	Fault n restart action is disabled.
1	Fault n restart action is enabled.

Bits 6:5 – BLANK[1:0] Recoverable Fault n Blanking Operation

These bits, select the blanking start point for recoverable Fault n.

Value	Name	Description
0x0	START	Blanking applied from start of the Ramp period
0x1	RISE	Blanking applied from rising edge of the waveform output
0x2	FALL	Blanking applied from falling edge of the waveform output
0x3	BOTH	Blanking applied from each toggle of the waveform output

Bit 4 – QUAL Recoverable Fault n Qualification

Setting this bit enables the recoverable Fault n input qualification.

Value	Description
0	The recoverable Fault n input is not disabled on CMPx value condition.
1	The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0).

Bit 3 – KEEP Recoverable Fault n Keep

Setting this bit enables the Fault n keep action.

Value	Description
0	The Fault n state is released as soon as the recoverable Fault n is released.
1	The Fault n state is released at the end of TCC cycle.

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Bits 1:0 – SRC[1:0] Recoverable Fault n Source

These bits select the TCC event input for recoverable Fault n.

Event system channel connected to MCE_x event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

Value	Name	Description
0x0	DISABLE	Fault input disabled
0x1	ENABLE	MCE _x (x=0,1) event input
0x2	INVERT	Inverted MCE _x (x=0,1) event input
0x3	ALTFAULT	Alternate fault (A or B) state at the end of the previous period.

39.8.6 Waveform Extension Control

Name: WEXCTRL
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
DTHS[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
DTLS[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
DTIEN3 DTIEN2 DTIEN1 DTIEN0								
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
OTMX[1:0]								
Access					R/W	R/W		
Reset					0	0		

Bits 31:24 – DTHS[7:0] Dead-Time High Side Outputs Value

This register holds the number of GCLK_TCCx clock cycles for the dead-time high side.

Bits 23:16 – DTLS[7:0] Dead-time Low Side Outputs Value

This register holds the number of GCLK_TCCx clock cycles for the dead-time low side.

Bits 8, 9, 10, 11 – DTIENx Dead-time Insertion Generator x Enable

Setting any of these bits enables the dead-time insertion generator for the corresponding output matrix. This will override the output matrix [x] and [x+WO_NUM/2], with the low side and high side waveform respectively.

Value	Description
0	No dead-time insertion override.
1	Dead time insertion override on signal outputs[x] and [x+WO_NUM/2], from matrix outputs[x] signal.

Bits 1:0 – OTMX[1:0] Output Matrix

These bits define the matrix routing of the TCC waveform generation outputs to the port pins, according to

[39.6.3.8. Waveform Extension.](#)

39.8.7 Driver Control

Name: DRVCTRL
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	FILTERVAL1[3:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	INVEN7	INVEN6	INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:28 – FILTERVAL1[3:0] Non-Recoverable Fault Input 1 Filter Value

These bits define the filter value applied on TCE1 event input line. When the TCE1 event input line is configured as a synchronous event, this value must be 0x0.

Bits 27:24 – FILTERVAL0[3:0] Non-Recoverable Fault Input 0 Filter Value

These bits define the filter value applied on TCE0 event input line. When the TCE0 event input line is configured as a synchronous event, this value must be 0x0.

Bits 16, 17, 18, 19, 20, 21, 22, 23 – INVENx Waveform Output x Inversion

These bits are used to select inversion on the output of channel x.

Writing a '1' to INVENx inverts output from WO[x].

Writing a '0' to INVENx disables inversion of output from WO[x].

Bits 8, 9, 10, 11, 12, 13, 14, 15 – NRVx NRVx Non-Recoverable State x Output Value

These bits define the value of the enabled override outputs, under non-recoverable fault condition.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – NREx Non-Recoverable State x Output Enable

These bits enable the override of individual outputs by NRVx value, under non-recoverable fault condition.

Value	Description
0	Non-recoverable fault tri-state the output.
1	Non-recoverable faults set the output to NRVx level.

39.8.8 Debug control

Name: DBGCTRL
Offset: 0x1E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
Access						FDDBD		DBGREN
Reset						0		0

Bit 2 – FDDBD Fault Detection on Debug Break Detection

This bit is not affected by software Reset and should not be changed by software while the TCC is enabled. By default this bit is zero, and the on-chip debug (OCD) fault protection is disabled. When this bit is written to '1', OCD break request from the OCD system will trigger non-recoverable fault. When this bit is set, OCD fault protection is enabled and OCD break request from the OCD system will trigger a non-recoverable fault.

Value	Description
0	No faults are generated when TCC is halted in Debug mode.
1	A non recoverable fault is generated and FAULTD flag is set when TCC is halted in Debug mode.

Bit 0 – DBGREN Debug Running State

This bit is not affected by software Reset and should not be changed by software while the TCC is enabled.

Value	Description
0	The TCC is halted when the device is halted in Debug mode.
1	The TCC continues normal operation when the device is halted in Debug mode.

39.8.9 Event Control

Name: EVCTRL
Offset: 0x20
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access					MCEO3	MCEO2	MCEO1	MCEO0
Reset					R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access					MCEI3	MCEI2	MCEI1	MCEI0
Reset					R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	TCEI1	TCEI0	TCINV1	TCINVO		CNTEO	TRGEO	OVFEO
Reset	R/W	R/W	R/W	R/W		R/W	R/W	R/W
	0	0	0	0		0	0	0
Bit	7	6	5	4	3	2	1	0
Access	CNTSEL[1:0]			EVACT1[2:0]			EVACT0[2:0]	
Reset	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27 – MCEO Match or Capture Channel x Event Output Enable

These bits control if the match/capture event on channel x is enabled and will be generated for every match or capture.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on channel x.

Bits 16, 17, 18, 19 – MCEI Match or Capture Channel x Event Input Enable

These bits indicate if the match/capture x incoming event is enabled

These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 14, 15 – TCEIx Timer/Counter Event Input x Enable

This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 12, 13 – TCINVx Timer/Counter Event x Invert Enable

This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.
1	Input event source x is inverted.

Bit 10 – CNTEO Timer/Counter Event Output Enable

This bit is used to enable the counter cycle event. When enabled, an event will be generated on begin or end of counter cycle depending of CNTSEL[1:0] settings.

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Value	Description
0	Counter cycle output event is disabled and will not be generated.
1	Counter cycle output event is enabled and will be generated depend of CNTSEL[1:0] value.

Bit 9 – TRGEO Retrigger Event Output Enable

This bit is used to enable the counter retrigger event. When enabled, an event will be generated when the counter retriggers operation.

Value	Description
0	Counter retrigger event is disabled and will not be generated.
1	Counter retrigger event is enabled and will be generated for every counter retrigger.

Bit 8 – OVFE0 Overflow/Underflow Event Output Enable

This bit is used to enable the overflow/underflow event. When enabled an event will be generated when the counter reaches the TOP or the ZERO value.

Value	Description
0	Overflow/underflow counter event is disabled and will not be generated.
1	Overflow/underflow counter event is enabled and will be generated for every counter overflow/underflow.

Bits 7:6 – CNTSEL[1:0] Timer/Counter Interrupt and Event Output Selection

These bits define on which part of the counter cycle the counter event output is generated.

Value	Name	Description
0x0	BEGIN	An interrupt/event is generated at begin of each counter cycle
0x1	END	An interrupt/event is generated at end of each counter cycle
0x2	BETWEEN	An interrupt/event is generated between each counter cycle.
0x3	BOUNDARY	An interrupt/event is generated at begin of first counter cycle, and end of last counter cycle.

Bits 5:3 – EVACT1[2:0] Timer/Counter Event Input 1 Action

These bits define the action the TCC will perform on TCE1 event input.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	DIR (asynch)	Direction control
0x3	STOP	Stop TC on event
0x4	DEC	Decrement TC on event
0x5	PPW	Period captured into CC0 Pulse Width on CC1
0x6	PWP	Period captured into CC1 Pulse Width on CC0
0x7	FAULT	Non-recoverable Fault

Bits 2:0 – EVACT0[2:0] Timer/Counter Event Input 0 Action

These bits define the action the TCC will perform on TCE0 event input 0.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	COUNTEV	Count on event.
0x3	START	Start TC on event
0x4	INC	Increment TC on EVENT
0x5	COUNT (async)	Count on active state of asynchronous event
0x6	STAMP	Capture overflow times (Max value)
0x7	FAULT	Non-recoverable Fault

39.8.10 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Access	Bit 31	30	29	28	27	26	25	24
Reset								
Access	Bit 23	22	21	20	19	18	17	16
Reset					MCx3	MCx2	MCx1	MCx0
Access	Bit 15	14	13	12	11	10	9	8
Reset	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		
Access	Bit 7	6	5	4	3	2	1	0
Reset					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Recoverable Fault B Interrupt Disable/Enable bit, which disables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Recoverable Fault A Interrupt Disable/Enable bit, which disables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Debug Fault State Interrupt Disable/Enable bit, which disables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Disable/Enable bit, which disables the Compare interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Counter Interrupt Disable/Enable bit, which disables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

Bit 1 – TRG Retrigger Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Retrigger Interrupt Disable/Enable bit, which disables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Disable/Enable bit, which disables the Overflow interrupt request.

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Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

Preliminary

39.8.11 Interrupt Enable Set

Name: INTENSET
Offset: 0x28
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					MC3	MC2	MC1	MC0
Reset					R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Access	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Reset	R/W	R/W	R/W	R/W	R/W	R/W		
Bit	7	6	5	4	3	2	1	0
Access					ERR	CNT	TRG	OVF
Reset					R/W	R/W	R/W	R/W

Bits 16, 17, 18, 19 – MC Match or Capture Channel x Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Non-Recoverable Fault x Interrupt Disable/Enable bit, which enables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Recoverable Fault B Interrupt Disable/Enable bit, which enables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Recoverable Fault A Interrupt Disable/Enable bit, which enables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Debug Fault State Interrupt Disable/Enable bit, which enables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Disable/Enable bit, which enables the Compare interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Retrigger Interrupt Disable/Enable bit, which enables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

Bit 1 – TRG Retrigger Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Retrigger Interrupt Disable/Enable bit, which enables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Disable/Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.

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Value	Description
1	The Overflow interrupt is enabled.

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39.8.12 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x2C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access					MC3	MC2	MC1	MC0
Reset					R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W	R/W	DFS	UFS		
Reset	0	0	0	0	R/W	R/W	0	0
Bit	7	6	5	4	3	2	1	0
Access					ERR	CNT	TRG	OVF
Reset					R/W	R/W	R/W	R/W

Bits 16, 17, 18, 19 – MC Match or Capture Channel x Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a match with the compare condition or once CCx register contain a valid capture value.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag. In Capture operation, this flag is automatically cleared when CCx register is read.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a Non-Recoverable Fault x occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Non-Recoverable Fault x interrupt flag.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault B occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Recoverable Fault B interrupt flag.

Bit 12 – FAULTA Recoverable Fault A Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault B occurs.

Writing a '0' to this bit has no effect.

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Writing a '1' to this bit clears the Recoverable Fault B interrupt flag.

Bit 11 – DFS Non-Recoverable Debug Fault State Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after an Debug Fault State occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Debug Fault State interrupt flag.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable

This flag is set when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD).

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Flag

This flag is set if a new capture occurs on a channel when the corresponding Match or Capture Channel x interrupt flag is one. In which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the error interrupt flag.

Bit 2 – CNT Counter Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a counter event occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the CNT interrupt flag.

Bit 1 – TRG Retrigger Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a counter retrigger occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the re-trigger interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after an overflow condition occurs.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

39.8.13 Status

Name: STATUS
Offset: 0x30
Reset: 0x00000001
Property: -

Bit	31	30	29	28	27	26	25	24
Access					CMP3	CMP2	CMP1	CMP0
Reset					R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access					CCBUFV3	CCBUFV2	CCBUFV1	CCBUFV0
Reset					R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
Reset	R/W	R/W	R/W	R/W	R	R	R	R
	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	PERBUFV		PATTBUFV	SLAVE	DFS	UFS	IDX	STOP
Reset	R/W		R/W	R	R/W	R/W	R	R
	0		0	0	0	0	0	1

Bits 24, 25, 26, 27 – CMP Channel x Compare Value

This bit reflects the channel x output compare value.

Value	Description
0	Channel compare output value is 0.
1	Channel compare output value is 1.

Bits 16, 17, 18, 19 – CCBUFV Channel x Compare or Capture Buffer Valid

For a compare channel, this bit is set when a new value is written to the corresponding CCBUFx register. The bit is cleared either by writing a '1' to the corresponding location when CTRLB.LUPD is set, or automatically on an UPDATE condition.

For a capture channel, the bit is set when a valid capture value is stored in the CCBUFx register. The bit is automatically cleared when the CCx register is read.

Bits 14, 15 – FAULTx Non-recoverable Fault x State

This bit is set by hardware as soon as non-recoverable Fault x condition occurs.

This bit is cleared by writing a one to this bit and when the corresponding FAULTxIN status bit is low.

Once this bit is clear, the timer/counter will restart from the last COUNT value. To restart the timer/counter from BOTTOM, the timer/counter restart command must be executed before clearing the corresponding STATEx bit. For further details on timer/counter commands, refer to available commands description ([39.8.3. CTRLBSET.CMD](#)).

Bit 13 – FAULTB Recoverable Fault B State

This bit is set by hardware as soon as recoverable Fault B condition occurs.

This bit can be clear by hardware when Fault B action is resumed, or by writing a '1' to this bit when the corresponding FAULTBIN bit is low. If software halt command is enabled (FAULTB.HALT=SW), clearing this bit will release the timer/counter.

Bit 12 – FAULTA Recoverable Fault A State

This bit is set by hardware as soon as recoverable Fault A condition occurs.

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This bit can be clear by hardware when Fault A action is resumed, or by writing a '1' to this bit when the corresponding FAULTAIN bit is low. If software halt command is enabled (FAULTA.HALT=SW), clearing this bit will release the timer/counter.

Bit 11 – FAULT1IN Non-Recoverable Fault 1 Input

This bit is set while an active Non-Recoverable Fault 1 input is present.

Bit 10 – FAULT0IN Non-Recoverable Fault 0 Input

This bit is set while an active Non-Recoverable Fault 0 input is present.

Bit 9 – FAULTBIN Recoverable Fault B Input

This bit is set while an active Recoverable Fault B input is present.

Bit 8 – FAULTAIN Recoverable Fault A Input

This bit is set while an active Recoverable Fault A input is present.

Bit 7 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. This bit is automatically cleared by hardware on UPDATE condition when CTRLB.LUPD is set, or by writing a '1' to this bit.

Bit 5 – PATTBUFV Pattern Generator Value Buffer Valid

This bit is set when a new value is written to the PATTBUF register. This bit is automatically cleared by hardware on UPDATE condition when CTRLB.LUPD is set, or by writing a '1' to this bit.

Bit 4 – SLAVE Slave

This bit is set when TCC is set in Slave mode. This bit follows the CTRLA.MSYNC bit state.

Bit 3 – DFS Debug Fault State

This bit is set by hardware in Debug mode when DDBGCTRL.FDDBD bit is set. The bit is cleared by writing a '1' to this bit and when the TCC is not in Debug mode.

When the bit is set, the counter is halted and the Waveforms state depend on DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 2 – UFS Non-recoverable Update Fault State

This bit is set by hardware when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD). The bit is cleared by writing a one to this bit.

When the bit is set, the waveforms state depend on DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 1 – IDX Ramp Index

In RAMP2 and RAMP2A operation, the bit is cleared during the cycle A and set during the cycle B. In RAMP1 operation, the bit always reads zero. For details on ramp operations, refer to [39.6.3.4. Ramp Operations](#).

Bit 0 – STOP Stop

This bit is set when the TCC is disabled either on a STOP command or on an UPDATE condition when One-Shot operation mode is enabled (CTRLBSET.ONESHOT=1).

This bit is clear on the next incoming counter increment or decrement.

Value	Description
0	Counter is running.
1	Counter is stopped.

39.8.14 Counter Value

Name: COUNT
Offset: 0x34
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
COUNT[23:16]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
COUNT[15:8]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
COUNT[7:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – COUNT[23:0] Counter Value

These bits hold the value of the Counter register.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0 (depicted)
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6

39.8.15 Pattern

Name: PATT
Offset: 0x38
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	PGV7	PGV6	PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PGV Pattern Generation Output Value
 This register holds the values of pattern for each waveform output.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PGE Pattern Generation Output Enable
 This register holds the enable status of pattern generation for each waveform output. A bit written to '1' will override the corresponding SWAP output with the corresponding PGVn value.

39.8.16 Waveform

Name: WAVE
Offset: 0x3C
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access					SWAP3	SWAP2	SWAP1	SWAP0
Reset					0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access			POL5	POL4	POL3	POL2	POL1	POL0
Reset			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access					CICCEN3	CICCEN2	CICCEN1	CICCEN0
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access	CIPEREN		RAMP[1:0]				WAVEGEN[2:0]	
Reset	R/W		R/W	R/W		R/W	R/W	R/W

Bits 24, 25, 26, 27 – SWAP Swap DTI Output Pair x

Setting these bits enables output swap of DTI outputs [x] and [x+WO_NUM/2]. Note the DTIxEN settings will not affect the swap operation.

Bits 16, 17, 18, 19, 20, 21 – POL Channel Polarity x

Setting these bits enables the output polarity in single-slope and dual-slope PWM operations.

Value	Name	Description
0	(single-slope PWM waveform generation)	Compare output is initialized to ~DIR and set to DIR when TCC counter matches CCx value
1	(single-slope PWM waveform generation)	Compare output is initialized to DIR and set to ~DIR when TCC counter matches CCx value.
0	(dual-slope PWM waveform generation)	Compare output is set to ~DIR when TCC counter matches CCx value
1	(dual-slope PWM waveform generation)	Compare output is set to DIR when TCC counter matches CCx value.

Bits 8, 9, 10, 11 – CICCEN Circular CC Enable x

Setting this bits enables the compare circular buffer option on the first four Compare/Capture channels. When the bit is set, CCx register value is copied-back into the CCx register on UPDATE condition.

Bit 7 – CIPEREN Circular Period Enable

Setting this bits enable the period circular buffer option. When the bit is set, the PER register value is copied-back into the PERB register on UPDATE condition.

Bits 5:4 – RAMP[1:0] Ramp Operation

These bits select Ramp operation (RAMP). These bits are not synchronized.

Value	Name	Description
0x0	RAMP1	RAMP1 operation
0x1	RAMP2A	Alternative RAMP2 operation

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Value	Name	Description
0x2	RAMP2	RAMP2 operation
0x3	RAMP2C	Critical RAMP2 operation

Bits 2:0 – WAVEGEN[2:0] Waveform Generation Operation

These bits select the waveform generation operation. The settings impact the top value and control if frequency or PWM waveform generation should be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Top	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/Event Up Down	
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3	Reserved	-	-	-	-	-	-	-
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	-	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	-	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	-

39.8.17 Period Value

Name: PER
Offset: 0x40
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
PER[17:10]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
PER[9:2]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
PER[1:0]				DITHER[5:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PER[17:0] Period Value

These bits hold the value of the TCC period count.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHER[5:0] Dithering Cycle Number

These bits hold the number of extra cycles that are added on the PWM pulse period every 64 PWM frames.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

39.8.18 Compare/Capture Channel x

Name: CC
Offset: 0x44 + n*0x04 [n=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

The CC_x register represents the 16-, 24- bit value, CC_x. The register has two functions, depending of the mode of operation.

For capture operation, this register represents the second buffer level and access point for the CPU and DMA.

For compare operation, this register is continuously compared to the counter value. Normally, the output from the comparator is then used for generating waveforms.

CC_x register is updated with the buffer value from their corresponding CCBUF_x register when an UPDATE condition occurs.

In addition, in match frequency operation, the CC0 register controls the counter period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CC[17:0] Channel x Compare/Capture Value

These bits hold the value of the Channel x compare/capture register.

Notes:

- When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.
- This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHER[5:0] Dithering Cycle Number

These bits hold the number of extra cycles that are added on the PWM pulse width every 64 PWM frames.

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Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

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39.8.19 Pattern Buffer

Name: PATTBUF

Offset: 0x64

Reset: 0x0000

Property: Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
	PGVB7	PGVB6	PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PGEB7	PGEB6	PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PGVB Pattern Generation Output Value Buffer

This register is the buffer for the PGV register. If double buffering is used, valid content in this register is copied to the PGV register on an UPDATE condition.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PGEB Pattern Generation Output Enable Buffer

This register is the buffer of the PGE register. If double buffering is used, valid content in this register is copied into the PGE register at an UPDATE condition.

39.8.20 Period Buffer Value

Name: PERBUF
Offset: 0x6C
Reset: 0xFFFFFFFF
Property: Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
PERBUF[17:10]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
PERBUF[9:2]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
PERBUF[1:0]				DITHERBUF[5:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PERBUF[17:0] Period Buffer Value

These bits hold the value of the Period Buffer register. The value is copied to PER register on UPDATE condition.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0] Dithering Buffer Cycle Number

These bits represent the PER.DITHER bits buffer. When the double buffering is enabled, the value of this bit field is copied to the PER.DITHER bits on an UPDATE condition.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

39.8.21 Channel x Compare/Capture Buffer Value

Name: CCBUF
Offset: 0x70 + n*0x04 [n=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

CCBUFx is copied into CCx at TCC update time

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
CCBUF[17:10]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
CCBUF[9:2]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
CCBUF[1:0]								
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CCBUF[17:0] Channel x Compare/Capture Buffer Value

These bits hold the value of the Channel x Compare/Capture Buffer Value register. The register serves as the buffer for the associated compare or capture registers (CCx). Accessing this register using the CPU or DMA will affect the corresponding CCBUFX status bit.

Notes:

1. When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.
2. This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0] Dithering Buffer Cycle Number

These bits represent the CCx.DITHER bits buffer. When the double buffering is enable, DITHERBUF bits value is copied to the CCx.DITHER bits on an UPDATE condition.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

40. ZBT Radio Subsystem

PIC32CX-BZ2 and WBZ45 supports on-chip IEEE 802.15.4 and 802.15.3 compliant ZB, Bluetooth Low Energy 5.2 interface with integrated transceivers. The Wireless Subsystem block comprises of on-chip ZB and Bluetooth 5.0 BBP/MAC, shared RF transceiver, and Radio Arbiter. This section provides key features of the on- chip Wireless modules.

With integrated Ultra Low Power 2.4 GHz ISM band single transceiver, dual modem, and dual MAC, the Radio supports dual Zigbee and Bluetooth 5.2 link protocols. An on board intelligent Radio Arbiter HW module establishes both the links simultaneously using single Radio Transmit/Recieve with programmable QoS. The RF transceiver includes dual Power Amplifiers architecture, and TR Switch. Therefore medium to high power application use cases are supported without external FEM.

Arbitration between Application, Bluetooth link stack, ZB link stack, and miscellaneous maintenance tasks is handled on the Cortex M4F (w/ DSP, FPU) CPU using available on-chip system memory resources via RTOS.

40.1 Features

2.4 GHz RF Transceiver

- Integrated 2.4 GHz Ultra-low Power RF Transceiver Shared between Bluetooth and Zigbee Modems and Link (MAC) Controllers
- Integrated 16 MHz ± 20 ppm Crystal Oscillator (External Low Cost Crystal)
- Two PA Design Architecture (LPA (+4 dBm) and MPA (+10 dBm)) to Improve TX Power Efficiency
- Low RBOM Two-port TRX RFFE Architecture
 - Integrated balun (single ended RF output) and TRX switch
- Hardware Radio Arbiter with Programmable QoS:
 - Resolution: up to per packet level
 - Time-division coexistence between Bluetooth and 802.15.4
 - Based on shared transceiver and antenna
 - Maintains connections of 802.15.4 and Bluetooth simultaneously

Bluetooth

- Bluetooth Low Energy 5.2 Certified
- Up to +10 dBm Programmable Transmit Output Power
- Typical Receiver Power Sensitivity:
 - -95 dBm for Bluetooth Low Energy 1 Mbps
 - -92 dBm for Bluetooth Low Energy 2 Mbps
 - -102 dBm for Bluetooth Low Energy 125 Kbps
 - -99 dBm for Bluetooth Low Energy 500 Kbps
 - Digital RSSI indicator (-90 dBm ~ -30 dBm)
- Bluetooth Supported Features:
 - 2M uncoded PHY
 - Long range (Coded PHY)
 - Channel selection algorithm #2
 - Advertising extensions, offloads CPU with hardware based scheduler
 - High duty cycle non-connectible advertising
 - Data length extensions
 - Secure connections
 - Privacy upgrades (with hardware white-list support)
- ECDH P256 Hardware Engine for Link Key Generation When Bluetooth Pairing
- AES128 Hardware Module for Real-Time Bluetooth Payload Data Encryption
- HCI Interface via UART

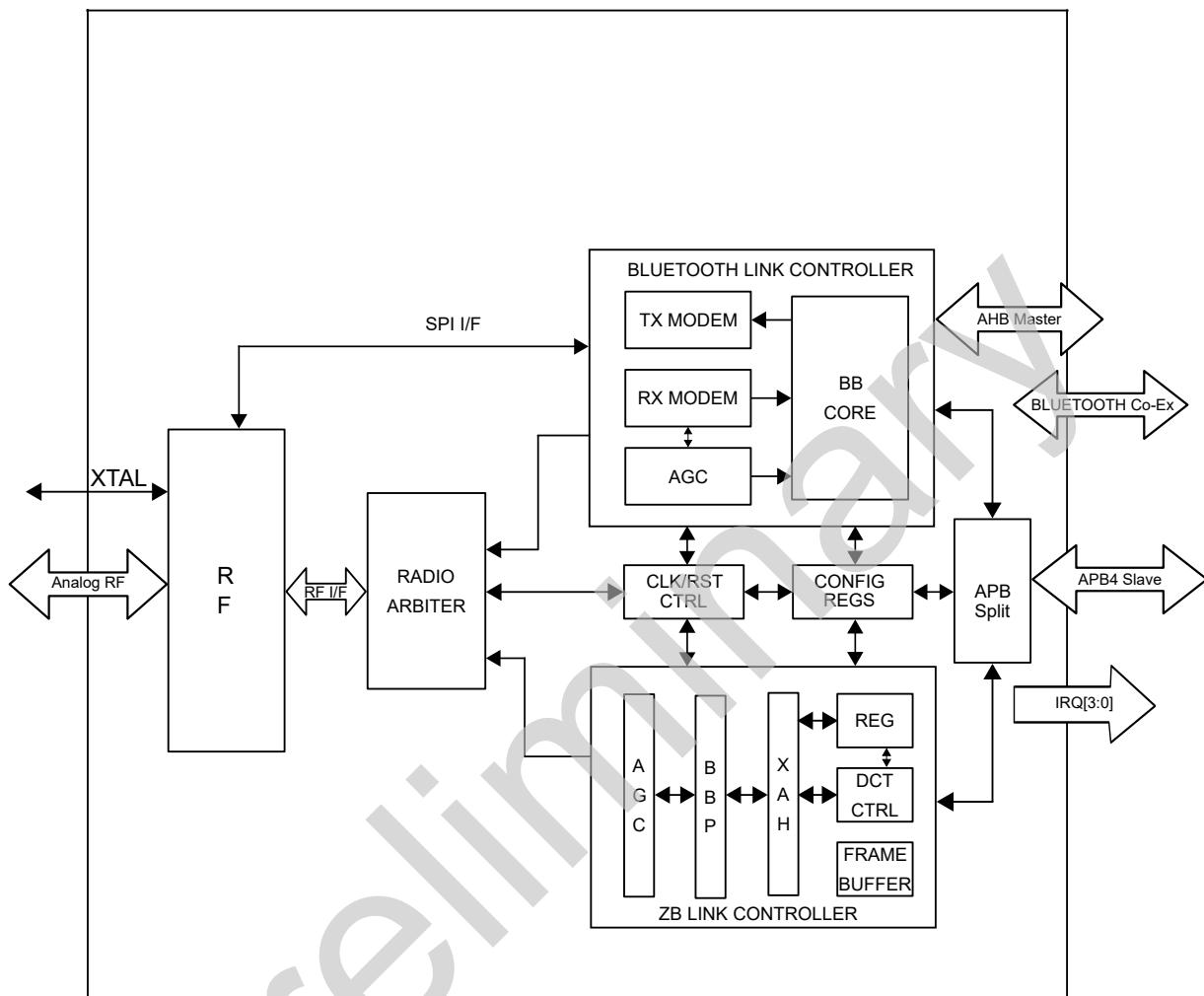
- Bluetooth Low Energy Profiles:
 - Bluetooth Low Energy peripheral and central roles
 - Bluetooth Low Energy APIs for application layer to implement standard or customize GATT based profiles/services
 - Microchip Transparent UART Service
 - Battery Service
 - Device Information Service
 - Multi-link and multi-role
- Bluetooth Low Energy Services:
 - Provisioning
 - Over-the-air (OTA) update (also known as DFU)
 - Advertisement/Beacon
 - Personalized configuration
 - Alert notification service

Zigbee

- PSDU data rate: 250 Kbps
 - Proprietary data rates: 500 Kbps, 1 Mbps, and 2 Mbps
- Programmable RX Mode
 - -103 dBm RX sensitivity in the Continuous mode
 - -98 dBm sensitivity in the RPC mode
 - RPC mode provides lower power consumption in RX mode to support California Green Energy Specification at the system level
- TX Output Power up to +10 dBm
- Hardware Assisted MAC
 - Auto acknowledge
 - Auto retry
 - Channel access back-off
- SFD Detection; Spreading; De-spreading; Framing; CRC-16 Computation
- Independent TX/RX Buffers for Improved CPU Offloading While Handling Zigbee Data
 - 128-byte TX and 128-byte RX frame buffer
- Hardware Security
 - Advanced Encryption Standard (AES)
 - True Random Number Generator (TRNG)
- Zigbee Stack Support
 - Zigbee 3.0 ready
 - Zigbee Pro 2015
 - Zigbee green power support (proxy, sink, and multi sensor)

40.2 Wireless Subsystem Top Level Diagram

Figure 40-1. Wireless Subsystem Top Level Diagram



40.3 Bluetooth Link Controller

The APB interface provide access to internal register banks of the macro. These registers are programmed by the host (FW) to set various configurations, trigger commands, read status, service interrupts and other functions.

All Bluetooth operations are carried out as transmit or receive tasks within the Link controller. There are several task masters:

- Firmware - Firmware can trigger tasks by writing the Task controller registers
- HW Schedule Controller - This is Bluetooth 5.0 Bluetooth Low Energy advertisement scheduler controller (Adv role)
- HW Scanner - This is Bluetooth 5.0 Bluetooth Low Energy advertisement scanner (Master/Central role)
- Bluetooth Low Energy advertisement controller - This is Bluetooth 4.2 advertisement controller (Adv role)

The requests from the task masters are arbitrated and is carried out by the task controller.

40.3.1 Hardware Schedule Controller

Hardware Schedule controller is a hardware accelerator that offloads the Bluetooth 5.0 advertising task from the firmware and executes it in hardware completely.

40.3.2 Hardware Scanner

Hardware Scanner is another hardware accelerator to be used in the Bluetooth Low Energy master / central mode. This offloads the Bluetooth Low Energy task of scanning for advertisements from the firmware. This enables fast scanning and quick connections.

40.3.3 Bluetooth Low Energy Advertisement Controller

Bluetooth Low Energy advertisement controller is Hardware controller that supports offloading of Bluetooth 4.2 advertisements. This is a simpler advertising scenario requiring much smaller memory.

The task controller manages overall TX/RX functionality and starts TX control FSM / RX control FSM in the baseband as per requirement to transmit/receive a packet. Task controller also manages co-existence interface with Wi-Fi. Task controller can also be used directly by the firmware to measure the RSSI across various Bluetooth channels which can then be used to generate an AFH channel map.

40.3.4 Bluetooth Clock Controller

The Bluetooth clock controller/Slot timer provides information on Bluetooth slots and slot boundary. The Bluetooth clock synchronization and clock adjustment due to RX window uncertainty is also handled by this module. These also control the timings for Bluetooth Low Energy non-TIFS tasks.

Tx/Rx control FSM (State machines) provide sequencing and control of various phases of a task. These control various elements in the Tx and Rx data path.

Crypto engine is used for AES encryption and decryption of transmit and receive data. This performs inline encryption as the data passes through the data path in the BB link controller. This block is also used to perform offline CMAC operation directly under application firmware control. This block is also used by the Bluetooth Low Energy privacy controller for the generation and decode of hash needed for resolving private addresses.

40.3.5 Bluetooth Low Energy Privacy Controller

Bluetooth Low Energy Privacy controller is to implement Bluetooth Low Energy privacy feature. It can be used in offline mode by the firmware to generate Resolvable Private Address (RPA) to be used for a transmission. And it is also used inline by the Rx Control FSM to resolve the RPA received in the packet before implementing the device filtering using the white list.

Channel Hop Controller implements the logic needed to compute the next RF channel frequency to be used .

Dedicated math unit for big number (128 bit) operations is available for FW to handle large number operations. This is programmed and used by FW directly. There is no direct use of this block by any other Hardware block.

For simple secure pairing, P256 ECC module is available to perform computationally intensive key matching procedures in hardware.

Transmit memory read controller reads the data from the common memory and feeds to the transmit data path for Bluetooth PDU creations and transmit. Receive memory write controller receives data from the Rx data path and write to the common memory.

40.4 ZIGBEE Link Controller

ZIGBEE Link Controller implements Zigbee 3.0 (802.15.4-2011) MAC and baseband functionality in hardware.

The CPU interface (APB Slave) provides access to internal registers of the macro. These registers are programmed by the host (FW) in order to kick off transmit/receive functionality along with the programming of other features. The APB Slave contains shadow registers for the status registers in the design for single cycle, contention free read accesses. Interrupt controller logic and also reside in APB slave module.

Separate 128 byte frame buffers are provided for TX and RX.

XAH module implements basic MAC functionality as well as hardware accelerator for features such as automatic acknowledgement, CSMA-CA and retransmission, automatic FCS check, etc.

BBP module implements Offset-QPSK PHY with 250 kb/s PSDU data rate. Higher data rates up to 2000 kb/s are also supported.

40.4.1 Transmit Operation

A frame transmission comprises of two actions, a write to Frame Buffer and the transmission of its contents. Both actions can be run in parallel if required by critical protocol timing.

40.4.2 Receive Operation

A frame reception comprises of two actions: The transceiver listens for, receives, and demodulates the frame to the Frame Buffer and signals the reception to the microcontroller. After that process, the microcontroller can read the available frame data from the Frame Buffer via the APB interface.

40.5 Radio Arbiter

Radio Arbiter determines the ownership of the Radio between ZigBee and Bluetooth link controllers. It also generates control to select between ZB/Bluetooth to drive the controls and Data to or from the RF.

By default, the Arbiter is IDLE and no Link controller has the ownership. The general intention of the design is to provide a radio arbiter that is flexible enough that the arbitration schemes can be tuned by the FW with real-application Bluetooth/ZB scenarios.

All design and intellectual property part of this arbiter design is a property of Microchip Inc. released under appropriate NDA.

40.5.1 Arbiter Modes

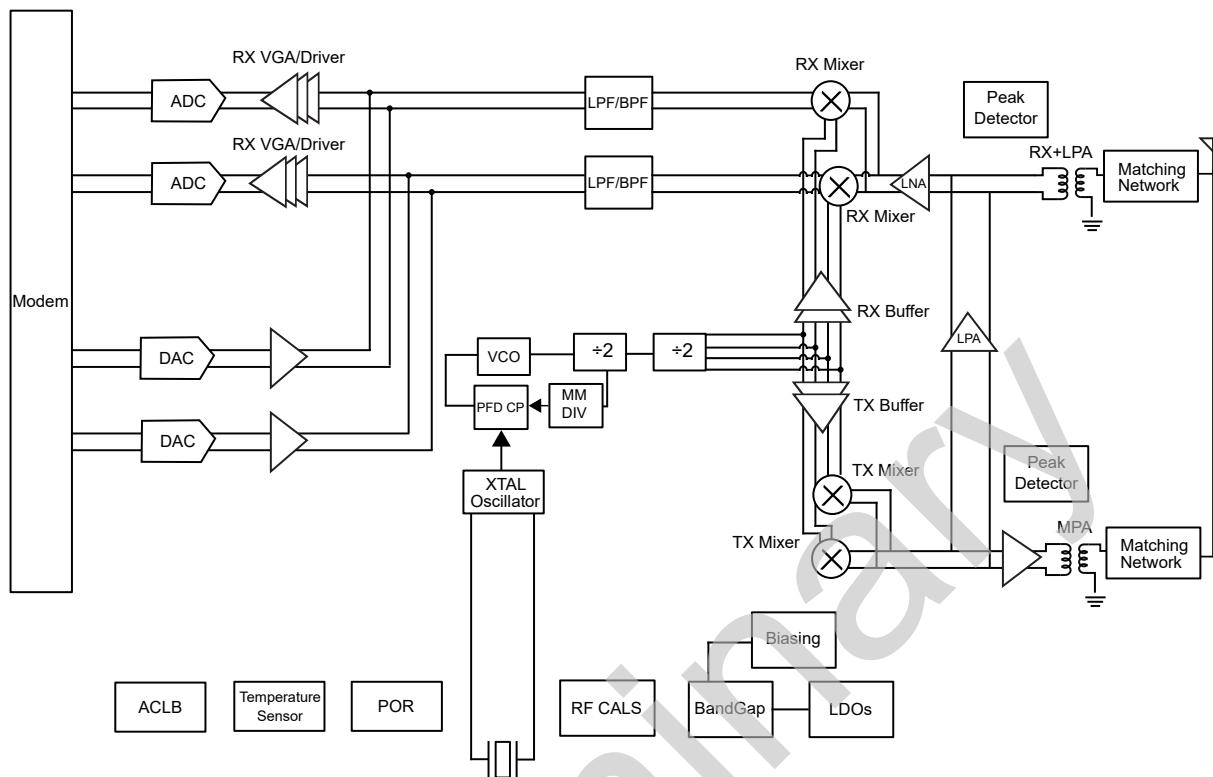
Following are the modes supported by the arbiter:

- Bluetooth static: Radio ownership is with Bluetooth Link controller
- ZB static: Radio ownership is with ZB Link controller
- Dynamic: Radio ownership decided dynamically at every arbitration event

40.6 RF Physical Layer

The top level block diagram of the transceiver architecture is as follows.

Figure 40-2. Transceiver Architecture



40.7 Frequency Synthesizer

PIC32CX-BZ2 and WBZ45 requires a 16 MHz for generating the local oscillator frequency between the 2.4 GHz to 2.48 GHz for the transmitter and receiver. The frequency synthesizer integrates all the passives for the loop filter inside the chip.

40.7.1 Transmit Mixer and Power Amplifier

PIC32CX-BZ2 and WBZ45 implements a direct conversion I/Q transmitter, the I/Q from the low pass filter of the Tx path is converted to the desired output frequency through an I/Q mixer which operates on the LO frequency from the Synthesizer, the VCO operates at 4x the LO frequency.

The supply for LPA and MPA is through separated power supply pins which can be connected to the output from the PMU with necessary de-coupling.

The LPA is a single stage amplifier provides ~6 dBm output power in standalone mode and ~4 dBm in LPA/MPA shared mode. Both LPA and MPA implements an on-chip BALUN, the LPA pin also act as the input to the RX section.

MPA is a 2 stage power amplifier designed to provide a maximum output power of ~10 dBm.

MPA also implements an on-chip BALUN to get a single ended TX output. MPA is NOT internally connected to the receiver.

It is mandatory to use the LPA pin for the Receiver path. On a typical application, the LPA and MPA can be connected directly eliminating the need for an external switch

40.7.2 Receiver

The receiver path starts with the LPA pin which is shared with the LPA path and the LNA. PIC32CX-BZ2 implements a low-IF differential receiver, the synthesizer generates the LO for down-conversion on the mixer which goes through a BPF filter to the ADC. The Receiver implements an AGC to adjust the LNA gain depending upon the input signal level.

40.8 RFLDO

The RF section has multiple LDO's to power the various power domains of the RF sub-system. All these LDO's can be powered up from the MLDO/DC-DC mode of the PMU and can get a 1.35V and generates a 1.2V internally to feed the corresponding RF sections. These LDO's need a by-pass capacitor on the output for their operation, see *Power Subsystem* from Related Links.

- RF-PLL
- BUCK-LPA
- BUCK-MPA
- BUCK-BB

Related Links

6. [Power Subsystem](#)

Preliminary

41. Electrical Characteristics

This chapter provides the Electrical Specification and Characteristic of PIC32CX-BZ2 and WBZ45 Modules across the operating temperature range of the product.

Electrical Characteristic at 125°C capture the characteristic of peripherals which have deviation of performance between 85°C and 125°C in which case only the 85°C specifications are captured on this chapter, see *Electrical Characteristics at 125°C* from Related Links for 125°C characteristic.

Related Links

[42. Electrical Characteristics at 125°C](#)

41.1 Absolute Maximum Electrical Characteristics

Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Table 41-1. Absolute Maximum Ratings

Parameter	Value
Ambient temperature under bias(^{Note})	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V _{DD} / V _{DDIO} with respect to GND	-0.3V to +4.0V
Voltage on any Non-5V tolerant pins, with respect to GND	-0.3V to (V _{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to GND when V _{DD} ≥ 1.9V	-0.3V to +5.25V
Voltage on any 5V tolerant pin with respect to GND when V _{DD} < 1.9V	-0.3V to (V _{DD} + 0.3V)
Maximum current out of GND pins	300 mA
Maximum current into V _{DD} pins ⁽²⁾	300 mA
Maximum output current sourced/sunk by any Low Current Mode I/O pin (4x drive strength)	10 mA
Maximum output current sourced/sunk by any High Current Mode I/O pin (8x drive strength)	15 mA
Maximum current sink by all ports	120 mA
Maximum current sourced by all ports ⁽²⁾	120 mA
ESD Qualification	
Human Body Model (HBM) per JESD22-A114	2000V
Charged Device Model (CDM) (ANSI/ESD STM 5.3.1)...(All pins / Corner pins)	+500V/- 500V

Notes:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- See Pinout and signal description tables for 5V tolerant pins.
- Maximum allowable current is a function of device maximum power dissipation (See *Thermal Operating Conditions* table in the *Thermal Specifications* from Related Links).

Related Links

[41.3. Thermal Specifications](#)

41.2 DC Electrical Characteristics

Table 41-2. Operating Frequency VS. Voltage

Param. No.	V _{DDIO} , V _{DDANA} Range	Temp. Range (in °C)	Max MCU Frequency	Comments
DC_5	1.9V to 3.6V	-40°C to +85°C	64 MHz	Industrial
DC_7	1.9V to 3.6V	-40°C to +125°C	64 MHz	Extended

Note: The same voltage must be applied to V_{DDIN} and V_{DDANA}.

41.3 Thermal Specifications

Table 41-3. Thermal Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices:					
Operating ambient temperature range	T _A	-40	—	+85	°C
Operating junction temperature range	T _J	-40	—	+105	°C
V-Temp Temperature Devices:					
Operating ambient temperature range	T _A	-40	—	+105	°C
Operating junction temperature range	T _J	-40	—	+125	°C
Extended Temperature Range:					
Operating ambient temperature range	T _A	-40	—	+125	°C
Operating junction temperature range	T _J	-40	—	+135	°C
Maximum allowed power dissipation	P _{DMAX}	(T _J – T _A)/Θ _{JA}			W

Table 41-4. Thermal Packaging Characteristics

Characteristics	Symbol	Typ	Max	Unit	Notes
Package thermal resistance, 32-pin QFN (5 mm x 5 mm x 0.9 mm)	Θ _{JA}	18	—	°C/W	(1)
Package thermal resistance, 48-pin QFN (7 mm x 7 mm x 1 mm)	Θ _{JA}	18	—	°C/W	(1)

Note:

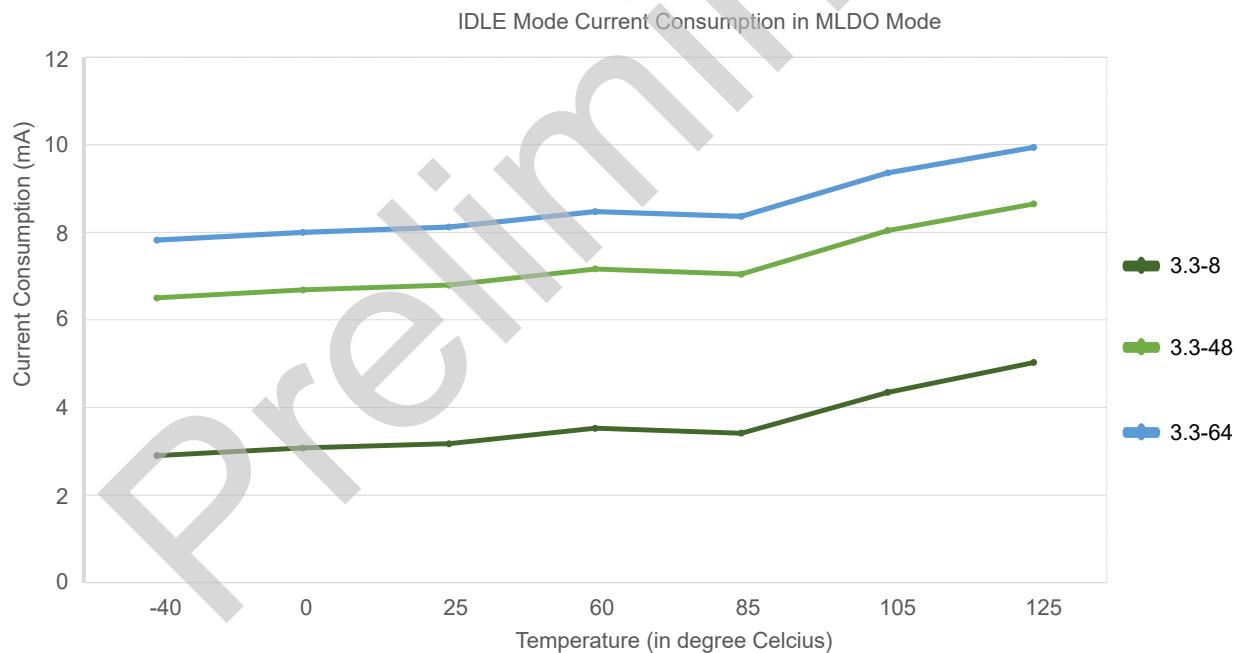
1. Junction to ambient thermal resistance, Θ_{JA} numbers are achieved by package simulations.

41.4 Active Current Consumption DC Electrical Specifications

Table 41-5. Active Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ ⁽¹⁾	Max.	Units	Conditions
APWR_1	I_{DD_ACTIVE} ^(2,3)	MCU I_{DD} in active mode w/LDO mode selected	PLL 64 MHz	131	—	$\mu\text{A}/\text{MHz}$	$V_{DD} = V_{DDANA} = 3.3\text{V}$
APWR_2			FRC 8 MHz	443			
APWR_3		MCU I_{DD} in active mode w/BUCK mode selected	PLL 64 MHz	76.8			
APWR_4			FRC 8 MHz	300			

Figure 41-1. IDLE Mode



PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. Typical value measured at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - RPA2 and RPA4 are configured as UART for communication.
 - RF system in IDLE state. Not transmitting or receiving packets.
 - All peripherals disabled (except SERCOM0).
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC disabled.
 - PMU 1 MHz clock derived from FRC. FRC is divided by 8.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - WCM memories configured in retention + NAP mode.
 - DSU is disconnected.
3. MCU running while (1) loop with 50 NOP instructions.

41.5 Idle Current Consumption DC Electrical Specifications

Table 41-6. Idle Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristic(s)	Clock/Freq	Typ ⁽¹⁾	Max.	Units	Conditions ⁽³⁾
IPWR_1	I_{DD_IDLE} ⁽²⁾	MCU I_{DD} in IDLE mode w/LDO mode selected	PLL 64 MHz	83	—	$\mu A/MHz$	$V_{DDIO} = V_{DDANA} = 3.3V$
IPWR_2			FRC 8 MHz	336			
IPWR_3		MCU I_{DD} in IDLE mode w/ BUCK mode selected	PLL 64 MHz	52.8	—		
IPWR_4			FRC 8 MHz	282			

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - RPA2 and RPA4 are configured as UART for communication.
 - All peripherals disabled (except SERCOM0 and EIC).
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC is disabled.
 - PMU is clocked at 1MHz from FRC. FRC divided by 8.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - Backup RAM in retention mode.
 - DSU is disconnected.
 - RF system clock gated.
 - Entry to sleep mode disabled and WFI instruction executed.
 - No active RF transmission or Reception during current measurement.

41.6 Sleep Current Consumption DC Electrical Specifications

Table 41-7. Sleep Current Consumption DC Electrical Specifications

DC Characteristics			V_{DDIO}	Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp			
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
SPWR_1	I_{DD_SLEEP}	MCU I_{DD} in Sleep mode w/LDO mode selected	3.3V	950	—	μA	XTAL _{ON}
			3.3V	620	—	μA	XTAL _{OFF}
SPWR_29		MCU I_{DD} in Sleep mode w/ BUCK mode selected	3.3V	470	—	μA	XTAL _{ON}
			3.3V	450	—	μA	XTAL _{OFF}

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled (except EIC).
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC is disabled.
 - CLDO configured at lowest possible voltage (VREG Trim = 0x07).
 - PMU configured to Buck PSM mode on Sleep Mode Entry with current sense disabled.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - Backup RAM in retention mode
 - DSU is disconnected.
 - RF system in low power configuration.
 - Entry to sleep mode enabled and WFI instruction executed.
 - In XTAL ON mode : PMU Buck clock is derived from POSC 16 MHz and scaled to 1 MHz. FRC is OFF.
 - In XTAL OFF mode : PMU is clocked from FRC and XTAL 16 MHz clock is disabled and clock configuration in CRU changed to FRC.

41.7 Deep Sleep Current Consumption DC Electrical Specifications

Table 41-8. Deep Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
BPWR_1	$I_{DD_BACKUP}^{(2)}$	MCU I_{DD} in Deep Sleep mode powered from V_{DDIO}	3.3V	1.2	—	μA	No backup RAM retained
BPWR_2			3.3V	1.5	—	μA	8 KB backup RAM retained

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled.
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC, POSC is disabled.
 - DSU is disconnected.
 - RF system in low power configuration.
 - DSWDT enabled and configured for wake-up.
 - Deep Sleep Entry configured and WFI instruction executed.

41.8 XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

Table 41-9. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
OPWR_1	$I_{DD_OFF}^{(2)}$	MCU I_{DD} in OFF mode powered from V_{DDIOX}	3.3V	0.12	—	μA	In OFF mode, the device is entirely powered-off. Note: This mode is left by pulling the RESET pin low, or when a power reset is done

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled.
 - DSU is disconnected.
 - RF system in low power configuration.
 - DSWDT disabled.
 - RTCC, POSC disabled.
 - Deep Sleep Entry configured and WFI instruction executed.

41.9 External XTAL and Clock AC Electrical Specifications

Table 41-10. External XTAL and Clock AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾
XOSC_1	FOSC_XOSC	XOSC Crystal frequency	—	16	—	MHz	
XOSC_1A	TOSC	$TOSC = 1/\text{FOSC}_XOSC$	—	0.0625	—	ns	See parameter XOSC1 for FOSC_XOSC value
XOSC_2	XOSC_ST ⁽²⁾	XOSC Crystal start-up time	—	—	2.5	ms	Crystal stabilization time only not oscillator ready ⁽²⁾

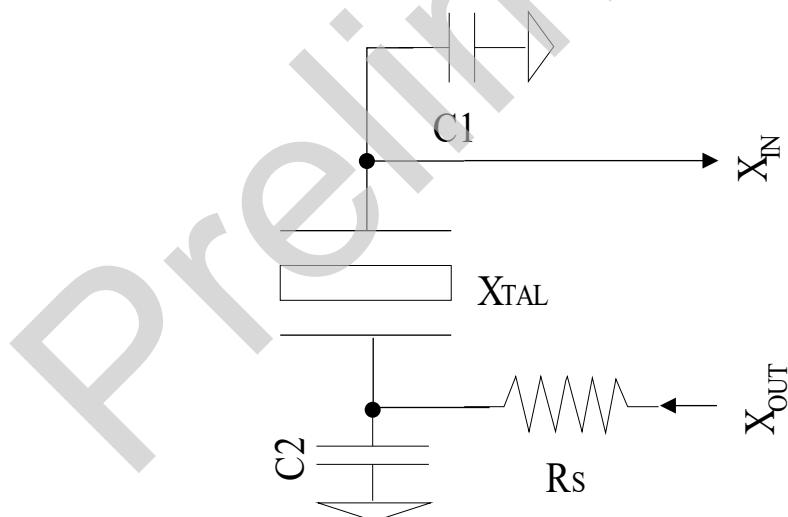
PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for Industrial Temp					
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾	
XOSC_3	CXIN	XOSC XIN Parasitic pin capacitance	—	0.35	—	pF	With Default Crystal trim settings	
XOSC_5	CXOUT	XOSC XOUT Parasitic pin capacitance	—	0.35	—	pF	With Default Crystal trim settings	
XOSC_11	CLOAD ⁽³⁾	XOSC Crystal FOSC = 16 MHz	—	9	—	pF		
XOSC_21	ESR	XOSC Crystal FOSC = 16 MHz	—	—	100	Ω		
XOSC_33	DLEVEL	MCU Crystal Oscillator Power Drive Level	—	—	100	μW		
XOSC_34	FREQ ERROR	Center Frequency Error	-30	—	+30	ppm	Across temperature	

Figure 41-2. External XTAL and Clock Diagram



PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. $V_{DDIO} = V_{DDANA} = 3.3V$.
2. Refer to RDP for information related to crystal trimming.
3. This is for guidance only. A major component of crystal start-up time is based on the 2nd party crystal MFG parasitics that are outside the scope of this specification.
4. The test conditions for crystal load capacitor calculation are as follows:
 - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W=0.175 mm, H=36 μ m, T=113 μ m)
 - Xtal PCB capacitance typical therefore \approx 2.5 pF for a tight PCB xtal layout
 - For CXIN and CXOUT within 4 pF of each other, Assume CXTAL_EFF = ((CXIN+CXOUT) / 2)
 - **Note:** Averaging CXIN and CXOUT will effect final calculated CLOAD value by less than 0.25 pF.

Equation 41-1. Equation 1:

*MFG CLOAD Spec = {([CXIN + C1] * [CXOUT + C2]) / [CXIN + C1 + C2 + CXOUT]} + estimated oscillator PCB stray capacitance*

Assuming C1 = C2 and CXin \approx CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

Equation 41-2. Equation 2 (In other words: Simplified Equation 1)

$C1 = C2 = ((2 * MFG CLOAD Spec) - CXTAL_EFF - (2 * PCB capacitance))$

Example:

- XTAL Mfg CLOAD Data Sheet Spec = 12 pF
- PCB XTAL trace Capacitance = 2.5 pF
- CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = ((CXIN+CXOUT) / 2)

$$CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 \text{ pF}$$

$$C1 = C2 = ((2 * MFG Cload spec) - CXTAL_EFF - (2 * PCB capacitance))$$

$$C1 = C2 = (24 - 5.5 - (2 * 2.5))$$

$$C1 = C2 = 13.5 \text{ pF} \text{ (Always rounded down)}$$

C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)

User C1=C2=13 pF CLOAD (max) spec

41.10 XOSC32 AC Electrical Specifications

Table 41-11. XOSC32 AC Electrical Specifications

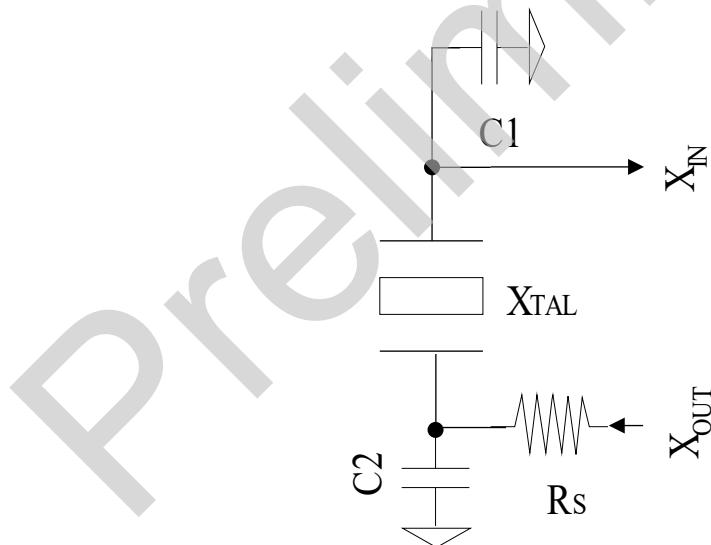
AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾
XOSC32_1	FOSC_XOSC32	XOSC32 Oscillator crystal frequency	—	32.768	—	kHz	XIN32, XOUT32 Secondary oscillator
XOSC32_3	CXIN32	XOSC32 XIN32 Parasitic pin capacitance	—	0.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the Module
				2.4			

PIC32CX-BZ2 and WBZ45 Family Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾
XOSC32_5	CXOUT32	XOSC32 XOUT32 Parasitic pin capacitance on PIC32CX-BZ2	—	0.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the Module
				2.4			
XOSC32_11	CLOAD_X32 ⁽³⁾	32.768 kHz Crystal load capacitance	—	11	—	pF	
XOSC32_13	ESR_X32	32.768 kHz Crystal ESR	—	75	—	KΩ	
XOSC32_15	TOSC32	TOSC32 = 1/ FOSC_XOSC32	—	30.518	—	μs	See parameter XOSC32_1 for FOSC_XOSC32 value
XOSC32_17	XOSC32_ST ⁽²⁾	XOSC32 Crystal start-up time	—	23	—	ms	This includes system delay and cannot be considered as the exact start-up time of SOSC clock as it is brought out on REFOx

Figure 41-3. XOSC32 Block Diagram



PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. $V_{DDIO} = V_{DDANA} = 3.3V$.
2. This is for guidance only. A major component of crystal start-up time is based on the 2nd party crystal MFG parasitics that are outside the scope of this specification. If this is a major concern, the customer would need to characterize this based on their design choices.
3. The test conditions for crystal load capacitor calculation are as follows:
 - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W=0.175 mm, H=36 μ m, T=113 μ m)
 - Xtal PCB capacitance typical therefore ~ 2.5 pF for a tight PCB xtal layout
 - For CXIN and CXOUT within 4 pF of each other, Assume CXTAL_EFF = ((CXIN / 2))
 - **Note:** Averaging CXIN and CXOUT will effect final calculated CLOAD value by less than the tolerance of the capacitor selection.

4. **Equation 41-3. Equation 1:**

*MFG CLOAD Spec = {[CXIN + C1] * [CXOUT + C2]} / [CXIN + C1 + C2 + CXOUT] + estimated oscillator PCB stray capacitance*

Assuming C1 = C2 and CXin \sim CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

Equation 41-4. Equation 2 (In other words: Simplified Equation 1)

$C1 = C2 = ((2 * MFG CLOAD Spec) - CXTAL_EFF - (2 * PCB capacitance))$

Example:

- XTAL Mfg CLOAD Data Sheet Spec = 12 pF
- PCB XTAL trace Capacitance = 2.5 pF
- CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = ((CXIN / 2))

$$CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 \text{ pF}$$

$$C1 = C2 = ((2 * MFG Cload spec) - CXTAL_EFF - (2 * PCB capacitance))$$

$$C1 = C2 = (24 - 5.5 - (2 * 2.5))$$

$$C1 = C2 = (24 - 5.5 - 5)$$

$$C1 = C2 = 13.5 \text{ pF} \text{ (Always rounded down)}$$

C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)

User C1 = C2 = 13 pF \leq CLOAD_X32 (max) spec

41.11 Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

Table 41-12. Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
LP32K_1	FOSC_LP32K	Output frequency	—	32.768	—	kHz	Factory default calibration
LP32K_3	LP32K_ACC	Accuracy	—	—	—	kHz	—
LP32K_9	RC32K_Duty	LPRC32K OSC duty cycle	—	50	—	%	—

41.12 FRC AC Electrical Specifications

Table 41-13. FRC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
FRC1	FINTFREQ	Internal FRC frequency	—	8	—	MHz	Factory calibrated and user trim bits set to zero
FRC2	TSUFRC	Start-up time of internal FRC	—	15	—	μs	Not characterized
FRC3	FACCU	FRC Accuracy	—	—	—	%	—
FRC5	DUTY_CYCLE	FRC Duty Cycle	—	50	—	%	—
FRC6	C_USE	FRC User Tune Frequency Drift	—	-1.625 +1.65	—	%	Frequency Drift = [(Maximum Frequency Measured - Minimum Frequency Measured) / (Default Frequency of 8 MHz)] * 100 Maximum Frequency drift possible by using the Frequency trim bits
FRC7	C_USER_STEP_SIZE	FRC User Tune Step size	—	0.046	—	%	Step Size = (% Drift Across Osc Tune) / (Total Number of Trim Bit Combinations); Change in frequency with incremental trim bit

41.13 Frequency AC Electrical Specifications

Table 41-14. Frequency AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
MCU_1	FCY	MCU Frequency of operation	—	—	64	MHz	$V_{DDIO(\min)} \text{ to } V_{DDIO(\max)}$
MCU_3	TCY	MCU Clock period	1/FCY			μs	

PLL (Phase Locked Loop) AC Electrical Specifications

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Table 41-15. PLL MHz (Phase Locked Loop)

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
PLL_1	PLL_FIN	PLL Input frequency	—	16	—	MHz	—
PLL_3	PLL_FOUT	PLL Output clock frequency	—	96	—	MHz	—
PLL_4	PLL_VCO_FREQ	PLL VCO Frequency (Fixed)	—	480	—	MHz	—

Note:

1. PLL input clock is 16 MHz XOSC.

41.14 QSPI Module Electrical Specifications

Table 41-16. QSPI Module Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
QSPI_1	FCLK	SQI Serial Clock Frequency • SDR Master Mode 0 & 2	—	—	32	MHz	—
QSPI_2	FCLK	SQI Serial Clock Frequency • SDR Master Mode 1 & 3	—	—	32	MHz	—
QSPI_3	TSCKH	Serial Clock High Time	—	8.9	—	ns	—
QSPI_5	TSCKL	Serial Clock Low Time	—	7.8	—	ns	—
QSPI_7	TSCKR	Serial Clock Rise Time	—	6.95	—	ns	—
QSPI_9	TSCKF	Serial Clock Fall Time	—	7.6	—	ns	—
QSPI_11	TCSS	CS Active Setup Time	—	7.3	—	ns	—

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
QSPI_13	TCSH	CS Active Hold Time	—	10.42	—	ns	—
QSPI_19	TDIS	Data In Setup Time	—	7.4	—	ns	—
QSPI_21	TDIH	Data In Hold Time	—	19.8	—	ns	—
QSPI_23	TDOH	Data Out Hold	—	18	—	ns	—
QSPI_25	TDOV	Data Out Valid	—	2.4	—	ns	—

Note:

1. $V_{DDIO} = 3.3\text{V}$, CLOAD=30 pF(MIN)

41.15 Power Supply DC Module Electrical Specifications

Table 41-17. Power Supply DC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_1	VDDCORE_CIN	VDDCORE(CLDO_OUT) Input Bypass parallel Capacitor pair ⁽⁵⁾	—	1	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_5	VDD33	VDD33 Input Bypass parallel Capacitor pair ⁽⁵⁾	—	10	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω (6)
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on tempearture on all VDDIO pins (6)

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_6	PMU_VDDIO	Input Bypass parallel Capacitor pair for the PMU Power Section ⁽⁵⁾	—	4.7	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5 Ω (6)
			—	—	—	nF	Ceramic XR7/X5R with ESR <0.5 Ω depending on temperature on all VDDIO pins (6)
REG_7	PMU_VDDP	Input Bypass parallel Capacitor pair for the PMU Power Section ⁽⁵⁾	—	1	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5 Ω (6)
			—	—	—	nF	Ceramic XR7/X5R with ESR <0.5 Ω depending on temperature on all VDDIN pins (6)
REG_9	VDDFLASH_CIN	VDD_FLASH Bypass parallel Capacitor pair ⁽⁵⁾	—	10	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5 Ω (6)
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5 Ω depending on temperature on all VDDFLASH pins (6)
REG_17	VDDANA_CIN	VDDANA Input Bypass parallel Capacitor pair ⁽⁵⁾	—	10	—	μF	Bulk Ceramic or solid Tantalum with ESR <0.5 Ω (6)
			—	0.1	—	nF	Ceramic XR7/X5R with ESR <0.5 Ω
REG_18	VDDANA_LEXT	VDDANA series Ferrite Bead DCR (DC Resistance)	—	—	0.1	Ω	≥ 600 Ohms @ 100 MHz
REG_19		Ferrite Bead current Rating	100	—	—	mA	—
REG_20	BUCK_PLL_CIN	VDD Bypass capacitor on the BUCK_PLL Input	—	1	—	μF	Ceramic XR7/X5R with ESR <0.5 Ω
REG_21	BUCK_BB_CIN	VDD Bypass capacitor on the BUCK_BB Input	—	1	—	μF	Ceramic XR7 with ESR <0.5 Ω
REG_22	BUCK_MP_A_CIN	VDD Bypass capacitor on the BUCK_LPA Input	—	1	—	μF	Ceramic XR7 with ESR <0.5 Ω

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_23	BUCK_LPA_CIN	VDD Bypass capacitor on the BUCK_MPA Input	—	1	—	μF	Ceramic XR7 with ESR <0.5 Ω
REG_24	BUCK_CLDO_CIN	VDD Bypass capacitor on the BUCK_CLDO Input	—	1	—	μF	Ceramic XR7 with ESR <0.5 Ω
REG_25	R_EXT	Master Bias for the reference current generation	—	30	—	k Ω	—
REG_27	VSW_L _{EXT} ^(2,3)	Buck Switch Mode Regulator Inductor Inductance	—	4.7	—	μH	Shielded Inductor ONLY
REG_29		Inductor DCR (DC Resistance)	—	—	0.22	Ω	—
REG_31		Inductor I_{SAT} Rating ⁽²⁾	250	—	—	mA	—
REG_32	VSW_CAP _{EXT}	Buck Switch Mode Regulator Bulk Capacitor Capacitance	10	—	—	μF	—
REG_32A		Buck Switch Mode Regulator Filtering Capacitor Capacitance	100	—	—	nF	—
REG_36	VDDCORE	VDDCORE Voltage Range	—	1.2	—	V	MCU Active, cache and prefetch disabled executing "while ⁽¹⁾ " from flash
REG_37	VDD33 ⁽⁴⁾	VDD33 Input Voltage Range	1.9	3.3	3.6	V	—
REG_39	VDDANA ⁽⁴⁾	VDDANA Input Voltage Range	1.9	3.3	3.6	V	—
REG_40	VDDREG	VDDREG Input Voltage Range	—	1.35	—	V	PMU Output Voltage
REG_43	SVDDIO_R	VDDIO Rise Ramp Rate to Ensure Internal Power-on Reset Signal	—	0.11	—	V/ μs	Failure to meet this specification may lead to start-up or unexpected behaviors

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_44	SVDDIO_F	VDDIO Falling Ramp Rate to Ensure Internal Power-on Reset Signal	—	—	—	V/ μs	Failure to meet this specification may cause the device to not detect reset
REG_45	VP0R+	Power-on Reset	1.54	1.59	1.65	V	VDDIO Power up/Down (See Param REG43, VDDIO Ramp Rate)
REG_45_A	VP0R-	Power-on Reset	1.53	1.56	1.59	V	VDDIO Power up/Down (See Param REG43, VDDIO Ramp Rate)
REG_47	VBOD33 ⁽⁴⁾	VDDIO BOD (All modes) ⁽⁴⁾	—	1.787	—	V	—
REG_48	VBOR12	BOR of the 1.2V regulator	—	1.09	—	V	—
REG_48A	VZBPOR33	Zero Power BOR	—	1.8	—	V	—
REG_49	VBOR33L2_H	BOR 3.3V low to high switch point	—	1.84	—	V	—
REG_50	VBOR1P2L_2H	BOR 1.2V low to high switch point	—	1.1	—	V	—
REG_51	VBOD12 _{HY} _ST_STEP	VBOD12 Hysteresis step size	—	10.5	—	mv	Step Size
REG_52	VBOD33 _{HY} _ST_STEP	VBOD33 Hysteresis step size	—	51.6	—	mv	Step Size
REG_53	TRST ⁽⁶⁾	External RESET valid active pulse width	—	11	—	μs	Minimum reset active time to guarantee MCU reset for the module. Reset filter circuit inside Module
			—	2.5	—	μs	Minimum reset active time to guarantee MCU reset for SoC with no reset filter circuit

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. Ferrite Bead ISAT(min) \geq (IDDANA(max) * 1.15)
2. Buck Inductor ISAT(min) \geq ((ICAPACITOR + IVDDCORE_MAX) * 1.2) when BUCK mode enabled (Shielded inductor only)
3. User must select either LDO or BUCK Mode. The modes are exclusive of each other.
4. VDD33 and VDDANA must be at the same voltage level
5. All bypass caps should be located immediately adjacent to pin(s) and on the same side of the PCB as the MCU. Each primary power supply group VDDIO, VDDANA, VDDCORE should have one bulk capacitor and all power pins everywhere a 100nf bypass cap.
6. The RESET pulse width is the minimum pulse width required on the IO pin after any filtering on the NMCLR pin

41.16 I/O PIN AC/DC Electrical Specifications

Table 41-18. I/O PIN AC/DC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
DI_1	VOL	Output voltage low (Drive Strength, 8x)	—	0.127	0.183	V	VDDIO = 3.3V @ IOL= 10 mA
		Output voltage low (Drive Strength, 4x)		0.228	0.324		VDDIO = 3.3V @ IOL= 10 mA
DI_2	VOL	Output voltage low (Drive Strength, 8x)	—	0.178	0.241	V	VDDIO = 3.3V @ IOL= 13 mA
		Output voltage low (Drive Strength, 4x)		0.292	0.439		VDDIO = 3.3V @ IOL= 13 mA
DI_3	VOL	Output voltage low (Drive Strength, 8x)	—	0.206	0.282	V	VDDIO = 3.3V @ IOL= 15 mA
DI_4	VOH	Output voltage low (Drive Strength, 8x)	2.289	3.519	—	V	VDDIO = 3.3V @ IOH= 5 mA
		Output voltage low (Drive Strength, 4x)	2.12	3.4	—		VDDIO = 3.3V @ IOH= 5 mA
DI_5	VOH	Output voltage low (Drive Strength, 8x)	2.23	3.48	—	V	VDDIO = 3.3V @ IOH= 7 mA
		Output voltage low (Drive Strength, 4x)	2.044	3.35	—		VDDIO = 3.3V @ IOH= 7 mA

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
DI_6	VOH	Output voltage High (Drive Strength, 8x)	2.174	3.136	—	V	$V_{DDIO} = 3.3\text{V}$ @ $\text{IOH}=10\text{ mA}$
DI_7	VIL	Output voltage low (Drive Strength, 8x)	0.5	0.75	—	V	$V_{DDIO} = 3.3\text{V}$
		Output voltage low (Drive Strength, 4x)	0.3	0.53	—		$V_{DDIO} = 3.3\text{V}$
DI_8	VIH	Input voltage high (Drive Strength, 8x)	2.6	2.85	3.3	V	$V_{DDIO} = 3.3\text{V}$ non 5V tolerant pins
			2.6	2.85	5.5		5V tolerant pins
		Input voltage high (Drive Strength, 4x)	2.6	2.85	3.3		$V_{DDIO} = 3.3\text{V}$ non 5V tolerant pins
			2.6	2.85	5.5		5V tolerant pins
DI_13	IIL	Input pin leakage current (Drive Strength, 8x)	—	71.8	—	nA	—
		Input pin leakage current (Drive Strength, 4x)	—	353	—	nA	—
DI_15	RPDWN	Internal Pull-Down (Drive Strength, 8x)	—	21.4	—	k Ω	$V_{DDIO} = 3.3\text{V}$
		Internal Pull-Down (Drive Strength, 4x)	—	3.9	—	k Ω	
DI_17	RPUP	Internal Pull-Up (Drive Strength, 8x)	—	18.65	—	—	
		Internal Pull-Up (Drive Strength, 4x)	—	3.3	—	k Ω	

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
DI_25	TRISE	I/O pin Rise Time (High Drive Strength, High load)	—	1.97	—	ns	$V_{DDIO} = 3.3\text{V}$
		I/O pin Rise Time (Low Drive Strength, High load)	—	10.709	—	ns	—
		I/O pin Rise Time (High Drive Strength, Standard load)	—	2.048	—	ns	—
		I/O pin Rise Time (Low Drive Strength, Standard load)	—	7.66	—	ns	—
DI_27	TFALL	I/O pin Fall Time (High Drive Strength, High load)	—	1.59	—	ns	—
		I/O pin Fall Time (Low Drive Strength, High load)	—	8.166	—	ns	—
		I/O pin Fall Time (High Drive Strength, Standard load)	—	1.619	—	ns	—
		I/O pin Fall Time (Low Drive Strength, Standard load)	—	5.146	—	ns	—

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. All measurements done at 3.3V at 25°C.
2. VIL source < (GND - 0.3). Characterized but not tested.
3. VIH source > (VDDIO + 0.3) for non-5V tolerant pins only.
4. Digital 5V tolerant pins do not have an internal high side Diode to VDDIO , and therefore, cannot tolerate any "positive" input injection current.
5. Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified $\sum I_{ICT}$ limit. To limit the injection current the user must insert a resistor in series RSERIES, (i.e. RS), between input source voltage and device pin. The resistor value is calculated according to:
 - For negative Input voltages less than (GND-0.3): $RS \geq \text{absolute value of } |(V_{IL} \text{ source} - (GND - 0.3)) / I_{ICL}|$
 - For positive input voltages greater than (VDDIO +0.3): $RS \geq |(V_{IH} \text{ source} - (VDDIO +0.3)) / I_{IICH}|$
 - For Vpin voltages >VDDIO +0.3 and <GND-0.3 then RS = the larger of the values calculated above
6. Highload = 50 pF and Standard load = 30 pF

41.17 I2C Module Electrical Specifications

Table 41-19. I2C Module Master Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
I2CM_1	TL0:SCL	Master Clock Low Time	100 kHz mode	—	5020	—	ns	VDDIOx = 3.3V,
			400 kHz mode	—	1280	—	ns	
			1 MHz mode	—	712	—	ns	
I2CM_5	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	19	—	ns	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf
			400 kHz mode	—	5	—	ns	
			1 MHz mode	—	5	—	ns	
I2CM_7	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	166	—	ns	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	154	—	ns	
			1 MHz mode	—	154	—	ns	

PIC32CX-BZ2 and WBZ45 Family Electrical Characteristics

.....continued

AC Characteristics				Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
I2CM_9	TSU:DAT	Data Input Setup Time	100 kHz mode	—	4900	—	ns	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	1200	—	ns	
			1 MHz mode	—	592	—	ns	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CM_11	THD:DAT	Data Input Hold Time	100 kHz mode	—	159	—	ns	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	93	—	ns	
			1 MHz mode	—	140	—	ns	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CM_13	TSU:STA	Start Condition Setup Time	100 kHz mode	—	5180	—	μs	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	1450	—	ns	
			1 MHz mode	—	867	—	ns	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CM_15	THD:STA	Start Condition Hold Time	100 kHz mode	—	4990	—	μs	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	1250	—	μs	
			1 MHz mode	—	666	—	μs	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CM_21	TAA:SCL	Output Valid from Clock	100 kHz mode	—	—	—	ns	VDDIOx = 3.3V, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	—	—	ns	
			1 MHz mode	—	—	—	ns	VDDIOx = 3.3V, IPULL-UP = 20 ma, CLOAD = 550 pf

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics				Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
I2CM_23	TBF:SDA	Bus Free Time (1)	100 kHz mode	—	TL0:SC L	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	TL0:SC L	—	ns	
			1 MHz mode	—	TL0:SC L	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 20 ma, CLOAD = 550 pf

Note:

1. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition)

Table 41-20. I2C Module Slave Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
I2CS_5	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	—	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	—	—	ns	
			1 MHz mode	—	—	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CS_7	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	—	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	—	—	ns	
			1 MHz mode	—	—	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 20 ma, CLOAD = 550 pf
I2CS_9	TSU:DAT	Data Input Setup Time	100 kHz mode	—	5580	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	1470	—	ns	
			1 MHz mode	—	—	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 20 ma, CLOAD = 550 pf

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
I2CS_11	THD:DAT	Data Input Hold Time	100 kHz mode	—	490	—	ns	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 3 ma, CLOAD = 400 pf
			400 kHz mode	—	490	—	ns	
			1 MHz mode	—	—	—	μs	$V_{DDIOx} = 3.3\text{V}$, IPULL-UP = 20 ma, CLOAD = 550 pf

Note:

1. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition)

41.18 SPI Module Electrical Specifications

Table 41-21. SPI Module Master Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics		Min.	Typ	Max.	Units	Conditions
MSP_1	FSCK	SCK Frequency	—	32	—	—	MHz	Fixed pins
			—	24	—	—		Remappable pins
MSP_3	TSCL	SCK Output Low Time	—	31.25	—	—	ns	—
MSP_5	TSCH	SCK Output High Time	—	31.25	—	—	ns	—
MSP_7	TSCF	SCK & MOSI Output Fall Time	—	1.8	—	—	ns	See parameter DI27 I/O spec
MSP_9	TSCR	SCK & MOSI Output Rise Time	—	1.8	—	—	ns	See parameter DI25 I/O spec

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
MSP_11	TMOV	MOSI Data Output Valid after SCK	—	11	—	ns	VDDIOx(min), CLOAD = 30 pf(MIN)
MSP_13	TMOH	MOSI hold after SCK	—	15	—	ns	
MSP_15	TMIS	MISO Setup Time of Data Input to SCK	—	23	—	ns	
MSP_17	TMIH	MISO Hold Time of Data Input to SCK	—	8	—	ns	

Note:

- Assumes VDDIOx(min) and 30pF external load on all SPIx pins unless otherwise noted.

Table 41-22. SPI Module Slave Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SSP_1	FSCK	SCK Frequency	—	16	16	MHz	VDDIOx = 1.9V or VDDIO(min) whichever is greater, CLOAD = 30 pf(MIN)
			—	—	—	—	—
SSP_3	TSCL	SCK Output Low Time	—	62.5	—	—	—
SSP_5	TSCH	SCK Output High Time	—	62.5	—	—	—
SSP_7	TSCF	SCK & MOSI Output Fall Time	—	3	—	ns	See parameter DI27 I/O spec
SSP_9	TSCR	SCK & MOSI Output Rise Time	—	26	—	ns	See parameter DI25 I/O spec

PIC32CX-BZ2 and WBZ45 Family Electrical Characteristics

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SSP_11	TSOV	MOSI Data Output Valid after SCK	—	21	—	ns	$V_{DDIO} = 3.3\text{V}$, CLOAD = 30 pF(MIN)
SSP_15	TSIS	MISO Setup Time of Data Input to SCK	7	23	—	ns	
SSP_17	TSIH	MISO Hold Time of Data Input to SCK	0	22	—	ns	

41.19 ADC Electrical Specifications

Table 41-23. ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
ADC_1	V_{DDANA}	ADC Supply	$V_{DDANA(min)}$	—	$V_{DDANA(max)}$	V	$V_{DDIO} = V_{DDANA}$
Reference Inputs							
ADC_3	$V_{REF}^{(4)}$	ADC Reference Voltage ⁽⁴⁾	—	—	V_{DDANA}	V	External Reference Voltage
Analog Input Range							
ADC_7	AFS	Full-Scale Analog Input Signal Range (Single-Ended)	0	—	V_{DDANA}	V	$V_{REF} = V_{DDANA(max)}$
ADC_9		Full-Scale Analog Input Signal Range (Differential)	$-V_{DDANA}/2$	—	$V_{DDANA}/2$	V	

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Table 41-24. ADC Single-Ended Mode AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions	
Single-Ended Mode ADC Accuracy								
SADC_11	Res	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 bit Resolution Ranges	
SADC_13	EN0B ⁽³⁾	Effective Number of bits	—	9.3	—	bits	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_19	INL ⁽³⁾	Integral Nonlinearity	—	-5.2 2.7	—	Lsb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_25	DNL ⁽³⁾	Differential Nonlinearity	—	-1 1.8	—	Lsb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_31	GERR ⁽³⁾	Gain Error	—	-0.7	—	Lsb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_37	E0FF ⁽³⁾	Offset Error	—	3.2	—	Lsb	2 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
Single-Ended Mode ADC Dynamic Performance								
SADC_49	SINAD ^(1,2,3)	Signal to Noise and Distortion	—	57.8	—	dB	$V_{REF} = V_{DDANA} = V_{DDIO} = 3.3\text{V}$ @ 12-bit resolution, max sampling rate ^(1,2)	
SADC_51	SNR ^(1,2,3)	Signal to Noise ratio	—	58.2	—			
SADC_53	SFDR ^(1,2,3)	Spurious Free Dynamic Range	—	66.25	—			
SADC_55	THD ^(1,2,3,5)	Total Harmonic Distortion	—	-71.3	—			

Notes:

1. Characterized with an analog input sine wave = (FTP(max) / 100). Example: FTP(max)=1 Msps/100 = 10 KHz sine wave.
2. Sinewave peak amplitude = 96% ADC_Full Scale amplitude input with 12-bit resolution.
3. Spec values collected under the following additional conditions:
 - a. 12-bit resolution mode.
 - b. All registers at reset default value otherwise not mentioned.
4. ADC Measurements done with 3.3V V_{REF} Voltage.
5. Value taken over 7 harmonics.
6. Referred to as AVDD in the Pinout and signal description tables for 5V tolerant pins..

PIC32CX-BZ2 and WBZ45 Family Electrical Characteristics

Table 41-25. ADC Conversion AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
ADC_Clock Requirements							
ADC_57	TAD	ADC Clock Period	—	20.83	—	ns	$V_{REF} = V_{DDANA} = 3.3\text{V}$
ADC Single-Ended Throughput Rates							
ADC_59	FTPR (Single-Ended Mode)	Throughput Rate ⁽²⁾ (Single-Ended)	—	1.7	—	MspS	12-bit resolution, DIV_SHR = 2
			—	0.773	—		12-bit resolution, DIV_SHR = 4

Notes:

1. Conversion_time = (SAMC_SHR+15)*TAD.
2. FTPR = $1 / ((\text{SAMC_SHR} + \text{Resolution} + 1) * (1 / (\text{ControlClk} / \text{DIV_SHR})))$.

Table 41-26. ADC Sample AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Temp					
Param. No.	Symbol	Characteristic s	Min.	Typical	Max.	Units	Conditions	
ADC_65	TCNV	Conversion Time ⁽¹⁾ (Single-Ended Mode)	14			TAD	12-bit resolution	
			12				10-bit resolution	
			10				8-bit resolution	
ADC_67		Conversion Time ⁽¹⁾ (Differential Mode)	14			TAD	12-bit resolution	
			12				10-bit resolution	
			10				8-bit resolution	
ADC_69	CSAMPL_E	ADC Internal Sample Cap	—	5	—	pf		
ADC_71	RSAMPL_E	ADC Internal impedance	—	—	200	Ω		

Note:

1. ADC Throughput Rate FTP = $((1 / ((\text{TSAMP} + \text{TCNV}) * \text{TAD})) / (\# \text{ of user active analog inputs in use on specific target ADC module}))$.

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

41.20 BLE RF Characteristics Electrical Specifications

Table 41-27. BLE RF Characteristics Electrical Specifications

Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
BTG1	FREQ	Frequency range of operation	2400	—	2480	MHz	—
BTTX1	TXPWR:MPA	Bluetooth transmit power MPA	—	11.5	—	dBm	—
BTTX2	TXPWR:LPA	Bluetooth transmit power LPA	—	4.0	—	dBm	—
BTX3	TXIB:1MBPS	In-band emission for FTX ± -2 MHz	—	-32	—	dBm	—
		In-band emission for FTX ± -(3+N) MHz	—	-45	—	dBm	—
BTX4	TXIB:2MBPS	In-band emission for FTX±-4MHz	—	-43	—	dBm	—
		In-band emission for FTX ± -5 MHz	—	-48	—	dBm	—
		In-band emission for FTX ± -(6+N) MHz	—	-51	—	dBm	—
BTRX1	RXSENSE	Receiver sensitivity @ 1 Mbps	—	-95.5	—	dBm	(1)
		Receiver sensitivity @ 2 Mbps	—	-92.5	—	dBm	(5)
		Receiver sensitivity @ S = 2	—	-98.5	—	dBm	(5)
		Receiver sensitivity @ S = 8	—	-102	—	dBm	(5)
BTRX2	MAXINSIG	Maximum input signal level @ 1 Mbps	—	0	—	dBm	—
		Maximum input signal level @ 2 Mbps	—	0	—	dBm	—
		Maximum input signal level @ S = 2	—	0	—	dBm	—
		Maximum input signal level @ S = 8	—	0	—	dBm	—
BTRX3 ⁽⁴⁾	CI1M:COCH	C/I Co channel rejection	—	13	—	dB	—
	CI1M: ± -1 MHz	C/I adjacent channel rejection	—	13	—	dB	—
	CI1M: ± -2 MHz	C/I adjacent channel rejection	—	13	—	dB	—
	CI1M:ADJ(3+n)	C/I alternate channel rejection	—	15	—	dB	—
	CI1M:IMG	C/I image frequency rejection	—	15	—	dB	—
	CI1M:IMG ± -1 MHz	C/I adjacent channel to image freq rejection	—	14	—	dB	—

PIC32CX-BZ2 and WBZ45 Family Electrical Characteristics

.....continued

Param. No.	Symbol	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
BTRX4 ⁽⁴⁾	CIS2:COCH	C/I Co channel rejection	—	11	—	dB	—
	CIS2: ± 1 MHz	C/I adjacent channel rejection	—	17	—	dB	—
	CIS2: ± 2 MHz	C/I adjacent channel rejection	—	18	—	dB	—
	CIS2:ADJ(3+n)	C/I alternate channel rejection	—	17	—	dB	—
	CIS2:IMG	C/I image frequency rejection	—	14	—	dB	—
	CIS2:IMG ± -1 MHz	C/I adjacent channel to image freq rejection	—	18	—	dB	—
BTRX5 ⁽⁴⁾	CIS8:COCH	C/I Co channel rejection	—	6	—	dB	—
	CIS8:±1 MHz	C/I adjacent channel rejection	—	13	—	dB	—
	CIS8: ± 2 MHz	C/I adjacent channel rejection	—	13	—	dB	—
	CIS8:ADJ(3+n)	C/I alternate channel rejection	—	14	—	dB	—
	CIS8:IMG	C/I image frequency rejection	—	8	—	dB	—
	CIS2:IMG ± -1 MHz	C/I adjacent channel to image freq rejection	—	16	—	dB	—
BTRX6 ⁽⁴⁾	CI2M:COCH	C/I Co channel rejection	—	13	—	dB	—
	CI2M: ± -2 MHz	C/I adjacent channel rejection	—	16	—	dB	—
	CI2M: ± -4 MHz	C/I adjacent channel rejection	—	19	—	dB	—
	CI2M:ADJ(6+2n)	C/I alternate channel rejection	—	16	—	dB	—
	CI2M:IMG	C/I image frequency rejection	—	13	—	dB	—
	CI2M:IMG ± -2 MHz	C/I adjacent channel to image freq rejection	—	19	—	dB	—
BTRX7 ⁽⁴⁾	BLOCK1M:<2 GHz	Blocking performance from 30 MHz to 2 GHz	—	20	—	dB	—
	BLOCK1M:2 GHz<SIG<2399 MHz	Blocking performance from 2003 MHz to 2399 MHz	—	14	—	dB	—
	BLOCK1M:2484 MHz<SIG<2977 MHz	Blocking performance between 2484 MHz to 2977 MHz	—	20	—	dB	—
	BLOCK1M:3 GHz<SIG<12.75 GHz	Blocking performance between 3 GHz to 12.5 GHz	—	20	—	dB	—
BTRX8 ⁽⁴⁾	BLE1M:INTERMOD	Inter modulation performance for BLEM	—	13.5	—	dB	—
	BLE2M:INTERMOD	Inter modulation performance for BLEM	—	19.5	—	dB	—

Notes:

1. Measured at 25°C, averaged across all voltages and channels
2. Measured on a board with the reference schematic.
3. All Measurement across voltage based on SIG specifications.
4. The specified value is the limit above the SIG specifications.
5. PSDU length = 37 channels = 2402/2426/2440/2480 MHz

41.21 Zigbee Specifications

Table 41-28. Zigbee Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
ZBG1	FREQ	Frequency range	2405	—	2480	MHz	
ZBG2	FCH	Channel spacing	—	5	—	MHz	
ZBG3	PSDU	Bit rate	—	250, 500, 1000, 2000	—	kbps	
ZBT1	TXOPMPA	Transmit output power MPA	—	11.5	—	dBm	(4)
ZBT2	TXOPLPA	Transmit output power LPA	—	4.0	—	dBm	(4)
ZBT3	POWERRANGE	Output power range	—	26	—	dB	TX power on ZB power levels from 0 to 15
ZBT4	EVM	Error vector magnitude	—	10	—	%RMS	
ZBRX1	SENS250	Receiver sensitivity in 250 kbps	—	-99	—	dBm	
	SENS500	Receiver sensitivity in 500 kbps	—	-96	—	dBm	
	SENS1M	Receiver sensitivity in 1 Mbps	—	-94	—	dBm	
	SENS2M	Receiver sensitivity in 2 Mbps	—	-88	—	dBm	
ZBRX2	PMAX	Maximum input level	—	0	—	dBm	
ZBRX3 ⁽³⁾	PACRP	Adjacent channel rejection +5 MHz	—	35	—	dB	
ZBRX4 ⁽³⁾	PACRN	Adjacent channel rejection -5 MHz	—	31	—	dB	
ZBRX5 ⁽³⁾	PALRP	Alternate channel rejection +10 MHz	—	17	—	dB	
ZBRX6 ⁽³⁾	PALRN	Alternate channel rejection -10 MHz	—	17	—	dB	
ZBRX7	LOLEAKLPA	LO leakage on LPA mode	—	-28	—	dB	(5)
ZBRX7A	LOLEAKMPA	LO leakage on MPA mode	—	-34	—	dB	(5)
ZBRX8	RSSIRANGE	Dynamic range of RSSI	—	40	—	dB	
ZBRX9	RSSIRES	Resolution of RSSI	—	TBC	—	dB	
ZBRX10	RSSIBASEVAL	Minimum value of RSSI	—	TBC	—	dBm	

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics

Notes:

1. Measured on a board with the reference schematic.
2. Measured across channels at 3.3V and according to 802.15.4 standard specifications.
3. Specified value is the margin above the 802.15.4 standard limits.
4. Measured across channels and voltages.
5. LO leakage on LPA mode, measured across voltage.

Preliminary

42. Electrical Characteristics at 125°C

This chapter provides the electrical specifications and characteristics at 125°C of PIC32CX-BZ2 and WBZ45 module.

42.1 Active Current Consumption DC Electrical Specifications

Table 42-1. Active Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Clock/Freq	Typ ⁽¹⁾	Max.	Units	Conditions
APWR_1	$I_{DD_ACTIVE}^{(2,3)}$	MCU I_{DD} in active mode w/LDO mode selected	PLL 64 MHz	8.4	--	mA	$V_{DD} = V_{DDANA} = 3.3\text{V}$
APWR_13		MCU I_{DD} in active mode w/BUCK mode selected		4.9			

Notes:

1. Typical value measured at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - RF system ON with default settings.
 - RPA2 and RPA4 are configured as UART for communication.
 - RF system is enabled and in IDLE state. Not transmitting or receiving packets.
 - All peripherals disabled (except SERCOM0).
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC is disabled.
 - PMU 1 MHz clock derived from FRC. FRC 8 MHz is divided by 8.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - Backup RAM in retention mode.
 - DSU is disconnected.
3. MCU running while (1) loop with 50 NOP instructions.

42.2 Idle Current Consumption DC Electrical Specifications

Table 42-2. Idle Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V _{DDIO} = V _{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Clock/Freq	Typ ⁽¹⁾	Max.	Units	Conditions ⁽³⁾
IPWR_1	I _{DD_IDLE} ⁽²⁾	MCU I _{DD} in IDLE mode w/LDO mode selected	PLL 64 MHz	5.3	—	mA	No active RF transmission or Reception
IPWR_13		MCU I _{DD} in IDLE mode w/BUCK mode selected		3.38	—		

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - RPA2 and RPA4 are configured as UART for communication.
 - All peripherals disabled (except SERCOM0).
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC is disabled.
 - PMU is clocked at 1MHz from FRC. FRC divided by 8.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - Backup RAM in retention mode.
 - DSU is disconnected.
 - RF system clock gated.
 - Entry to sleep mode disabled and WFI instruction executed.

42.3 Sleep Current Consumption DC Electrical Specifications

Table 42-3. Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
SPWR_1	$I_{DD_STANDBY}^{(2)}$	MCU I_{DD} in Sleep mode w/LDO mode selected	3.3V	950	—	μA	XTAL = ON
			3.3V	620	—	μA	XTAL = OFF
SPWR_29		MCU I_{DD} in Sleep mode w/BUCK mode selected	3.3V	470	—	μA	XTAL = ON
			3.3V	450	—	μA	XTAL = OFF

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled.
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC is disabled.
 - CLDO configured at lowest possible voltage (VREG Trim = 0x07).
 - PMU Configured to Buck PSM mode on Sleep Mode Entry with the Current sense disabled.
 - Cache enabled and configured wait states PFMWS[3:0] as 0xF.
 - Backup RAM in retention mode
 - DSU is disconnected.
 - RF system in low power configuration.
 - Entry to sleep mode enabled and WFI instruction executed.
 - In XTAL ON mode : PMU Buck clock is derived from POSC 16 MHz and scaled to 1 MHz. FRC is OFF.
 - In XTAL OFF mode : PMU is clocked from FRC and XTAL 16 MHz clock is disabled and clock configuration in CRU changed to FRC.

42.4 Deep Sleep Current Consumption DC Electrical Specifications

Table 42-4. Deep Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
BPWR_1	$I_{DD_BACKUP}^{(2)}$	MCU I_{DD} in Deep Sleep mode powered from V_{DDIO}	3.3V	1.2	—	μA	No backup RAM retained
			3.3V	1.43	—	μA	8 KB backup RAM retained

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled.
 - All PB clocks divided by 16.
 - LPRC set as LPCLK.
 - SOSC, POSC is disabled.
 - DSU is disconnected.
 - RF system in low power configuration.
 - DSWDT enabled and configured for wake-up.
 - Deep Sleep Entry configured and WFI instruction executed.

42.5 XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

Table 42-5. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ ⁽¹⁾	Max.	Units	Conditions
OPWR_1	$I_{DD_OFF}^{(2)}$	MCU I_{DD} in OFF mode powered from V_{DDIOX}	3.3V	0.12	—	μA	In OFF mode, the device is entirely powered-off. Note: This mode is left by pulling the RESET pin low, or when a power reset is done

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

Notes:

1. Typical value measured during characterization at 3.3V and 25°C.
2. The test conditions are as follows:
 - All GPIO except RPA3 pulled up. RPA3 is pulled down.
 - All peripherals disabled.
 - DSU is disconnected.
 - RF system in low power configuration.
 - DSWDT disabled.
 - RTCC, POSC disabled.
 - Deep Sleep Entry configured and WFI instruction executed.

42.6 External XTAL and Clock AC Electrical Specifications

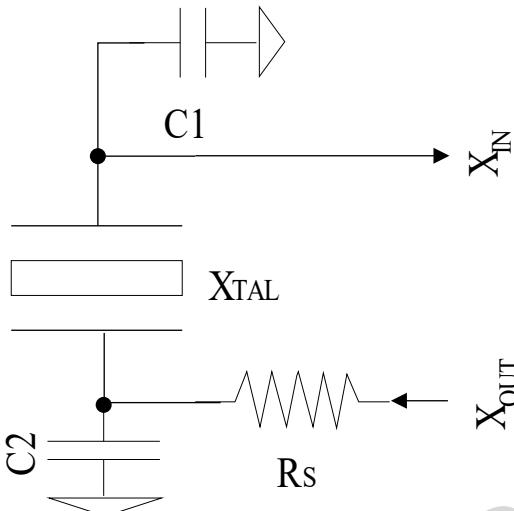
Table 42-6. External XTAL and Clock AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp					
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾	
XOSC_1	FOSC_XOSC	XOSC Crystal frequency	—	16	—	MHz		
XOSC_1A	TOSC	$\text{TOSC} = 1/\text{FOSC}_\text{XOSC}$	—	0.0625	—	ns	See parameter XOSC1 for FOSC_XOSC value	
XOSC_2	XOSC_ST ⁽²⁾	XOSC Crystal start-up time	—	—	2.5	ms	Crystal stabilization time only not oscillator ready ⁽²⁾	
XOSC_3	CXIN	XOSC XIN Parasitic pin capacitance	—	0.35	—	pF	With Default Crystal trim settings	
XOSC_5	CXOUT	XOSC XOUT Parasitic pin capacitance	—	0.35	—	pF	With Default Crystal trim settings	
XOSC_11	CLOAD ⁽³⁾	XOSC Crystal FOSC = 16 MHz	—	9	—	pF		
XOSC_21	ESR	XOSC Crystal FOSC = 16 MHz	—	—	100	Ω		
XOSC_33	DLEVEL	MCU Crystal Oscillator Power Drive Level	—	—	100	μW		

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

Figure 42-1. External XTAL and Clock Diagram



Notes:

1. $V_{DDIO} = V_{DDANA} = 3.3V$.
2. This is for guidance only. A major component of crystal start-up time is based on the 2nd party crystal MFG parasitic that are outside the scope of this specification. If this is a major concern the customer would need to characterize this based on their design choices.
3. The test conditions for crystal load capacitor calculation are as follows:
 - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W=0.175 mm, H=36 μm, T=113 μm).
 - Xtal PCB capacitance typical therefore ≈ 2.5 pF for a tight PCB Xtal layout.
 - For CXIN and CXOUT within 4 pF of each other, Assume CXTAL_EFF = ((CXIN+CXOUT) / 2).
 - **Note:** Averaging CXIN and CXOUT will effect final calculated CLOAD value by less than 0.25 pF.

Equation 42-1. Equation 1:

*MFG CLOAD Spec = {([CXIN + C1] * [CXOUT + C2]) / [CXIN + C1 + C2 + CXOUT]} + estimated oscillator PCB stray capacitance*

Assuming C1 = C2 and CXin ≈ CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

Equation 42-2. Equation 2 (In other words: Simplified Equation 1)

$$C1 = C2 = ((2 * MFG CLOAD Spec) - CXTAL_EFF - (2 * PCB capacitance))$$

Example:

- XTAL Mfg CLOAD Data Sheet Spec = 12 pF
- PCB XTAL trace Capacitance = 2.5 pF
- CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = ((CXIN+CXOUT) / 2)

$$CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 \text{ pF}$$

$$C1 = C2 = ((2 * MFG CLOAD spec) - CXTAL_EFF - (2 * PCB capacitance))$$

$$C1 = C2 = (24 - 5.5 - (2 * 2.5))$$

$$C1 = C2 = 13.5 \text{ pF (Always rounded down)}$$

C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)

User C1=C2=13 pF CLOAD (max) spec

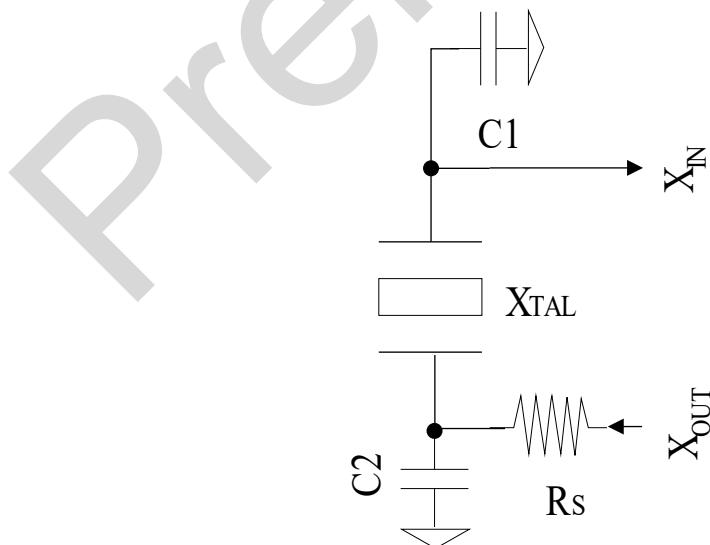
4. Maximum start up time user selectable in XOSCCTRL.STARTUP.

42.7 XOSC32 AC Electrical Specifications

Table 42-7. XOSC32 AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions ⁽¹⁾
XOSC32_1	FOSC_XOSC32	XOSC32 Oscillator crystal frequency	—	32.768	—	kHz	XIN32, XOUT32 Secondary oscillator
XOSC32_3	CXIN32	XOSC32 XIN32 Parasitic pin capacitance	—	0.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the Module
				2.4			
XOSC32_5	CXOUT32	XOSC32 XOUT32 Parasitic pin capacitance on PIC32CX-BZ2	—	0.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the Module
				2.4			
XOSC32_11	CLOAD_X32 ⁽³⁾	32.768 kHz Crystal load capacitance	—	11	—	pF	
XOSC32_13	ESR_X32	32.768 kHz Crystal ESR	—	75	—	KΩ	
XOSC32_15	TOSC32	TOSC32 = 1/ FOSC_XOSC32	—	30.518	—	μs	See parameter XOSC32_1 for FOSC_XOSC32 value
XOSC32_17	XOSC32_ST ⁽²⁾	XOSC32 Crystal start-up time	—	4	—	TOSC	Crystal stabilization time only not oscillator ready ⁽²⁾

Figure 42-2. XOSC32 Block Diagram



PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

Notes:

1. $V_{DDIO} = V_{DDANA} = 3.3V$.
2. This is for guidance only. A major component of crystal start-up time is based on the 2nd party crystal MFG parasitic that are outside the scope of this specification. If this is a major concern, the customer would need to characterize this based on their design choices.
3. The test conditions for crystal load capacitor calculation are as follows:
 - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W=0.175 mm, H=36 μm, T=113 μm)
 - Xtal PCB capacitance typical therefore ~ 2.5 pF for a tight PCB Xtal layout
 - For CXIN and CXOUT within 4 pF of each other, Assume CXTAL_EFF = $((CXIN+CXOUT) / 2)$
 - **Note:** Averaging CXIN and CXOUT will effect final calculated CLOAD value by less than the tolerance of the capacitor selection.

Equation 42-3. Equation 1:

*MFG CLOAD Spec = {[CXIN + C1] * [CXOUT + C2]} / [CXIN + C1 + C2 + CXOUT] + estimated oscillator PCB stray capacitance*

Assuming C1 = C2 and CXin \sim CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

Equation 42-4. Equation 2 (In other words: Simplified Equation 1)

$$C1 = C2 = ((2 * MFG CLOAD Spec) - CXTAL_EFF - (2 * PCB capacitance))$$

Example:

- XTAL Mfg CLOAD Data Sheet Spec = 12 pF
- PCB XTAL trace Capacitance = 2.5 pF
- CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = $((CXIN+CXOUT) / 2)$

$$CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 \text{ pF}$$

$$C1 = C2 = ((2 * MFG CLOAD spec) - CXTAL_EFF - (2 * PCB capacitance))$$

$$C1 = C2 = (24 - 5.5 - (2 * 2.5))$$

$$C1 = C2 = (24 - 5.5 - 5)$$

$$C1 = C2 = 13.5 \text{ pF} \text{ (Always rounded down)}$$

C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)

User C1 = C2 = 13 pF \leq CLOAD_X32 (max) spec

4. User selectable in OSC32KCTRL.STARTUP.

42.8 Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

Table 42-8. Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated)				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
LP32K_1	FOSC_LPRC32K	Output frequency	—	32.768	—	kHz	$V_{DDIO} = V_{DDANA} \geq V_{DDANA(\min)}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp $\leq +125^{\circ}\text{C}$ (in other words, Factory default calibration)

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
LP32K_9	RC32K_Duty	LPRC32K OSC duty cycle	—	50	—	%	$V_{DDIO} = V_{DDANA} \geq V_{DDANA(\min)}$

42.9 FRC AC Electrical Specifications

Table 42-9. FRC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
FRC1	FINTFREQ	Internal FRC frequency	—	8	—	MHz	
FRC2	TSUFRC	Start-up time of internal FRC	—	15	—	μs	
FRC5	DUTY_CYCLE	FRC Duty Cycle	—	50	—	%	
FRC6	C_USE	FRC User Tune Frequency Drift	—	-1.625 +1.65	—	%	Frequency Drift = [(Maximum Frequency Measured - Minimum Frequency Measured) / (Default Frequency of 8 MHz)] * 100 Maximum Frequency drift possible by using the Frequency trim bits
FRC7	C_USER_STEP_SIZE	FRC User Tune Step size	—	0.046	—	%	Step Size = (% Drift Across Osc Tune) / (Total Number of Trim Bit Combinations); Change in frequency with incremental trim bit

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Electrical Characteristics at 125°C

42.10 MCU Frequency AC Electrical Specifications

Table 42-10. Frequency AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
MCU_1	FCY	MCU Frequency of operation	—	—	64	MHz	$V_{DDIO(\min)} \text{ to } V_{DDIO(\max)}$
MCU_3	TCY	MCU Clock period	1/FCY			ns	

PLL (Phase Locked Loop) AC Electrical Specifications

Table 42-11. FDPLLxx MHz (Fractional Digital Phase Locked Loop)

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
PLL_1	PLL_FIN	PLL Input frequency	—	16	—	MHz	Over full voltage and temperature operating ranges
PLL_3	PLL_FOUT	PLL Output clock frequency	—	96	—	MHz	
PLL_4	PLL_VCO_FREQ	PLL VCO Frequency (Fixed)	—	480	—	MHz	

Note:

1. PLL input clock is the 16 MHz XOSC.

42.11 ADC Electrical Specifications

Table 42-12. ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
ADC_1	V_{DDANA}	ADC Supply	$V_{DDANA(\min)}$	—	$V_{DDANA(\max)}$	V	$V_{DDIOx} = V_{DDANA}$
Reference Inputs							

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions	
ADC_3	$V_{REF}^{(4)}$	ADC Reference Voltage ⁽⁴⁾	—	—	V_{DDANA}	V	External Reference Voltage	
Analog Input Range								
ADC_7	AFS	Full-Scale Analog Input Signal Range (Single-Ended)	0	—	V_{DDANA}	V	$V_{REF} = V_{DDANA(max)}$	
ADC_9		Full-Scale Analog Input Signal Range (Differential)	$-V_{DDANA}/2$	—	$V_{DDANA}/2$	V		

Table 42-13. ADC Single-Ended Mode AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions	
Single-Ended Mode ADC Accuracy								
SADC_11	Res	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 bit Resolution Ranges	
SADC_13	EN0B ⁽³⁾	Effective Number of bits	—	9.3	—	bits	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_19	INL ⁽³⁾	Integral Nonlinearity	—	-5.2	—	LSb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_25			—	2.7	—			
SADC_31	GERR ⁽³⁾	Gain Error	—	-1	—	LSb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_37			—	1.8	—			
SADC_31	GERR ⁽³⁾	Offset Error	—	-0.7	—	LSb	1.6 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
SADC_37	E0FF ⁽³⁾	Offset Error	—	3.2	—	LSb	2 Msps, Internal V_{REF} , $V_{DDANA} = V_{DDIO} = 3.3\text{V}$	
Single-Ended Mode ADC Dynamic Performance								

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

.....continued

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
SADC_49	SINAD ^(1,2,3)	Signal to Noise and Distortion	—	57.8	—	dB	$V_{REF} = V_{DDANA} = V_{DDIO} = 3.3\text{V}$ @ 12-bit resolution, max sampling rate ^(1,2)
SADC_51	SNR ^(1,2,3)	Signal to Noise ratio	—	58.2	—		
SADC_53	SFDR ^(1,2,3)	Spurious Free Dynamic Range	—	66.25	—		
SADC_55	THD ^(1,2,3)	Total Harmonic Distortion	—	-71.3	—		

Notes:

- Characterized with an analog input sine wave = (FTP(max) / 100). Example: FTP(max)=1 MMsps/100 = 10 KHz sine wave.
- Sinewave peak amplitude = 96% ADC_Full Scale amplitude input with 12-bit resolution.
- Spec values collected under the following additional conditions:
 - 12-bit resolution mode.
 - All registers at reset default value otherwise not mentioned.
- ADC Measurements done with 3.3V V_{REF} Voltage.
- Value taken over 7 harmonics.

Table 42-14. ADC Conversion AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
ADC_Clock Requirements							
ADC_57	TAD	ADC Clock Period	—	20.83	—	ns	$V_{REF} = V_{DDANA} = 3.3\text{V}$
ADC Single-Ended Throughput Rates							
ADC_59	FTPR (Single-Ended Mode)	Throughput Rate ⁽²⁾ (Single-Ended)	—	1.7	—	Msps	12-bit resolution, DIV_SHR = 2
			—	0.773	—		12-bit resolution, DIV_SHR = 4

Notes:

- Conversion_time = (SAMC_SHR+15)*TAD.
- FTPR = 1 / ((SAMC_SHR + Resolution + 1) * (1 / (ControlClk / DIV_SHR))).

PIC32CX-BZ2 and WBZ45 Family

Electrical Characteristics at 125°C

Table 42-15. ADC Sample AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Temp					
Param. No.	Symbol	Characteristic s	Min.	Typical	Max.	Units	Conditions	
ADC_65	TCNV	Conversion Time ⁽¹⁾ (Single-Ended Mode)	14			TAD	12-bit resolution	
			12				10-bit resolution	
			10				8-bit resolution	
ADC_67		Conversion Time ⁽¹⁾ (Differential Mode)	14			TAD	12-bit resolution	
			12				10-bit resolution	
			10				8-bit resolution	
ADC_69	CSAMPL E	ADC Internal Sample Cap	—	5	—	pF		
ADC_71	RSAMPL E	ADC Internal impedance	—	—	200	Ω		

Note:

1. ADC Throughput Rate FTP = ((1 / ((TSAMP + TCNV) * TAD)) / (# of user active analog inputs in use on specific target ADC module)).

43. Packaging Information

This chapter provides the information on package markings, dimension and footprint of the PIC32CX-BZ2 and WBZ45 family.

43.1 PIC32CX-BZ2 SoC Packaging Information

Note: For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/en-us/support/package-drawings.

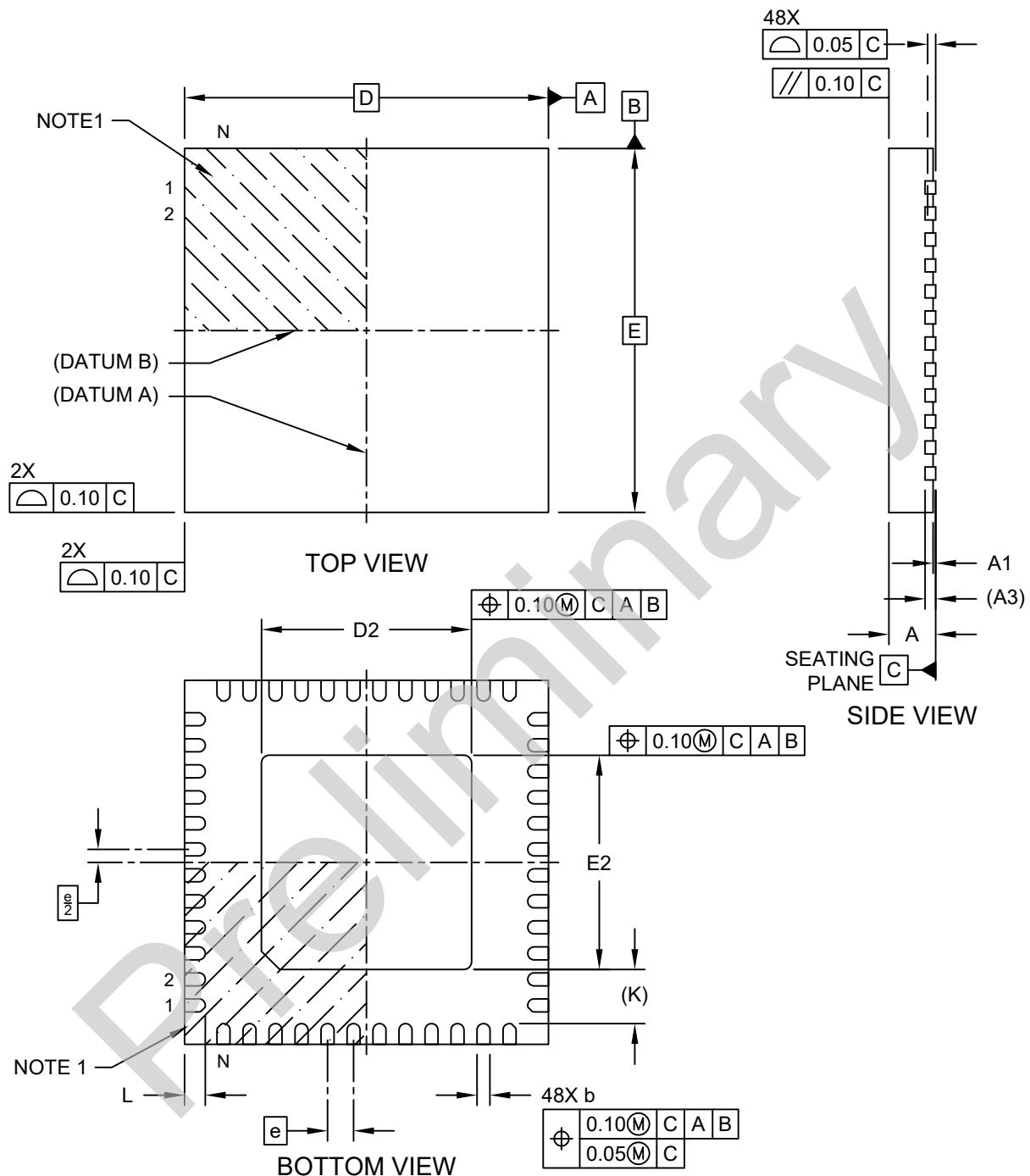
The following images illustrate the packaging information of the PIC32CX1012BZ25048, which has 48-lead very thin quad flat, no lead package (MYX) - 7x7x0.9 mm body [VQFN] with 4.04x4.12 mm exposed pad.

Preliminary

PIC32CX-BZ2 and WBZ45 Family

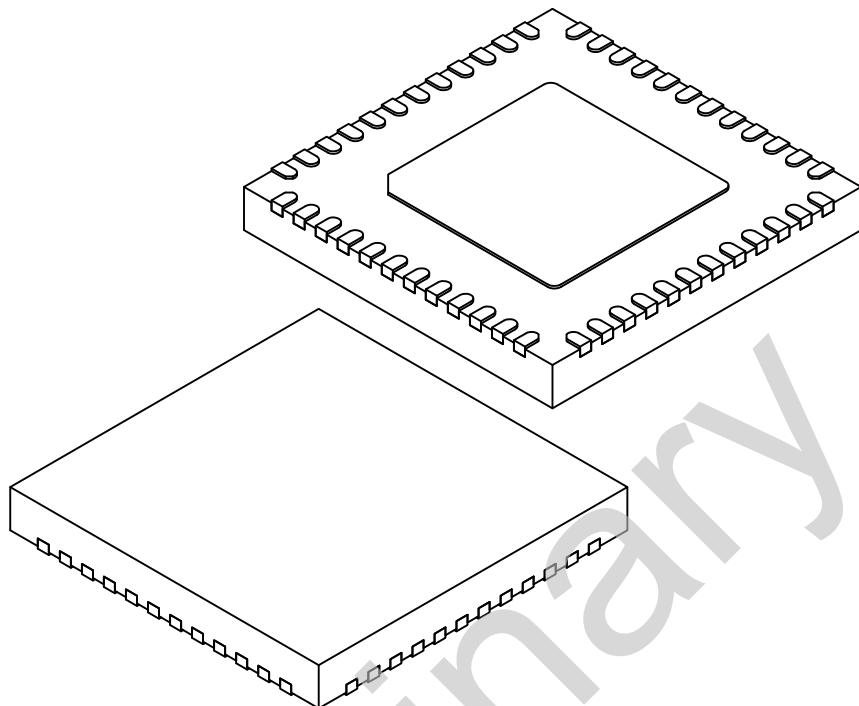
Packaging Information

Figure 43-1. PIC32CX1012BZ25048 SoC Packaging Dimension



PIC32CX-BZ2 and WBZ45 Family Packaging Information

Figure 43-2. PIC32CX1012BZ25048 SoC Package Outline Drawing



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals		N		
Pitch		e		
Overall Height		A	0.80	0.85
Standoff		A1	0.00	0.02
Terminal Thickness		A3	0.20 REF	
Overall Length		D	7.00 BSC	
Exposed Pad Length		D2	3.94	4.04
Overall Width		E	7.00 BSC	
Exposed Pad Width		E2	4.02	4.12
Terminal Width		b	0.18	0.25
Terminal Length		L	0.35	0.40
Terminal-to-Exposed-Pad		K	1.04 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

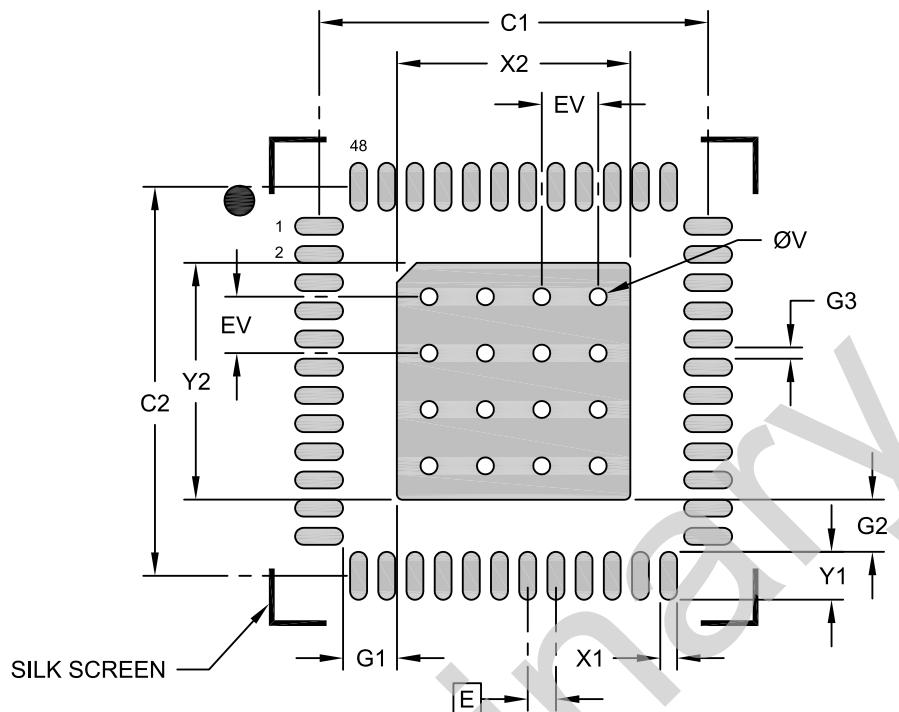
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

PIC32CX-BZ2 and WBZ45 Family

Packaging Information

Figure 43-3. PIC32CX1012BZ25048 SoC Recommended Land Pattern



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch		E		0.50 BSC
Optional Center Pad Width	X2			4.14
Optional Center Pad Length	Y2			4.20
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.96		
Contact Pad to Center Pad (X24)	G2	0.93		
Contact Pad to Contact Pad (X44)	G3	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

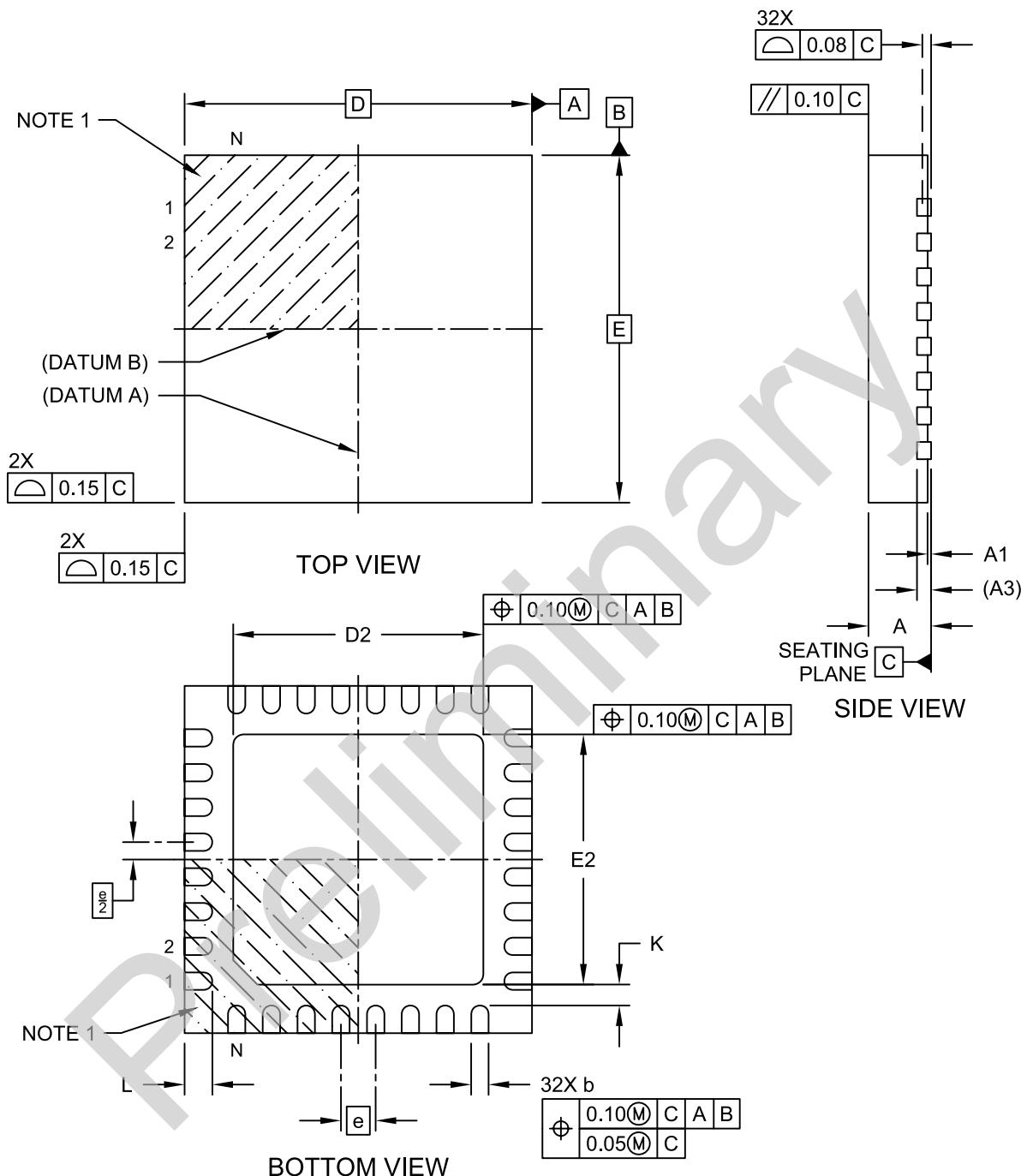
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

The following images illustrate the packaging information of the PIC32CX1012BZ24032, which has 32-lead very thin plastic quad flat, no lead package (S8B) - 5x5 mm body [VQFN] with 3.6x3.6 mm exposed pad.

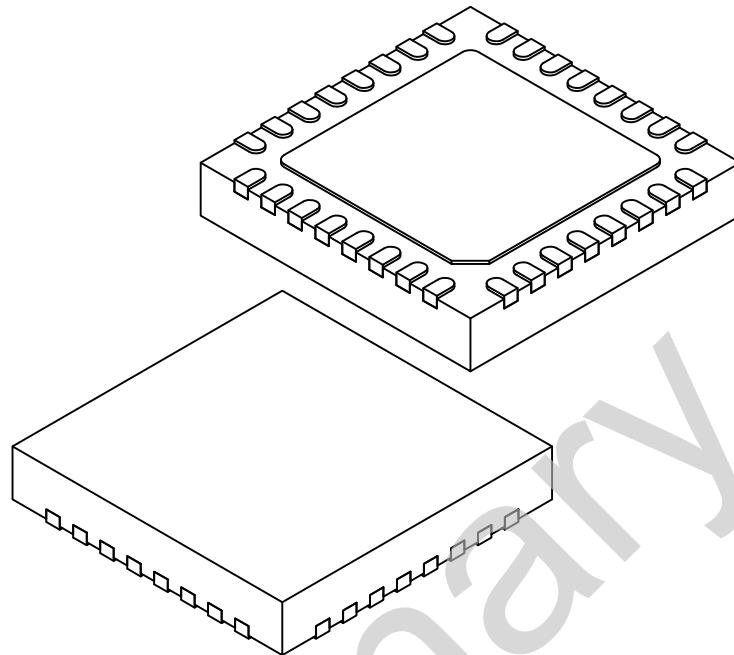
PIC32CX-BZ2 and WBZ45 Family Packaging Information

Figure 43-4. PIC32CX1012BZ24032 SoC Packaging Dimension



PIC32CX-BZ2 and WBZ45 Family Packaging Information

Figure 43-5. PIC32CX1012BZ24032 SoC Package Outline Drawing



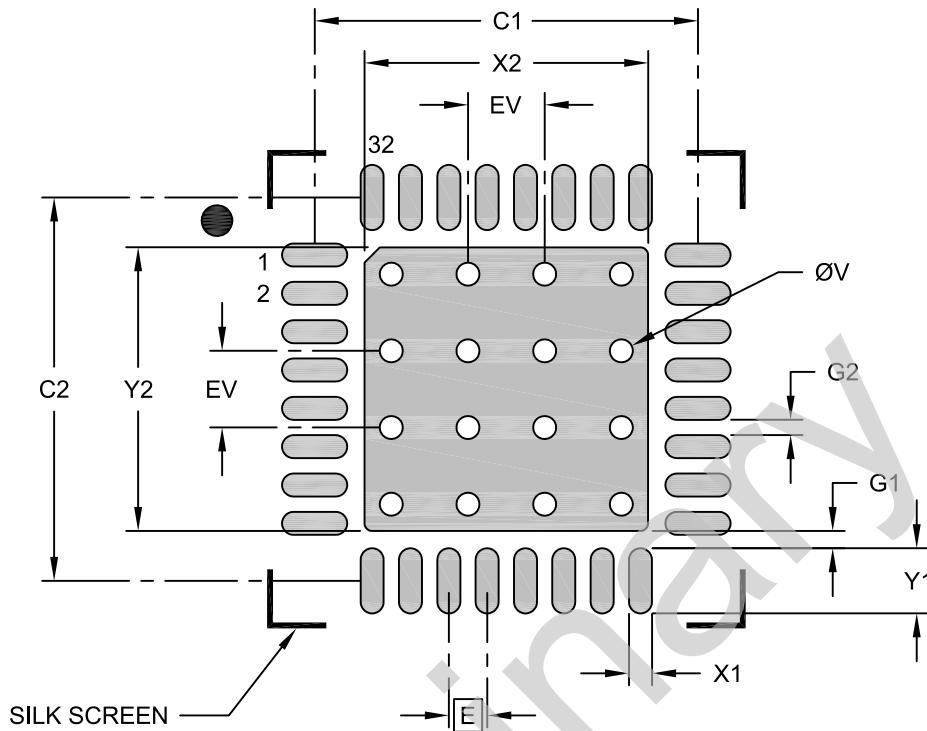
Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
 2. Package is saw singulated
 3. Dimensioning and tolerancing per ASME Y14.5M
- BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

PIC32CX-BZ2 and WBZ45 Family Packaging Information

Figure 43-6. PIC32CX1012BZ24032 SoC Recommended Land Pattern



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

43.2 WBZ45 Module Packaging Information

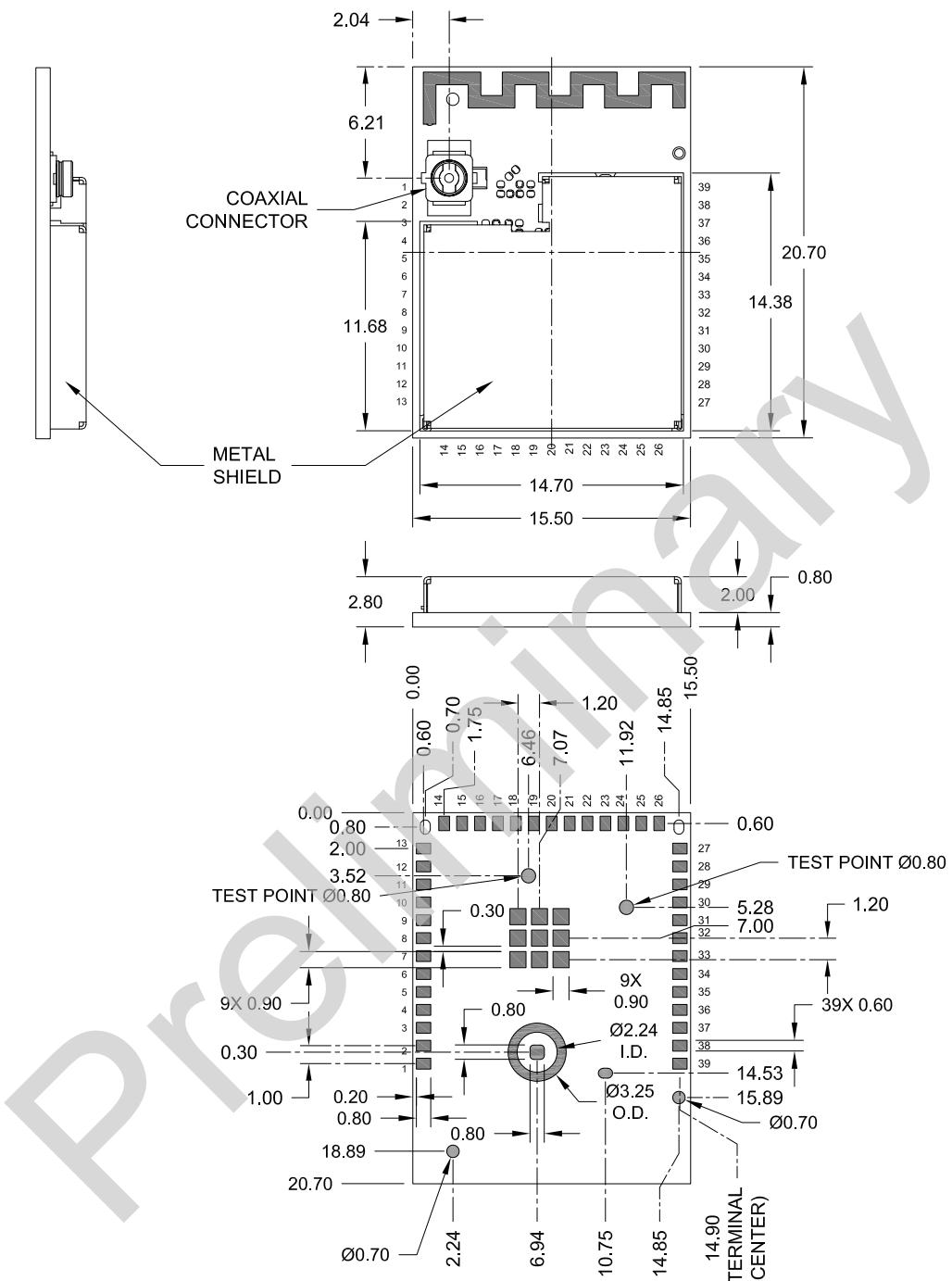
Note: For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/en-us/support/package-drawings.

The following images illustrate the packaging information of the WBZ451, which has 39-lead PCB module (ZSX) -15.5x20.7x2.8 mm body (module) with metal shield and coaxial connector.

PIC32CX-BZ2 and WBZ45 Family

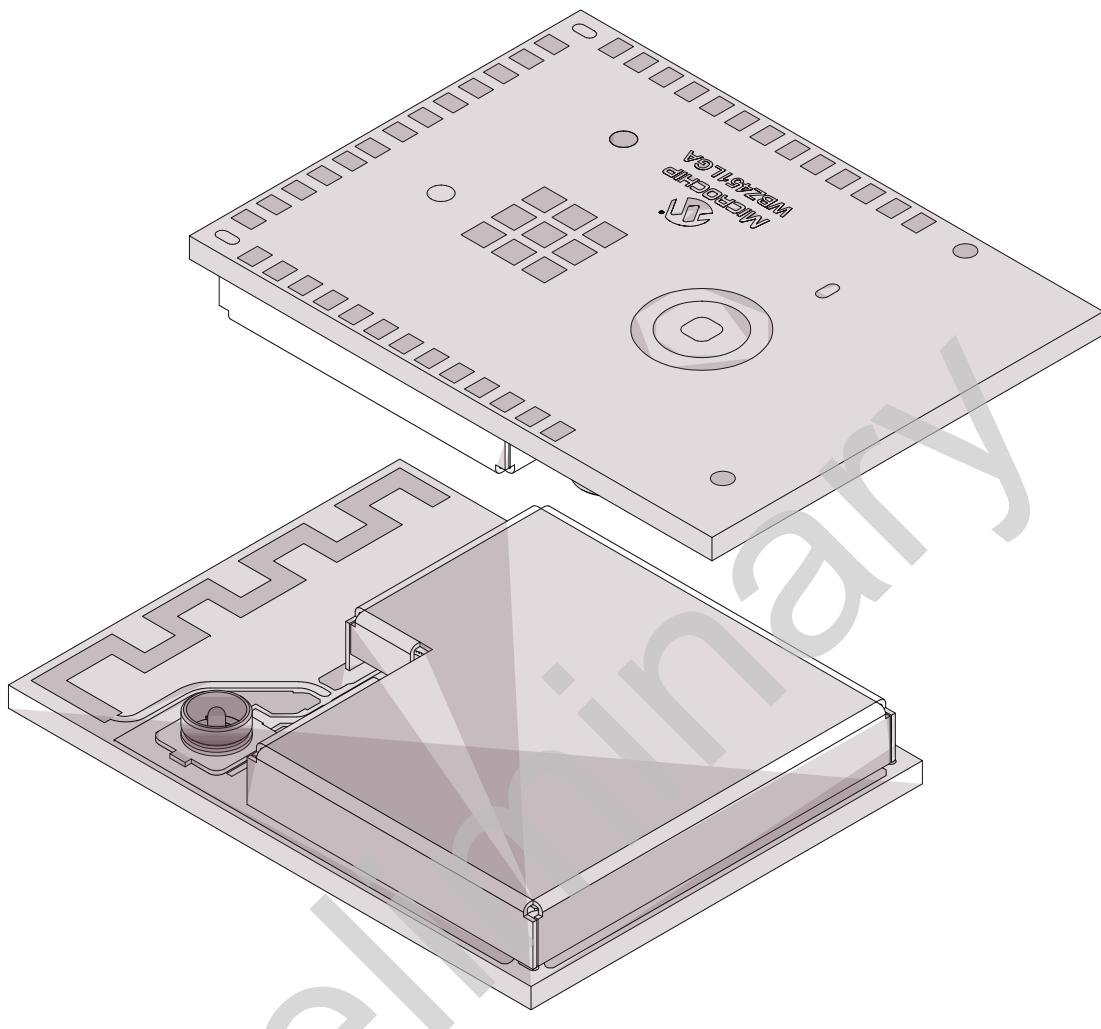
Packaging Information

Figure 43-7. Dimensions and Top, Bottom, and Side Views of WBZ451 Module



PIC32CX-BZ2 and WBZ45 Family Packaging Information

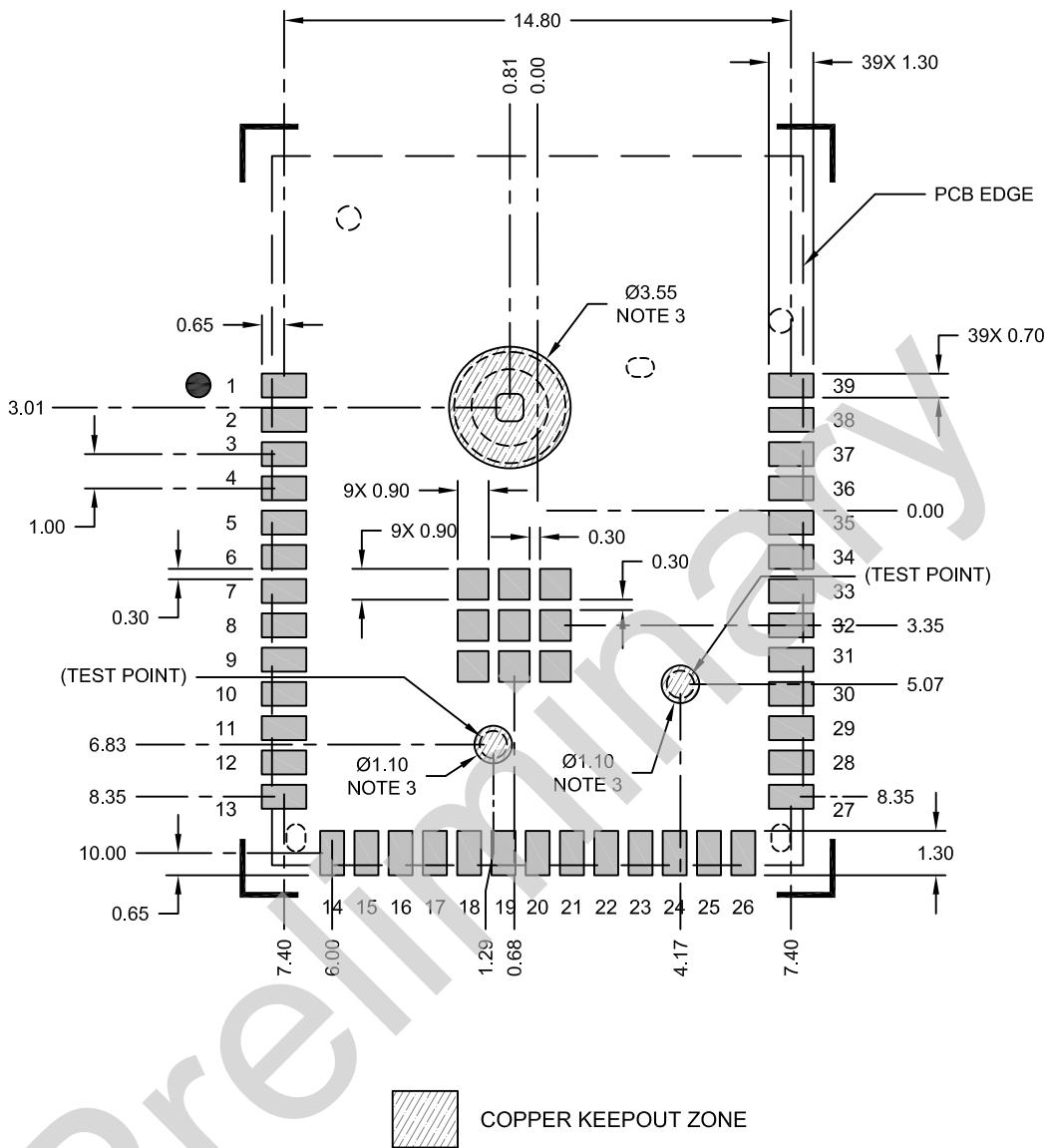
Figure 43-8. WBZ451 Module Package Outline Drawing



PIC32CX-BZ2 and WBZ45 Family

Packaging Information

Figure 43-9. Recommended Land Pattern of WBZ451 Module



Notes:

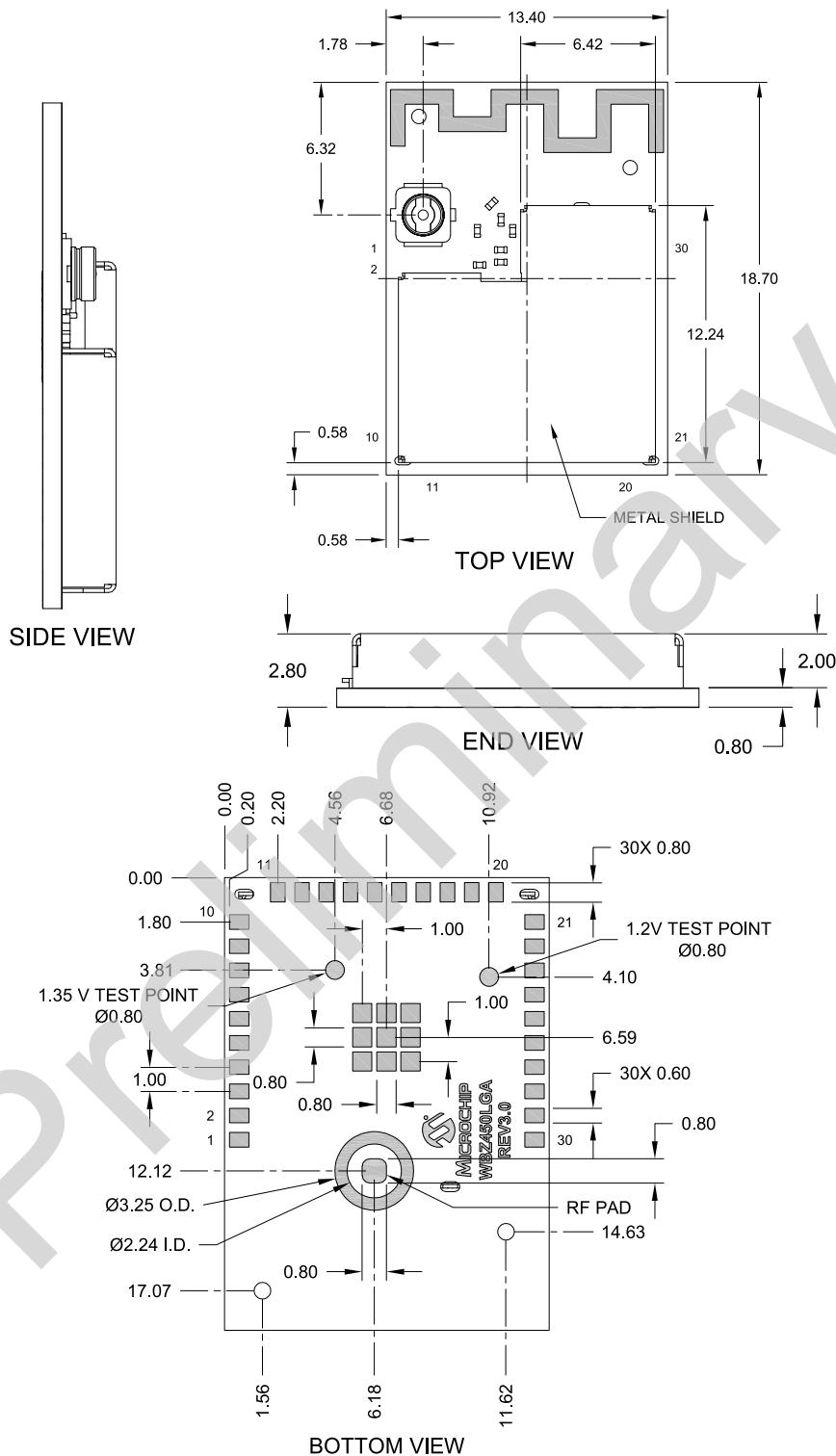
1. All dimensions are in millimeters.
 2. Keep this area free from all metal, including ground fill.
 3. Keep these areas free from routes and exposed copper. Ground fill with solder mask may be placed here.

The following images illustrate the packaging information of the WBZ450, which has 30-lead PCB module (ZRX) -13.4x18.7x2.8 mm body (module).

PIC32CX-BZ2 and WBZ45 Family

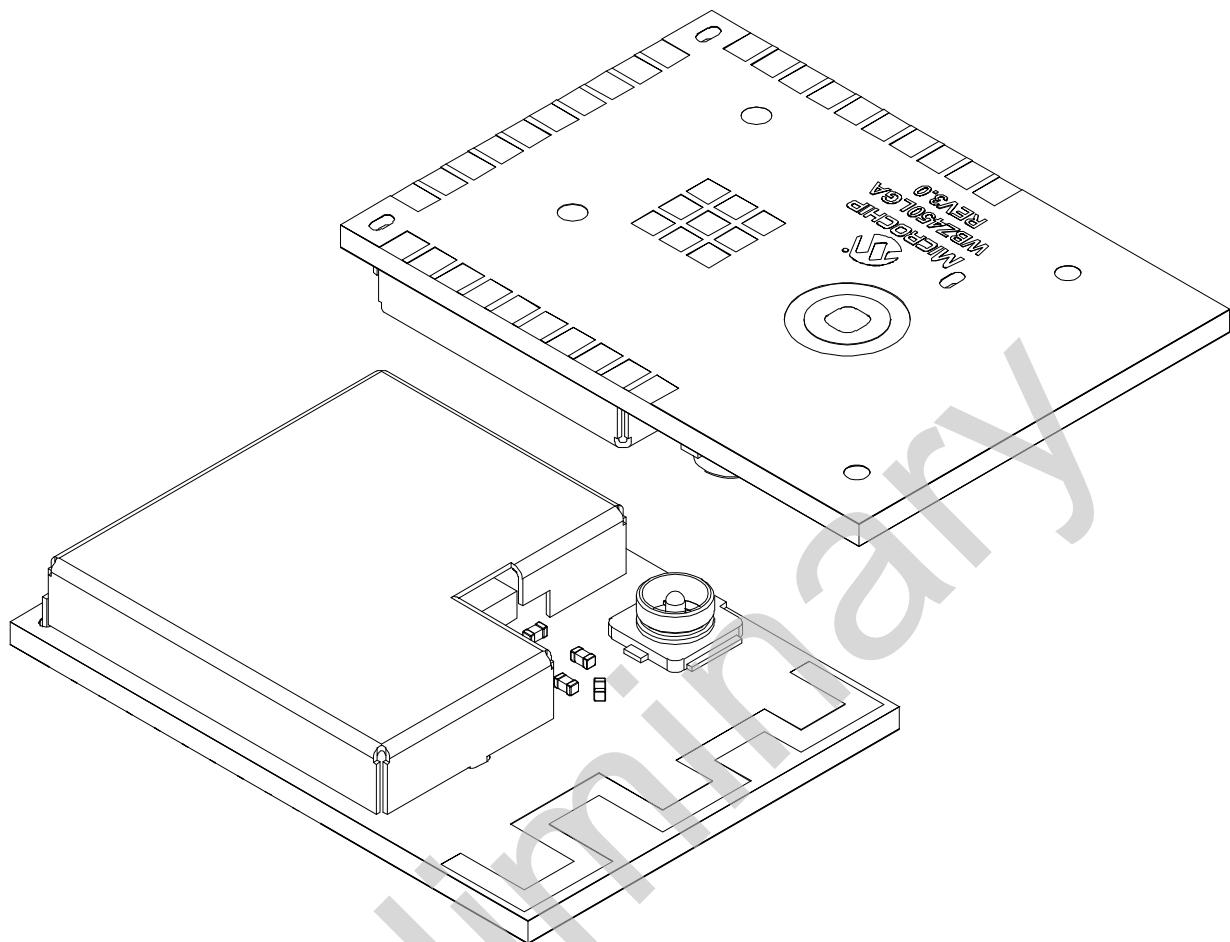
Packaging Information

Figure 43-10. Top, Bottom, End and Side Views of WBZ450 Module



PIC32CX-BZ2 and WBZ45 Family Packaging Information

Figure 43-11. WBZ450 Module Package Outline Drawing



PIC32CX-BZ2 and WBZ45 Family

Document Revision History

44. Document Revision History

Revision	Date	Section	Description
A	01/2022	Document	Initial revision

Preliminary

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